NEC

MOS INTEGRATED CIRCUIT

μPD64084

THREE-DIMENSIONAL Y/C SEPARATION LSI WITH ON-CHIP MEMORY

DESCRIPTION

The μPD64084 realizes a high precision Y/C separation by the three-dimension signal processing for NTSC signal.

This product has the on-chip 4-Mbit memory for flame delay, a high precision internal 10-bit A/D converter and D/A converter, and adapting 10-bit signal processing (only for luminance signal) and high picture quality. The μPD64084 is completely single-chip system of 3D Y/C separation.

This LSI includes the Wide Clear Vision ID signal (Japanese local format) decoder and ID-1 signal decoder.

FEATURES

- On-chip 4-Mbit frame delay memory.
- 2 operation mode
  - Motion adaptive 3D Y/C separation
  - 2D Y/C separation + Frame recursive Y/C NR
- Embedded 10-bit A/D converter (1ch), 10-bit D/A converters (2ch), and System clock generator.
- Embedded Y coring, Vertical enhancer, Peaking filter, and Noise detector.
- Embedded ID-1 signal decoder, and WCV-ID signal decoder.
- I^2C bus control.
- Dual power supply of 2.5 V and 3.3 V.
  - For digital : DV_{DD} = 2.5 V
  - For analog : AV_{DD} = 2.5 V
  - For DRAM : DV_{DDRAM} = 2.5 V
  - For I/O : DV_{DDIO} = 3.3 V

ORDERING INFORMATION

	Part number	Package
★	μPD64084GC-8EA-A[Note1]	100-pin plastic LQFP (fine pitch) (14 × 14 mm)
	μPD64084GC-8EA-Y[Note2]	100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Notes 1. Lead-free product

2. High-thermal-resistance product

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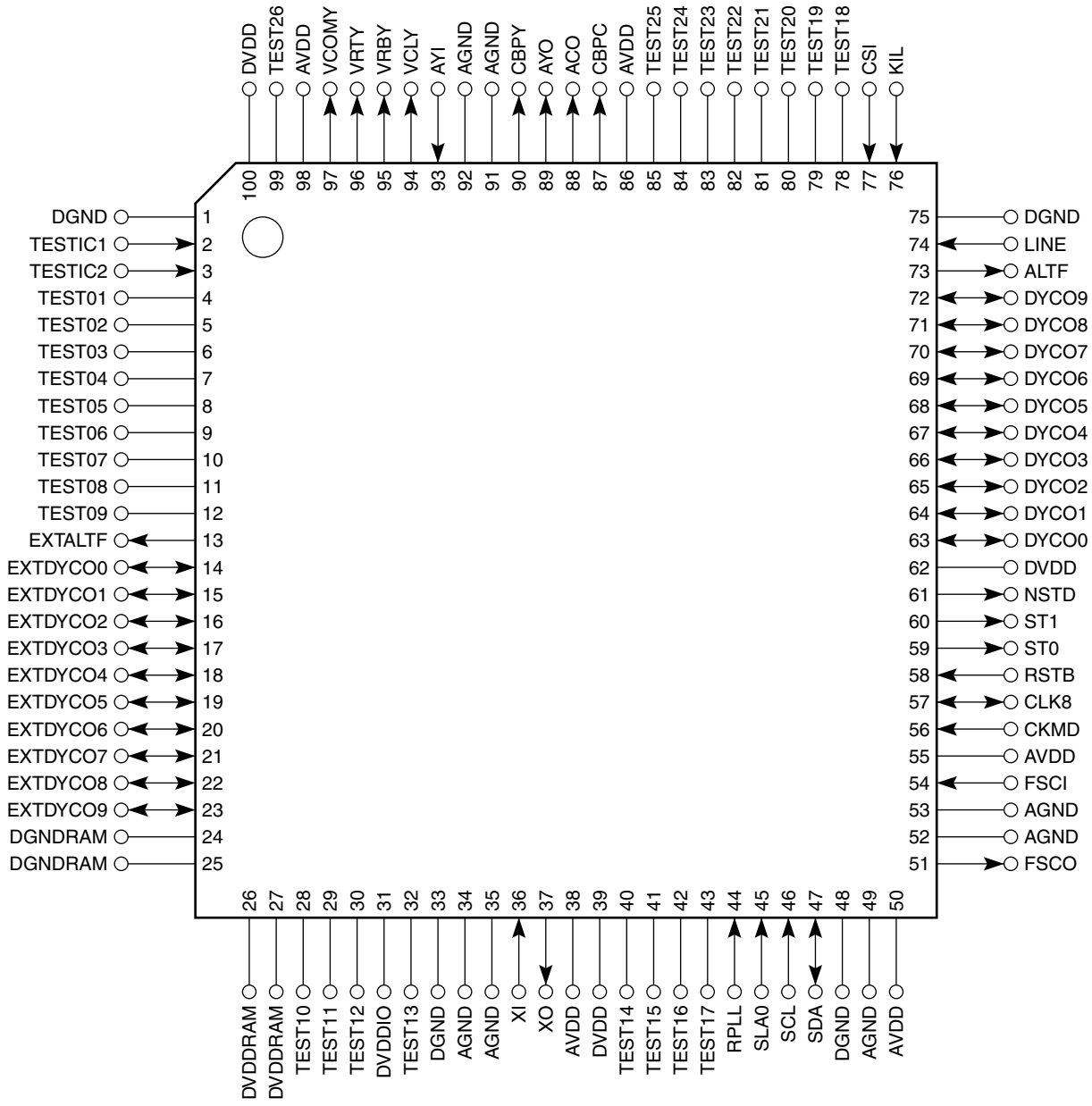
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

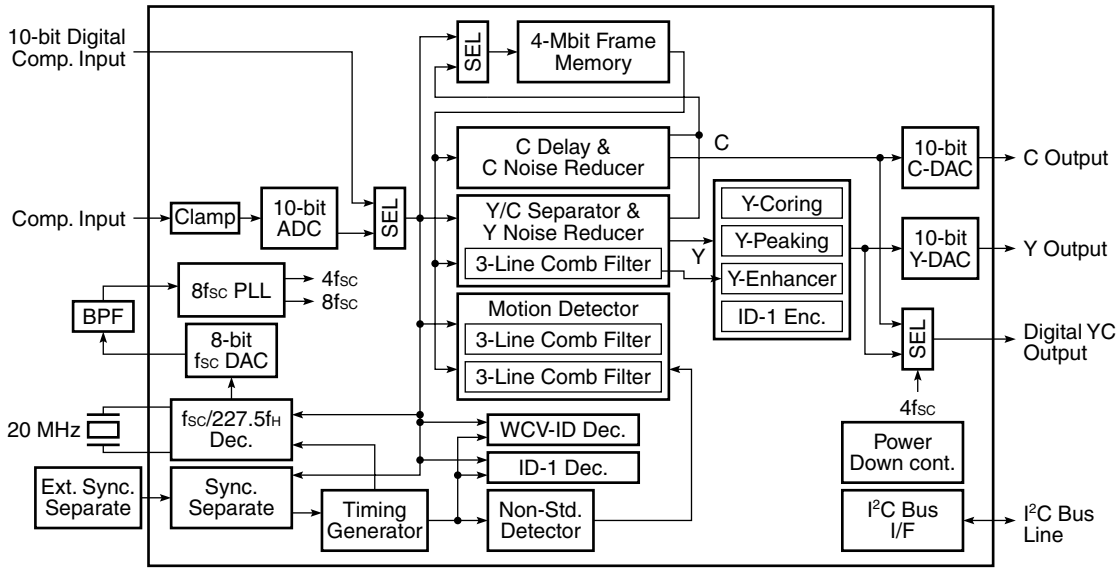
- 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
  μPD64084GC-8EA-A
  μPD64084GC-8EA-Y



PIN NAME

ACO	: Analog C (Chroma) Signal Output
AGND	: Analog Section Ground
ALTF	: Alternate Flag for Digital YC Output
AVDD	: Analog Section Power Supply
AYI	: Analog Composite Signal Input
AYO	: Analog Y (Luma) Signal Output
CBPC	: C-DAC Phase Compensation Output
CBPY	: Y-DAC Phase Compensation Output
CKMD	: Clock Mode Selection
CLK8	: 8f_{SC} Clock Input / Output
CSI	: Composite Sync. Input (Active-low)
DGND	: Digital Section Ground
DVDD	: Digital Section Power Supply
DVDDIO	: Digital I/O Section Power Supply
DVDDRAM	: Internal DRAM Section Power Supply
DYCO0 to DYCO9	: Digital YC Signal (Alternative) Input / Outputs
EXTALTF	: Extend Alternate Flag for Digital YC Output
EXTDYCO0 to EXTDYCO9	: Extend Digital YC Signal (Alternative) Input / Outputs
FSCI	: f_{SC} (Subcarrier) Input
FSCO	: f_{SC} (Subcarrier) Output
KIL	: Killer Selection
LINE	: Inter-Line Separate Selection
NSTD	: Non Standard Detection Monitor
RPLL	: Testing Selection
RSTB	: System Reset (Active-low)
SCL	: Serial Clock Input
SDA	: Serial Data Input / Output
SLA0	: Slave Address Selection
ST1, ST0	: Inner States Monitor
TEST01 to TEST26	: Testing Selection
TESTIC1, TESTIC2	: IC Testing Section
VCLY	: Clamp Voltage Output for ADC
VRTY	: Top Voltage Reference Output for ADC
VRBY	: Bottom Voltage Reference Output for ADC
VCOMY	: Common Mode Reference Output for ADC
XI	: X'tal input
XO	: X'tal output

BLOCK DIAGRAM



TERMINOLOGY

This manual use the abbreviation listed below:

ADC : A/D (Analog to Digital) converter
DAC : D/A (Digital to Analog) converter
LPF : Low-pass filter
BPF : Band-pass filter
Y signal, or Luma : Luminance, or luminance signal
C signal, or Chroma : Color signal, or chrominance signal
f_{SC} : Color subcarrier frequency = 3.579545 MHz
$4f_{SC}$: 4 times f_{SC}, burst locked clock = 14.318180 MHz
$8f_{SC}$: 8 times f_{SC}, burst locked clock = 28.636360 MHz
f_H : Horizontal sync frequency = 15.734 kHz
$910f_H$: 910 times f_H, line locked clock = 14.318180 MHz
$1820f_H$: 1820 times f_H, line locked clock = 28.636360 MHz
f_V : Vertical sync frequency = 59.94 Hz
NR : Noise reduction
YNR : Luminance (Y) noise reduction
CNR : Chrominance (C) noise reduction
WCV-ID : Wide Clear Vision standard ID signal (Japan only)
ID-1 : ID signal of EIAJ CPR-1204

In the following diagrams, a serial bus register is enclosed in a box: 

CONTENTS

1. PIN FUNCTIONS

1.1 Pin Functions

Table 1-1. Pin Functions (1/2)

No.	Symbol	I/O	Level	Buffer type PU/PD [kΩ]	Description
1, 33, 48, 75	DGND	-	-	-	Digital section ground
2, 3	TESTIC1, TESTIC2	I	LVTTL	3.3 V PD:50	IC testing (Grounded)
4-12, 28-30, 78-85, 99	TEST01-TEST09, TEST10-TEST12, TEST18-TEST25, TEST26	-	-	-	Device test (Open)
13	EXTALTF	O	LVTTL	3.3 V 3 mA	Extended alternate flag output (This pin is enable in EXTDYCO = 1)
14 - 23	EXTDYCO0-EXTDYCO9	I/O	LVTTL 3-state	3.3 V 3 mA	Extended digital I/O (These pins are enable in EXTDYCO = 1)
24, 25	DGNDRAM	-	-	-	DRAM section ground
26, 27	DVDDRAM	-	-	-	DRAM section 2.5 V supply voltage
31	DVDDIO	-	-	-	I/O terminal section 3.3 V supply voltage
32, 40-43	TEST13, TEST14-TEST17	-	-	-	Device Test (Grounded)
34, 35	AGND	-	-	-	X'tal oscillation circuit section gound
36	XI	I	Analog	2.5 V	f_{SC} generator reference clock input (X'tal is connected.)
37	XO	O	Analog	2.5 V	f_{SC} generator reference clock inverted output (X'tal is connected.)
38	AVDD	-	-	-	X'tal oscillation circuit section 2.5 V supply voltage
39, 62, 100	DVDD	-	-	-	Digital section 2.5 V supply voltage
44	RPLL	I	LVTTL	3.3 V PD:50	Test pin (Grounded)
45	SLA0	I	LVTTL	3.3 V	I^2C bus slave address selection input (L : B8h / B9h, H : BAh / BBh)
46	SCL	I	Schmitt Fail Safe	3.3 V	I^2C bus clock input (Connected to system SCL line)
47	SDA	I/O	Schmitt Fail Safe	3.3 V 6 mA	I^2C bus data input/output (Connected to system SDA line)
49	AGND	-	-	-	f_{SC} generator DAC section ground
50	AVDD	-	-	-	f_{SC} generator DAC section 2.5 V supply voltage
51	FSCO	O	Analog	2.5 V	f_{SC} generator f_{SC} output
52, 53	AGND	-	-	-	8f_{SC}-PLL ground
54	FSCI	I	Analog	2.5 V	8f_{SC}-PLL f_{SC} input
55	AVDD	-	-	-	8f_{SC}-PLL section 2.5 V supply voltage
56	CKMD	I	LVTTL	3.3 V PD:50	Clock mode test input (Grounded) ('L' : Normal mode, 'H' : 8fsc clock external input mode)

Table 1-1. Pin Functions (2/2)

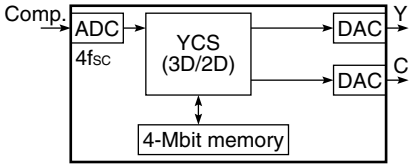
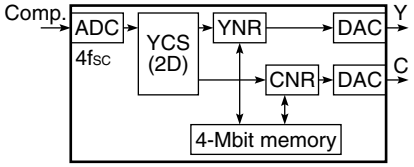
No.	Symbol	I/O	Level	Buffer type PU/PD [kΩ]	Description
57	CLK8	I/O	LVTTL 3-state	3.3 V 6 mA	CKMD = 0 : 8f_{SC} clock output CKMD = 1 : 8fsc clock input
58	RSTB	I	Schmitt	3.3 V PU:50	System reset input (Active-low) (Active-low reset pulse is input from the outside.)
59	ST0	O	LVTTL	3.3 V 3 mA	Internal signal monitor output 0
60	ST1	O	LVTTL	3.3 V 3 mA	Internal signal monitor output 1
61	NSTD	O	LVTTL	3.3 V 3 mA	Nonstandard signal detection monitor output ('L' : standard, 'H' : nonstandard)
63-72	DYCO0-DYCO9	I/O	LVTTL 3-state	3.3 V 3 mA	EXADINS=0: Digital YC signal alternate output EXADINS=1: Digital video data input for external ADC (Pull down unuse lower bit pins via resistor) DYCO0 is the LSB, DYCO9 is the MSB.
73	ALTF	O	LVTTL	3.3 V 3 mA	EXADINS=0: Digital YC signal alternate flag output ('L' : C, 'H' : Y) EXADINS=1: 4f_{SC} clock output for external ADC
74	LINE	I	LVTTL	3.3 V PD:50	Forced inter-line processing selection input ('L' : ordinary processing, 'H' : forced inter-line processing)
76	KIL	I	LVTTL	3.3 V PD:50	External killer input ('L' : ordinary processing, 'H' : forced Y/C separation stop)
77	CSI	I	Schmitt	3.3 V PU:50	Composite sync input (Active-low)
86	AVDD	-	-	-	Y-DAC and C-DAC 2.5 V supply voltage
87	CBPC	O	Analog	2.5 V	C-DAC phase compensation output
88	ACO	O	Analog	2.5 V	C-DAC analog C signal output
89	AYO	O	Analog	2.5 V	Y-DAC analog Y signal output
90	CBPY	O	Analog	2.5 V	Y-DAC phase compensation output
91	AGND	-	-	-	Y-DAC and C-DAC ground
92	AGND	-	-	-	ADC ground
93	AYI	I	Analog	2.5 V	ADC analog composite signal input
94	VCLY	O	Analog	2.5 V	ADC clamp potential output
95	VRBY	O	Analog	2.5 V	ADC bottom reference voltage output
96	VRTY	O	Analog	2.5 V	ADC top reference voltage output
97	VCOMY	O	Analog	2.5 V	ADC common mode reference voltage
98	AVDD	-	-	-	ADC 2.5 V supply voltage

2. SYSTEM OVERVIEW

2.1 Operation Modes

The μPD64084 can operate in the following major four signal processing modes. Mode selection is performed according to NRMD on the serial bus.

Table 2-1. Operation Modes

Serial bus setting Mode name	Function [Note]	Pin input	System clock	Feature Model diagram
NRMD = 0 YCS mode	Y/C separation	AYI : Composite signal	Burst locked clock ($4f_{SC}$, $8f_{SC}$)	• For standard signals, motion-adaptive three-dimensional Y/C separation is performed. • For nonstandard signals, inter-line Y/C separation is performed. 
NRMD = 1 YCS+ mode	2D Y/C separation and YCNR	AYI : Composite signal	Burst locked clock ($4f_{SC}$, $8f_{SC}$)	• Inter-line Y/C separation and Frame recursive YNR and CNR is performed. 

Note 3D Y/C separation, Frame-recursive YNR/CNR, each function is independence. So these don't operate at the same time.

2.2 Filter Processing

Table 2-2 lists filters used in each mode.

★ **Table 2-2. Filter Matrix**

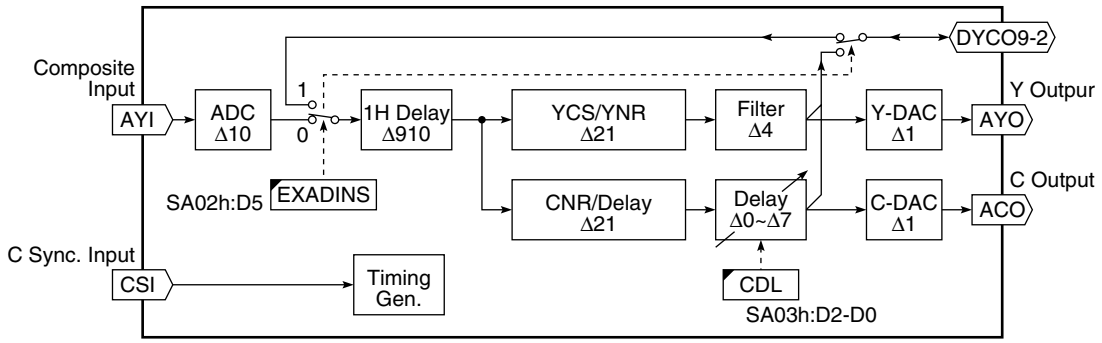
Mode	Standard / nonstandard / killer signal detection	Filter selected			
		Effective-picture period		Blanking period	
		Still picture portion	Moving picture portion	Horizontal (11 μs)	Vertical (1H to 22H)
YCS mode (NRMD = 0)	Standard signal detected	Frame comb	Line comb		Band-pass Note
	Nonstandard signal detected	Line comb			Band-pass Note
	Killer signal detected	Y output: Through (Y/C separation stop) C output: Separated C signal			
YCS+ mode (NRMD = 1)	Standard or horizontal nonstandard signal detected	Line comb + Frame recursive		Line comb	Band-pass Note
	Vertical nonstandard signal detected	Line comb			Band-pass Note
	Killer signal detected	Y output: Through (Y/C separation stop) C output: Separated C signal			
Vertical contour compensation / Y peaking	-	Active			Through

Note Setting serial bus register SA09h: D0 (VFLTH) enables through output.

2.3 System Delay

The following diagram shows a model of system delays (video signal delays).

Figure 2-1. System Delay Model



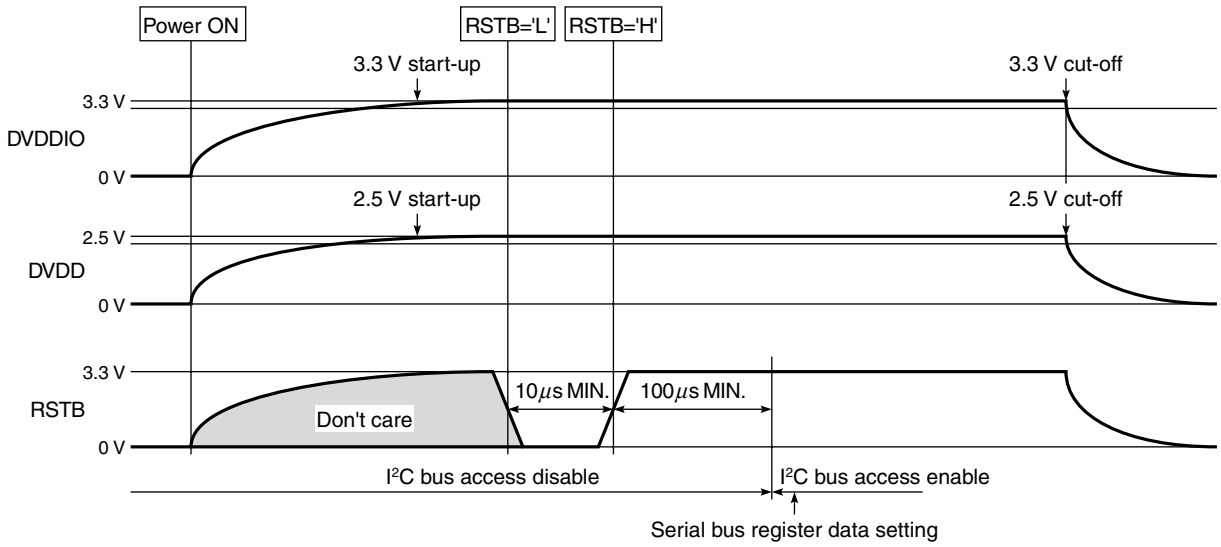
Remark Δ1 corresponds to a one-clock pulse delay (4f_{SC} or 910 f_H = about 69.8 ns).

2.4 Start-up of Power Supply and Reset

It is necessary to reset the I²C bus interface immediately when it is supplied with power. When reset, the I²C bus interface releases its SDA line and becomes operative. In addition, its write register is previously loaded with an initial value.

<1> When the power is switched on, wait until the power supply line reaches and settles on a 3.3-V/2.5-V level before starting initialization.
<2> Initialize the I²C bus interface circuit by keeping the RSTB pin at a low level for at least 10 μs.
<3> Start communication on the I²C bus interface after 100 μs from pull up the RSTB pin to a high level.

Figure 2-2. I²C Bus Interface Reset Sequence

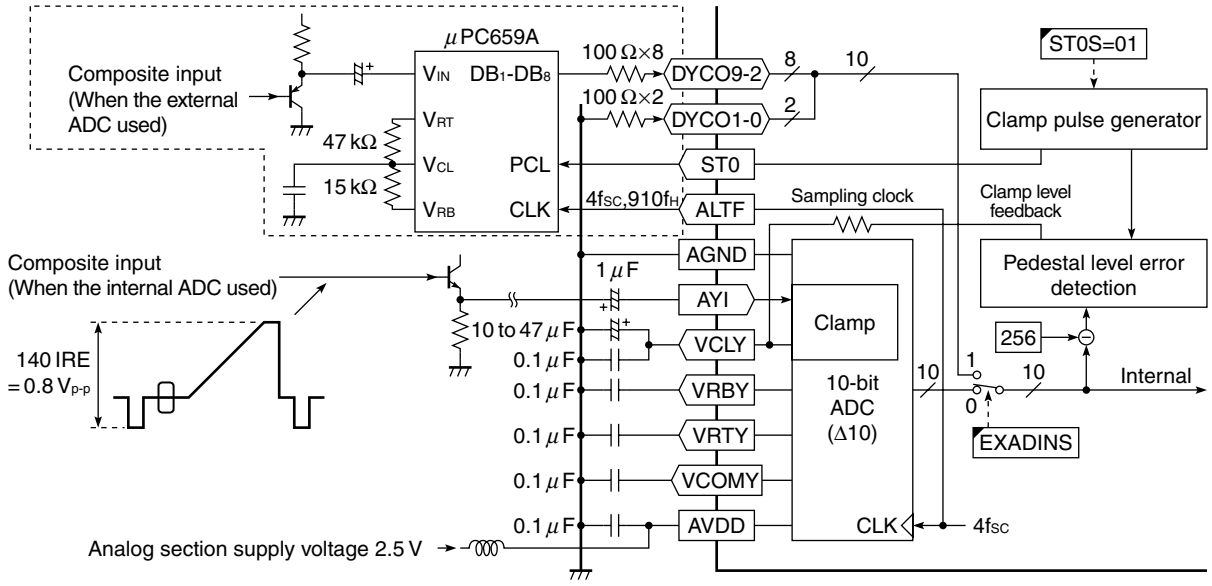


Caution Reset is always necessary whether using the serial bus register or not.

3. VIDEO SIGNAL INPUT BLOCK

This block converts analog video signals to digital form.

Figure 3-1. Video Signal Input Block Diagram



3.1 Video Signal Inputs

The composite signal is input to the AYI pin. This analog video (composite) signal converts to digital video signal at internal 10-bit ADC (EXADINS = 0).

In case of external ADC used, 10-bit composite signals in digital form are input to the DYCO9 to DYCO0 pins (EXADINS = 1).

3.2 Pedestal Level Reproduction

This circuit reproduces the pedestal level of a video signal. The pedestal level error detection circuit detects the difference between that level and the internal fixed value of 256 LSB levels, and outputs the feedback level.

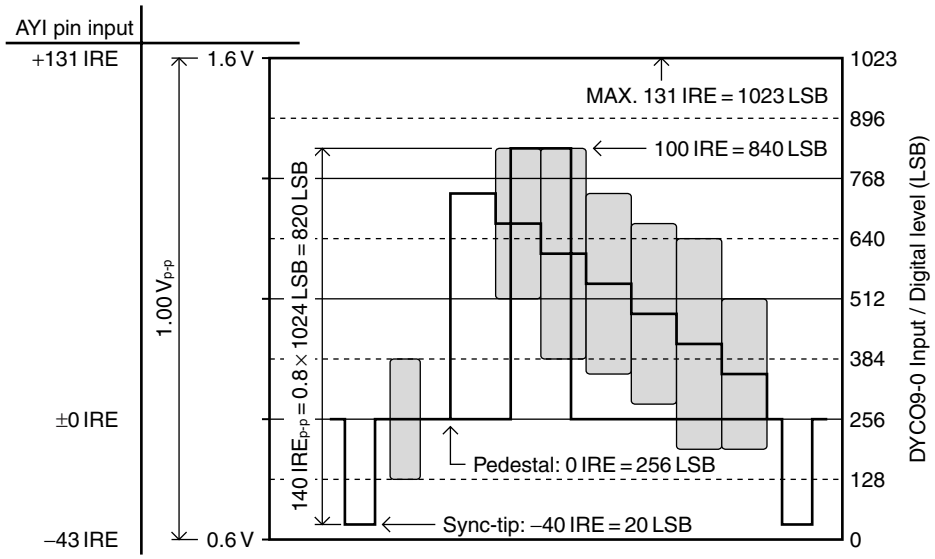
This output signal is connected to VCLY pin via internal resistor to feed back to video signal for fixing pedestal level to 256 LSB. Pull down the VCLY pin via a 0.1 μF bypass capacitor and a 10 to 47 μF electrolysis capacitor for loop filter.

Caution In case of H-Sync input level is bigger than 256LSB, this pedestal level also becomes over 256LSB. Do not use this circuit when the external ADC is used.

3.3 Video Signal Input Level

It is necessary to limit the level of video (composite) signal inputs to within a certain range to cope with the maximum amplitude of the video signal and variations in it. Figure 3-2 shows the waveform of the video signal input whose amplitude is 140 IRE_{p-p} = 820 LSB (0.8 times a maximum input range of 1024 LSB). In this case, it is possible to input a white level of up to 131 IRE for the Y signal and up to 175 IRE_{p-p} for the C signal.

Figure 3-2. Video Signal Input Waveform Example (for 75% Color Bar Input)



Remark The recommended input level of video signals is 140 IRE_{p-p} = 0.8 V_{p-p} (1.00 V × 0.8).

3.4 Pin Treatment

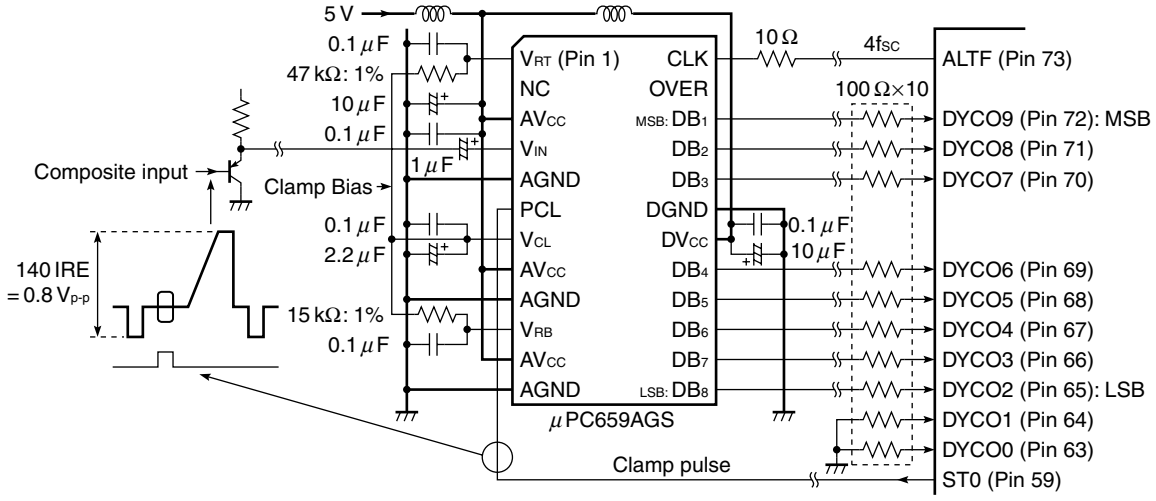
- Supply 2.5 V to the AVDD pins. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible for the ground lines of each bypass capacitor and the AGND pins so as to minimize their impedance.
- Connect a video signal to the AYI pin by capacitive coupling. Maintain low input impedance for video signals. Be sure to keep the wiring between the capacitor and the AYI pin as short as possible.
- Pull down the VRTY, VRBY and VCOMY reference voltage pins via a 0.1 μF bypass capacitor.
- Pull down the VCLY pin via a 0.1 μF bypass capacitor and a 10 to 47 μF electrolysis capacitor.
- Do not bring the digital system wiring (especially the memory system) close to this block and the straight downward of the IC.

3.5 External ADC Connection Method

Setting up EXADINS = 1 on the serial bus puts the IC in the external ADC mode. In this mode, the ALTF pin is used to output 4fSC sampling clock pulses, and the DYCO9 to DYCO0 pins are used to receive digital data inputs. Setting up ST0S = 01 on the serial bus causes a clamp pulse to be output from the ST0 pin. It is used as a pedestal clamp pulse for external ADC. The clamp potential for the pedestal level of external ADC must be determined so that the sampled value becomes about 256 ±8LSB. Supply converted 10-bit data to the DYCO9 to DYCO0 pins via a 100 Ω resistor. For using 8-bit ADC (exp. μPC659A), Pull down the DYCO1 and DYCO0 pins via 100 Ω resistor.

In this mode, for ADC in the μPD64084, keep the VRTY, VRBY and VCOMY pins open, and pull down the VCLY and AYI pins via a 0.1 μF capacitor.

Figure 3-3. Example of Application Circuit Set Up for External ADC

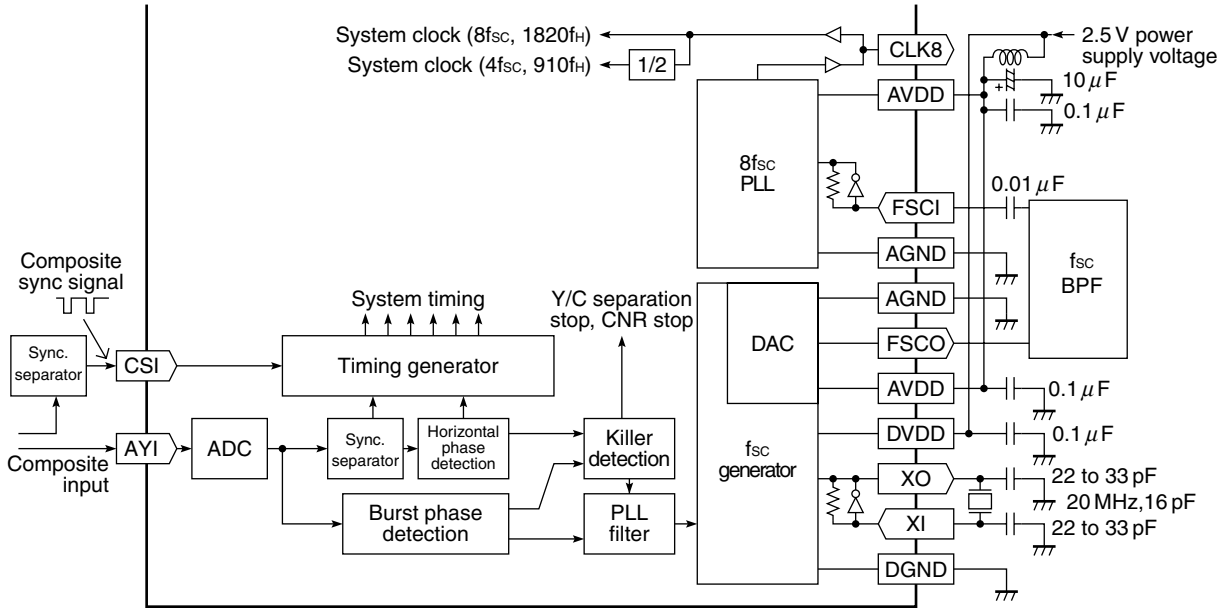


Remark Serial bus registers setting: EXADINS = 1, ST0S = 01

4. CLOCK/TIMING GENERATION BLOCK

This block generates system clock pulses and timing signals from video signals.

Figure 4-1. Clock/Timing Generation Block Diagram



4.1 Sync Separator and Timing Generator

These sections separate horizontal and vertical sync signals from the composite signal sampled at $4f_{SC}$ or $910f_H$, and generate system timing signals by using them as references.

4.2 Composite Sync Signal Input

An active-low composite sync signal separated from the video signal is input at the CSI pin. This input is used as a reference signal to lock onto sync at the timing generator.

4.3 Horizontal/Burst Phase Detection Circuit

The horizontal phase detection circuit extracts the horizontal sync signal from the Y signal sampled at $4f_{SC}$ or $910f_H$ to detect a horizontal phase error. This phase error is used for generation of $227.5f_H$ and timing generator. The burst phase detection circuit extracts the burst signal from the composite signal sampled at $4f_{SC}$ to detect a burst phase error. This phase error is used for f_{SC} generation.

4.4 PLL Filter Circuit

The PLL filter circuit integrates a burst or horizontal phase error to determine the oscillation frequency of the f_{SC} generator ahead.

4.5 Killer Detection Circuit

The killer detection circuit compares the amplitude of the burst signal with the KILR value set on the serial bus to judge on a color killer. If the burst amplitude becomes smaller than or equal to the set KILR value when the burst locked clock is operating, the f_{SC} generator is allowed to free-run.

4.6 fsc Generator

The fsc generator generates fsc (or 227.5fH when the line locked clock is running) from an oscillation frequency determined in the PLL filter. fsc is converted by internal DAC to an analog sine waveform before it is output from the FSCO pin. Because this output contains harmonic components, they must be removed using an external band-pass filter (BPF) connected via a buffer, before the analog sine waveform is input to the FSCI pin via a capacitor. The fsc generator uses a 20 MHz free-run clock pulse as a reference.

4.7 8fsc-PLL Circuit

The 8fsc-PLL circuit generates 8fsc (or 1820fH) from fsc (or 227.5fH) input at the FSCI pin. The 8fsc signal is output from the CLK8 pin. It is also used as the internal system clock.

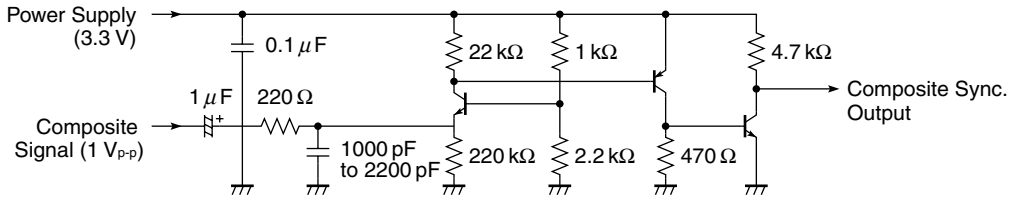
4.8 Pin Treatment

- Supply 2.5 V to the AVDD pins. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible for the ground lines of each bypass capacitor and the DGND and AGND pins so as to minimize their impedance.
- Connect a 20-MHz Crystal resonator across the XI and XO pins. Provide guard areas using ground patterns to keep these pins from interfering with other blocks. Table 4-1 shows the crystal resonator specification example.
- Connect a BPF to the FSCO pin via an emitter follower. Supply the fsc signal to the FSCI pin via a capacitor.
- Pull down the RPLL pin via a 0 Ω resistor.
- Input an active-low composite sync signal to the CSI pin. Figure 4-2 shows the external composite sync separator application circuit example.

Table 4-1. Crystal Resonator Specification Example

Parameter	Specification
Frequency	20.000000 MHz
Load Capacitance	16 pF
Equivalent Serial Resistance	40 Ω or less
Frequency Permitted Tolerance	50 ppm or less
Frequency Temperature Tolerance	50 ppm or less

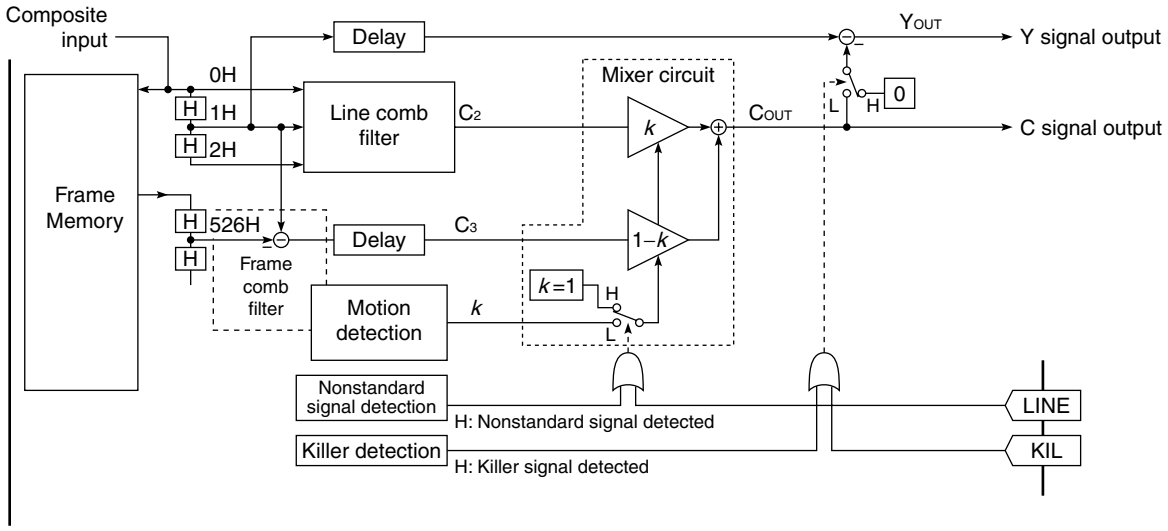
Figure 4-2. External Composite Sync Separator Application Circuit Example



5. COMB FILTER BLOCK

This block performs Y/C separation or frame comb type YNR according to the result of checks in various detection circuits.

Figure 5-1. Comb Filter Block Diagram



5.1 Line Comb Filter

The C signal is separated from video signals that have been delayed by 0H, 1H, and 2H. This filter serves as a logical comb filter based on inter-line correlation to reduce dot and cross-color interference. The filter output (C_2) is used in the moving picture portion of standard signals, nonstandard signals, and blanking periods.

5.2 Frame Comb Filter

The C signal is separated from video signals that have been delayed by 1H and 526H. The filter output (C_3) is used in still picture portions by the motion detection circuit.

5.3 Mixer Circuit

The mixer circuit mixes C signals to adapt to the motion according to the motion factor from the motion detection circuit. In other words, C_{OUT} is generated by mixing the line comb filter output (C_2) and the frame comb filter output (C_3) by a mixture ratio according to the motion factor k (0 to 1). If the input signal is a nonstandard signal, or if the LINE pin is at a high level, C_2 is output without performing motion-adaptive mixture.

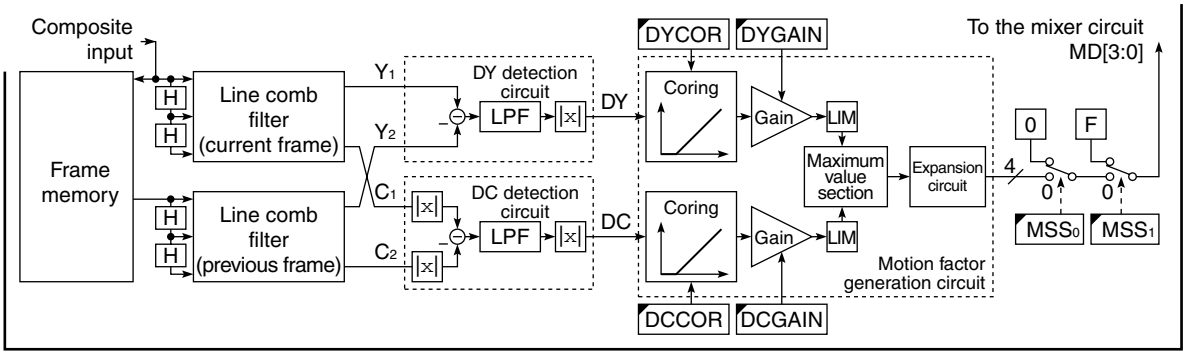
5.4 C Signal Subtraction

The Y_{OUT} signal is separated by subtracting the C_{OUT} signal from a composite video signal that has been delayed by 1H. Subtraction is quitted when the killer detection circuit detects that the input signal is a color killer signal (monochrome signal or non-burst signal) or that the KIL pin is at an 'H' level.

6. MOTION DETECTION BLOCK

This block generates a 4-bit motion factor indicating an inter-frame motion level from the video signal inter-frame difference. This motion factor is used as a mixture ratio to indicate how the frame and line comb filter outputs are mixed. This block is used in the YCS mode.

Figure 6-1. Motion Detection Block Diagram



6.1 Line Comb Filter

Before obtaining an inter-frame difference, the line comb filter performs Y/C separation for the composite signals of both frames.

6.2 DY Detection Circuit

The DY detection circuit detects a Y signal inter-frame difference. After a Y signal difference between the current and previous frames is obtained, its absolute value, obtained by limiting the frequency band for the Y signal difference using an LPF, is output as a Y frame difference signal, or a DY signal.

6.3 DC Detection Circuit

The DC detection circuit detects a C signal inter-frame difference. After a C signal difference between the current and previous frames is obtained, its absolute value, obtained by limiting the frequency band for the C signal difference using an LPF, is output as a C frame difference signal, or a DC signal. Because the phase of the C signal is inverted between frames, the absolute values of the C signals of both frames have been obtained before the difference is obtained.

6.4 Motion Factor Generation Circuit

The motion factor generation circuit generates a 4-bit motion factor from the DY and DC signals. The first coring circuit performs coring according to the DYCOR and DCCOR settings on the serial bus to block weak signals like noise. The gain adjustment circuits ahead perform gain adjustment according to the DYGAIN and DCGAIN settings on the serial bus to specify the sensitivity of the motion factor. These outputs are limited to a 4-bit width, and one having a higher level is selected for output by the maximum value selection circuit. The selected signal is expanded horizontally, then output as a final motion factor.

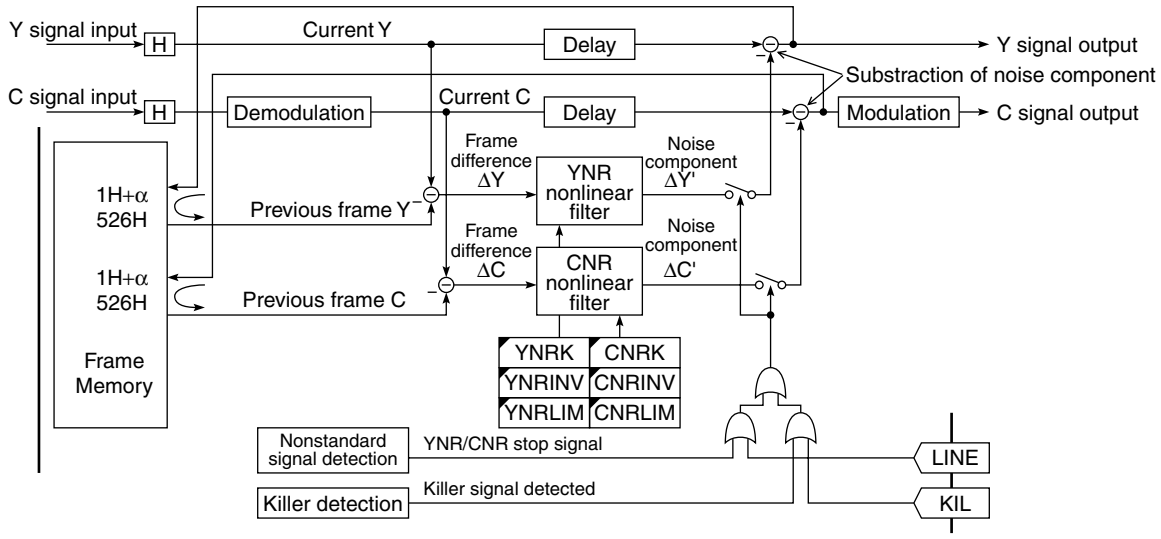
6.5 Forcible Control for The Motion Factor

The motion factor can be set to 0 (forced stop) or a maximum value (forced motion) using the MSS signal on the serial bus.

7. YNR/CNR BLOCK

This block performs frame recursive YNR and CNR. It is used in the YCS+ mode.

Figure 7-1. YNR/CNR Block Diagram



7.1 YNR/CNR Processing

The frame difference (ΔY) signal is generated by subtracting the previous frame Y signal from the current frame Y signal. The noise component ΔY' signal is extracted by eliminating the motion component of the ΔY signal at the nonlinear filter. Noise components are reduced by subtracting the noise component ΔY' signal from the current frame Y signal. At the same time, the Y signal submitted to noise reduction is delayed by a frame to be used to generate ΔY for the next frame. This way the frame recursive YNR is configured. Much the same processing is performed for the C signal to reduce noise components.

7.2 Nonlinear Filter

The ΔY' and ΔC' noise components are extracted from ΔY and ΔC. ΔY and ΔC contain inter-frame motion components and noise components. Subtracting ΔY and ΔC from the current frame Y and C signals causes inter-frame motion components to remain in the output picture. To solve this problem, a nonlinear filter that passes only low-amplitude signals is used; generally, motion components have a large amplitude, while noise components have a small amplitude. How nonlinear the filter is to be is specified using YNRK, YNRLIM, YNRINV, CNRK, CNRLIM, and CNRINV on the serial bus.

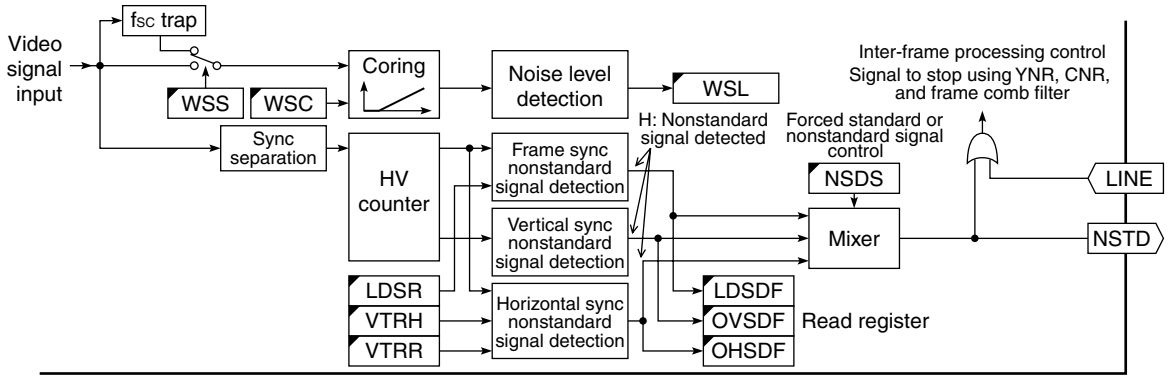
7.3 YNR/CNR Operation Stop

If the nonstandard signal detection circuit detects a vertical nonstandard signal or frame sync nonstandard signal, or the LINE pin is at a high level, the killer detection circuit detects a color killer signal, or the KIL pin is at a high level, YNR and CNR operations are stopped.

8. NONSTANDARD SIGNAL DETECTION BLOCK

This block detects nonstandard signals not conforming to the NTSC standard, such as VCR playback signals, home TV game signals, and Laser-Disc special playback signals. The detection result is used to stop inter-frame video processing. (and selects intra-field video processing forcibly.)

Figure 8-1. Nonstandard Signal Detection Block Diagram



8.1 Horizontal Sync Nonstandard Signal Detection

The horizontal sync nonstandard signal detection circuit detects signals not having a standard relationship between f_{SC} and f_H ($f_{SC} = 227.5f_H$) like a VCR playback signal. The sensitivity of detection is set using VTRR and VTRH on the serial bus. If the circuit detects a nonstandard signal, it stops using the frame comb filter. The detection result can be read using OHSDF on the serial bus.

8.2 Vertical Sync Nonstandard Signal Detection

The vertical sync nonstandard signal detection circuit detects signals not having a standard relationship between f_H and f_V ($f_H = 262.5f_V$) like a VCR special playback signal and home TV game signal. The sensitivity of detection cannot be set. If the circuit detects a nonstandard signal, it stops using the frame comb filter, YNR, and CNR. The detection result can be read using OVSDF on the serial bus.

8.3 Frame Sync Nonstandard Signal Detection

The frame sync nonstandard signal detection circuit detects signals out of horizontal sync phase between frames, such as a laser-disc special playback signal. The sensitivity of detection is set using LDSR on the serial bus. If the circuit detects a nonstandard signal, it stops using the frame comb filter, YNR, and CNR. The detection result can be read using LDSDF on the serial bus.

8.4 Forced Standard or Nonstandard Signal Control

It is possible to specify either forced standard or nonstandard signal control using NSDS on the serial bus.

8.5 Noise Level Detection

The noise level detection circuit detects a noise level in the flat portion of a video signal. The sensitivity of detection is set using WSCOR on the serial bus. The detection result can be read using WSL on the serial bus; it is not used in the IC. The detection result can be processed in a microprocessor to find a weak electric field.

9. WCV-ID DECODER / ID-1 DECODER BLOCK

This block decodes ID-1 signal of 20H/283H and an identification control signal superimposed on a wide clear vision signal of 22H and 285H (The wide clear vision standard applies only in Japan).

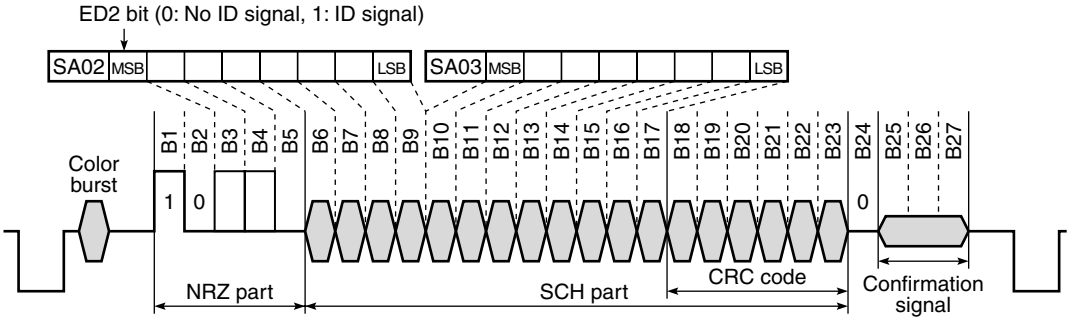
9.1 WCV-ID Decoder

The WCV-ID decoder checks whether the video signal contains an ID signal by examining mainly the following seven items. If all these items turn out to be normal, an ID signal is detected. The check and decode results are output to the ED2 bit and bits B3 to B17 on the serial bus, respectively. In addition, the phase of the confirmation signal is detected.

<1> A difference in DC level between B1 and B2 is not smaller than a certain value.
<2> The DC level of the SCH part is not higher than a certain value.
<3> The f_{SC} amplitude of the NRZ part is not larger than a certain value.
<4> The f_{SC} amplitude of the SCH part is not smaller than a certain value (if FSCOFF = 0),
<5> Items <1> to <4> continue for at least 12 fields.
<6> The parity of the NRZ part (B3 to B5) is normal. Note
<7> The CRC of the NRZ part and SCH part (B3 to B23) is normal. Note

Note If an error is detected in item <6> or <7>, bits B3 to B17 on the serial bus hold the decoded value for the previous field.

Figure 9-1. Wide Clear Vision ID Signal Configuration



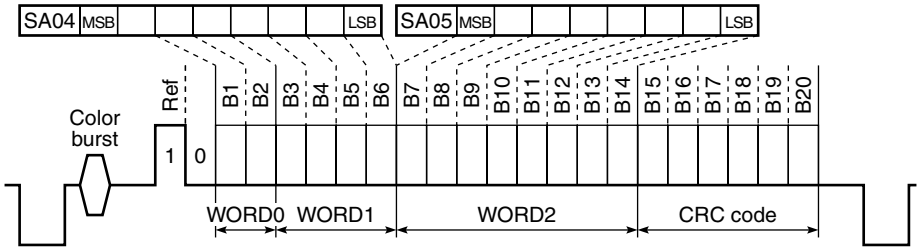
9.2 ID-1 Decoder

The ID-1 decoder checks whether the video signal contains an ID-1 signal by examining mainly the following five items. If all these items turn out to be normal, an ID signal is detected.

<1> A difference of DC level between Ref signal and the pedestal level is not smaller than a certain value.
<2> The width of each bit is not smaller than a certain value.
<3> Items <1> to <2> continue for at least 6 fields. (When FELCHK register is set to zero, this check is disable)
<4> CRC check is passed.

Remark If any errors are detected in item <1> to <3>, the output for serial bus hold the decoded value for the previous field.
If item <3> is disabled by setting FELCHK register to zero, CRC check is also disabled.
If any errors are detected by CRC check, the output for serial bus will be initialized.
Initial values of serial bus registers are WORD0 = 00, WORD1 = 1111, WORD2 = 00h.

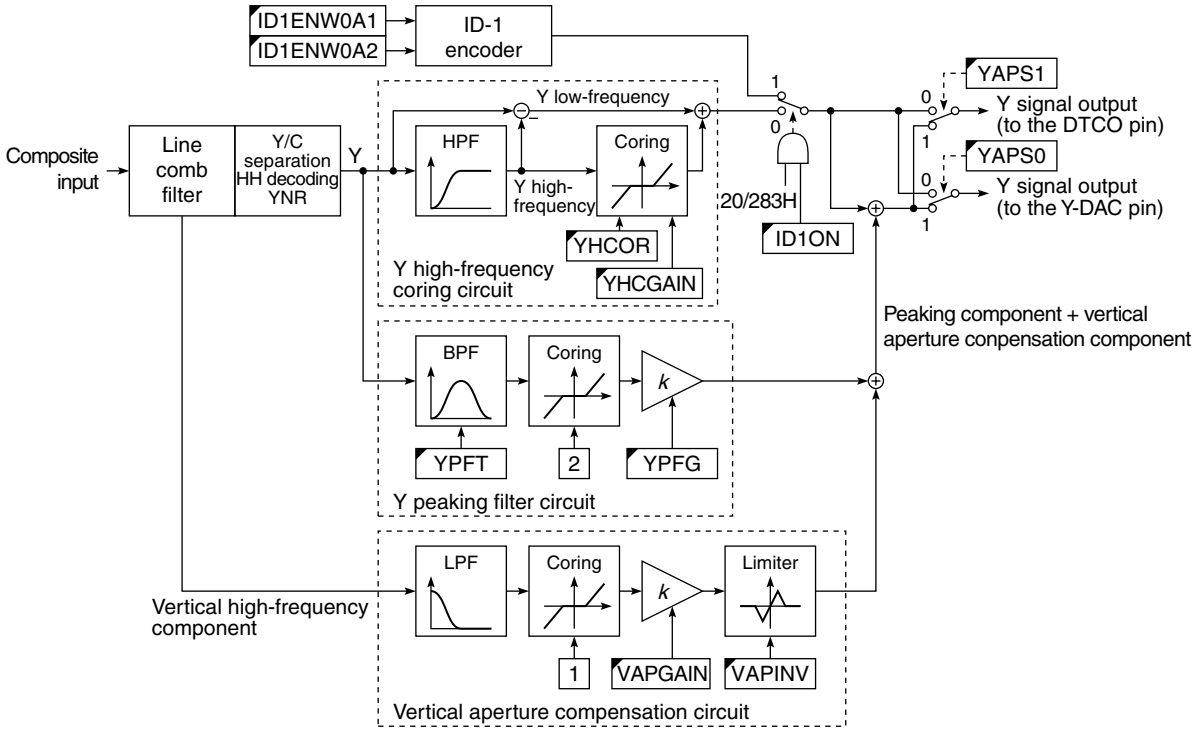
Figure 9-2. ID-1 Signal Configuration



10. Y SIGNAL OUTPUT PROCESSING BLOCK

After Y/C separation or Y Noise reduction, this block performs high-frequency coring, peaking, and vertical aperture compensation for the Y signal submitted to YNR processing.

Figure 10-1. Y Signal Output Processing Block Diagram



10.1 Y High-Frequency Coring Circuit

The Y high-frequency coring circuit performs coring for the high-frequency component of the Y main line signal. It works as a simplified noise reducer, because it can eliminate high-frequency components at 1 LSB to 3 LSB levels. The coring level is set using YHCOR on the serial bus.

<1> HPF circuit : Separates the input Y signal into the low- and high-frequency components.

<2> Coring circuit : Performs coring for Y high-frequency components according to the YHCOR setting, and outputs a Y signal by adding the Y high- and low-frequency components after they are submitted to coring. The coring effect can set 1/2 times by the YHCGAIN setting.

10.2 Y Peaking Filter Circuit

The Y peaking filter circuit performs peaking processing for the Y signal to correct the frequency response of the Y signal.

<1> BPF circuit : Extracts high-frequency components from the original Y signal according to the YPFT setting on the serial bus. The center frequency of the BPF can be selected from 3.58, 3.86, 4.08, and 4.22 MHz.

<2> Coring circuit : Performs ±2LSB (in 8-bit terms) coring for Y high-frequency components to prevent S/N deterioration during peaking processing.

<3> Gain adjustment circuit : Performs gain adjustment for peaking components according to the YPFG setting on the serial bus. The gain to be added can be changed in 16 steps over a range between −1.000 times and +0.875 times.

<4> Addition to the main line : Y peaking components, together with vertical aperture compensation components, are added to the Y signal.

10.3 Vertical Aperture Compensation Circuit

The vertical aperture compensation circuit extracts vertical contour components from a Y signal and adds them to the Y signal to emphasize contours.

<1> Line comb filter : Extracts vertical high-frequency components from the video signal.

<2> LPF circuit : Eliminates C signal components and Y signal slant components to extract vertical contour components.

<3> Coring circuit : Performs ±1LSB (in 8-bit terms) coring for vertical high-frequency components to prevent S/N deterioration during aperture compensation.

<4> Gain adjustment circuit : Performs gain adjustment for aperture compensation components according to the VAPGAIN setting on the serial bus.

<5> Limiter circuit (nonlinear processing) :

Performs limit processing for aperture compensation components according to the VAPINV setting on the serial bus. Signals for which contours are to be emphasized are rather weak ones. Uniform emphasis would result in initially large signals becoming too large. To solve this problem, the limiter circuit blocks signals larger than the VAPINV setting, thereby disabling contour emphasis for large signals.

<6> Addition to the main line : Vertical aperture compensation components, together with Y peaking components, are added to the Y signal.

10.4 Turning On/Off Y Peaking and Vertical Aperture Compensation

The YAPS setting on the serial bus can be used to turn Y peaking and vertical aperture compensation on and off.

10.5 ID-1 Encoder

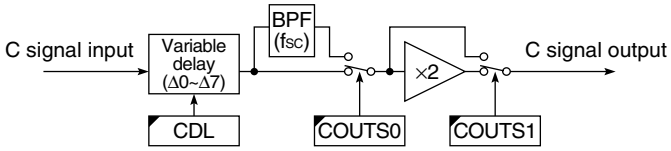
Bit information conforming to the ID-1 standard (CPX-1204) can be superimposed on the Y signal output at 20H/283H. ID1ENON on the serial bus specifies whether to turn on or off superimposition. ID1ENW0A1 and ID1ENW0A2 specify the bit information to be superimposed.

If ID-1 information has already be superimposed on the original signal, it will be replaced with the newly specified ID-1 information.

11. C SIGNAL OUTPUT PROCESSING BLOCK

After Y/C separation, the C signal output processing block performs delay adjustment, BPF processing, and gain adjustment for the C signal submitted to CNR processing.

Figure 11-1. C Signal Output Processing Block Diagram



11.1 C Signal Delay Adjustment

The delay time of the C signal can be varied in a range between 0 and 7 clock pulses (4f_{SC}) according to CDL on the serial bus. This way, the delay of the C signal relative to the Y signal can be set to anywhere between −4 clock pulses (−280 ns) and +3 clock pulses (+210 ns).

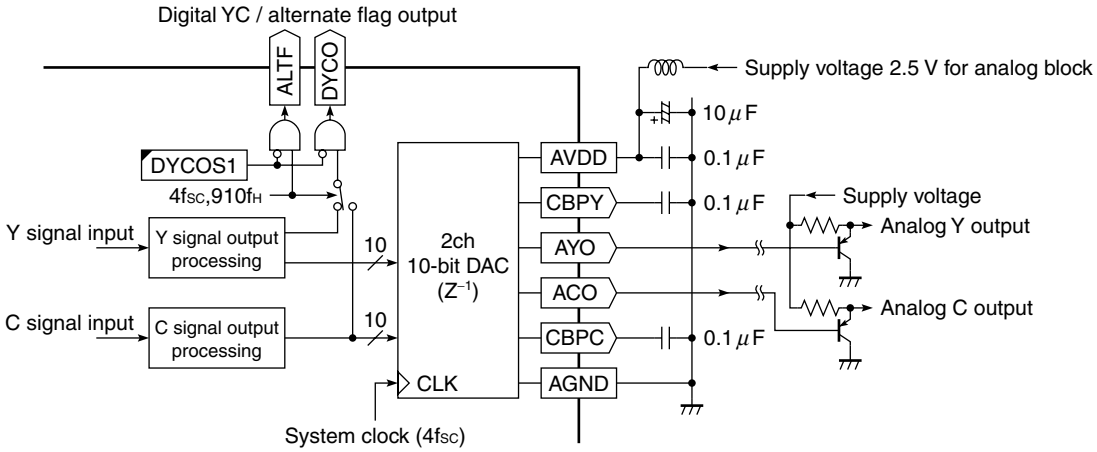
11.2 BPF and Gain Processing

COUTS on the serial bus can be used to specify whether to insert a BPF. It can also be used to specify the gain (×2 or ×1).

12. VIDEO SIGNAL OUTPUT BLOCK

The video signal output block can convert digital video signals to analog form. It can also output digital video signals without performing D/A conversion.

Figure 12-1. Video Signal Output Block Diagram



12.1 Digital YC Output Processing

When setting up DYCOS = 00 on the serial bus, DYCO9 (MSB) to DYCO0 (LSB) pins alternately output 10 bits of Y signals in straight binary and 10 bits of C signals in offset binary. And ALTF pin outputs alternative flag of Y or C signals. When ALTF = 'L' means "C Signal Outputs", when ALTF = 'H' means "Y Signal Outputs".

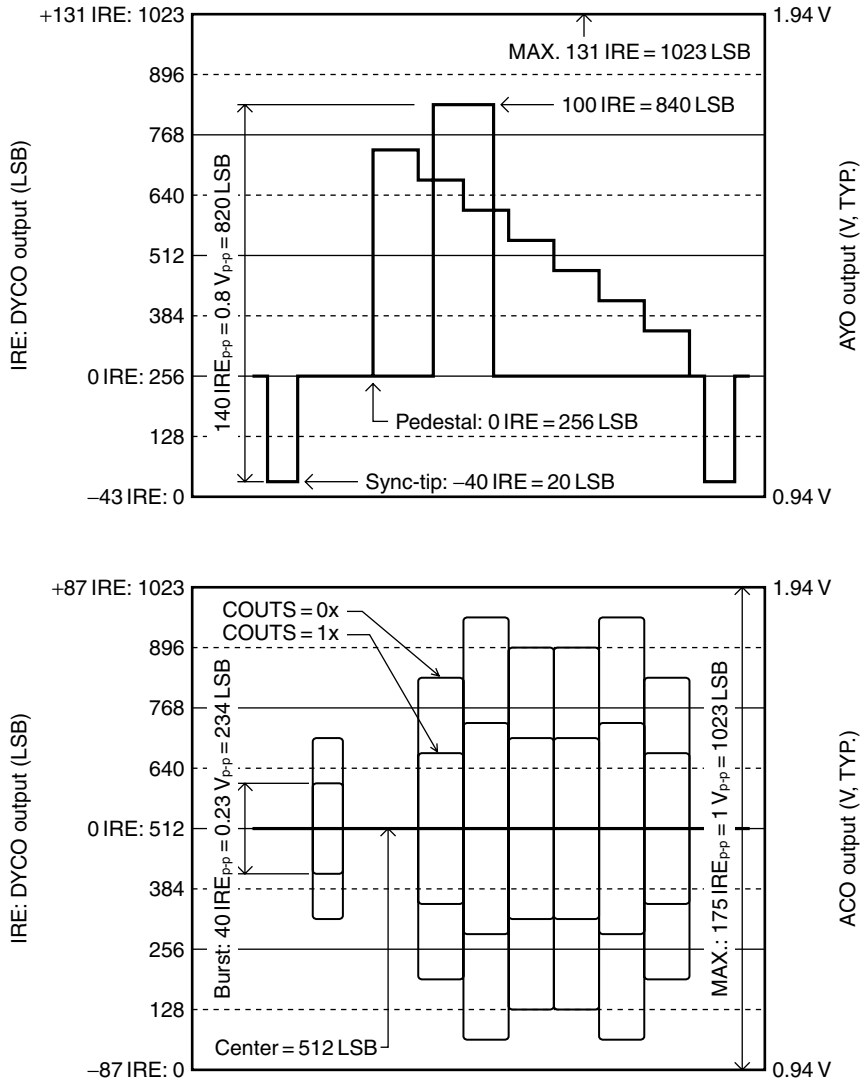
When setting up DYCOS = 1x on the serial bus, DYCO9 (MSB) to DYCO0 (LSB) and ALTF pins are high-impedance. When the DYCO pins are not used, setting DYCOS = 1x on the serial bus reduces radiation noise of these pins.

When the external ADC is used, DYCO9 to DYCO0 pins are used as the digital input terminal of video signal. So the digital YC output is not available.

12.2 Video Signal Output Level

Figure 12-2 shows sample waveforms that would be observed at the AYO and ACO pins after a typical video signal is input (see **3. VIDEO SIGNAL INPUT BLOCK**).

Figure 12-2. Video Signal Output Waveform Example (for 75 % Color Bar Input)



12.3 Pin Treatment

- Supply 2.5 V to the AVDD pins and supply 3.3 V to the DVDDIO pin. Isolate them sufficiently from the digital section power supply.
- Use as wide wiring patterns as possible as the ground lines of each bypass capacitor and the AGND pins so as to minimize their impedance.
- Pull down the CBPY and CBPC pins via a 0.1 μF bypass capacitor.
- When DAC aren't used, connect AGND pin to digital ground, AVDD pin to digital power supply, and AYO, ACO, CBPY and CBPC pins set open.
- When the digital I/O pin DYCO9 to DYCO0 aren't used, these pins set open.

13. EXTEND DIGITAL INPUT / OUTPUT

This device have the extend digital I/O terminals EXTDYCO9-EXTDYCO0 in addition to DYCO9-DYCO0.

Using these terminals, the digital in to digital out system is available.

Table 13-1. Mode setting for extend digital I/O terminals

Serial bus			Condition of each terminals					
EXTDYCO	EXADINS	DYCOS[1]	DYCOn	EXTDYCOn	ALTF	EXTALTF	A/D	D/A
0	0	0	OUT	Low Note	FLAG	Low	ON	ON
0	1	x	IN	Low Note	4fsc	Low	OFF	ON
0	0	1	Low Note	Low Note	Low	Low	ON	ON
1	0	0	OUT	Low Note	FLAG	Low	ON	ON
1	1	0	OUT	IN	FLAG	4fsc	OFF	ON
1	0	1	Low Note	OUT	Low	FLAG	ON	ON
1	1	1	IN	OUT	4fsc	FLAG	OFF	ON

Note By setting HIZEN (SA16h, D4) = 1, these pin status are set to Hi-Z.

13.1 Usage of extend digital I/O terminals

The extended digital I/O pin EXTDYCO9 to EXTDYCO0 becomes effective by setting serial bus to EXTDYCO = 1.

At this time, internal ADC can not be available. The I/O mode selection of EXTDYCO9 to EXTDYCO0 are set by serial bus DYCOS.

When using input mode of DYCOn or EXTDYCOn pins, insert serial resistor in the lines.

13.2 Digital YC output format

The specification of the digital input and output for the extended digital I/O pin EXTDYCO9 to EXTDYCO0 is same as usual digital I/O pin DYCO9 to DYCO0. When using in input mode, input 10-bit digitized composite video signal that is sampled by 4fsc. And when using in output mode, EXTDYCO9 (MSB) to EXTDYCO0 (LSB) pins alternately output 10 bits of Y signals in straight binary and 10 bits of C signals in offset binary. And EXTALTF pin outputs alternative flag of Y or C signals. When ALTF = 'L' means "C Signal Outputs", when ALTF = 'H' means "Y Signal Outputs".

The internal ADC and extended digital I/O can’t work at the same time. And extended digital I/O pins have 3.3 V resistant.

13.3 Pin Treatment

- When the extended digital I/O pin EXTDYCO9 to EXTDYCO0 aren't used, these pins set open.

★ 14. DIGITAL CONNECTION WITH GHOST REDUCER IC μPD64031A

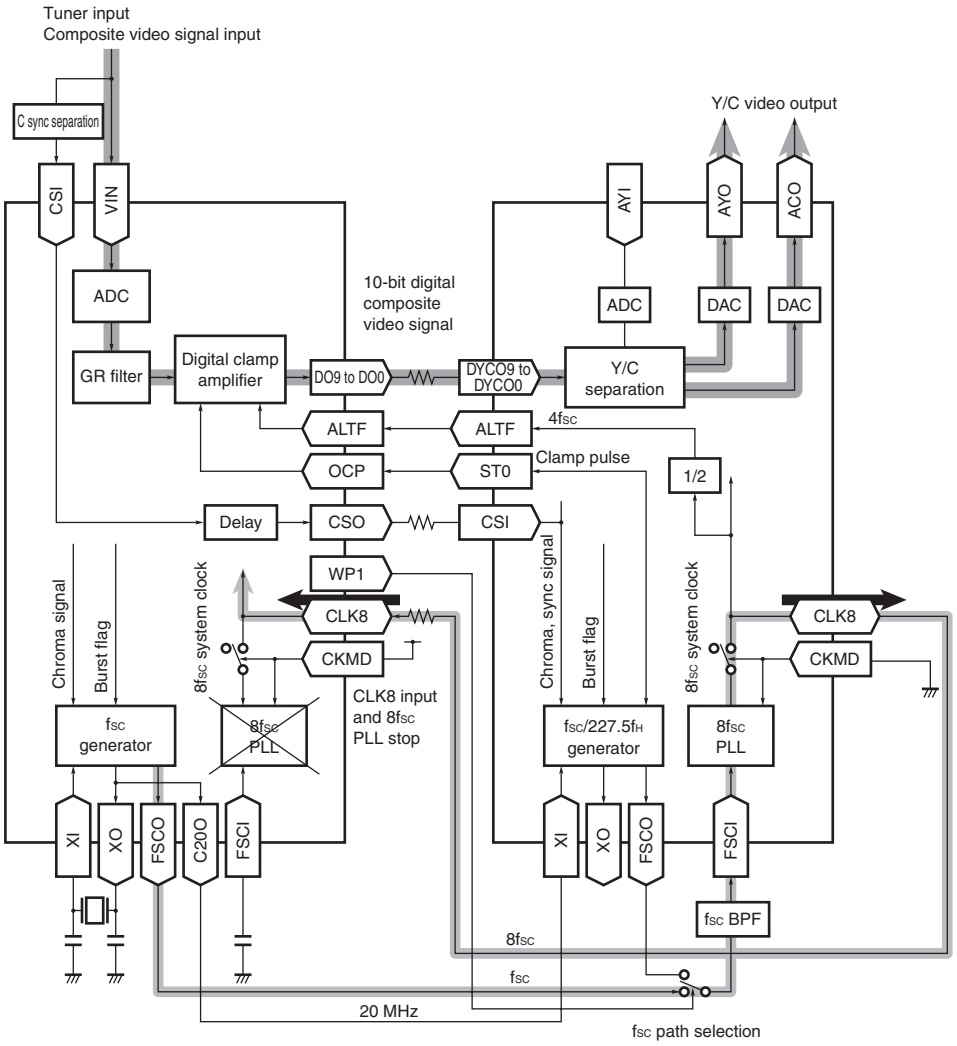
The μPD64084 can perform processing from ghost reduction to three-dimension Y/C separation digitally in 10-bit units when it is directly connected to NEC Electronics' ghost reducer IC μPD64031A.

Figure 14-1 shows the system configuration when the μPD64031A and μPD64084 are digitally connected directly.

14.1 Outline

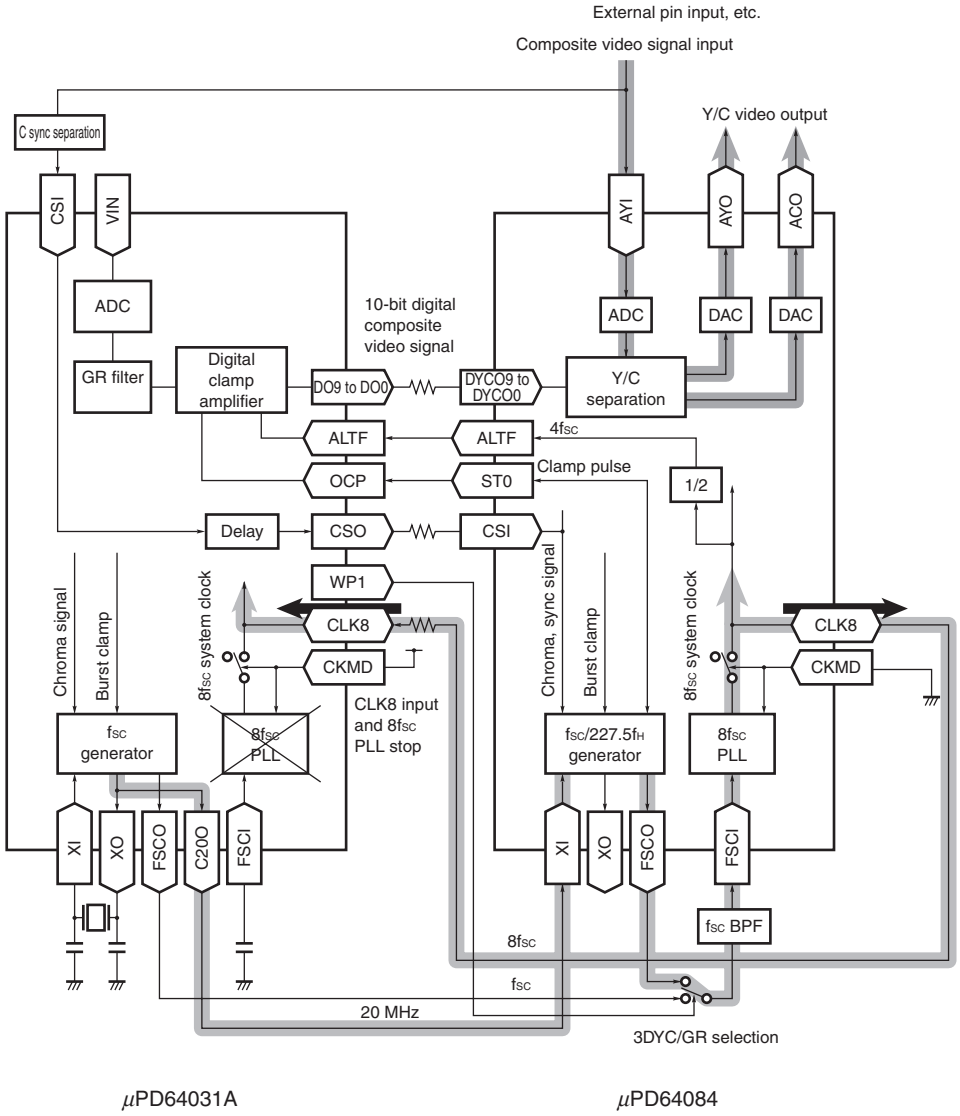
When signals are input from a ground wave tuner, the composite video signal is first input to the A/D converter of the μPD64031A, where the ghost of the signal is reduced. The digital clamp circuit then adjusts the pedestal level, and the digital amplifier circuit adjusts the amplitude of the signal. As a result, a 10-bit digital composite video signal is sent to the three-dimension Y/C separation IC μPD64084. The μPD64084 then performs processing such as Y/C separation and outputs a Y/C video signal that has been converted into an analog signal (see Figure 14-1).

Figure 14-1. Example of Digital Connection System with Ghost Reducer (when signals are input from tuner)



When signals are input from video (composite or S input), the μPD64031A is not used, and the video signal is directly input to the A/D converter of the μPD64084 (see Figure 14-2).

Figure 14-2. Example of Digital Connection System without Ghost Reducer (when signals are input from external source)



14.2 System Configuration and Control Method

14.2.1 Selecting video signal input path

When a video signal is input from a tuner or external pin, the input path of the video signal must be selected. This selection is made by a serial bus register of the μPD64084. If the signal is input from a tuner when the ghost reducer is used, a digital video signal input pin is selected by the μPD64084. When signals are input from other external pins (such as those of a VCR, DVD, video camera, or game machine), the internal A/D converter of the μPD64084 is made valid, so that the video signal directly input to the μPD64084 becomes valid.

For details on how to set the pins and registers, see **Table 14-1 and Table 14-2 in Section 14.3**.

14.2.2 Selecting mode according to clock and video signal input path

When the μPD64031A and μPD64084 are digitally connected directly, the system clock must be shared by the two ICs. When the ghost reducer is used (when signals are input from a tuner), the μPD64031A generates burst lock clock fSC, as shown in Figure 14-1. This fSC goes through an external BPF and is input to the 8fSC PLL of the μPD64084, where system clocks (8fSC and 4fSC) are generated. These system clocks are used by the μPD64084, and are also supplied to the μPD64031A by the μPD64084 from the CLK8 pin.

When the ghost reducer is not used (when signals are input from an external source), the video signal is not input to the μPD64031A, and only the μPD64084 operates. It is therefore necessary that the burst clock generated by the μPD64084 be used.

To switch the path of inputting fSC to the fSC BPF between the FSCO pin of the μPD64031A and the FSCO pin of the μPD64084, an analog switch is necessary in the input block of the fSC BPF.

This analog switch is controlled by the WP1 pin of the μPD64031A. The WP1 pin is controlled by register DIR3DYC (SA08h: D7 and D6) of the μPD64031A (that selects a three-dimension Y/C separation digital connection mode). By changing the setting of this register depending on whether the ghost reducer is used or not, the analog switch can be controlled by the signal output from the WP1 pin. In this way, the fSC path can be changed.

A 20-MHz crystal oscillator that generates the basic clock for the fSC generator should be provided to the μPD64031A. When the ghost reducer is not used and the μPD64084 operates alone, the 20-MHz clock output from the C20O pin of the μPD64031A is used.

For details on how to set the pins and registers, see **Table 14-1 and Table 14-2 in Section 14.3**.

14.3 Setting of Digital Direct-Connected System

14.3.1 Hardware setting

See the pin connection and setting in the following table to digitally connect the μPD64031A and μPD64084 directly.

Table 14-1. Pin Setting for Digital Direct-Connection

μPD64031A Pin	Signal Direction	μPD64084 Pin	Function
DO9 to DO0 (pins 6 to 15)	→	DYCO0 to DYCO9 (pins 63 to 72)	10-bit digital video signal interface
N3D (pin 3)	→	LINE (pin 74)	Three-dimension processing prohibiting flag Register N3D1STEN of the μPD64031A (SA01h: D5) must be set.
CSO (pin 4)	→	CSI (pin 77)	Composite sync signal The signal from the sync separation circuit connected to the μPD64031A is shared by the μPD64084.
ALTF (pin 5)	←	ALTF (pin 73)	Digital clamp clock ($4f_{SC}$) Register ADCLKS of the μPD64084 (SA15h: D7 and D6) must be set.
OCP (pin 18)	←	ST0 (pin 59)	Clamp pulse for digital clamp circuit Register ST0S of the μPD64084 (SA07h: D1 and D0) must be set.
CLK8 (pin 30)	←	CLK8 (pin 57)	System clock ($8f_{SC}$) Register CLK8OFF of the μPD64084 (SA07h: D4) must be set.
FSCO (pin 47)	→	FSCI (pin 54)	Burst lock clock (connected via an analog switch)
C20O (pin 54)	→	XI (pin 36)	20-MHz reference clock
CKMD (pin 31)	–	–	Fixed to high level (external clock mode)
WP1 (pin 35)	–	–	Connected to analog switch (control signal output) This pin is controlled by register DIR3DYC of the μPD64031A (SA08h: D7 and D6) to select a clock path.
EXDAS (pin 58)	–	–	Fixed to high level (digital output is valid)
FSCI (pin 40)	–	–	Fixed to GND (f_{SC} generator is not used)
–	–	FSCO (pin 51)	Connected to analog switch
–	–	XO (pin 37)	Open

14.3.2 Register setting

Correctly set the following registers when digitally connecting the μPD64031A and μPD64084 directly.

Also refer to the following table for register setting to specify whether the ghost reducer is used or not.

Table 14-2. Register Setting

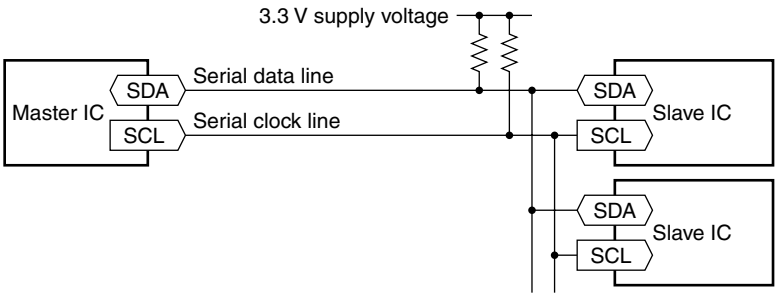
Register	With Ghost Reducer Used	With Ghost Reducer Not Used	Remark
μPD64031A			
EXDAS (SA01h: D7)	1	Don't care	Digital data output setting
N3D1STEN (SA01h: D5)	1	Don't care	3-dimesnion processing prohibiting flag setting
CLK20LOW (SA01h: D2)	0	Don't care	20-MHz clock output setting
ADCPMD (SA04h: D5, D4)	10		ADC input bias mode setting
DIR3DYC (SA08h: D7, D6)	10	11	Mode selection (WP1 pin control)
DCPAG (SA08h: D5 to D3)	101	Don't care	Digital clamp characteristic setting
DCPEN (SA09h: D6)	1	Don't care	Digital clamp selection
DCPLPFS (SA09h: D5)	1	Don't care	Error calculation block LPF selection
DCPVEN (SA09h: D4)	1	Don't care	Clamp timing setting
DCP_TEST (SA09h: D3 to D0)	1111	Don't care	Permissible error range during clamping
μPD64084			
EXADINS (SA02h: D5)	1	0	Internal ADC selection
CLK8OFF (SA07h: D4)	0		$8f_{SC}$ output setting
ST0S (SA07h: D1, D0)	01	Don't care	Clamp pulse output setting
ADCLKS (SA15h: D7, D6)	01	11	ALTF clock delay setting
HIZEN (SA16h: D4)	1		Digital input / output status select

15. I²C BUS INTERFACE

15.1 Basic Specification

The I²C bus is a two-wire bi-directional serial bus developed by Philips. It consists of a serial data line (SDA) for communication between ICs and a serial clock line (SCL) for establishing sync in communication.

Figure 15-1. I²C Bus Interface



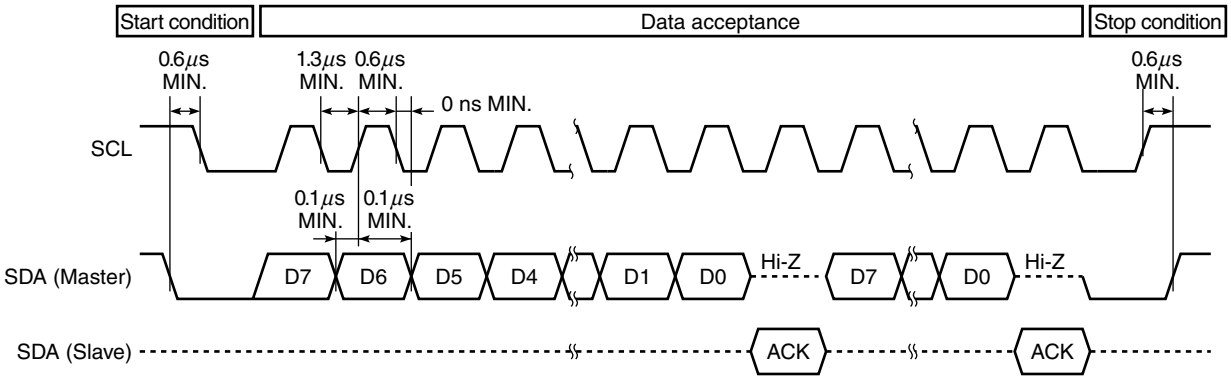
The following procedure is used to transfer data from the master IC to a slave IC.

<1> Start condition : To start communication, hold the SCL at a high level, then pull down the SDA from a high to a low level.

<2> Data transfer : To transfer data, pull up the SCL from a low to a high, while holding the current state of the SDA. Data transfer is carried out in units of 9 bits, that is, 8 data bits (D7 to D0, MSB first) plus an acknowledgment bit (ACK). A selected slave IC sets the SDA to a low when it receives bit 9 to send acknowledgment.

<3> Stop condition : To terminate communication, pull up the SDA from a low to a high upon acknowledgment, while keeping the SCL at a high.

Figure 15-2. Start Condition, Data Transfer, and Stop Condition Formats



15.2 Data Transfer Formats

Immediately when the master IC satisfies the start condition, each slave receives a slave address. If the received slave address matches that of a slave IC, communication begins between the slave IC and the master IC. If not, the SDA line is released. Two sets of slave addresses can be specified according to the SLA pin.

Table 15-1. Slave Address

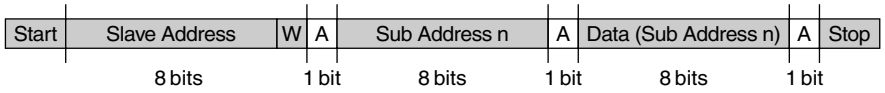
SLA pin setting (Unchangeable when power is on)	Slave address	
	Write mode	Read mode
L or open	B8h (1011 1000b)	B9h (1011 1001b)
H	BAh (1011 1010b)	BBh (1011 1011b)

(1) Write mode formats (reception mode for slaves)

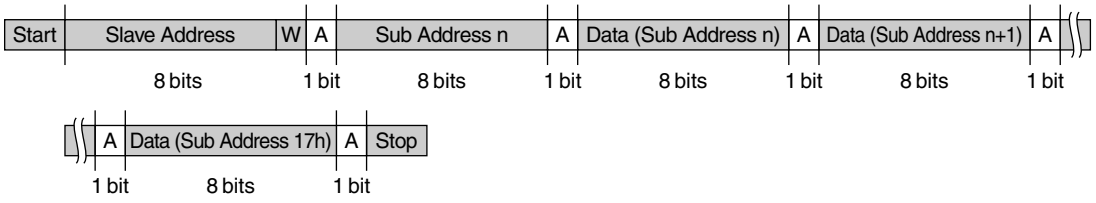
If a slave IC receives its write-mode slave address in byte 1, it continues to receive a subaddress in byte 2 and data in the subsequent bytes. The subaddress auto-increment function enables continuous data reception.

Figure 15-3. Write Mode Formats

(a) One-byte write format



(b) Multiple-byte write format



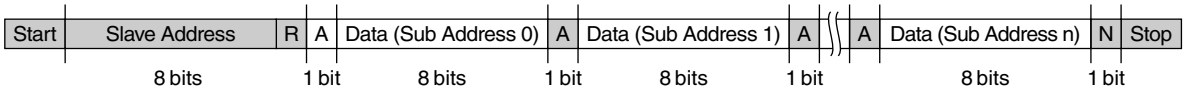
Remark Start : Start condition
Stop : Stop condition
Sr : Restart condition
W : Write mode specification (= 0)
R : Read mode specification (= 1)
A : Acknowledgment
N : No-acknowledgment
XXX : Master Device
XXX : Slave Device (μPD64084)

(2) Read mode format (transmission mode for slaves)

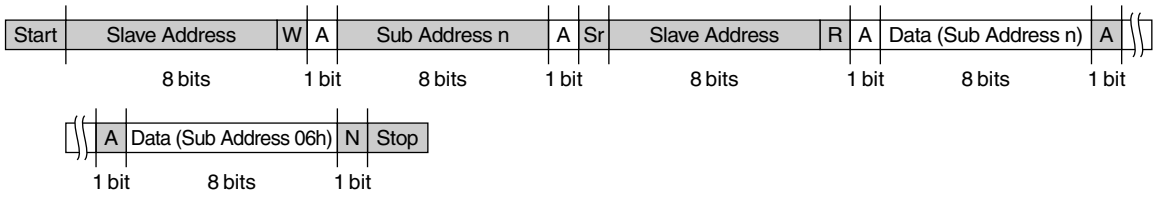
If a slave IC receives its read-mode slave address in byte 1, it sends data in byte 2 and the subsequent bytes. No subaddress is specified in this mode. Transmission begins always at address 0. Before establishing a stop condition, the master IC must send no-acknowledgment and release the SDA line.

Figure 15-4. Read Mode Format

(a) Single read format



(b) Multiple read format



Remark Start : Start condition Stop : Stop condition Sr : Restart condition
W : Write mode specification (= 0) R : Read mode specification (= 1)
A : Acknowledgment N : No-acknowledgment
XXX : Master Device XXX : Slave Device (μPD64084)

15.3 Initialization

The serial bus registers are initialized when the μPD64084 is reset (RSTB). The I^2C bus interface become operative after 100 μs from reset operation. In addition, its write register is previously loaded with an initial value.

For the reset operation, refer to **2.4 Start-up of Power Supply and Reset**.

15.4 Serial Bus Registers

The μPD64084 incorporates twenty-four 8-bit write registers and seven 8-bit read registers. Writing to the write registers is possible in the write mode (with a slave in reception mode), while reading from the read registers is possible in the read mode (with a slave in transmission mode). The following table lists how each serial bus register is mapped.

(1) Write register mapping

Slave address: 10111000b = B8h (SLA0 = L), 10111010b = BAh (SLA0 = H)

	Data Map (SA00-SA17)							
SA	D7	D6	D5	D4	D3	D2	D1	D0
00	0	NRMD	0	1	COUTS		YAPS	
01	CLKS		NSDS		MSS		KILS	
02	DYCOS		EXADINS	MFREEZE	PECS		EXCSS	
03	0	CPP	HDP			CDL		
04	DYCOR				DYGAIN			
05	DCCOR				DCGAIN			
06	YNRK	YNRINV	YNRLIM		CNRK	CNRINV	CNRLIM	
07	ID1ON	ID1W0A1	ID1W0A2	CLK8OFF	ST1S		ST0S	
08	WSC		VTRH		VTRR		LDSR	
09	WSS	ID1DECON	TH		FELCHK	TT		VFLTH
0A	VAPGAIN			VAPINV				
0B	0	0	YPFT		YPFG			
0C	V1PSEL		VEGSEL		CC3N	C0HS	CLPH	SELD2FH
0D	0	0	SELD1FL	0	0	1	0	1
0E	0	0	0	0	1	0	0	0
0F	0	1	0	0	0	1	0	0
10	YHCOR		YHCGAIN	ED2OFF	OVST	CSHDT	KCTT	
11	SHT0	SHT1	VCT	OTT	CLKG2D	CLKGGT	CLKGEB	CLKGT
12	HPLLFS	BPLLFS	FSCFG	PLLFG	KILR			
13	HSSL				VSSL			
14	BGPS				BGPW			
15	ADCLKS		ADPDS	NSDSW	NRZOFF	FSCOFF	VTVH	
16	SYSPDS		EXTDYCO	HIZEN	VLSEL	VLTYPE	0	0
17	CNROFS	HCNTFSYN	ADCLPFSW	ADCLPSTP	0	0	0	0

Caution It may be necessary to change set values on the serial bus depending on the results of performance evaluation conducted by NEC Electronics.

(2) Read register mapping

Slave address: 10111001b = B9h (SLA0 = L), 10111011b = BBh (SLA0 = H)

	Data Map (SA00 - SA06)							
SA	D7	D6	D5	D4	D3	D2	D1	D0
00	VER		-	KILF	NSDF	LDSDF	OVSDF	OHSDF
01	WSL							
02	ED2	B3	B4	B5	B6	B7	B8	B9
03	B10	B11	B12	B13	B14	B15	B16	B17
04	-	-	ID1W0		ID1W1			
05	ID1W2							
06	DCLEVH	CRCCH	DCFEL	CRCCFEL	HOLD1	-	-	-

15.5 Serial Bus Register Functions

Table 15-2 lists the function of each write register. The initial and typical values for each register were determined for evaluation purposes by NEC Electronics. They are not necessarily optimum values.

(1) Write Register

Table 15-2. Write Register Functions (1/14)

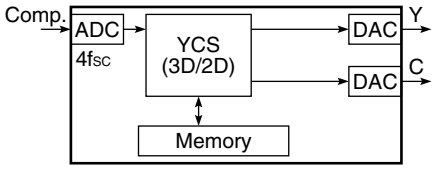
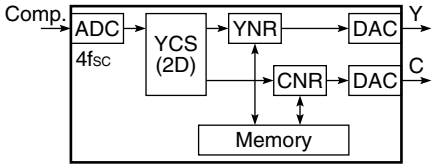
SA	Bit	Name and function	Description	Typical value	Initial value
00	D7	-	Undefined	0	0
	D6	**NRMD** Specifies an operation mode.	0 : YCS mode : Y/C separation (burst locked clocking)  1 : YCS+ mode : 2D Y/C separation and YNR/CNR (burst locked clocking) 	-	0
	D5-D4	-	Undefined	01	01
	D3-D2	**COUTS** Specifies the way the C signal is output. (Common to digital and analog outputs)	00: Input-to-output gain of 2, without BPF processing 01: Input-to-output gain of 2, with BPF processing 10: Input-to-output gain of 1, without BPF processing 11: Input-to-output gain of 1, with BPF processing	11	11
	D1-D0	**YAPS** Specifies Y signal output correction. (Vertical aperture compensation and Y peaking filtering)	00: Correction is disabled for both analog and digital outputs. 01: Correction is enabled for only analog outputs. 10: Correction is enabled for only digital outputs. 11: Correction is enabled for both analog and digital outputs.	11	11

Table 15-2. Write Register Functions (2/14)

SA	Bit	Name and function	Description	Typical value	Initial value
01	D7-D6	**CLKS** Specifies whether to force use of the system clock.	00: Automatic setting (in an operation mode specified by NRMD) 01: Forced burst locked clocking 1x: Forced line (horizontal) locked clocking **Caution If the specified setting does not match the input signal, a malfunction may occur.**	00	00
	D5-D4	**NSDS** Specifies whether to force standard/nonstandard signal processing.	00: Adaptive processing (performed according to whether a nonstandard signal is detected) 01: Forced standard signal processing (performed regardless of whether a nonstandard signal is detected) 10: Forced horizontal sync nonstandard signal processing 11: Forced vertical sync nonstandard signal processing (forced inter-line processing) **Caution If the specified setting does not match the input signal, a malfunction may occur.**	00	00
	D3-D2	**MSS** Specifies whether to force inter-frame or inter-line processing.	00: Adaptive processing (performed according to the LINE pin input and motion detection signal) 01: Forced inter-frame processing (performed according to the LINE pin input) 1x: Forced inter-line processing	00	00
	D1-D0	**KILS** Specifies whether to force killer processing	00: Adaptive processing (performed according to the KIL pin input and internal killer detection results) 01: Internal killer detection is not used (processing is performed according to the KIL pin input only). 1x: Forced killer processing In killer processing, subtraction of the C signal from Comp. Signal is disabled.	01	01

Table 15-2. Write Register Functions (3/14)

SA	Bit	Name and function	Description	Typical value	Initial value
02	D7-D6	**DYCOS** Specifies DYCO pin input/output.	In case of EXTDYCO = 0 00: Y/C separation signal alternate output 01: Test mode (setting prohibited) 1x: Low* High impedance In case of EXDYCO = 1 00: DYCO9-0 : Output, EXTDYCO9-0 : Input (When EXADINS=0, Low Note) 01: Test mode (setting prohibited) 1x: DYCO9-0 : Input (When EXADINS=0, Low Note), EXTDYCO9-0 : Output **Note** If HIZEN (SA16h, D4) = 1, then HI-Z.	10	10
	D5	**EXADINS** Specifies whether to select external ADC.	0: Internal ADC 1: External ADC (digital video signal, converted from analog form, is input to the DYCO9 to DYCO0 pins)	0	0
	D4	**MFREEZE** External memory test bit	0: Normal mode 1: Test mode (setting prohibited)	0	0
	D3-D2	**PECS** Specifies a pedestal error correction test bit.	00: Normal setting 01: Test setting (setting prohibited) 10: Test setting (setting prohibited) 11: Test setting (setting prohibited)	00	00
	D1-D0	**EXCSS** Specifies whether to use external C sync input.	00: Internally separated sync signal is always used (CSI input is not used). 01: Sync signal input at the CSI pin is used during out-of-sync state. 1x: Sync signal input at the CSI pin is always used.	01	01
03	D7	-	Undefined	0	0
	D6	**CPP** Specifies the clamp pulse width of internal ADC	0 : 2.2 μs 1 : 1.1 μs	0	0
	D5-D3	**HDP** Fine adjustment of system horizontal phase	000: −1.12 μs to 100: ±0.00 μs (Typ.) to 111: +0.84 μs Fine-adjusts the horizontal-processing phase with respect to the horizontal sync signal (0.28 μs/step).	100	100
	D2-D0	**CDL** Fine adjustment of C signal output delay	000: −280 ns to 100: ±0 ns (Typ.) to 111: +210 ns Fine-adjusts the C signal phase with respect to the Y signal (70 ns/step).	100	100

Table 15-2. Write Register Functions (4/14)

SA	Bit	Name and function	Description	Typical value	Initial value
04	D7-D4	**DYCOR** DY detection coring level (Y motion detection coring)	0000: Coring 0 (Closer to motion pictures) to 1111: Large amount of coring (Closer to still pictures) The coring level for inter-frame Y difference detection is specified. A signal smaller than specified is assumed to be noise, resulting in '0' being output.	0010	0010
	D3-D0	**DYGAIN** DY detection gain (Y motion detection gain)	0000: Gain of 0 (Closer to still pictures) to 1111: Maximum gain (Closer to motion pictures) Inter-frame Y difference detection gain is specified.	1001	1001
05	D7-D4	**DCCOR** DC detection coring level (C motion detection coring)	0000: Coring 0 (Closer to motion pictures) to 1111: Large amount of coring (Closer to still pictures) The coring level for inter-frame C difference detection is specified. A signal smaller than specified is assumed to be noise, resulting in 0 being output.	0011	0011
	D3-D0	**DCGAIN** DC detection gain (C motion detection gain)	0000: Gain of 0 (Closer to still pictures) to 1111: Maximum gain (Closer to motion pictures) Inter-frame C difference detection gain is specified.	0110	0110

Table 15-2. Write Register Functions (5/14)

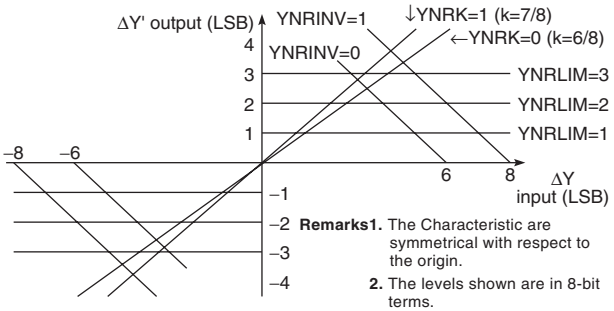
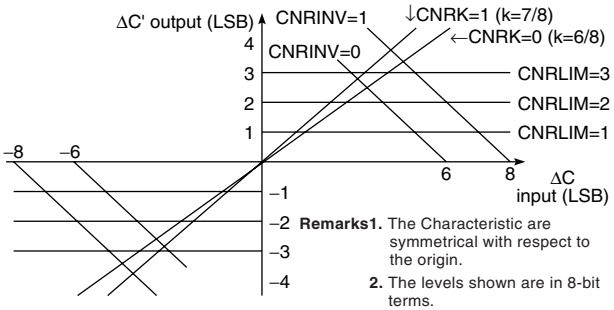
SA	Bit	Name and function	Description	Typical value	Initial value
06	D7	**YNRK** Specifies the frame recursive YNR nonlinear filter gain.	0: x 6/8 (small noise reduction effect and small after-image) 1: x 7/8 (large noise reduction effect and large after-image) The magnitude of the NR effect is specified.	0	0
	D6	**YNRINV** Specifies the frame recursive YNR nonlinear filter convergence level.	0: 6 LSB (small noise reduction effect and small after-image) 1: 8 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in 0 being output.	0	0
	D5-D4	**YNRLIM** Specifies the frame recursive YNR nonlinear filter limit level.	00: 0 LSB (YNR off) to 11: 3 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in a limit value being output. Nonlinear characteristic curve based on YNRK, YNRINV, and YNRLIM 	01	01
	D3	**CNRK** Specifies the frame recursive CNR nonlinear filter gain.	0: x 6/8 (small noise reduction effect and small after-image) 1: x 7/8 (large noise reduction effect and large after-image) The magnitude of the NR effect is specified.	0	0
	D2	**CNRINV** Specifies the frame recursive CNR nonlinear filter convergence level.	0: 6 LSB (small noise reduction effect and small after-image) 1: 8 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in 0 being output.	0	0
	D1-D0	**CNRLIM** Specifies the frame recursive CNR nonlinear filter limit level.	00: 0 LSB (CNR off) to 11: 3 LSB (large noise reduction effect and large after-image) An input larger than specified is assumed to be a motion component, resulting in a limit value being output. Nonlinear characteristic curve based on CNRK, CNRINV, and CNRLIM 	01	01

Table 15-2. Write Register Functions (6/14)

SA	Bit	Name and function	Description	Typical value	Initial value
07	D7	**ID1ENON** Specifies whether to superimpose ID-1 specification ID signal.	0: Through (no superimposition) 1: Forced superimposition **Caution Do not set this bit to 1 during no-signal state.**	-	0
	D6	**ID1ENW0A1** Specifies whether to set bit A1 of ID-1 word 0.	0: 0 (transmission aspect of 4:3) 1: 1 (transmission aspect of 16:9)	-	0
	D5	**ID1ENW0A2** Specifies whether to set bit A2 of ID-1 word 0.	0: 0 (image display format = normal) 1: 1 (image display format = letter box)	-	0
	D4	**CLK8OFF** Specifies the state of the CLK8 pin output.	0: Active-low (to output $8f_{SC}$ clock pulse) 1: Fixed to low level (to reduce radiation noise)	1	0
	D3-D2	**ST1S** Specifies internal signal monitor output for the ST1 pin.	00: I^2C SDA inversed pulse 01: Internal ADC clamp pulse (active-high) 10: Composite sync (active-low) 11: H sync (active-high)	-	00
	D1-D0	**ST0S** Specifies internal signal monitor output for the ST0 pin.	00: Reserved 01: External ADC clamp pulse (active-high) 10: HV blanking (active-high) 11: V sync (active-low)	-	00

Table 15-2. Write Register Functions (7/14)

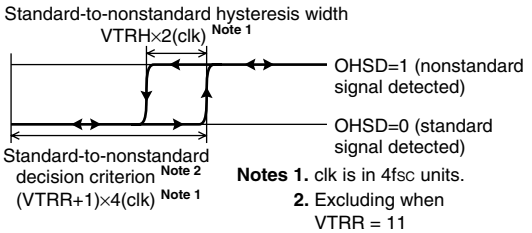
SA	Bit	Name and function	Description	Typical value	Initial value
08	D7-D6	**WSC** Specifies the amount of noise detection coring.	00: 0LSB (high detection sensitivity) 01: 1LSB 10: 2LSB 11: 3LSB (low detection sensitivity) Specifies an input coring value for the noise detection circuit. Detection results are not used within the device.	01	01
	D5-D4	**VTRH** Specifies hysteresis for horizontal sync nonstandard signal detection (out-of-horizontal sync intra-field)	00: Hysteresis off (width of 0 clock pulses) 01: Low hysteresis (width of 2 clock pulses) 10: Medium hysteresis (width of 4 clock pulses) 11: High hysteresis (width of 6 clock pulses) For horizontal sync nonstandard signal detection, a criterion value to detect an out-of-horizontal sync state intra-field is decreased by a value indicated above.	01	01
	D3-D2	**VTRR** Specifies sensitivity for horizontal sync nonstandard signal detection (out-of-horizontal sync intra-field)	00: High detection sensitivity (width of ±4 clock pulses) 01: Medium detection sensitivity (width of ±8 clock pulses) 10: Low detection sensitivity (width of ±12 clock pulses) 11: Detection off If the degree of out-of-horizontal sync state intra-field becomes larger than specified, a horizontal sync nonstandard signal is assumed to have been detected. Horizontal sync nonstandard signal detection characteristic curve  **Notes 1.** clk is in 4fSC units. **2.** Excluding when VTRR = 11	01	01
	D1-D0	**LDSR** Specifies sensitivity for frame sync nonstandard signal detection (out-of-horizontal sync inter-frame)	00: High detection sensitivity (width of 0.5 clock pulses) 01: Medium detection sensitivity (width of 1 clock pulse) 10: Low detection sensitivity (width of 1.5 clock pulses) 11: Detection off If the degree of out-of-horizontal sync state inter-frame becomes larger than specified, a frame sync nonstandard signal is assumed to have been detected.	10	10

Table 15-2. Write Register Functions (8/14)

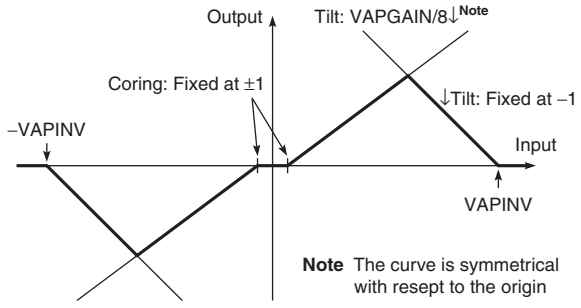
SA	Bit	Name and function	Description	Typical value	Initial value
09	D7	**WSS** Specifies the pre-filter characteristic of noise detection.	0 : Normal (μPD64082 compatible) 1 : fsc trap	0	0
	D6	**ID1DECON** ID-1 decoder	0 : disable 1 : enable When decoding is disable, The output of register is following. WORD0=00, WORD1=1111, WORD2=00h	1	1
	D5-D4	**TH** ID-1 decorder check level	01 : Strict 00 : 10 : 11 : Loose	00	00
	D3	**FELCHK** ID-1 decoder Field check enable	0 : 6 fields check is disable 1 : 6 fields check is enable	1	1
	D2-D1	**TT** ID-1 decoder pulse width level	00 : 8CLK 01 : 2CLK 10 : 4CLK 11 : 16CLK	00	00
	D0	**VFILTH** Specifies the vertical blanking (1H to 22H) BPF	0: BPF enable 1: BPF disable (through)	0	0
0A	D7-D5	**VAPGAIN** Specifies a vertical aperture compensation gain.	000: Correction off to 111: Maximum correction (0.875 times)	-	000
	D4-D0	**VAPINV** Specifies a vertical aperture compensation convergence point.	00000: Correction off to 11111: Maximum correction Vertical aperture compensation characteristic curve based on VAPGAIN and VAPINV  **Note** The curve is symmetrical with resept to the origin	-	00000

Table 15-2. Write Register Functions (9/14)

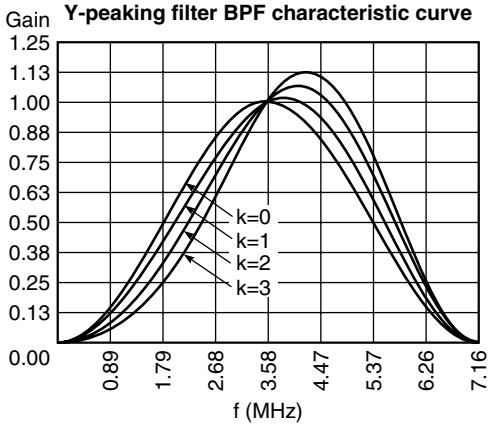
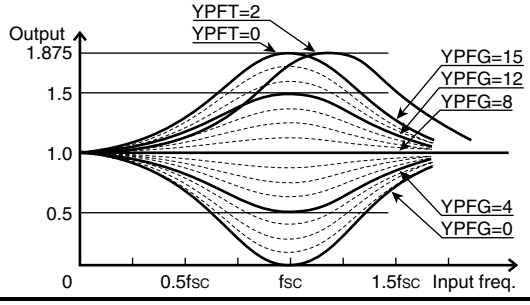
SA	Bit	Name and function	Description	Typical value	Initial value
0B	D7	**TEST** Test bit	0: Normal mode 1: Test mode (setting prohibited)	0	0
	D6	**TEST** Test bit	0: Normal mode 1: Test mode (setting prohibited)	0	0
	D5-D4	**YPFT** Specifies the Y peaking filter (BPF) center frequency.	00: 3.58 MHz, 01: 3.86 MHz, 10: 4.08 MHz, 11: 4.22 MHz **Y-peaking filter BPF characteristic curve** 	11	11
	D3-D0	**YPFG** Specifies a Y peaking filter gain.	0000: −1.0 times to 1000: ±0.0 times to 1111: +0.875 times **Y signal output frequency characteristic curve based on YPFT and YPFG** 	1000	1000

Table 15-2. Write Register Functions (10/14)

SA	Bit	Name and function	Description	Typical value	Initial value
0C	D7-D6	**V1PSEL** Line comb filter horizontal dot interference suppression level	00: Suppression off 01: Low suppression level 10: Medium suppression level 11: High suppression level Horizontal dot interference is reduced at inter-line Y/C separation.	10	10
	D5-D4	**VEGSEL** Line comb filter vertical dot interference suppression level	00: Suppression off 01: Low suppression level 10: Medium suppression level 11: High suppression level Vertical dot interference is reduced at inter-line Y/C separation.	10	10
	D3	**CC3N** Selects a line comb filter C separation filter characteristic.	0: Narrow bandwidth 1: Wide bandwidth	0	0
	D2	**C0HS** Specifies C signal delay time extension at NR	0: 1H delay 1: No 1H delay	0	0
	D1	**CLPH** ADC clamp test bit	0: Normal mode 1: Test mode (setting prohibited)	0	0
	D0	**SELD2FH** Specifies DC detection High-frequency sensitivity.	0: Low sensitivity, Closer to still pictures 1: High sensitivity, Closer to motion pictures	0	0
0D	D7	-	0	0	0
	D6	-	0	0	0
	D5	**SELD1FL** Specifies DY detection low-frequency sensitivity.	0: Low sensitivity, Closer to still pictures 1: High sensitivity, Closer to motion pictures	0	0
	D4	-	0	0	0
	D3	-	0	0	0
	D2-D0	-	101	101	101
0E	D7-D4	-	0000	0000	0000
	D3-D0	-	1000	1000	1000
0F	D7-D4	-	0100	0100	0100
	D3-D0	-	0100	0100	0100

Table 15-2. Write Register Functions (11/14)

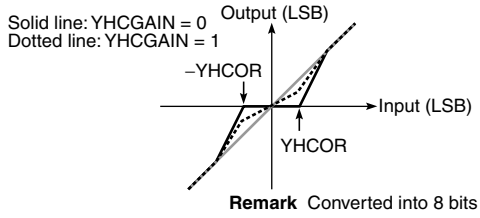
SA	Bit	Name and function	Description	Typical value	Initial value
10	D7-D6	**YHCOR** Specifies Y output high frequency component coring.	00: Coring off 01: Small amount of coring (±1 LSB: 8-bit terms) 10: Medium amount of coring (±2 LSB: 8-bit terms) 11: Large amount of coring (±3 LSB: 8-bit terms) Coring characteristic curve (for high-frequency component only)  **Remark** Converted into 8 bits	00	00
	D5	**YHCGAIN** Specifies Y output high-frequency component coring gain.	0: Normal (×1) 1 :1/2 gain Refer to **YHCOR (SA10h, D7-D6)**	0	0
	D4	**ED2OFF** Specifies WCV-ID detection circuit.	0: Normal mode 1: Forced WCV-ID detection circuit turned off	0	0
	D3	**OVST** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D2	**CSHDT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D1-D0	**KCTT** H / V counter test bit	0x: Normal mode 1x: Test mode	00	00

Table 15-2. Write Register Functions (12/14)

SA	Bit	Name and function	Description	Typical value	Initial value
11	D7	**SHT1** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D6	**SHT0** Nonstandard signal detection test bit	0: Normal mode 1: Test mode	0	0
	D5	**VCT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D4	**OTT** H / V counter test bit	0: Normal mode 1: Test mode	0	0
	D3	**CLKG2D** Clock generator section test bit	0: Test mode 1: Normal mode	1	1
	D2	**CLKGGT** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
	D1	**CLKGEB** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
	D0	**CLKGT** Clock generator section test bit	0: Normal mode 1: Test mode	0	0
12	D7	**HPLLFS** Specifies the horizontal PLL filter.	0: Slow convergence 1: Quick convergence	-	1
	D6	**BPLLFS** Specifies the burst PLL filter.	0: Quick convergence 1: Slow convergence	1	1
	D5	**FSCFG** Specifies the burst extraction gain.	0: High gain 1: Low gain	0	0
	D4	**PLLFG** Specifies the PLL loop gain.	0: Low gain (slow convergence) 1: High gain (quick convergence)	1	1
	D3-D0	**KILR** Killer detection reference	0000: Detection off 0001: Low detection sensitivity to 1111: High detection sensitivity	0010	1010
13	D7-D4	**HSSL** Horizontal sync slice level	0000: 4LSB to 1111: 19LSB (in 8-bit input terms, 1LSB/step)	1111	1111
	D3-D0	**VSSL** Vertical sync slice level	0000: HSSL setting + 0LSB to 1111: HSSL setting + 15LSB (in 8-bit input terms, 1LSB/step)	1000	1000

Table 15-2. Write Register Functions (13/14)

SA	Bit	Name and function	Description	Typical value	Initial value
14	D7-D4	**BGPS** Specifies the internal burst gate start position.	0000: H sync center + 2 μs to 1111: H sync center + 5.75 μs Calculation of gate start position from the H sync center : 0.25 × BGPS + 2.0 (μs)	0101	0101
	D3-D0	**BGPW** Specifies the internal burst gate width.	0000: 0.5 μs to 1111: 4.25 μs Calculation of gate width : 0.25 × BGPW + 0.5 (μs)	0011	0011
15	D7-D6	**ADCLKS** Specifies the ADC clock delay.	00: 0 ns typically (setting prohibited) 01: 3 ns typically 10: 17.5 ns typically 11: 20.5 ns typically	11	11
	D5	**ADPDS** Specifies whether to use ADC power-down.	0: Do not stop operation of ADC not in use.(High current drain) 1: Stop operation of ADC not in use. (Low current drain)	1	1
	D4	**NRDSW** Nonstandard detection section test	0: Normal mode 1: Test mode	0	0
	D3	**NRZOFF** WCV-ID detection NRZ section check	0: NRZ section amplitude check on 1: NRZ section amplitude check off	0	0
	D2	**FSCOFF** WCV-ID detection FSC section check	0: FSC amplitude check on 1: FSC amplitude check off	0	0
	D1-D0	**VTVH** Specifies WCV signal no-image section processing (only letter box signal is valid).	00: Ordinary processing 01: Forced inter-frame Y/C separation 10: Forced inter-line Y/C separation 11: Forced through (composite signal is output.)	00	00

Table 15-2. Write Register Functions (14/14)

SA	Bit	Name and function	Description	Typical value	Initial value
16	D7-D6	**SYSPDS** System power down	00: Normal operation 01: Mode1 (D/A, Memory Access stop, Total current :mid) 10: Mode2 (Memory Access stop, Total current: High 11: Mode3 (A/D, D/A, Memory Access stop, Total current : Low) **Remark** All register data are kept in power down term.Reset is not required for re-start.	00	00
	D5	**EXTDYCO** Extended digital I/O enable	0: EXTDYCO9-EXTDYCO0 disable 1: EXTDYCO9-EXTDYCO0 enable	0	0
	D4	**HIZEN** Digital input / output status select	0: Low 1: Hi-Z	0	0
	D3	**VLSEL** Test bit	0: Normal mode 1: Test mode	0	0
	D2	**VLTYPE** Test bit	0: Normal mode 1: Test mode	0	0
	D1	-	Undefined	0	0
	D0	-	Undefined	0	0
17	D7	**CNROFS** CNR section test bit	0: Normal mode 1: Test mode	0	0
	D6	**HCNTFSYN** Nonstandard signal detection test bit	0: Normal mode 1: Test mode (Forced H counter synchronize) Do not use “1” setting in the YCS mode.	0	0
	D5	**ADCLPFSW** ADC clamp test bit	0: Normal mode 1: Clamp level feedback disable	0	0
	D4	**ADCLPSTP** ADC clamp test bit	0: Normal mode 1: Clamp disable	0	0
	D3-D0	-	Undefined	0000	0000

(2) Read Register

Table 15-3. Read Register Functions (1/2)

SA	Bit	Name and function	Description	Initial value
00	D7-D6	**VER** Product Version Code	Version code of μPD64084 is '01'(Fixed)	-
	D5	-	Undefined	-
	D4	**KILF** Killer detection flag	0: Color signal detected 1: Killer signal (non-burst signal) detected	-
	D3	**NSDF** Horizontal sync signal detection flag	0: Sync signal detected 1: No sync signal detected	-
	D2	**LDSDF** Frame sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as laser disc special playback signal)	-
	D1	**OVSDF** Vertical sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as VCR special playback signal and home TV game signal)	-
	D0	**OHSDF** Horizontal sync nonstandard signal detection flag	0: Standard signal detected 1: Nonstandard signal detected (such as VCR ordinary playback signal)	-
01	D7-D0	**WSL** Noise level detection data	00000000: Closer to low noise 11111111: Closer to high noise	-
02	D7	**ED2** WCV-ID signal detection flag	0: Invalid (no WCV-ID signal detected) 1: Valid (WCV-ID signal detected)	-
	D6-D0	**B3-B9** WCV-ID signal decoding result		-
03	D7-D0	**B10-B17** WCV-ID signal decoding result		-
04	D7-D6	-	Undefined	-
	D5-D4	**ID1W0** Decoded Data of ID-1 WORD0	Decoded data of WORD0 (2 bits)	00
	D3-D0	**ID1W1** Decoded Data of ID-1 WORD1	Decoded data of WORD0 (4 bits)	1111
05	D7-D0	**ID1W1** Decoded Data of ID-1 WORD2	Decoded data of WORD0 (8 bits)	00h

Table 14-3. Read Register Functions (2/2)

SA	Bit	Name and function	Description	Initial value
06	D7	**DCLEVH** ID-1 Decode Reference signal detect	0 : Reference signal is not detected 1 : Reference signal is detected	-
	D6	**CRCCH** ID-1 Decode CRC check	0 : Error 1 : Normal	-
	D5	**DCFEL** ID-1 Decode Reference signal Field check	0 : Error 1 : Normal	-
	D4	**CRCCFEL** ID-1 Decode CRC field check	0 : Error 1 : Normal	-
	D3	**HOLD1** ID-1 Decode signal availability check detection result	0 : Error 1 : Normal	-
	D2-D0	-	Undefined	-

16. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = +25°C Unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Digital section supply voltage	DV_{DD}		−0.3 to +3.6	V
Analog section supply voltage	AV_{DD}		−0.3 to +3.6	V
DRAM section supply voltage	DV_{DDRAM}		−0.3 to +3.6	V
I/O section supply voltage	DV_{DDIO}		−0.3 to +4.6	V
Input voltage	V_I	3.3 V-resistant input pins	−0.3 to +4.6	V
Output current	I_O		−10 to +10	mA
Package allowable dissipation	P_D	When mounted on an epoxy-glass board (T_A = +70 °C, 100 mm × 100 mm, 2 layer, 1.6-mm thick)	964	mW
Operating ambient temperature	T_A	Device ambient temperature	0 to +70	°C
Operating junction temperature	$T_{J:MAX}$	Upper limit to junction temperature	+125	°C
Storage temperature	T_{stg}		−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Digital section supply voltage	DV_{DD}		2.3	2.5	2.7	V
Analog section supply voltage	AV_{DD}		2.3	2.5	2.7	V
DRAM section supply voltage	DV_{DDRAM}		2.3	2.5	2.7	V
I/O section supply voltage	DV_{DDIO}		3.0	3.3	3.6	V
High-level input voltage	V_{IH}	3.3 V-resistant buffer	2.0		3.6	V
Low-level input voltage	V_{IL}		0		0.8	V
High-level input voltage	V_{IH}	Schmitt input pin	0.7 × DV_{DDIO}		3.6	V
Low-level input voltage	V_{IL}		0		0.3 × DV_{DDIO}	V
Reference clock input frequency	f_{XI}	XI pin	19.998	20.000	20.002	MHz
Reference clock input amplitude	V_{XI}		0.8		DV_{DDIO}	V_{p-p}
Subcarrier input frequency	f_{FSCI}	FSCI pin		3.579545		MHz
Subcarrier input amplitude	V_{FSCI}		0.45		AV_{DD}	V_{p-p}
Composite Video signal input amplitude	V_{AYI}	AYI pin, Picture + Sync. amp. (140 IRE_{p-p}), AV_{DD} = 2.5 V		0.8		V_{p-p}
Composite signal Sync. signal input amplitude	$V_{AYI(S)}$	AYI pin, Sync. amp. (40 IRE_{p-p}), AV_{DD} = 2.5 V		229 (±0 dB)	288 (+2 dB)	mV_{p-p}

Digital Section DC Characteristics

(DV_{DD} = DV_{DDRAM} = 2.5 ±0.2 V, DV_{DDIO} = 3.3 ±0.3 V, DGND = DGNDRAM = 0 V, T_A = 0 to +70°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Digital section current drain	DI_{DD}	DVDD and DGND pins			37	100	mA
	DI_{DDRAM}	DVDDRAM and DGNDRAM pins			15	50	mA
	DI_{DDIO}	DVDDIO and DGND pins			12	20	mA
Input leakage current	I_{LI}	Ordinary input	V_I = DV_{DDIO} or 0 V	−10	0	+10	μA
High-level input current	I_{IH}	Pull-down type	V_I = DV_{DDIO}	20	83	200	μA
Low-level input current	I_{IL}	Pull-up type	V_I = 0 V	−200	−83	−20	μA
High-level output current 1	I_{OH1}	6.0 mA type	V_{OH1} = 2.4 V			−6.0	mA
Low-level output current 1	I_{OL1}		V_{OL1} = 0.4 V	+6.0			mA
High-level output current 2	I_{OH2}	3.0 mA type	V_{OH2} = 2.4 V			−2.0	mA
Low-level output current 2	I_{OL2}		V_{OL2} = 0.4 V	+3.0			mA
Low-level output current 3	I_{OL3}	N-ch. open drain	V_{OL3} = 0.4 V	+6.0			mA
Output leakage current	I_{LO}	3-state, open drain	V_O = DV_{DDIO} to DGND	−10	0	+10	μA

Analog Section DC Characteristics

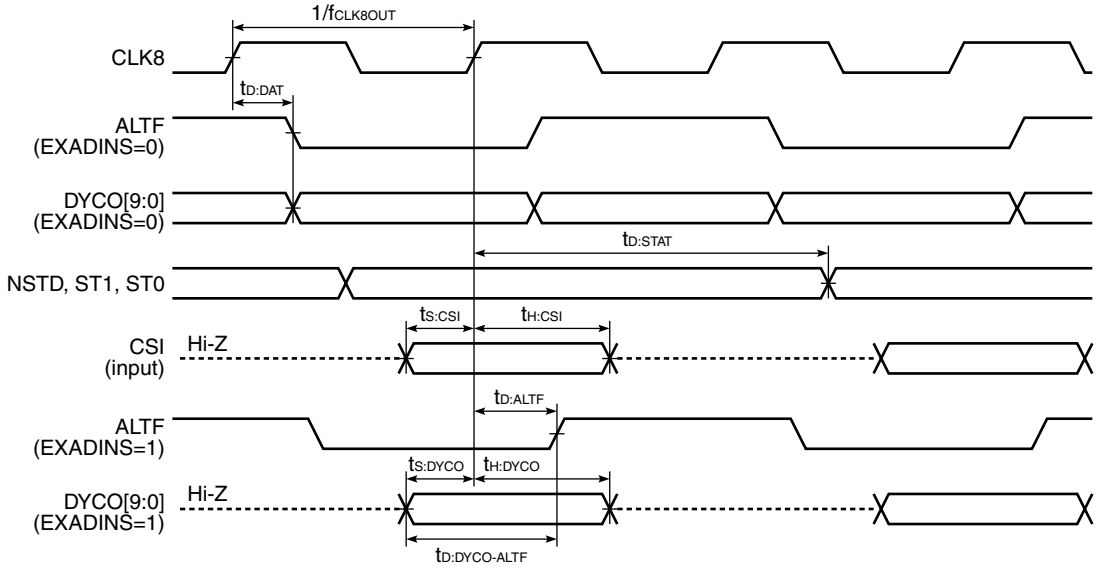
(AV_{DD} = 2.5 ±0.2 V, AGND = 0 V, T_A = +25°C Unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog section current drain	AI_{DD}	AVDD and AGND pins		50	100	mA
ADC resolution	RES_{ADY}	AYI pin, AV_{DD} = 2.5 V, $f_S = 4 f_{SC}$,	-	10	-	bit
ADC integral linearity error	ILE_{ADY}	DG_{AD}, DP_{AD} : NTSC 100 IRE RAMP		±3.0	±6.0	LSB
ADC differential linearity error	DLE_{ADY}			±1.0	±2.0	LSB
ADC differential gain	DG_{ADY}			±2.0	±3.0	%
ADC differential phase	DP_{ADY}			±1.0	±3.0	Deg
ADC reference voltage(low)	V_{RBADY}			0.75		V
ADC reference voltage(high)	V_{RTADY}			1.25		V
ADC analog input range	V_{INAY}			1.00		V
ADC clamp pin voltage	V_{CLY}			0.70		V
ADC analog input capacitance	C_{INAD}	$AV_{DD} = V_{IN}$ = 0 V, f_{IN} = 1 MHz		10		pF
DAC resolution	RES_{DA}	AYO and ACO pins,	-	10	-	bit
DAC integral linearity error	ILE_{DA}	AV_{DD} = 2.5 V, $f_S = 4f_{SC}$		±3.5	±4.5	LSB
DAC differential linearity error	DLE_{DA}	DG_{AD}, DP_{AD} : NTSC 100 IRE RAMP		±0.5	±1.0	LSB
DAC differential gain	DG_{DA}			±1.0	±3.0	%
DAC differential phase	DP_{DA}			±1.0	±3.0	deg
DAC full-scale output voltage	V_{FSDA}	AYO and ACO pins, AV_{DD} = 2.5 V	1.77	1.94	2.08	V
DAC zero-scale output voltage	V_{ZSDA}		0.77	0.94	1.07	V
DAC output amplitude	V_{OPPDA}			1.00		V_{p-p}
f_{SC} DAC resolution	RES_{FSC}	FSCO pin	-	8	-	bit

Digital Section AC Characteristics

(DV_{DD} = DV_{DDRAM} = 2.5 ±0.2 V, DV_{DDIO} = 3.3 ±0.3 V, DGND = DGNDRAM = 0 V, CL = 15 pF, t_r = t_f = 2 ns, T_A = 0 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Video data output delay	$t_{D:DAT}$	CLK8↑ → DYCOn, ALTF (EXADINS = 0)	3	9	20	ns
Internal signal monitor output delay	$t_{D:STAT}$	CLK8↑→ NSTD, ST1, ST0	35	45	55	ns
CSI input set-up time	$t_{S:CSI}$	CSI → CLK8↑	0			ns
CSI input hold time	$t_{H:CSI}$	CLK8↑ → CSI	15			ns
ALTF output delay + DYCOn input set-up time	$t_{D:DYCO-ALTF}$	CLK8↑ → ALTF + : $t_{S:DYCO}$: EXADINS = 1, ADCLKS = xx			35	ns
ALTF output delay 0	$t_{D:ALTF0}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 00	3		23	ns
ALTF output delay 1	$t_{D:ALTF1}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 01	5		25	ns
ALTF output delay 2	$t_{D:ALTF2}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 10	18		38	ns
ALTF output delay 3	$t_{D:ALTF3}$	CLK8↑ → ALTF : EXADINS = 1, ADCLKS = 11	20		40	ns
DYCOn input set-up time	$t_{S:DYCO}$	DYCOn → CLK8↑ : EXADINS = 1	0			ns
DYCOn hold time	$t_{H:DYCO}$	CLK8↑ → DYCOn : EXADINS = 1	10			ns
Input capacitance	C_I	DV_{DD} = V_I = 0 V, f_{IN} = 1 MHz		10	15	pF



Clock and Timing Generation Section AC Characteristics

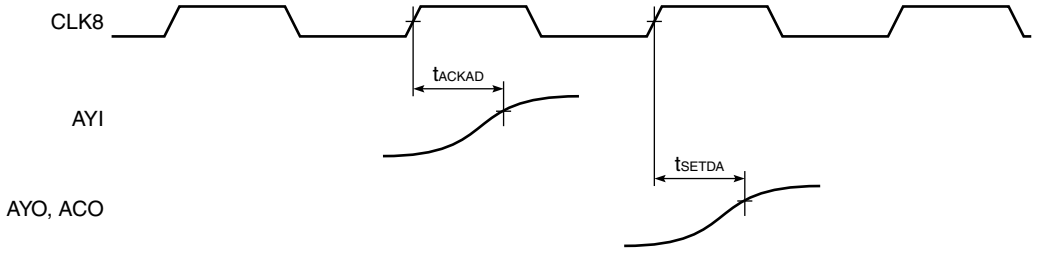
(DV_{DD} = DV_{DDRAM} = AV_{DD} = 2.5 ±0.2 V, DV_{DDIO} = 3.3 ±0.3 V, DGND = DGNDRAM = AGND = 0 V, C_L = 15 pF, T_A = 0 to + 70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Subcarrier output frequency	f_{FSCO}	FSCO pin		3.579545		MHz
Subcarrier output amplitude	V_{FSCO}	FSCO pin, AV_{DD} = 3.3 V		1.00		V_{p-p}
Clock output frequency	$f_{CLK8OUT}$	CLK8 pin, CKMD pin = DGND, CLK8OFF (SA07:D4) = 0		28.63636		MHz
Clock output duty factor	$D_{CLK8OUT}$		45	50	55	%
f_{SC} pull-in range (in f_{SC} terms)	f_{bp}	When the burst locked clock operation		±600		Hz
Horizontal sync attenuation (Capture range)	V_{hi}	Sync input amplitude, HSSL = 1111, VSSL = 1000	−8	0		dB
Vertical sync attenuation (Capture range)	V_{vi}	(assumed to be 0dB when inputting 40IRE = 59LSB)	−6	0		dB

ADC and DAC Section AC Characteristics (AV_{DD} = 2.5 ± 0.2 V, AGND = 0 V, C_L = 15 pF, T_A = +25 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ADC acquisition time Note	t_{ACKAD}	CLK8↑ → AYI		7		ns
DAC setting time Note	t_{SETDA}	CLK8↑ → AYO, ACO		15		ns

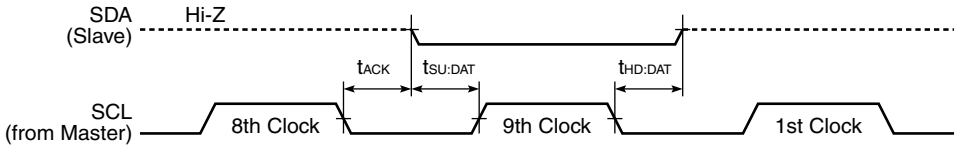
Note Excluding data conversion delay



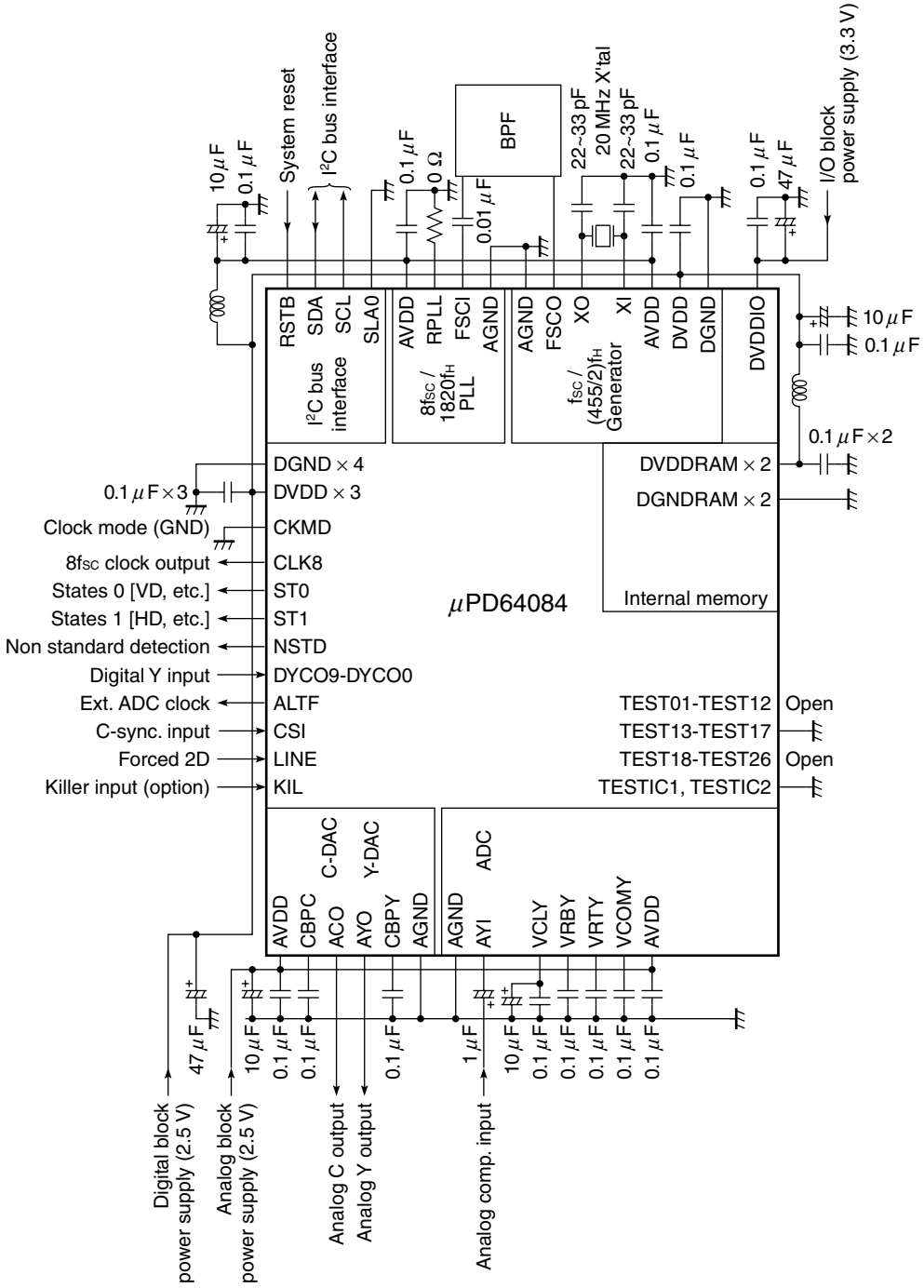
I²C Bus Interface Section AC Characteristics

(DV_{DD} = 2.5 ± 0.2 V, DGND = 0 V, C_L = 15 pF, T_A = 0 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SDA pin ACK response delay	t_{ACK}	SCL↓ → SDA↓			500	ns
SDA data set-up time	$t_{SU:DAT}$	SDA:L → SCL↑	100			ns
SDA data hold time	$t_{HD:DAT}$	SCL↓ → SDA:Hi-Z	0			ns



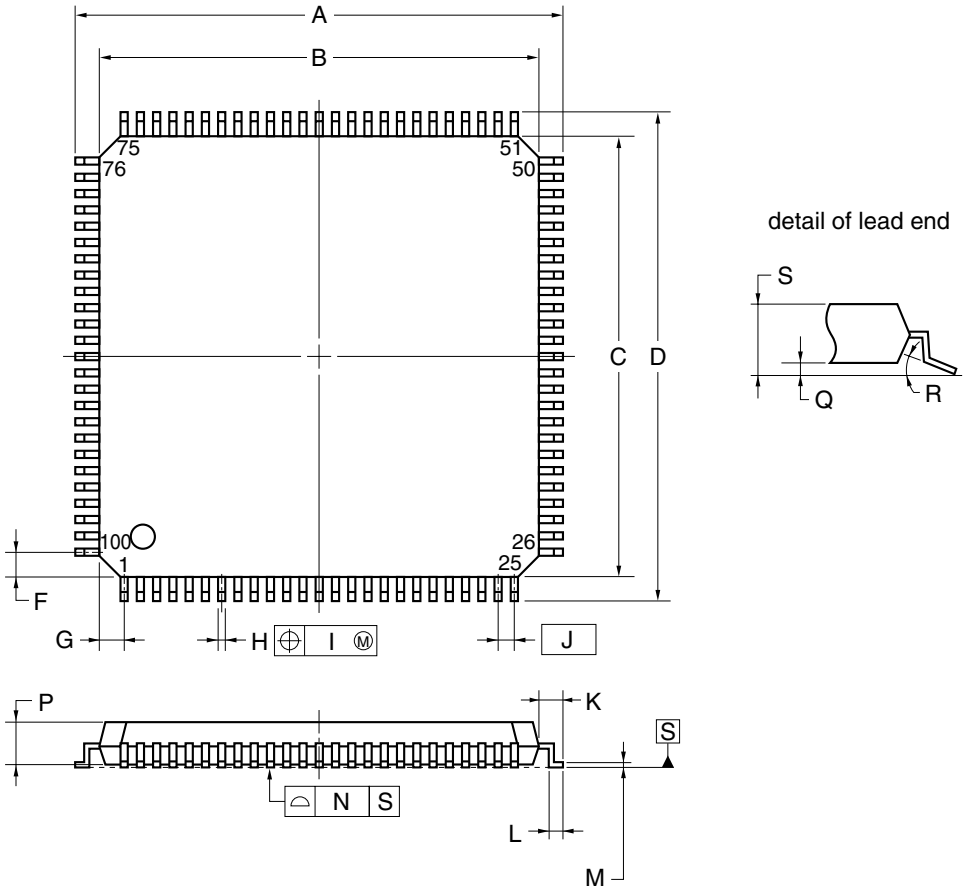
17. APPLICATION CIRCUIT EXAMPLE



Caution This application circuit and the circuit parameters are for reference only, and not intended for use in actual design-ins.

18. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

19. RECOMMENDED SOLDERING CONDITIONS

The μPD64084 should be solderd and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, content an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Table 19-1. Surface Mounting Type Soldering Conditions

- **μPD64084GC-8EA-A[Note1]: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)**
- **μPD64084GC-8EA-Y[Note2]: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260 °C or below, Time: 30 s. Max. (at 210°C or higher), Count: three times or less, Exposure limit: 7 days [Note3] (after that, prebake at 125°C for 10 to 72 hours) <Caution> Products packed in a medium other than a heat-resistance tray (such as a magazine, taping, and non-heat-resistance tray) cannot be baked.	IR60-107-3
Partial heating	Pin temperature: 300°C Max., Time: 3 s. Max. (per pin row)	-

Notes 1. Lead-free product

2. High-thermal-resistance product

3. After opening the dry pack, store it at 25 °C or less and 65 % RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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