DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6951

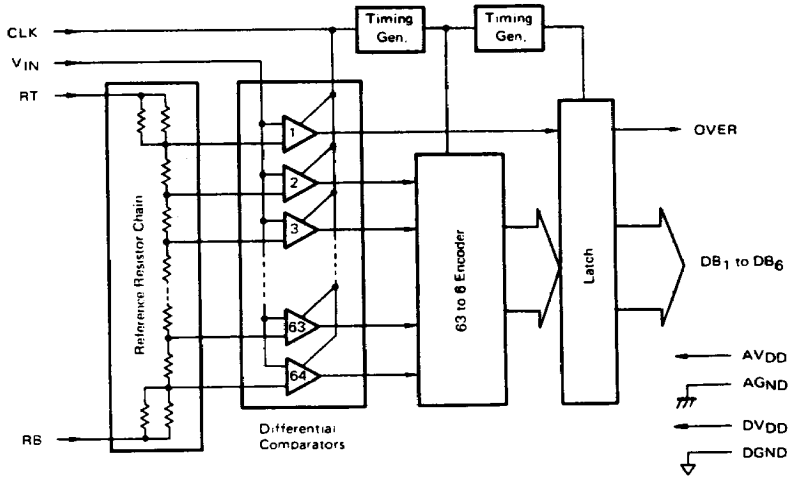
6 BIT D/A CONVERTER FOR VIDEO SIGNAL PROCESSING CMOS LSI

The μPD6951 is an 6 bit A/D converter designed for use in video applications. The high-speed CMOS processing technology and full-parallel conversion technics adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 20 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and high-speed facsimile.

FEATURES

- Resolution : 6 bits
- Conversion rate : 20 Msps
- Linearity : ±0.5 LSB MAX.
- Reference voltage : 2.5 V TYP.
- Power supply voltage : +5 V single
- Low power consumption (125 mW TYP.)
- TTL compatible (Digital output)
- 18 pin plastic DIP, and 20 pin plastic SOP (375 mil)

BLOCK DIAGRAM



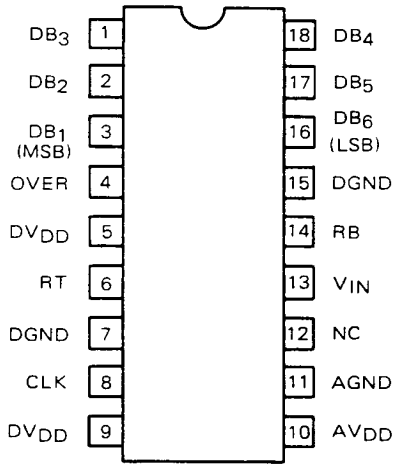
ORDERING INFORMATION

Ordering Name	Package
μPD6951C	18 pin plastic DIP (300 mil)
μPD6951G	20 pin plastic SOP (375 mil)

The * mark outside the columns denotes major points where revisions or additions are made in this edition.

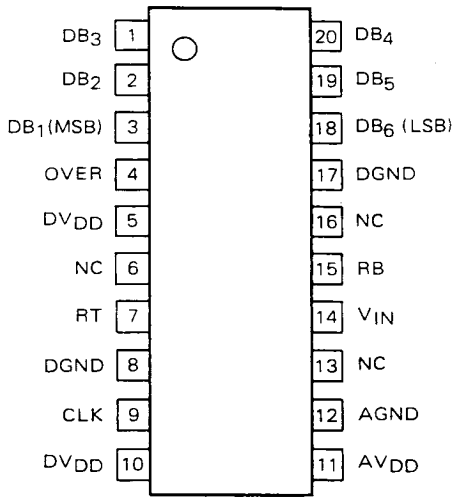
CONNECTION DIAGRAM (Top View)

μPD6951C



1	DB_3	Digital output (3rd)
2	DB_2	Digital output (2nd)
3	DB_1	Digital output (MSB)
4	OVER	Over range
5	DV_{DD}	Digital power supply
6	RT	Reference voltage (high voltage side)
7	DGND	Digital GND
8	CLK	Clock input
9	DV_{DD}	Digital power supply
10	AV_{DD}	Analog power supply
11	AGND	Analog GND
12	NC	No connection
13	V_{IN}	Analog input
14	RB	Reference voltage (low level side)
15	DGND	Digital GND
16	DB_6	Digital input (LSB)
17	DB_5	Digital input (5th)
18	DB_4	Digital input (4th)

μPD6951G



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4	OVER	Over range
5	DV_{DD}	Digital power supply
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9	CLK	Clock input
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11	AV_{DD}	Analog power supply
12	AGND	Analog GND
13	NC	No connection
14	V_{IN}	Analog input
15	RB	Reference voltage (low level side)
16	NC	No connection
17	DGND	Digital GND
18	DB_6	Digital input (LSB)
19	DB_5	Digital input (5th)
20	DB_4	Digital input (4th)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to V_{DD}+0.3	V
Output terminal voltage	−0.3 to V_{DD}+0.3	V
Analog power supply voltage	DV_{DD}−0.3 to DV_{DD}+0.3	V
Analog GND voltage	DGND−0.3 to DGND+0.3	V
Operating temperature range	−20 to +75	°C
Storage temperature range	−40 to +125	°C

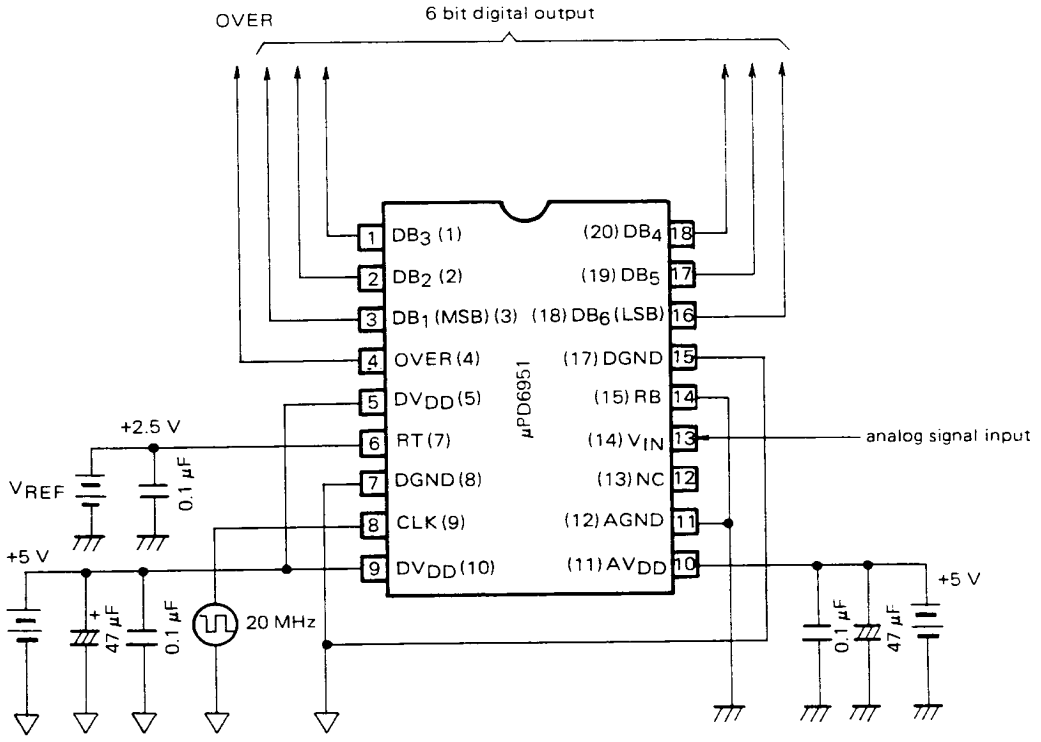
RECOMMENDED OPERATING CONDITION (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	AV_{DD},DV_{DD}	4.5	5.0	5.5	V	AGND=DGND=0 V
Reference voltage	V_{REF}	2.0	2.5	3.6	V	$V_{REF}=V_{RT}-V_{RB}$
RT input voltage	V_{RT}	2.0	2.5	3.6	V	
RB input voltage	V_{RB}	0		1.6	V	
Sampling clock	f_{samp}	0.01		20	MHz	
Sampling clock low level pulse width	t_{PWL}	25			ns	
Sampling clock high level pulse width	t_{PWH}	25			ns	
CLK input high level	V_{IH}	2.7			V	
CLK input low level	V_{IL}			0.6	V	
Analog input voltage	V_{AIN}	0		AV_{DD}	V	

ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = AV_{DD} = DV_{DD} = 5 V ±0.5 V, f_{samp} = 20 MHz)

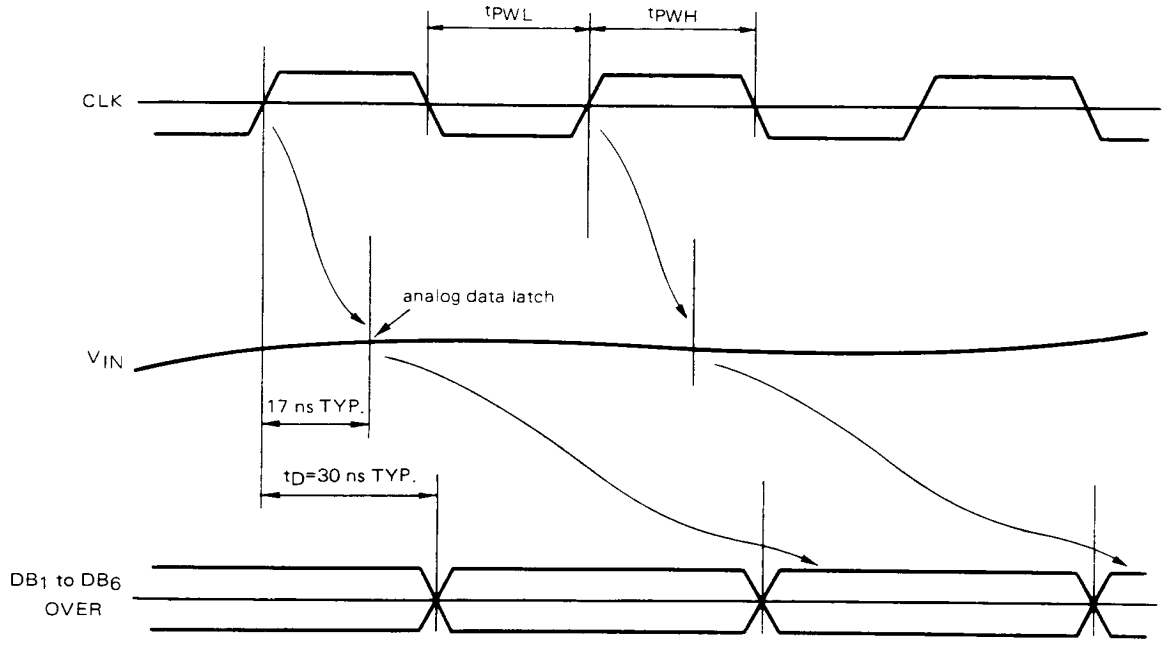
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I_{DD}		25	35	mA	$I_{DD}=AI_{DD}+DI_{DD}$, $AV_{DD}=DV_{DD}$=5.0 V
Resolution	RES		6		bit	
Non-linearity	NL		±0.3	±0.5	LSB	V_{DD}=5.0±0.25 V, V_{REF}=2.5 V, T_a=0 to 60 °C
Differential non-linearity	DNL		±0.3	±0.5	LSB	V_{DD}=5.0±0.25 V, V_{REF}=2.5 V, T_a=0 to 60 °C
Data output delay time	t_D	20	30	40	ns	CLK ↑→ DB_1 to 6, OVER
Data output high level voltage	V_{OH}	2.8			V	I_{OH}=−1.0 mA
Data output low level voltage	V_{OL}			0.4	V	I_{OL}=1.8 mA
Reference resistance	R_{REF}		1.3		kΩ	Between RT and RB
Analog input resistance	R_{IN}		1		MΩ	
Analog input capacitance	C_{IN}		50		pF	
CLK input current	I_{IN}			20	μA	V_{IN}=GND or DV_{DD}

TEST CIRCUIT



( ) shows pins number of μPD6951G. μPD6951G has two more NC terminals, pin 6 and pin 16. There is no necessity to connect.

TIMING CHART



PIN DESCRIPTIONS

(/) shows pins number. Right one is μPD6951G's and left one is μPD6951C's terminal number.

DGND (Pins 7, 15/8, 17) Digital system ground

AGND (Pin 11/12) Analog system ground

DV_{DD} (Pins 5, 9/5, 10) Digital system power supply (+5 V)

AV_{DD} (Pin 10/11) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.1 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6951C pins. Supply the digital system power from the analog power line through the low path filter to prevent from luch up.

RT (Pin 6/7) Reference voltage input pin (high voltage side)

RB (Pin 14/15) Reference voltage input pin (low voltage side)

These pins are the reference voltage V_{REF} input pins.

V_{IN} (Pin 13/14) Analog input pin

The input analog signal applied to this pin is latched synchronized with the rising edge of the sampling clock and is subsequently obtained as an 6 bit digital signal from pins DB_1 thru DB_6.

Note: Since the electrostatic resistivity of the analog input pin is a little lower than other pins to achieve the required input characteristics, this input should be handled with extra care.

DB_1 to DB_6 (Pins 1 to 3, and 16 to 18/1 to 3, and 18 to 20) Digital data output pins

DB_1 to DB_6 are the 6 bit digital data output pins. The code format is binary, and the output voltage level is TTL compatible.

The analog signal applied to the analog input pin is latched at the rising edge of the sampling clock, converted to digital data, and then obtained as the output at the next rising edge of the sampling clock.

analog input	digital output						
	OVER	DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6 (LSB)
0 V (RB) to 1/2 LSB	0	0	0	0	0	0	0
1/2 LSB to (1+1/2) LSB	0	0	0	0	0	0	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(62+1/2) LSB to (63+1/2) LSB	0	1	1	1	1	1	1
(63+1/2) LSB to 2.5 V (RT)	1	1	1	1	1	1	1
2.5 V (RT) to V_{DD}	1	1	1	1	1	1	1

$$LSB = \frac{VRT - VRB}{64}$$

OVER (Pin 4/4) Over range output pin

This output signal indicates analog signal overflow. A high level output is generated if the input voltage level of the analog input V_{IN} exceeds (63+1/2). LSB where LSB is $(V_{RT} - V_{RB})/64$.

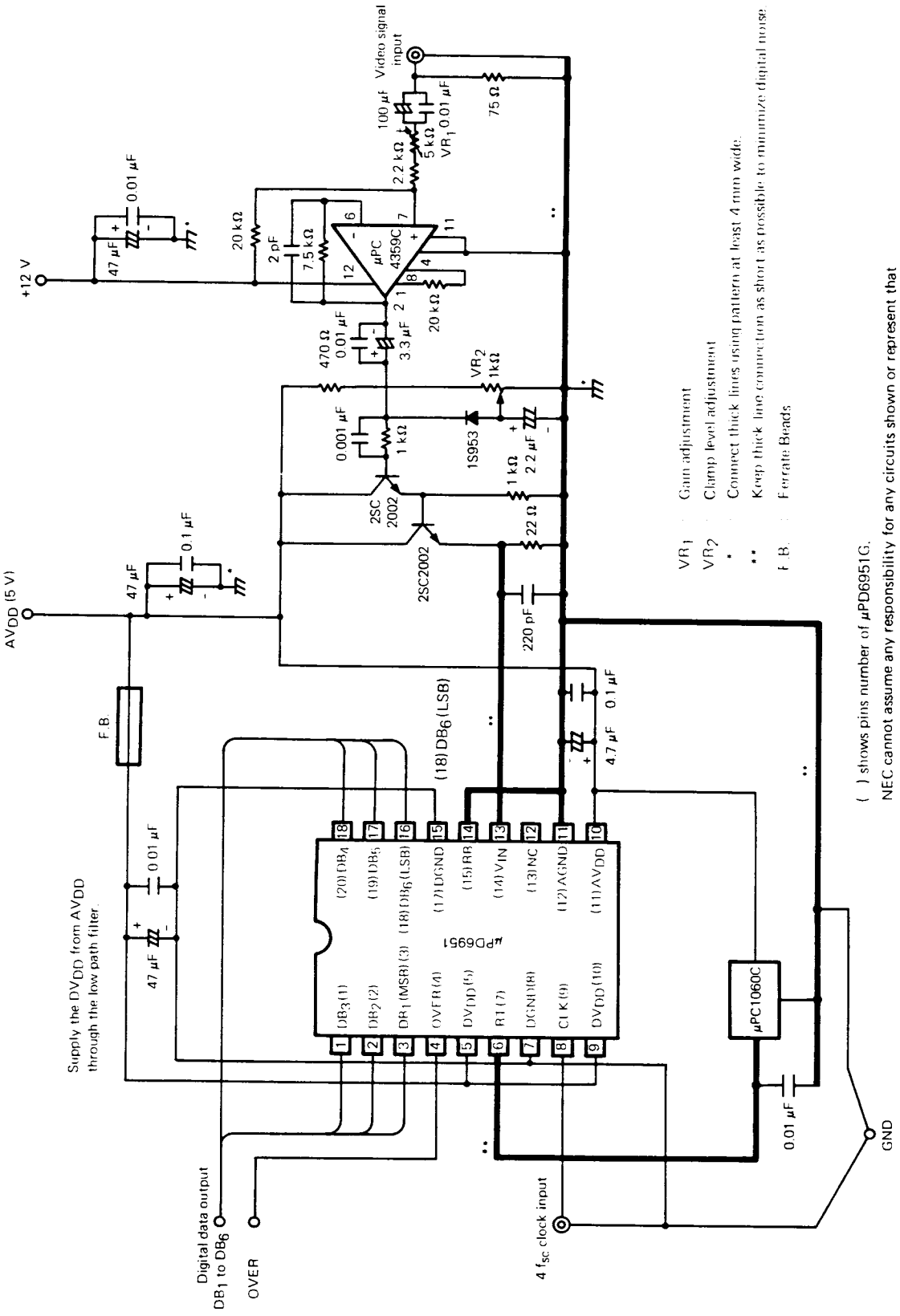
CLK (Pin 8/9) Sampling clock input pin

The analog signal is latched by the rising edge of the clock signal applied to the A/D converter sampling clock input pin. The complete sequence of events involved in A/D conversion (comparison, encoding, latching, data output) is synchronized with this clock signal. The maximum clock frequency is 20 MHz.

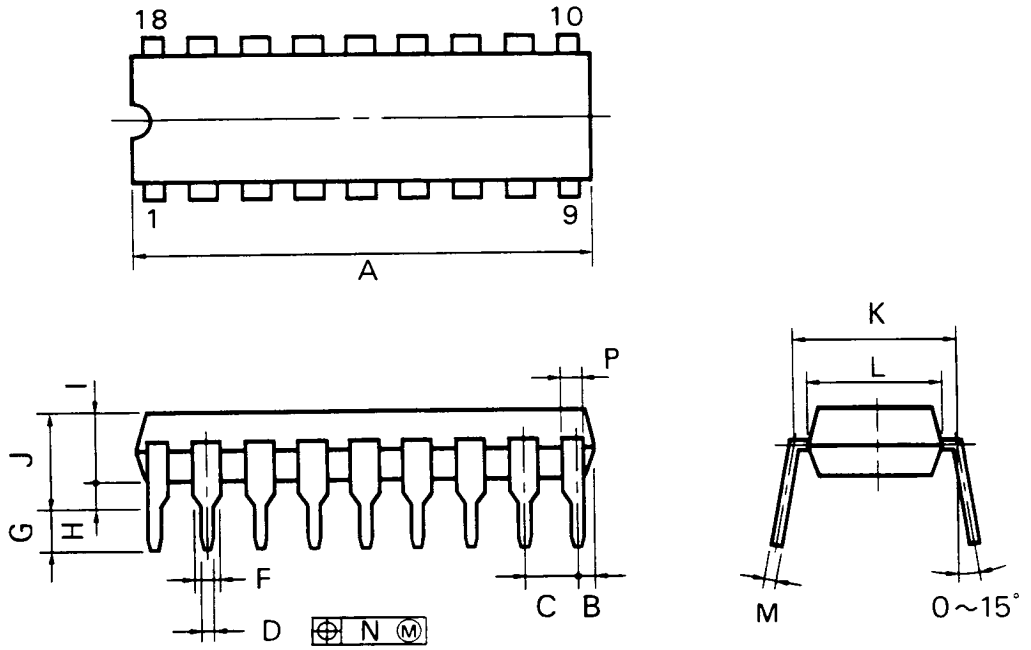
NC (Pin 12/6, 13, 16) No connection pin

These pins may be connected to analog ground.

APPLICATION CIRCUIT



18PIN PLASTIC DIP (300 mil)



P18C-100-300A,C

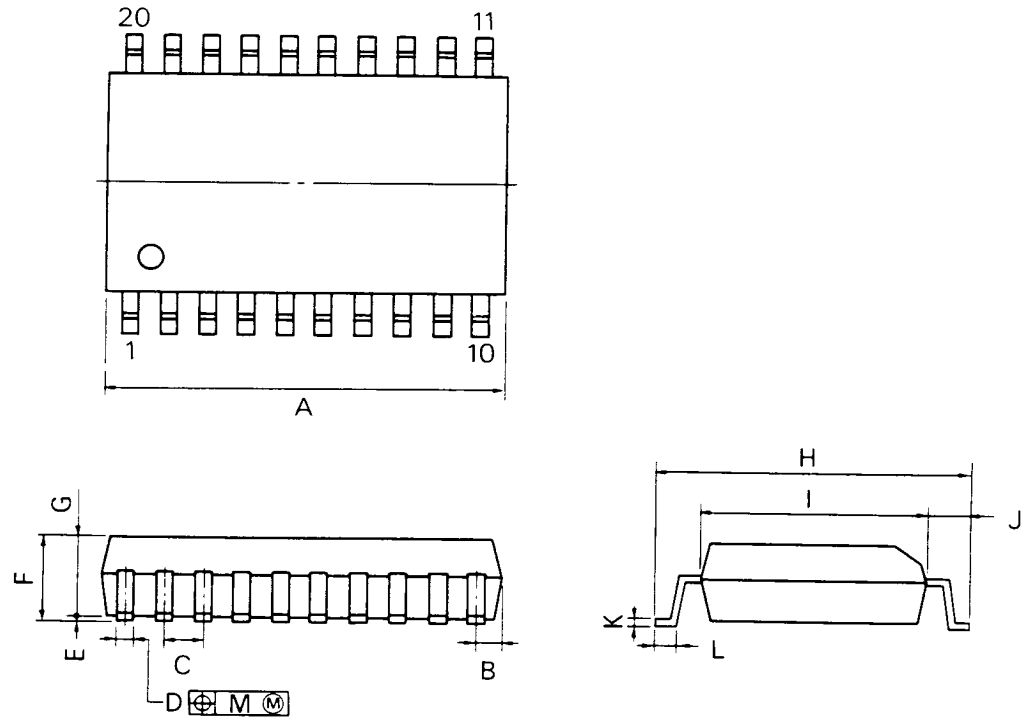
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.

20PIN PLASTIC SOP (375 mil)



P20GM-50-375B

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.00 MAX.	0.512 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{-0.10}_{-0.05}$	$0.016^{-0.004}_{-0.003}$
E	$0.1^{-0.2}_{-0.1}$	$0.004^{-0.008}_{-0.004}$
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	$10.3^{-0.3}$	$0.406^{-0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{-0.10}_{-0.05}$	$0.006^{-0.004}_{-0.002}$
L	$0.8^{\pm 0.2}$	$0.031^{-0.009}_{-0.008}$
M	0.12	0.005

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