NEC

MOS INTEGRATED CIRCUIT

μPD703003

V853™

32/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD703003 is a member of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. This microcontroller provides on-chip features, including a 32-bit CPU core, ROM, RAM, interrupt controller, real-time pulse unit, a serial interface, an A/D converter, a D/A converter, and PWM signal units.

See the following manuals for a detailed description of this product's functions. Be sure to use these manuals as a reference for design.

V853 USER'S MANUAL, HARDWARE:	**U10913E**
V850 FAMILY USER'S MANUAL, ARCHITECTURE:	**U10243E**

FEATURES

- Number of instructions: 74
- Minimum instruction execution time
  30 ns (during 33-MHz operation)
- General registers
  32 bits × 32 registers
- Instruction set optimized for control applications
- On-chip memory ROM: 128 Kbytes
  RAM: 4 Kbytes
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- 8/9/10/12-bit resolution PWM: 2 channels
- Power saving functions

APPLICATIONS

- AV: Video cameras, VCRs, etc.
- Office equipment: PPCs, LBPs, printers, etc.
- Industrial equipment: motor controllers, NC machine tools, etc.
- Communications equipment: Mobile telephones, etc.

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The mark ★ shows major revised points.

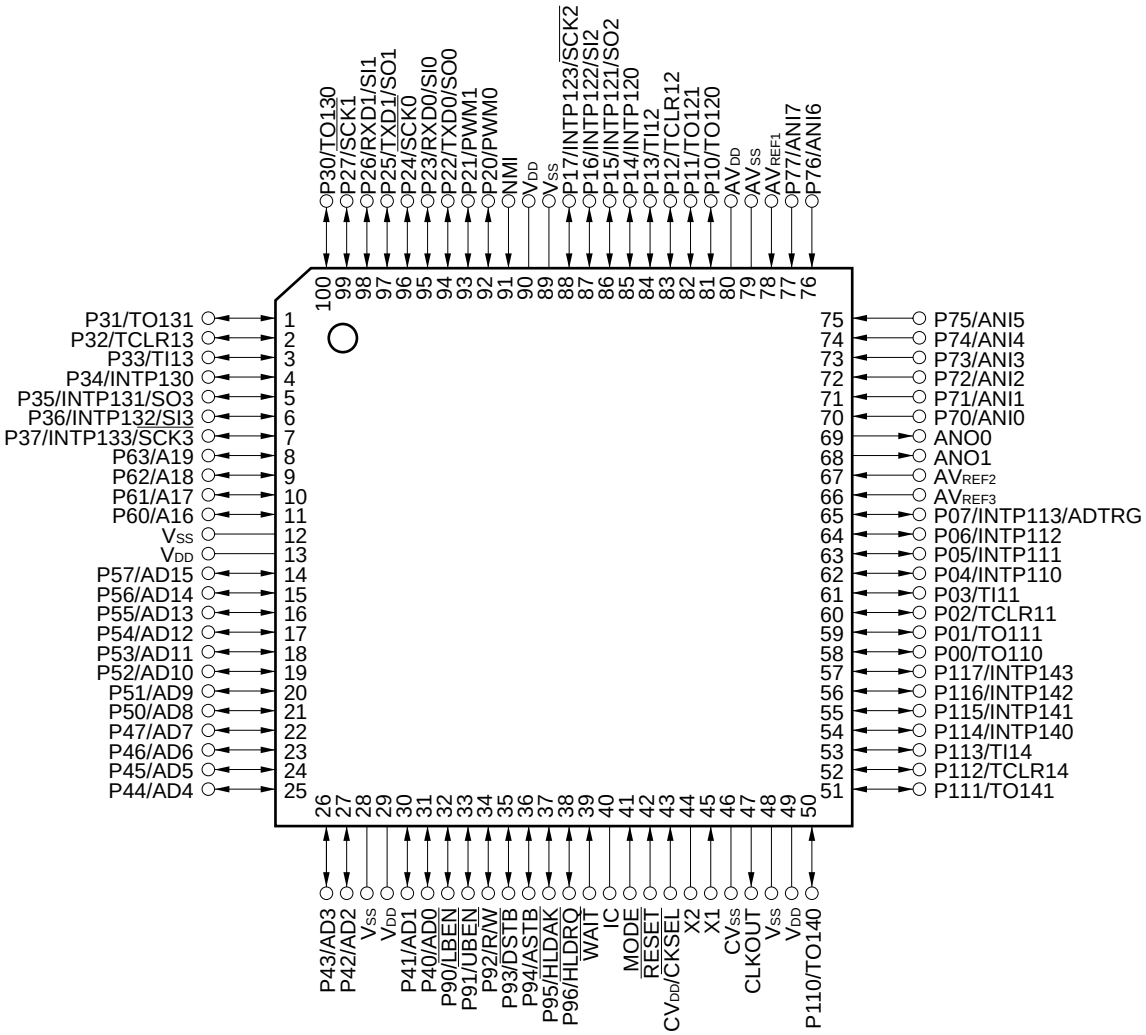
ORDERING INFORMATION

Part Number	Package	Maximum operating frequency (MHz)
μPD703003GC-25-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	25
μPD703003GC-33-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	33

Remark "xxx" indicates ROM code suffix.

PIN CONFIGURATION

- **100-Pin Plastic QFP (fine pitch) (14 × 14 mm)**
  μPD703003GC-25-xxx-7EA
  μPD703003GC-33-xxx-7EA



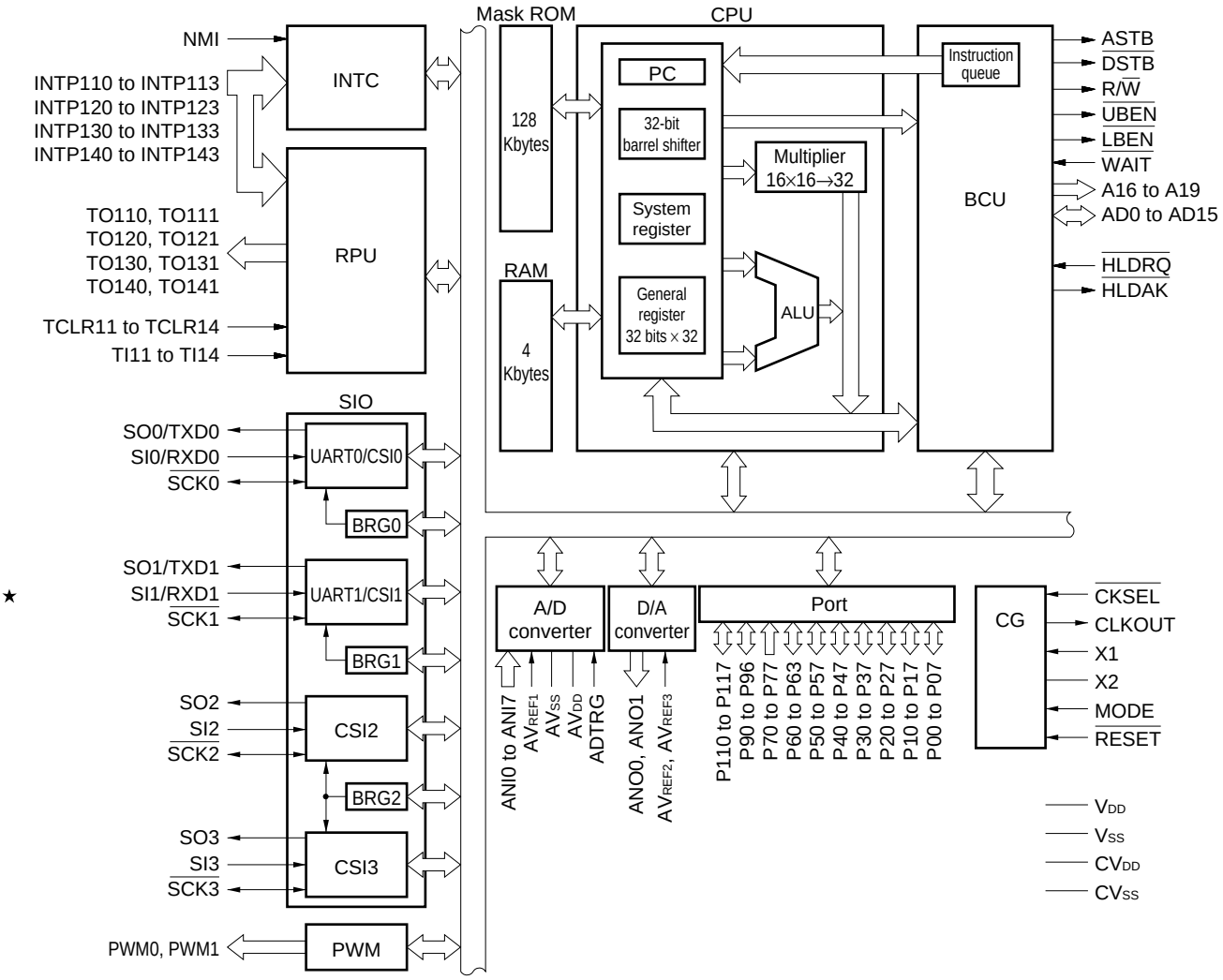
★

Caution Connect the IC pin directly to VSS.

PIN NAMES

A16 to A19	:	Address Bus	P30 to P37	:	Port3
AD0 to AD15	:	Address/Data Bus	P40 to P47	:	Port4
ADTRG	:	AD Trigger Input	P50 to P57	:	Port5
ANI0 to ANI7	:	Analog Input	P60 to P63	:	Port6
ANO0, ANO1	:	Analog Output	P70 to P77	:	Port7
ASTB	:	Address Strobe	P90 to P96	:	Port9
AV_{DD}	:	Analog V_{DD}	P110 to P117	:	Port11
AV_{REF1} to AV_{REF3}	:	Analog Reference Voltage	PWM0, PWM1	:	Pulse Width Modulation
AV_{SS}	:	Analog V_{SS}	$\overline{RESET}$	:	Reset
CV_{DD}	:	Power Supply for Clock Generator	R/$\overline{W}$	:	Read/Write Status
CV_{SS}	:	Ground for Clock Generator	RXD0, RXD1	:	Receive Data
$\overline{CKSEL}$	:	Clock Select	$\overline{SCK0}$ to $\overline{SCK3}$	:	Serial Clock
CLKOUT	:	Clock Output	SI0 to SI3	:	Serial Input
$\overline{DSTB}$	:	Data Strobe	SO0 to SO3	:	Serial Output
$\overline{HLDAK}$	:	Hold Acknowledge	TO110, TO111,	:	Timer Output
$\overline{HLDRQ}$	:	Hold Request	TO120, TO121,		
IC	:	Internally Connected	TO130, TO131,		
INTP110 to INTP113,	:	Interrupt Request from Peripherals	TO140, TO141		
INTP120 to INTP123,			TCLR11 to TCLR14	:	Timer Clear
INTP130 to INTP133,			TI11 to TI14	:	Timer Input
INTP140 to INTP143			TXD0, TXD1	:	Transmit Data
$\overline{LBEN}$	:	Lower Byte Enable	$\overline{UBEN}$	:	Upper Byte Enable
MODE	:	Mode	$\overline{WAIT}$	:	Wait
NMI	:	Non-maskable Interrupt Request	X1, X2	:	Crystal
P00 to P07	:	Port0	V_{DD}	:	Power Supply
P10 to P17	:	Port1	V_{SS}	:	Ground
P20 to P27	:	Port2			

INTERNAL BLOCK DIAGRAM



CONTENTS

★ 1. DIFFERENCES AMONG PRODUCTS

Item			μPD703003	μPD703003A	μPD703004A	μPD703025A	μPD70F3003	μPD70F3003A	μPD70F3025A
Internal ROM			Mask ROM				Flash memory		
			128 Kbytes		96 Kbytes	256 Kbytes	128 Kbytes		256 Kbytes
Internal RAM			4 Kbytes			8 Kbytes	4 Kbytes		8 Kbytes
Operation mode	Normal operation mode	Single-chip mode	Implemented						
		ROM-less mode	Implemented	Not implemented			Implemented	Not implemented	
	Flash memory programming mode		Not implemented				Implemented		
V_{PP} pin			Not implemented				Implemented		
Value of CKC register when reset			00H	MODE = 0 : 03H MODE = 1 : 00H			00H	MODE = 0 : 03H MODE = 1 : 00H	
Electrical specifications			Power consumption levels vary (see specific product's data sheet).						
Others			Noise tolerance and noise emission vary, depending on the circuit scale and mask layout.						

2. LIST OF PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function Pin
P00	I/O	Port 0 8-bit I/O port Input/output mode can be specified bitwise	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port Input/output mode can be specified bitwise	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/$\overline{\text{SCK2}}$
P20	I/O	Port 2 8-bit I/O port Input/output mode can be specified bitwise	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P30	I/O	Port 3 8-bit I/O port Input/output mode can be specified bitwise	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/$\overline{\text{SCK3}}$
P40 to P47	I/O	Port 4 8-bit I/O port Input/output mode can be specified bitwise	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port Input/output mode can be specified bitwise	AD8 to AD15

(2/2)

Pin Name	I/O	Function	Alternate Function Pin
P60 to P63	I/O	Port 6 4-bit I/O port Input/output mode can be specified bitwise	A16 to A19
P70 to P77	Input	Port 7 8-bit input port	ANI0 to ANI7
P90	I/O	Port 9 7-bit I/O port Input/output mode can be specified bitwise	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			$\overline{\text{HLDAK}}$
P96			$\overline{\text{HLDRQ}}$
P110	I/O	Port 11 8-bit I/O port Input/output mode can be specified bitwise	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

2.2 Non-port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function Pin
TO110	Output	Pulse signal output from timers 11 to 14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal input for timers 11 to 14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock input for timers 11 to 14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt request input, shared as external capture trigger input for timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt request input, shared as external capture trigger input for timer 12	P14
INTP121			P15/SO2
INTP122			P16/SI2
INTP123			P17/$\overline{\text{SCK2}}$
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/$\overline{\text{SCK3}}$
INTP140	Input	External maskable interrupt request input, shared as external capture trigger input for timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Alternate Function Pin
$\overline{SCK0}$	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
$\overline{SCK1}$			P27
$\overline{SCK2}$			P17/INTP123
$\overline{SCK3}$			P37/INTP133
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	PWM pulse signal output	P20
PWM1			P21
AD0 to AD7	I/O	16-bit multiplexed address/data bus for external memory expansion	P40 to P47
AD8 to AD15			P50 to P57
A16 to A19	Output	High-order address bus used for external memory expansion	P60 to P63
$\overline{LBEN}$	Output	External data bus's low-order byte enable signal output	P90
$\overline{UBEN}$		External data bus's high-order byte enable signal output	P91
R/$\overline{W}$	Output	External read/write status output	P92
$\overline{DSTB}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
$\overline{HLDAK}$	Output	Bus hold acknowledge output	P95
$\overline{HLDRQ}$	Input	Bus hold request input	P96
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
ANO0, ANO1	Output	Analog output to D/A converter	—
NMI	Input	Nonmaskable interrupt request input	—
CLKOUT	Output	System clock output	—
★ $\overline{CKSEL}$	Input	Input for specifying clock generator's operation mode	CV_{DD}
$\overline{WAIT}$	Input	Control signal input for inserting wait in bus cycle	—
MODE	Input	Operation mode select	—
$\overline{RESET}$	Input	System reset input	—
X1	Input	Oscillator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV_{REF1}	Input	Reference voltage input for A/D converter	—
AV_{REF2}	Input	Reference voltage input for D/A converter	—
AV_{REF3}			—
AV_{DD}	—	Positive power supply for A/D converter	—
AV_{SS}	—	Ground potential for A/D converter	—
★ CV_{DD}	—	Positive power supply for on-chip clock generator	$\overline{CKSEL}$
CV_{SS}	—	Ground potential for on-chip clock generator	—
V_{DD}	—	Positive power supply	—
V_{SS}	—	Ground potential	—
IC	—	Internally connected pin (connect directly to V_{SS})	—

2.3 I/O Circuits of Pins and Processing of Unused Pins

Table 2-1 lists I/O circuit type of respective pins and processing method (recommended connection method) when not used. Figure 2-1 illustrates the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

Table 2-1. I/O Circuits of Pins and Processing of Unused Pins (1/2)

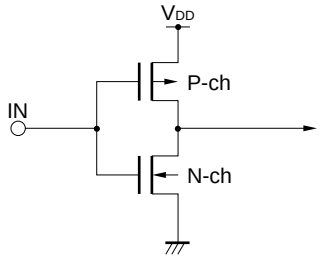
Pin	I/O Circuit Type	Recommended Connection Method
P00/TO110, P01/TO111	5	Input: Connect to V_{DD} or V_{SS} separately via a resistor Output: Leave open
P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113/ADTRG	8	
P10/TO120, P11/TO121	5	
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/$\overline{SCK2}$	8	
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5	
P23/RXD0/SI0, P24/$\overline{SCK0}$	8	
P25/TXD1/SO1	5	
P26/RXD1/SI1, P27/$\overline{SCK1}$	8	
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13 P34/INTP130	8	
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/$\overline{SCK3}$	10-A	
P40/AD0 to P47/AD7	5	
P50/AD8 to P57/AD15		
P60/A16 to P63/A19		
P70/ANI0 to P77/ANI7	9	Connect directly to V_{SS}
P90/$\overline{LBEN}$	5	Input: Connect to V_{DD} or V_{SS} separately via a resistor Output: Leave open
P91/$\overline{UBEN}$		
P92/R/$\overline{W}$		
P93/$\overline{DSTB}$		
P94/ASTB		
P95/$\overline{HLDAK}$		
P96/$\overline{HLDRQ}$		
P110/TO140, P111/TO141		
P112/TCLR14, P113/TI14 P114/INTP140 to P117/INTP143	8	
ANO0, ANO1	12	Leave open
NMI	2	Connect directly to V_{SS}

Table 2-1. I/O Circuits of Pins and Processing of Unused Pins (2/2)

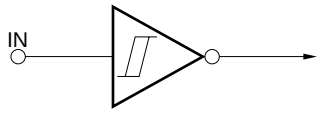
Pin	I/O Circuit Type	Recommended Connection Method
CLKOUT	3	Leave open
$\overline{\text{WAIT}}$	1	Connect directly to V_{DD}
MODE	2	—
$\overline{\text{RESET}}$		
★ $CV_{DD}/\overline{\text{CKSEL}}$		
AV_{REF1} to AV_{REF3}, AV_{SS}	—	Connect directly to V_{SS}
AV_{DD}	—	Connect directly to V_{DD}
IC	—	Connect directly to V_{SS}

Figure 2-1. I/O Circuits of Pins

Type 1

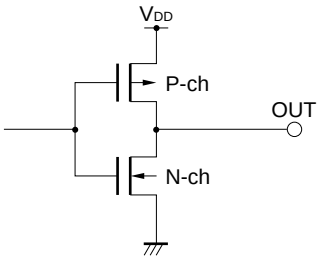


Type 2

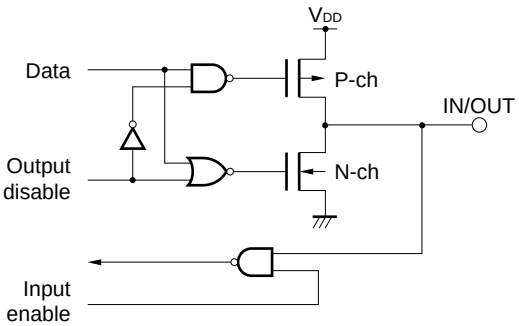


Schmitt trigger input with hysteresis characteristics

Type 3



Type 5



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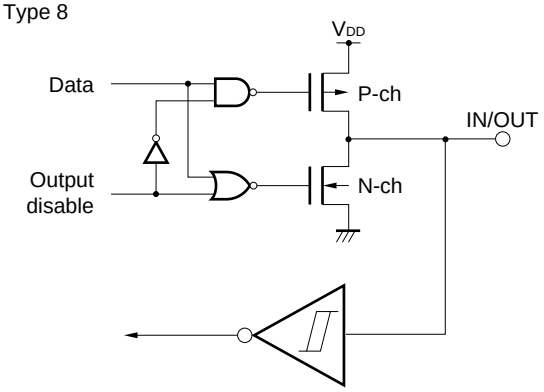
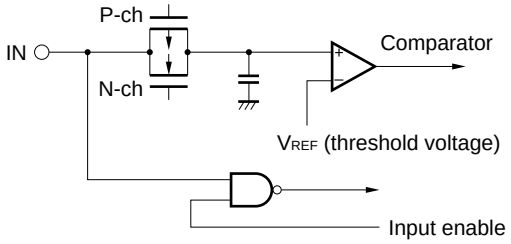
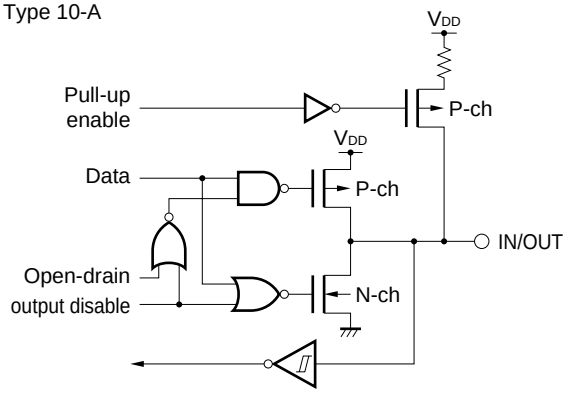


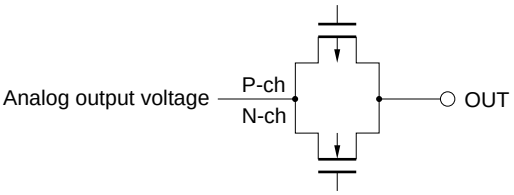
Type 9



Type 10-A



Type 12



3. FUNCTION BLOCKS

3.1 Internal Units

3.1.1 CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other instruction processing.

Other dedicated on-chip hardware, such as the multiplier (16 bits × 16 bits) and the barrel shifter (32 bits) help accelerate processing of complex instructions.

3.1.2 Bus control unit (BCU)

The BCU starts a required bus cycle based on the physical address obtained by the CPU. When an instruction is fetched from external memory space and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in a prefetch queue.

3.1.3 ROM

ROM is mapped to the address space starting at 00000000H. The MODE pin can be used to select an access enable/disable setting. ROM can be accessed by the CPU in one clock cycle when an instruction is fetched.

3.1.4 RAM

RAM is mapped to the address space starting at FFFFE000H. RAM can be accessed by the CPU in one clock cycle when data accessed.

3.1.5 Ports

In addition to the 75 pins (port 0 to port 11) comprising I/O ports (of which eight pins comprise an input-only port), various port pin and control pin functions can be selected for these pins.

3.1.6 Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP110 to INTP113, INTP120 to INTP123, INTP130 to INTP133, and INTP140 to INTP143) from on-chip peripheral hardware and external hardware. Eight interrupt priority levels can be specified for these interrupt requests, and multiplexed servicing control can be performed for interrupt sources.

3.1.7 Clock generator (CG)

An on-chip PLL enables the CPU operating clock to be supplied to resonators connected to pins X1 and X2 at 5× frequency, 1× frequency, and 1/2× frequency. It can also be connected to an external clock instead of to the resonator.

3.1.8 Real-time pulse unit (RPU)

The RPU includes a four-channel 16-bit timer/event counter and a one-channel 16-bit interval timer, which enables measurement of pulse intervals and frequency as well as programmable pulse output.

3.1.9 Serial interface (SIO)

Four channels are comprised of two kinds of serial interfaces: an asynchronous serial interface (UART) and a clock-synchronized serial interface (CSI). Two of these four channels are switchable between the UART and CSI and the other two channels are fixed as CSI.

For UART, data is transferred via the TXD and RXD pins. The baud rate is determined by the on-chip baud rate generator. For CSI, data is transferred via the SO, SI, and $\overline{SCK}$ pins. The baud rate can be determined by the on-chip baud rate generator or it can be supplied from an external source.

One of the two CSI-fixed channels is used as the serial clock output, and serial output is sent via an N-ch open drain output.

3.1.10 Pulse width modulation (PWM)

There are two channels of selectable 8/9/10/12-bit resolution PWM signal outputs. When a low pass filter is externally connected, PWM output can be used as D/A converter output. This is suitable for actuator control applications, such as in motors.

3.1.11 A/D converter (ADC)

This is a high-speed, high-resolution 10-bit A/D converter that includes eight analog input pins. It converts using the sequential conversion method.

3.1.12 D/A converter (DAC)

This is an 8-bit resolution D/A converter that includes two channels. It converts using the R-2R conversion method.

4. CPU FUNCTIONS

The CPU employs a RISC-based architecture and uses five-stage pipeline control to enable single-clock execution of almost all instructions.

The features of the CPU functions are shown below.

- Minimum instruction execution time
  30 ns (during internal 33-MHz operation)
- Address space: 16-Mbyte linear
- General registers: 32 bits × 32 registers
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- 32-bit shift instruction: 1 clock
- Long/short format
- Four types of bit manipulation instructions
  - Set
  - Clear
  - Not
  - Test

5. BUS CONTROL FUNCTIONS

The features of the bus control functions are shown below.

- Shared as port pins, connectable to external device
- Wait functions
  - Programmable wait function for up to three states per two blocks
  - External wait function using $\overline{\text{WAIT}}$ pin
- Idle state insertion function
- Bus mastering arbitration function
- Bus hold function

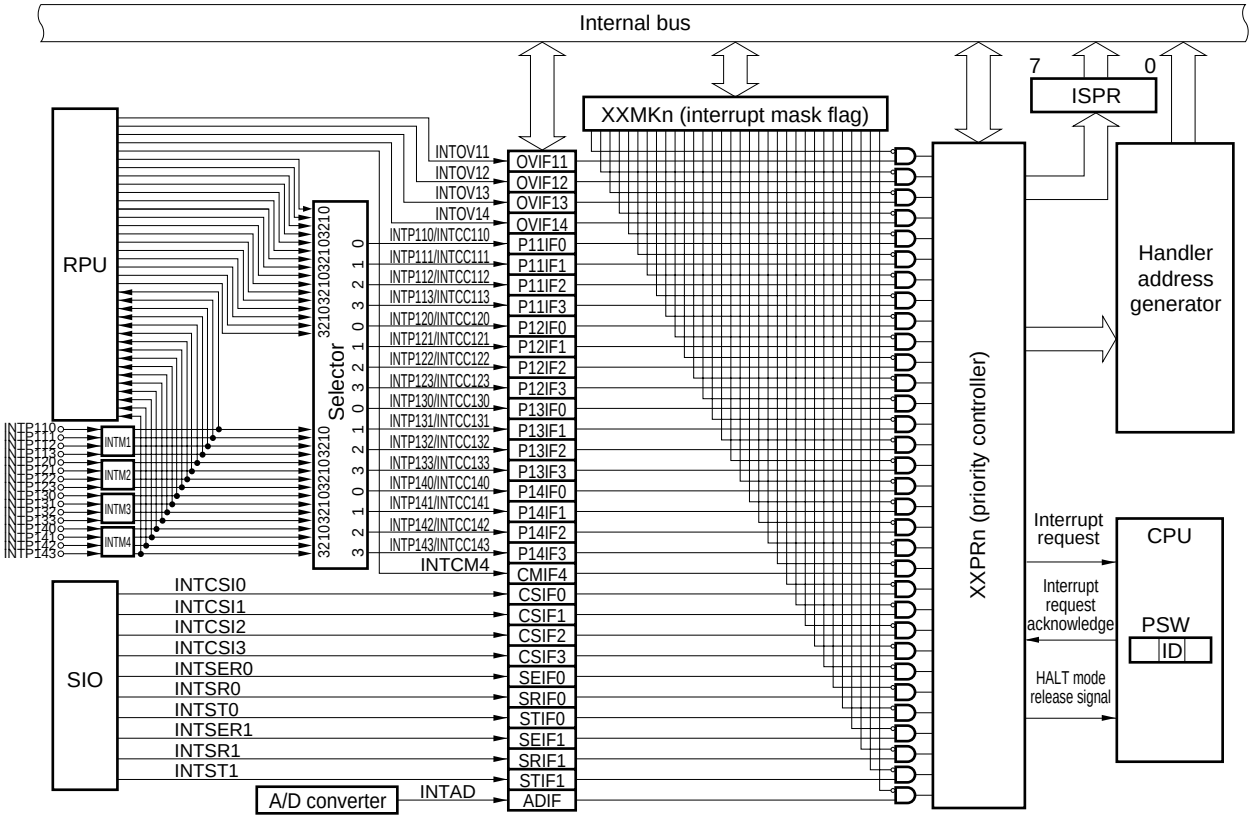
6. INTERRUPT/EXCEPTION HANDLING FUNCTIONS

The features of the interrupt/exception handling functions are shown below.

- Interrupts
  - Nonmaskable interrupt: 1 source
  - Maskable interrupt: 32 sources
  - 8-level programmable priority control
  - Multiple interrupt control based on priority levels
  - Mask specification for each maskable interrupt request
  - Noise elimination, edge detection, and valid edge specification for external interrupt requests
- Exceptions
  - Software exceptions: 32 sources
  - Exception trap: 1 source (invalid instruction code exception)

The configuration of the interrupt/exception handling functions is shown below.

Figure 6-1. Block Diagram of Maskable Interrupt



XX: Name of peripheral unit (OV, P11 to P14, CM, CS, SE, SR, ST, AD)

n: Peripheral unit number (if none exists, then 0 to 4 or 11 to 14)

Interrupt/exception sources are shown in Table 6-1.

Table 6-1. List of Interrupts (1/2)

Type	Category	Interrupt/Exception Source				Default Priority Level	Exception Code	Handler Address	Restored PC
		Name	Control Register	Trigger Source	Unit				
Reset	Interrupt	RESET	—	Reset input	—	—	0000H	00000000H	Undefined
Nonmaskable	Interrupt	NMI	—	NMI input	—	—	0010H	00000010H	nextPC
Software exception	Exception	TRAP0n[Note]	—	TRAP instruction	—	—	004nH[Note]	00000040H	nextPC
	Exception	TRAP1n[Note]	—	TRAP instruction	—	—	005nH[Note]	00000050H	nextPC
Exception trap	Exception	ILGOP	—	Undefined instruction code	—	—	0060H	00000060H	nextPC
Maskable	Interrupt	INTOV11	OVIC11	Timer 11 overflow	RPU	0	0080H	00000080H	nextPC
	Interrupt	INTOV12	OVIC12	Timer 12 overflow	RPU	1	0090H	00000090H	nextPC
	Interrupt	INTOV13	OVIC13	Timer 13 overflow	RPU	2	00A0H	000000A0H	nextPC
	Interrupt	INTOV14	OVIC14	Timer 14 overflow	RPU	3	00B0H	000000B0H	nextPC
	Interrupt	INTP110/INTCC110	P11IC0	Match between INTP110 and CC110	Pin/RPU	4	00C0H	000000C0H	nextPC
	Interrupt	INTP111/INTCC111	P11IC1	Match between INTP111 and CC111	Pin/RPU	5	00D0H	000000D0H	nextPC
	Interrupt	INTP112/INTCC112	P11IC2	Match between INTP112 and CC112	Pin/RPU	6	00E0H	000000E0H	nextPC
	Interrupt	INTP113/INTCC113	P11IC3	Match between INTP113 and CC113	Pin/RPU	7	00F0H	000000F0H	nextPC
	Interrupt	INTP120/INTCC120	P12IC0	Match between INTP120 and CC120	Pin/RPU	8	0100H	00000100H	nextPC
	Interrupt	INTP121/INTCC121	P12IC1	Match between INTP121 and CC121	Pin/RPU	9	0110H	00000110H	nextPC
	Interrupt	INTP122/INTCC122	P12IC2	Match between INTP122 and CC122	Pin/RPU	10	0120H	00000120H	nextPC
	Interrupt	INTP123/INTCC123	P12IC3	Match between INTP123 and CC123	Pin/RPU	11	0130H	00000130H	nextPC
	Interrupt	INTP130/INTCC130	P13IC0	Match between INTP130 and CC130	Pin/RPU	12	0140H	00000140H	nextPC
	Interrupt	INTP131/INTCC131	P13IC1	Match between INTP131 and CC131	Pin/RPU	13	0150H	00000150H	nextPC
	Interrupt	INTP132/INTCC132	P13IC2	Match between INTP132 and CC132	Pin/RPU	14	0160H	00000160H	nextPC
	Interrupt	INTP133/INTCC133	P13IC3	Match between INTP133 and CC133	Pin/RPU	15	0170H	00000170H	nextPC
	Interrupt	INTP140/INTCC140	P14IC0	Match between INTP140 and CC140	Pin/RPU	16	0180H	00000180H	nextPC
	Interrupt	INTP141/INTCC141	P14IC1	Match between INTP141 and CC141	Pin/RPU	17	0190H	00000190H	nextPC
	Interrupt	INTP142/INTCC142	P14IC2	Match between INTP142 and CC142	Pin/RPU	18	01A0H	000001A0H	nextPC
	Interrupt	INTP143/INTCC143	P14IC3	Match between INTP143 and CC143	Pin/RPU	19	01B0H	000001B0H	nextPC
	Interrupt	INTCM4	CMIC4	Signal matches CM4	RPU	20	01C0H	000001C0H	nextPC
	Interrupt	INTCSI0	CSIC0	CSI0 send/receive completion	SIO	21	01D0H	000001D0H	nextPC
	Interrupt	INTCSI1	CSIC1	CSI1 send/receive completion	SIO	22	01E0H	000001E0H	nextPC
	Interrupt	INTCSI2	CSIC2	CSI2 send/receive completion	SIO	23	01F0H	000001F0H	nextPC

Note n represents a value between 0 and FH.

Remarks 1. Default priority: The default priority level is the level that takes precedence when multiple maskable interrupt requests having the same priority level occur at the same time. The highest priority level is level 0.

Restored PC: This is the PC value that is saved to EIPC or FEPC when interrupt or exception handling is activated. However, if an interrupt occurs during execution of the DIVH (divide) instruction, the recovered PC value is the PC value of the current instruction (DIVH).

2. The invalid instruction execution address can be obtained (using restored PC-4) when an invalid instruction code exception occurs.

Table 6-1. List of Interrupts (2/2)

Type	Category	Interrupt/Exception Source				Default Priority Level	Exception Code	Handler Address	Restored PC
		Name	Control Register	Trigger Source	Unit				
Maskable	Interrupt	INTCSI3	CSIC3	CSI3 transmit/receive completion	SIO	24	0200H	00000200H	nextPC
	Interrupt	INTSER0	SEIC0	UART0 receive error	SIO	25	0210H	00000210H	nextPC
	Interrupt	INTSR0	SRIC0	UART0 receive completion	SIO	26	0220H	00000220H	nextPC
	Interrupt	INTST0	STIC0	UART0 transmit completion	SIO	27	0230H	00000230H	nextPC
	Interrupt	INTSER1	SEIC1	UART1 receive error	SIO	28	0240H	00000240H	nextPC
	Interrupt	INTSR1	SRIC1	UART1 receive completion	SIO	29	0250H	00000250H	nextPC
	Interrupt	INTST1	STIC1	UART1 transmit completion	SIO	30	0260H	00000260H	nextPC
	Interrupt	INTAD	ADIC	A/D conversion completion	ADC	31	0270H	00000270H	nextPC

Remarks 1. Default priority: The default priority level is the level that takes precedence when multiple maskable interrupt requests having the same priority level occur at the same time. The highest priority level is level 0.

Restored PC: This is the PC value that is saved to EIPC or FEPC when interrupt or exception handling is started. However, if an interrupt occurs during execution of the DIVH (divide) instruction, the restored PC value is the PC value of the current instruction (DIVH).

2. The invalid instruction execution address can be obtained using (restored PC-4) when an invalid instruction code exception occurs.

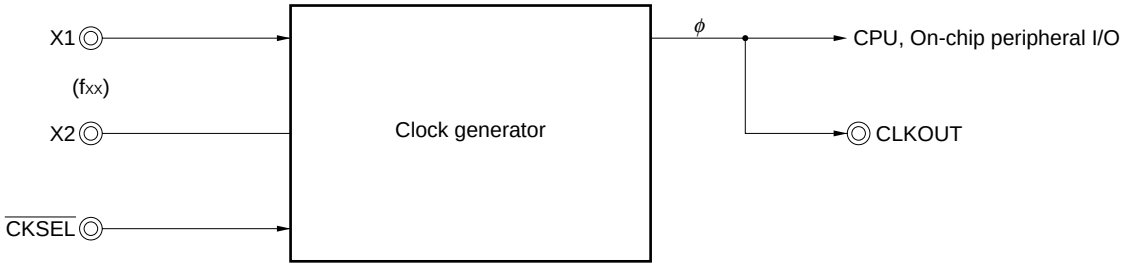
7. CLOCK GENERATION FUNCTIONS

The features of the clock generation functions are shown below.

- Multiplier function using PLL clock synthesizer
- Clock sources
  - Oscillation via resonator connection (PLL mode): $f_{XX} = \phi, 2 \times \phi, \phi/5$
  - External clock (PLL mode): $f_{XX} = \phi, 2 \times \phi, \phi/5$
  - External clock (direct mode): $f_{XX} = 2 \times \phi$
- Power saving control
  - HALT mode
  - IDLE mode
  - Software STOP mode
  - Clock output inhibit mode

The configuration of the clock generation functions is shown below.

★ **Figure 7-1. Block Diagram of Clock Generation Functions**



Remark ϕ : internal system clock

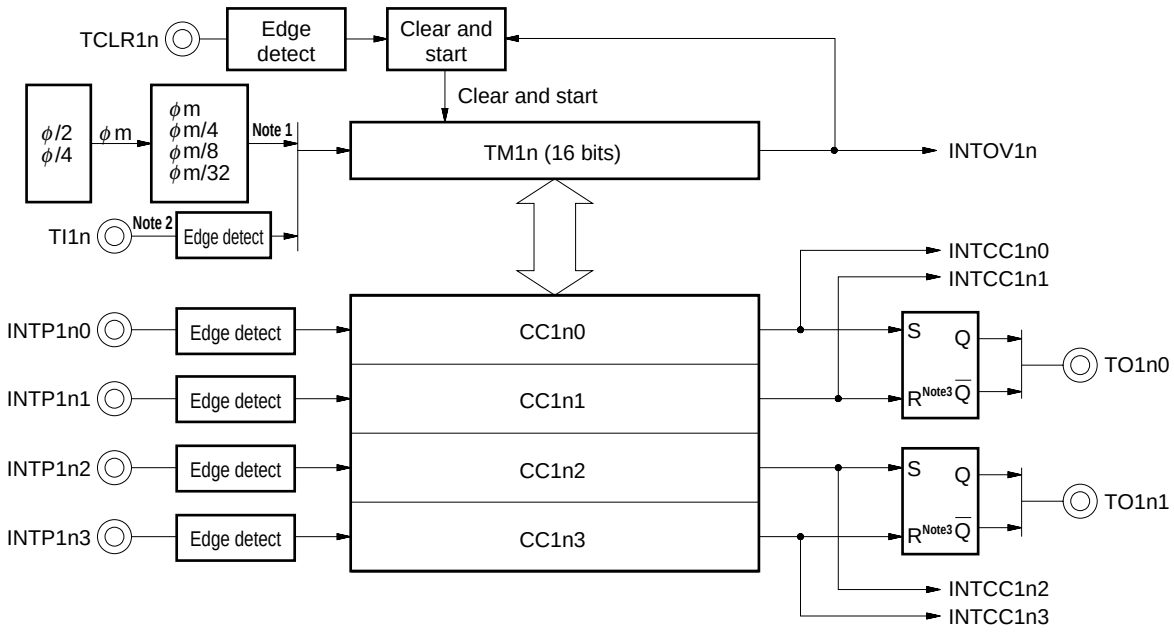
8. TIMER/COUNTER FUNCTIONS (REAL-TIME PULSE UNIT)

The features of the timer/counter functions are shown below.

- Measurement of pulse interval and frequency, programmable pulse output
  - 16-bit measurements enabled
  - Generates a variety of pulse patterns (interval pulse, one-shot pulse, etc.)
- Timer 1
  - 16-bit timer/event counter
  - Count clock sources: two types (selection of an internal system clock division, external pulse input)
  - Capture/compare (shared) registers: 16
  - Count clear pins: TCLR11 to TCLR14
  - Interrupt sources: 20 types
  - External pulse outputs: 8
- Timer 4
  - 16-bit interval timer
  - Count clock: selected from an internal system clock division
  - Compare register: 1
  - Interrupt sources: 1

The configurations of the timer/counter functions are shown below.

Figure 8-1. Block Diagram of Timer 1 (16-bit timer/event counter)



Notes 1. Internal count clock

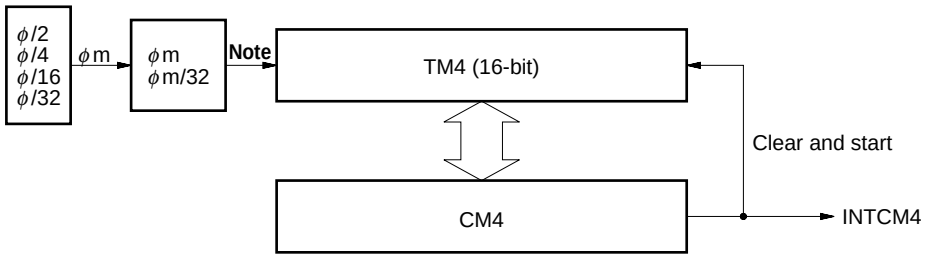
2. External count clock

3. Priority to reset

Remark φ : internal system clock

n = 1 to 4

Figure 8-2. Block Diagram of Timer 4 (16-bit interval timer)



Note Internal count clock

Remark φ : Internal system clock

9. SERIAL INTERFACE FUNCTIONS (SIO)

Two types and six channels of serial interfaces are provided.
Up to four channels may be used at the same time.

(1) Asynchronous serial interfaces 0, 1 (UART0, UART1): 2 channels
(2) Clock-synchronized serial interfaces 0 to 3 (CSI0 to CSI3): 4 channels

Caution UART0 and CSI0 are a shared pin, as are UART1 and CSI1. Either one can be selected via a register (ASIM00, ASIM10).

9.1 Asynchronous Serial Interfaces 0, 1 (UART0, UART1)

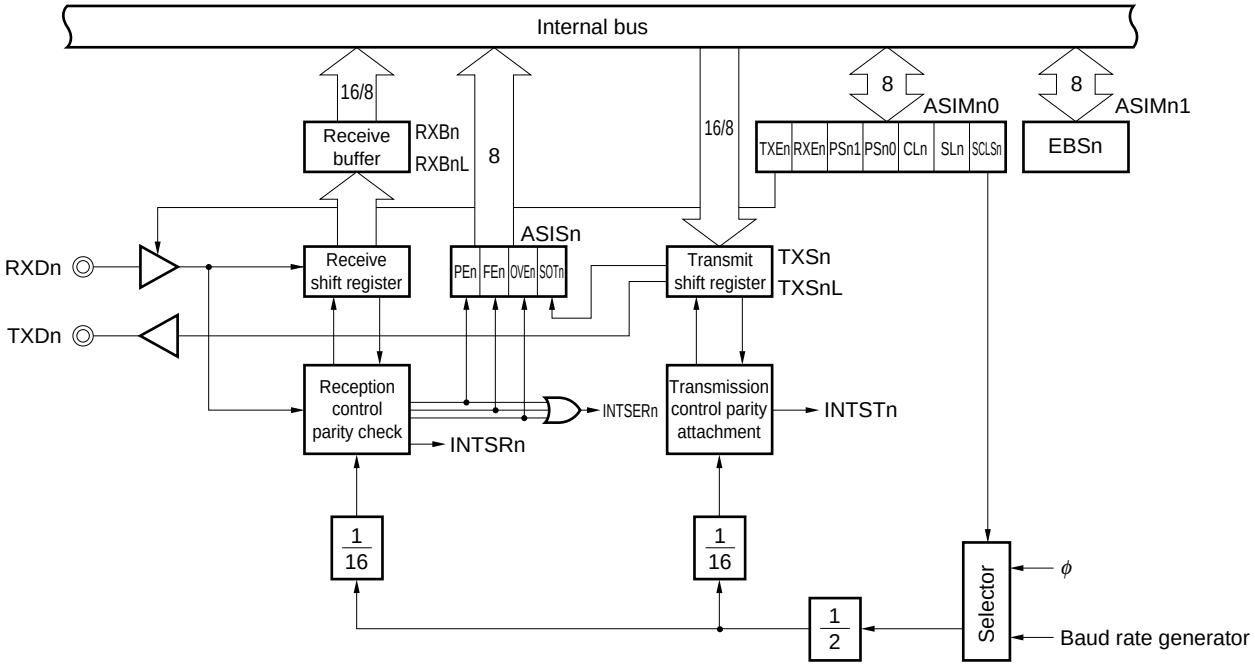
The features of the asynchronous serial interfaces 0, 1 (UART0, UART1) are shown below.

- Transfer rate
  150 bps to 76800 bps (@ ϕ = 33-MHz operation, using baud rate generator)
★ 110 bps to 307200 bps (@ ϕ = 20-MHz operation, using baud rate generator)
★ Maximum 1031 Kbytes (@ ϕ = 33-MHz operation, using ϕ/2)
- Full duplex communications: Receive buffer (RXBn) included
- Two-pin configuration
  TXDn: output pin for transmit data
  RXDn: input pin for receive data
- Reception error detection function
  - Parity error
  - Framing error
  - Overrun error
- Three types of interrupt sources
  - Reception error interrupt (INTSERn)
  - Reception completion interrupt (INTSRn)
  - Transmission completion interrupt (INTSTn)
- The character length of transmit and receive data is specified via the ASIMn0, ASIMn1 register
- Character lengths: 7 or 8 bits, or 9 bits (if using expansion bit)
- Parity function: even, odd, zero, or no parity
- Transmission stop bits: 1 or 2 bits
- On-chip baud rate generator

Remark n = 0, 1
ϕ : internal system clock

The configuration of the asynchronous serial interfaces 0, 1 (UART0, UART1) are shown below.

Figure 9-1. Block Diagram of Asynchronous Serial Interfaces 0, 1 (UART0, UART1)



Remark n = 0, 1

ϕ : internal system clock

9.2 Clock-synchronized Serial Interfaces 0 to 3 (CSI0 to CSI3)

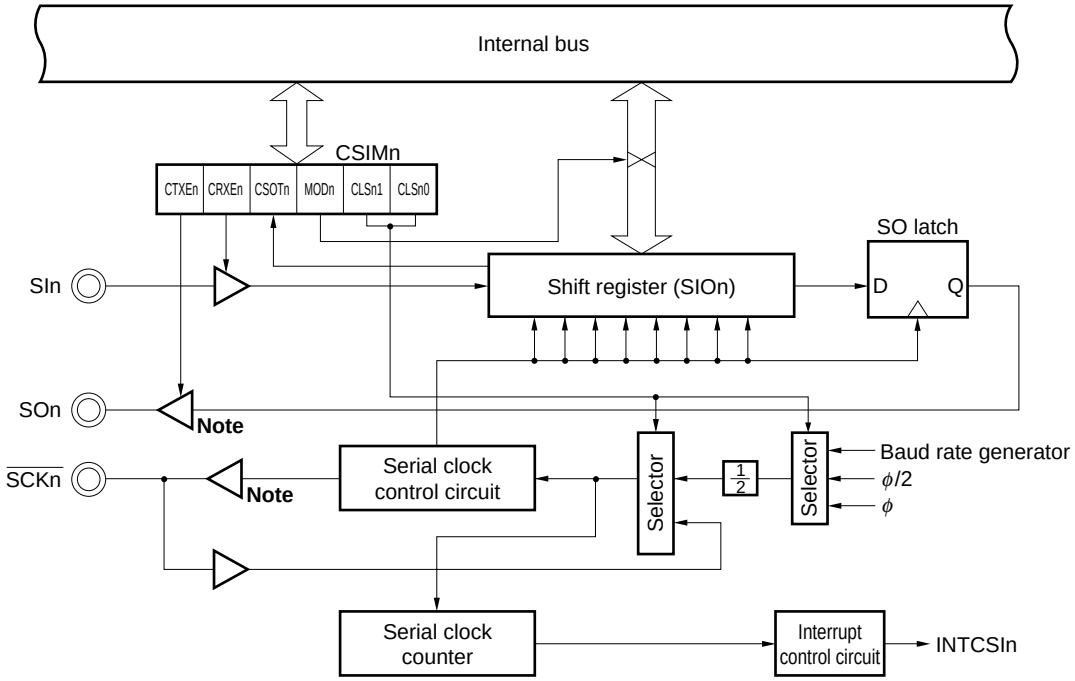
The features of the clock-synchronized serial interfaces 0 to 3 (CSI0 to CSI3) are shown below.

- Number of channels: 4 channels (CSIn)
- High-speed transfer
  MAX 8.25 Mbps (@ ϕ = 33-MHz operation)
- Half-duplex communications
- Character length uses 8-bit unit
- Switchable byte ordering (MSB first or LSB first)
- Selectable external serial clock input/internal serial clock output
- 3-wire type
  SOn: Serial data output
  SIn: Serial data input
  $\overline{\text{SCK}}$n: Serial clock I/O
- Interrupt source: 1 type
  - Transmission/reception completion interrupt (INTCSIn)

Remark n = 0 to 3
ϕ : internal system clock

The configuration of the clock-synchronized serial interfaces 0 to 3 (CSI0 to CSI3) is shown below.

Figure 9-2. Block Diagram of Clock-synchronized Serial Interfaces 0 to 3 (CSI0 to CSI3)



Note SO0 to SO2, $\overline{SCK0}$ to $\overline{SCK2}$: CMOS outputs
SO3, $\overline{SCK3}$: N-ch open-drain outputs

Remark n = 0 to 3
ϕ : internal system clock

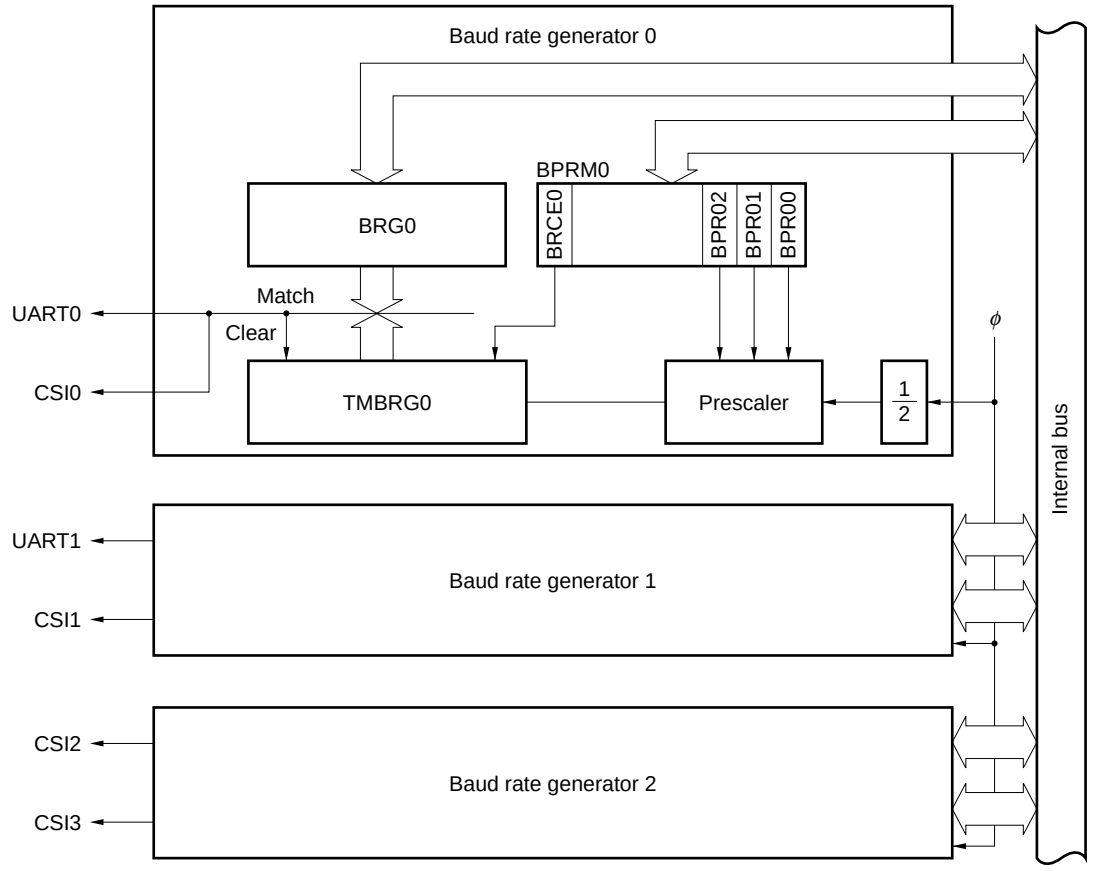
9.3 Baud Rate Generators 0 to 2 (BRG0 to BRG2)

The features of the baud rate generators 0 to 2 (BRG0 to BRG2) are shown below.

- Serial clock can be selected via baud rate generator output and ϕ (internal system clock)
- Identical baud rates during transmission and reception

The configuration of the baud rate generators 0 to 2 (BRG0 to BRG2) is shown below.

★ **Figure 9-3. Block Diagram of Baud Rate Generators 0 to 2 (BRG0 to BRG2)**



10. PWM UNIT

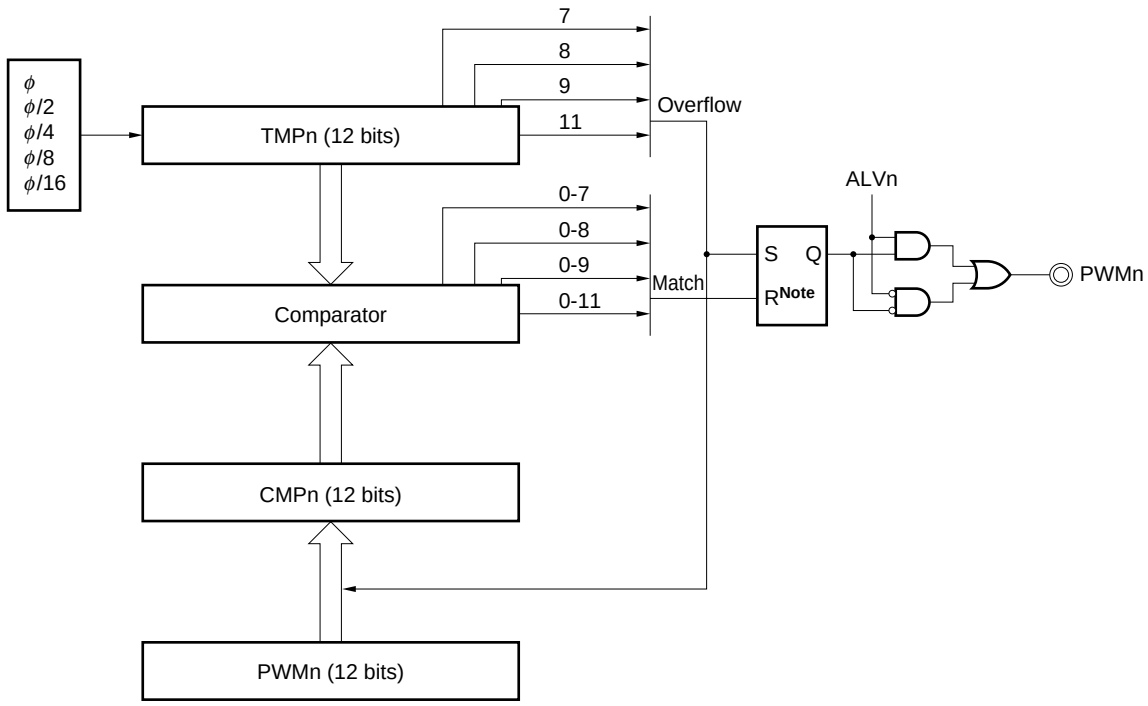
The features of the PWM unit are shown below.

- PWMn: 2 channels
- Selectable active level for PWMn output pulse
- Operating clock selectable as ϕ, ϕ/2, ϕ/4, ϕ/8, or ϕ/16 (ϕ : internal system clock)
- PWMn output resolution selectable as 8, 9, 10, or 12 bits

Remark n = 0, 1

The configuration of the PWM unit is shown below.

Figure 10-1. Block Diagram of PWM Unit



Note Priority to reset

Remark n = 0, 1
ϕ : internal system clock

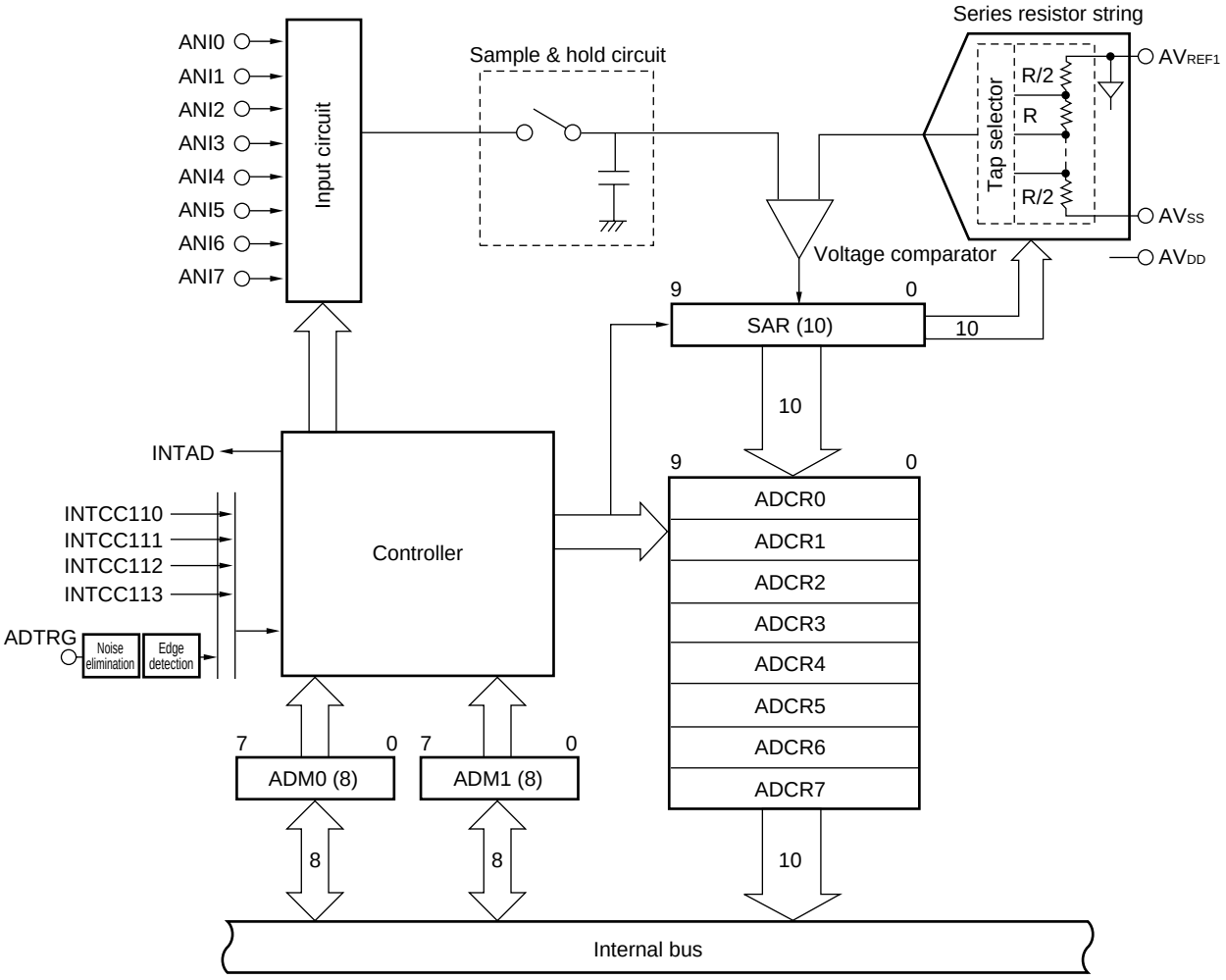
11. A/D CONVERTER

The features of the A/D converter are shown below.

- Analog inputs: 8 channels
- On-chip 10-bit A/D converter
- On-chip A/D conversion result registers (ADCR0 to ADCR7)
  10 bits × 8 registers
- A/D conversion trigger modes
  A/D trigger mode
  Timer trigger mode
  External trigger mode
- Sequential conversion method

The configuration of the A/D converter is shown below.

★ **Figure 11-1. Block Diagram of A/D Converter**



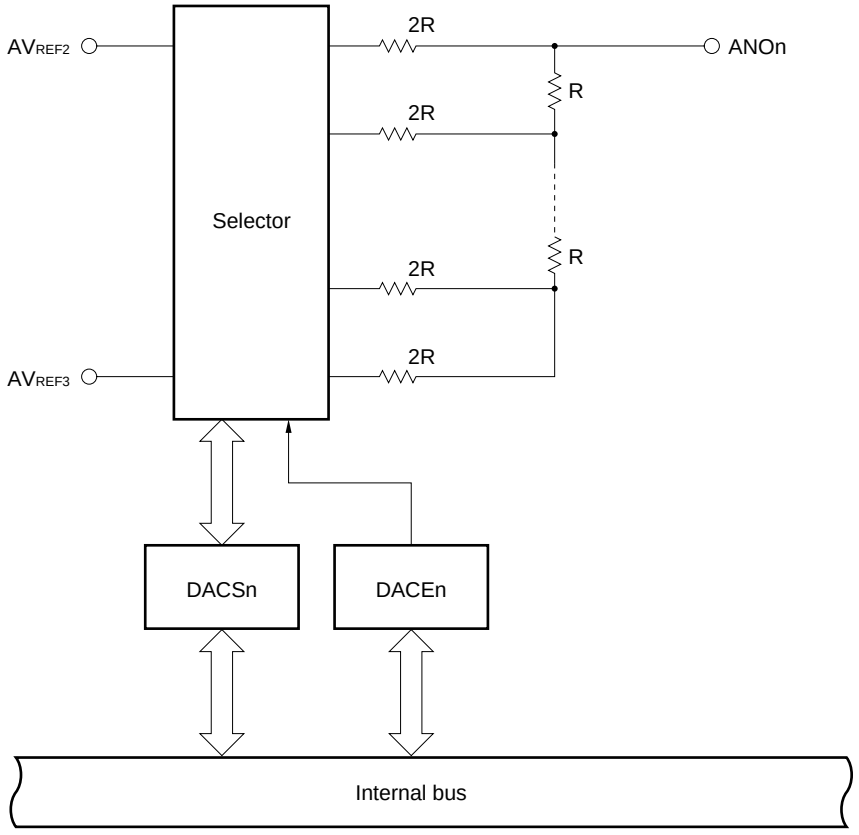
12. D/A CONVERTER

The features of the D/A converter are shown below.

- 8-bit resolution D/A converter: 2 channels
- R-2R conversion method

The configuration of the D/A converter is shown below.

Figure 12-1. Block Diagram of D/A Converter



Remark n = 0, 1

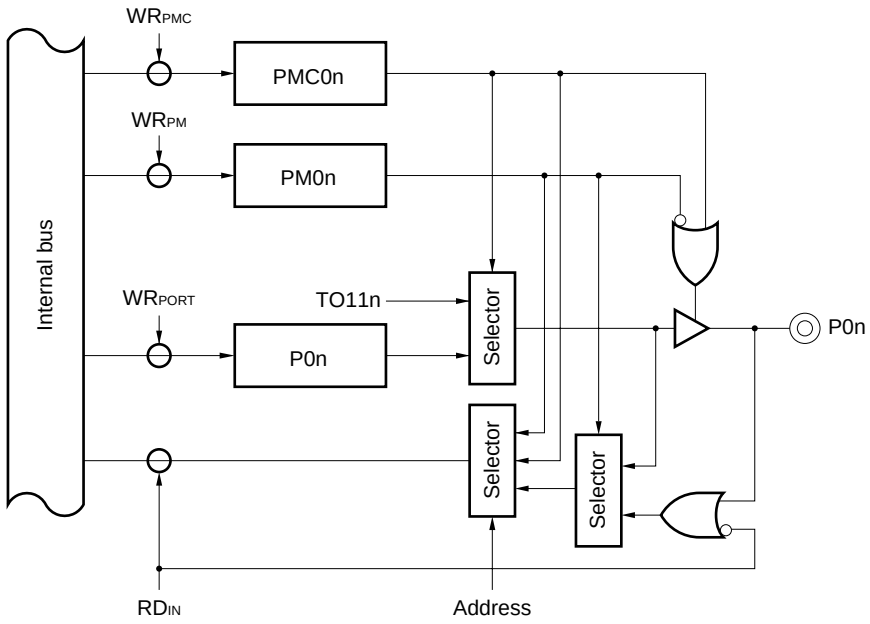
13. PORT FUNCTIONS

The features of the port functions are shown below.

- Number of ports
  Input-only ports: 8
  I/O ports: 67
- Alternated as I/O pins for other peripheral functions
- I/O setting can be specified bitwise
- Noise elimination
- Edge detection

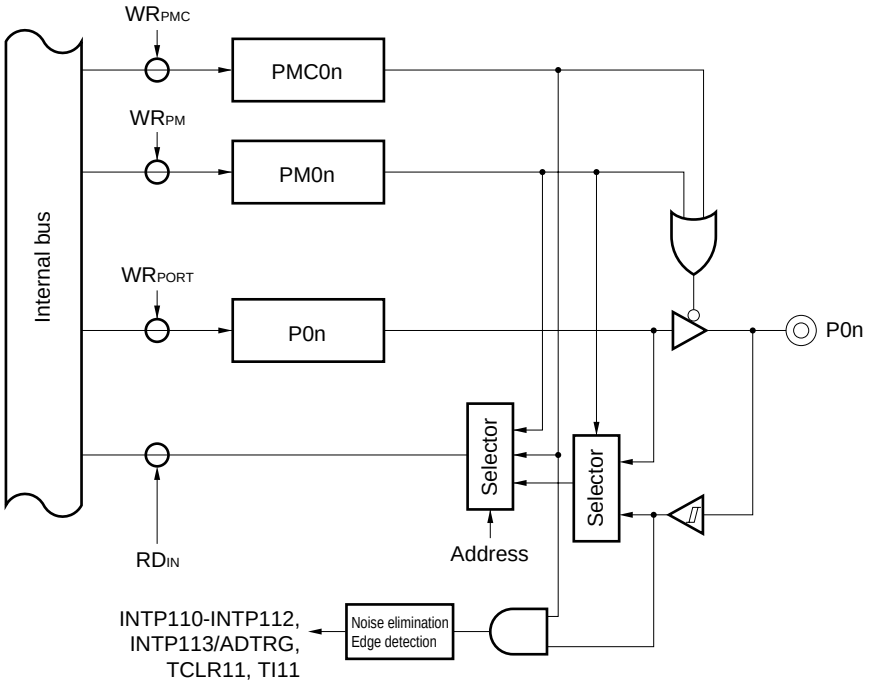
The configurations of the port functions are shown below.

Figure 13-1. Block Diagram of P00 and P01 (Port 0)



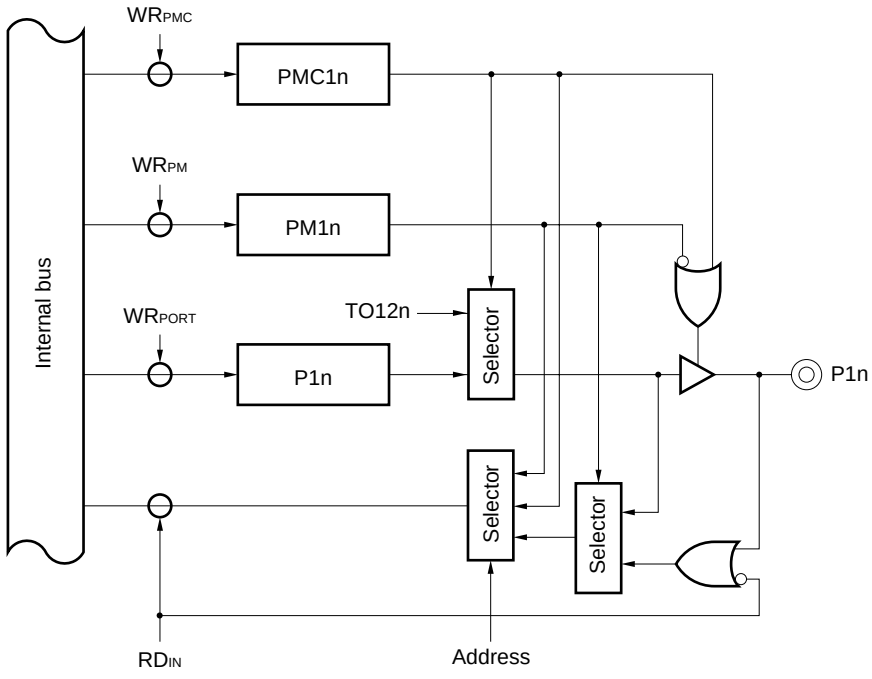
Remark n = 0, 1

Figure 13-2. Block Diagram of P02 to P07 (Port 0)



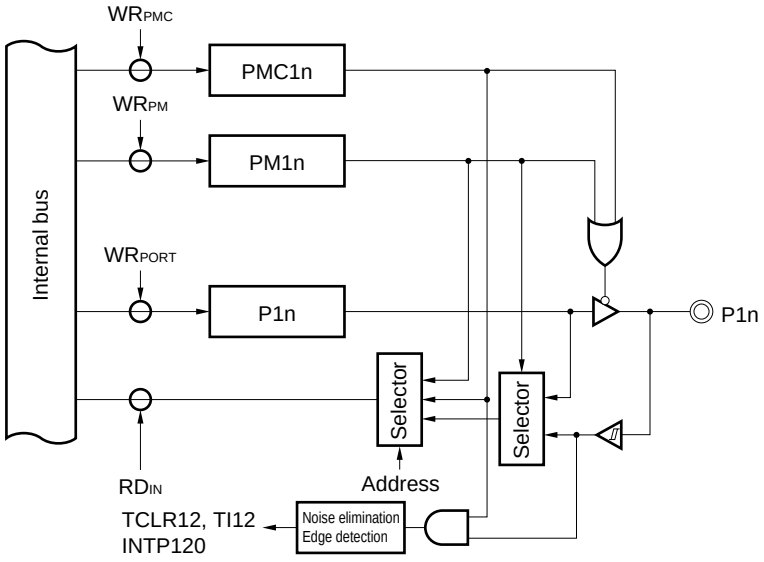
Remark n = 2 to 7

Figure 13-3. Block Diagram of P10 and P11 (Port 1)



Remark n = 0, 1

Figure 13-4. Block Diagram of P12 to P14 (Port 1)



Remark n = 2 to 4

Figure 13-5. Block Diagram of P15 (Port 1)

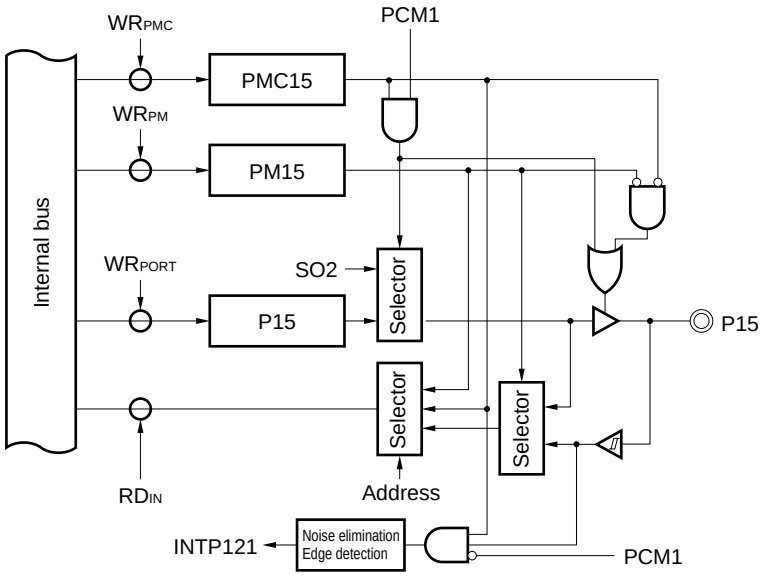


Figure 13-6. Block Diagram of P16 (Port 1)

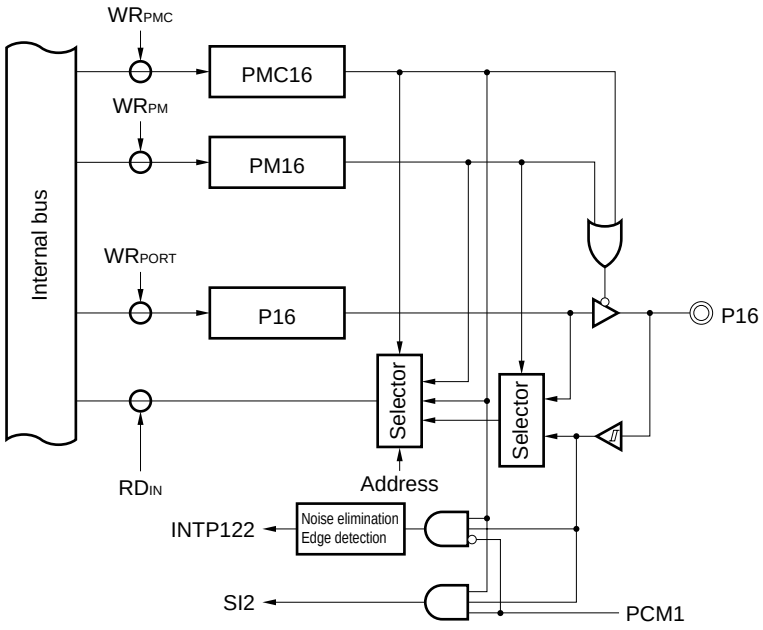


Figure 13-7. Block Diagram of P17 (Port 1)

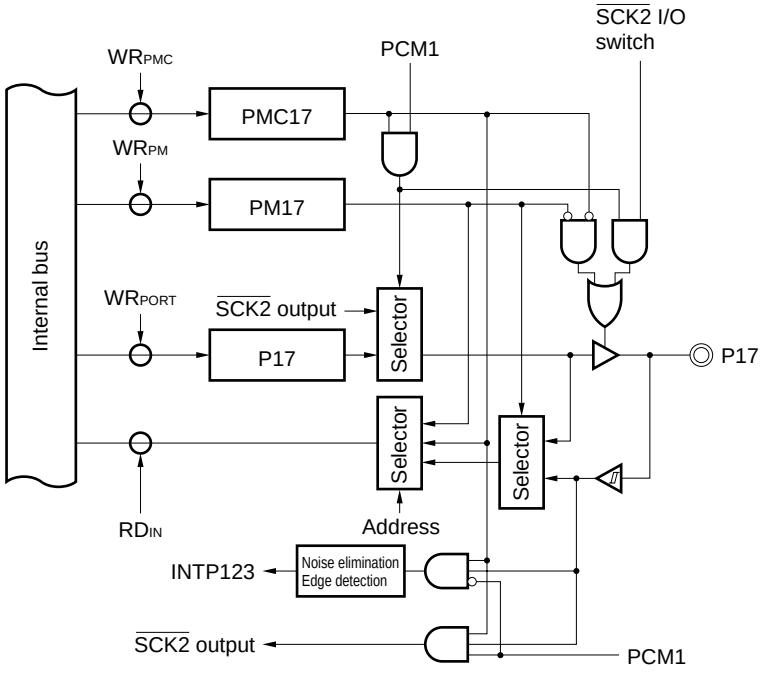
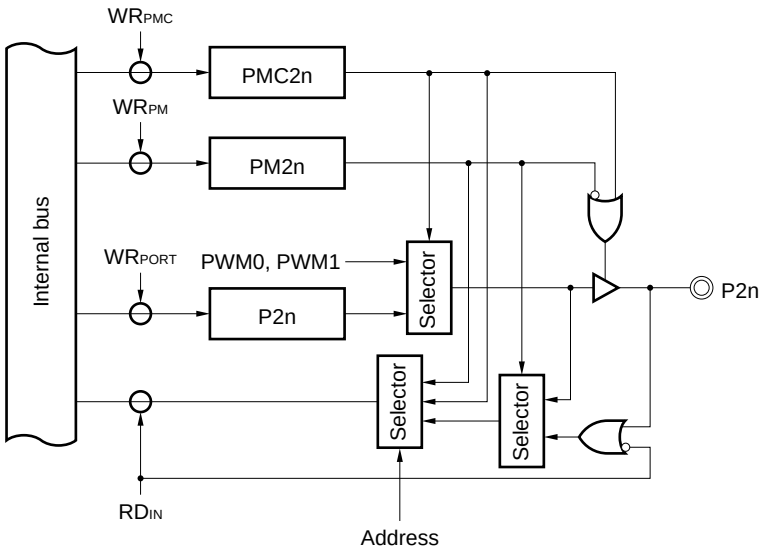
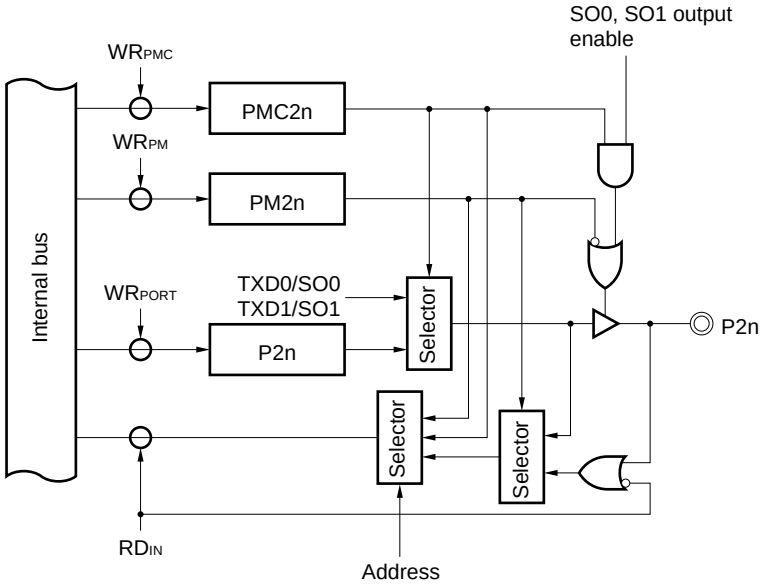


Figure 13-8. Block Diagram of P20 and P21 (Port 2)



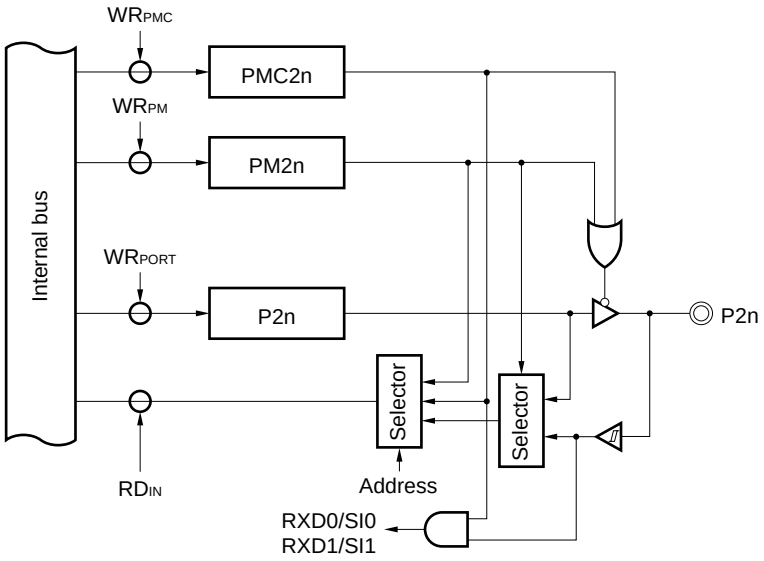
Remark n = 0, 1

Figure 13-9. Block Diagram of P22 and P25 (Port 2)



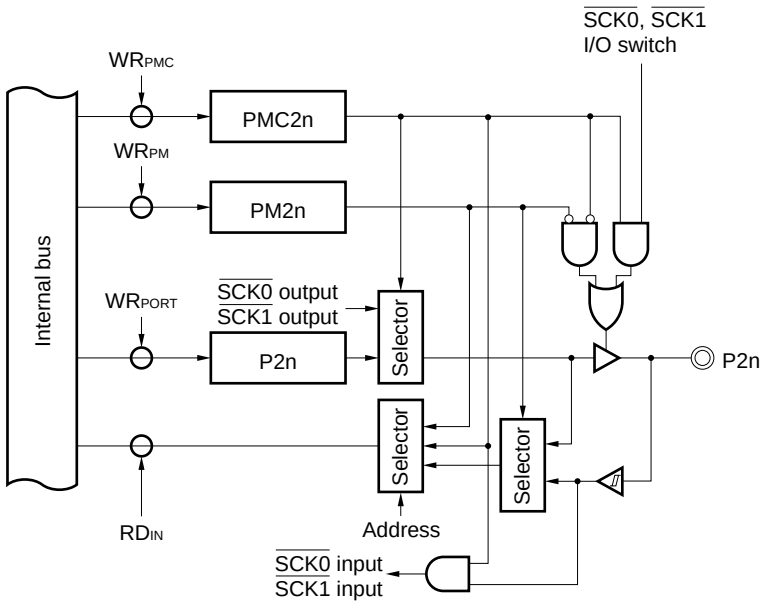
Remark n = 2, 5

Figure 13-10. Block Diagram of P23 and P26 (Port 2)



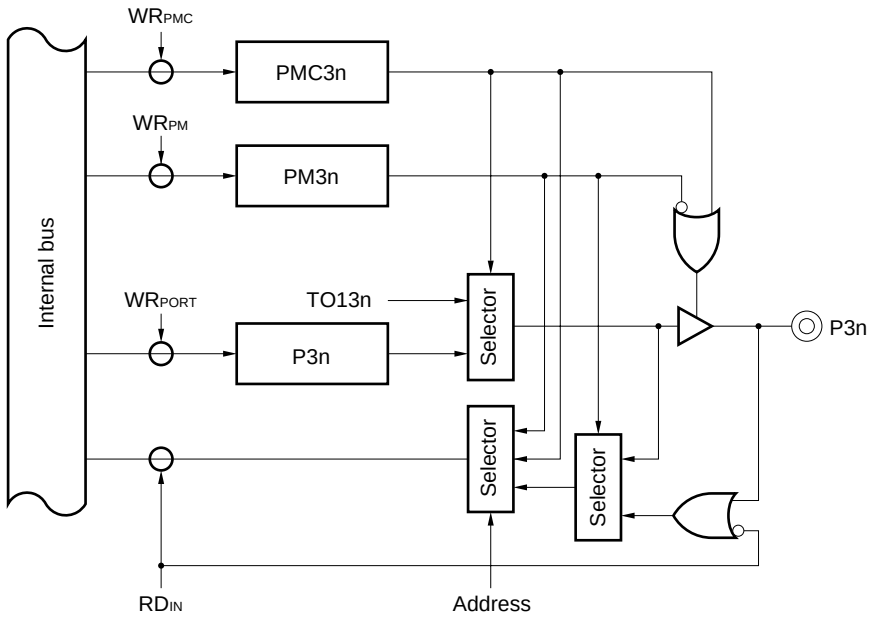
Remark n = 3, 6

Figure 13-11. Block Diagram of P24 and P27 (Port 2)



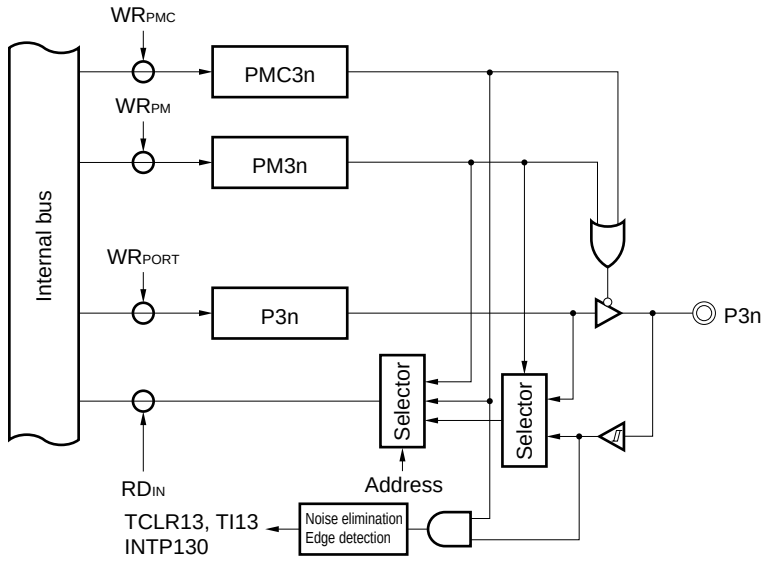
Remark n = 4, 7

Figure 13-12. Block Diagram of P30 and P31 (Port 3)



Remark n = 0, 1

Figure 13-13. Block Diagram of P32 to P34 (Port 3)



Remark n = 2 to 4

Figure 13-14. Block Diagram of P35 (Port 3)

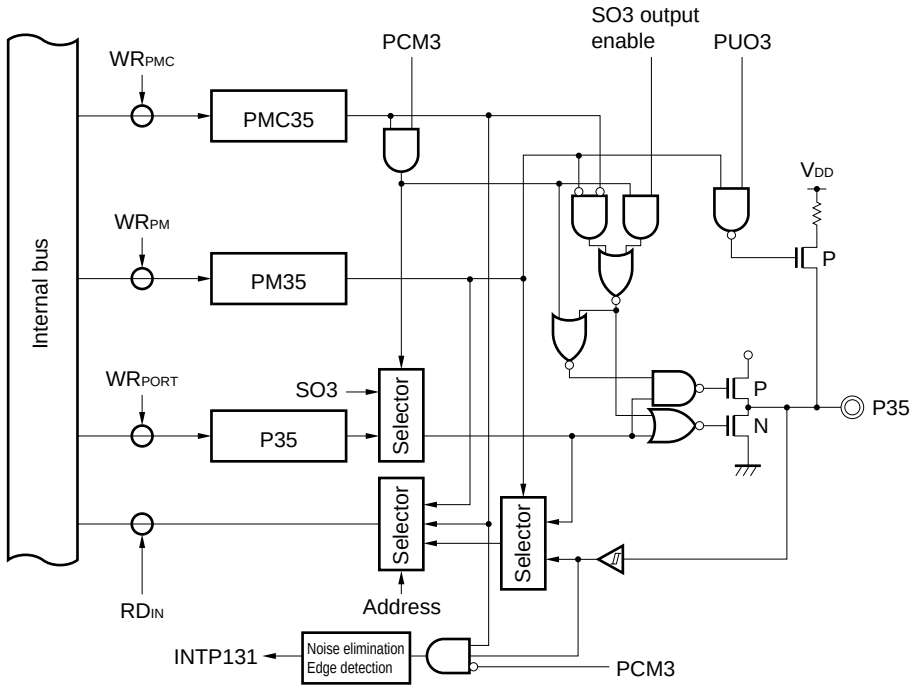


Figure 13-15. Block Diagram of P36 (Port 3)

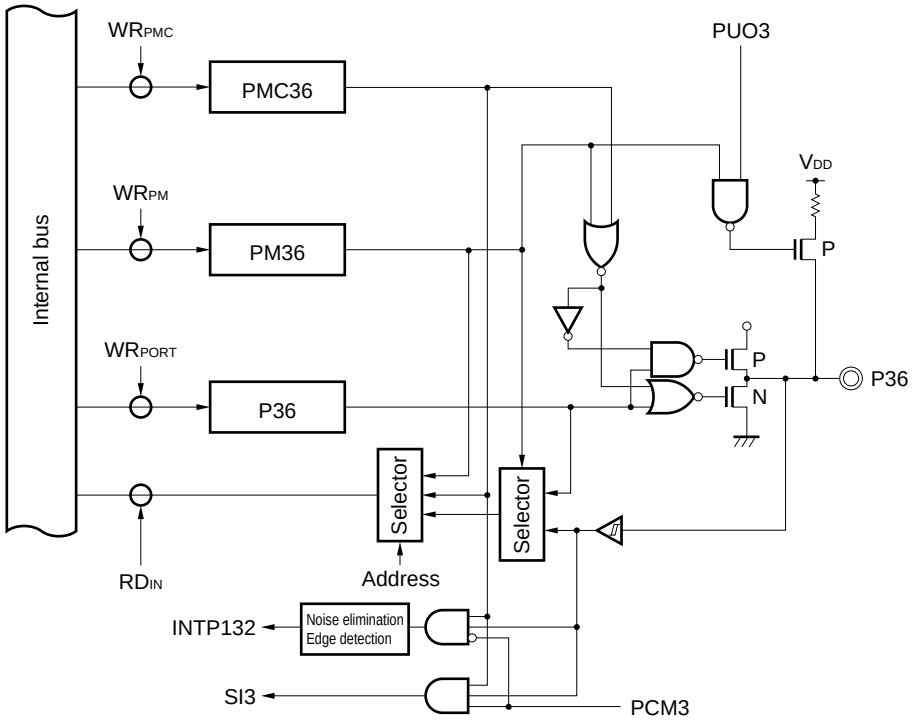


Figure 13-16. Block Diagram of P37 (Port 3)

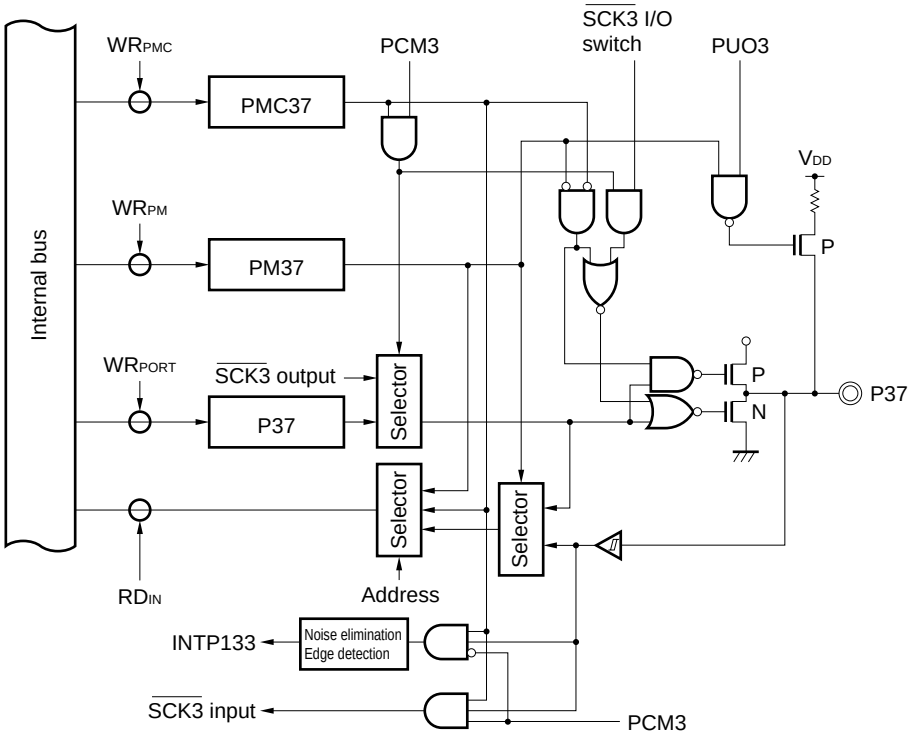
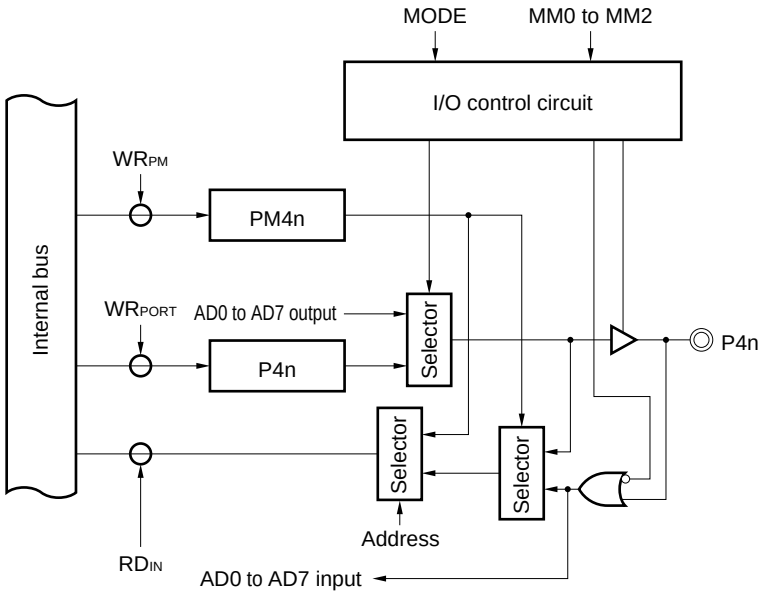
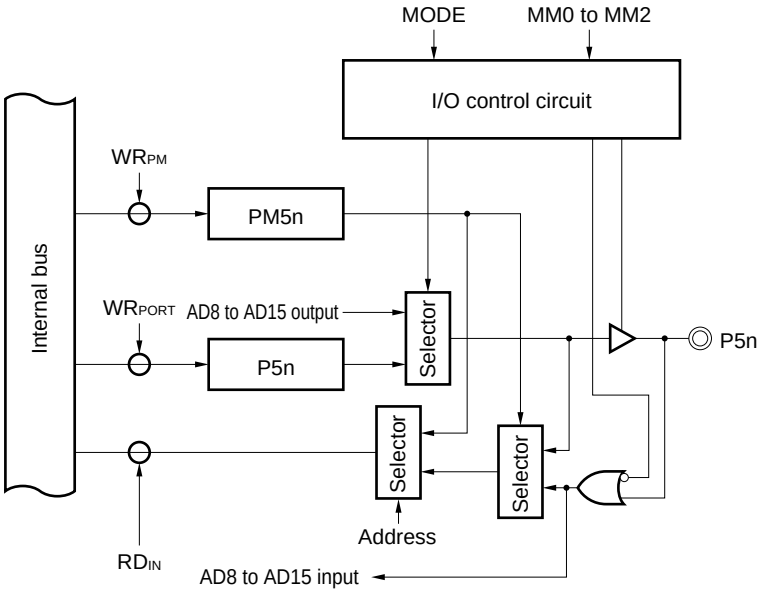


Figure 13-17. Block Diagram of P40 to P47 (Port 4)



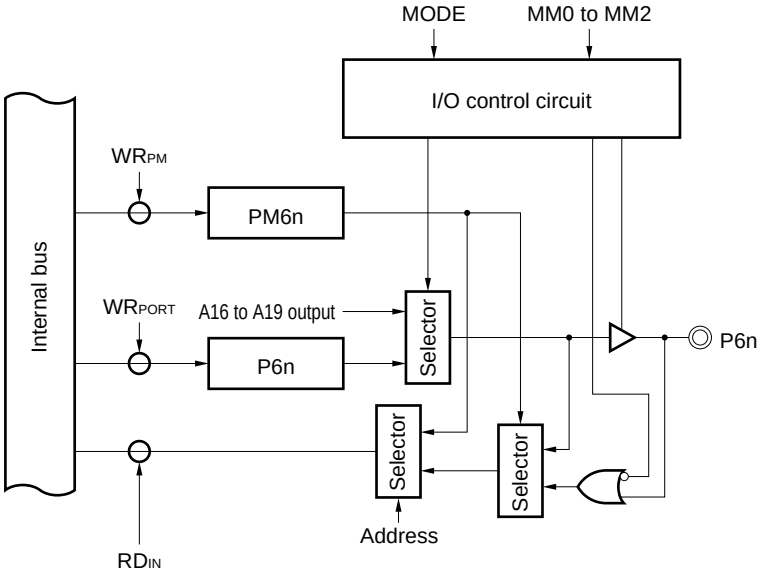
Remark n = 0 to 7

Figure 13-18. Block Diagram of P50 to P57 (Port 5)



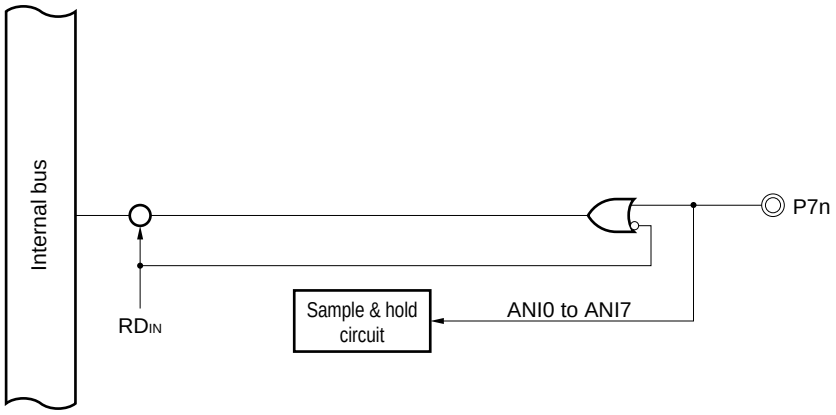
Remark n = 0 to 7

Figure 13-19. Block Diagram of P60 to P63 (Port 6)



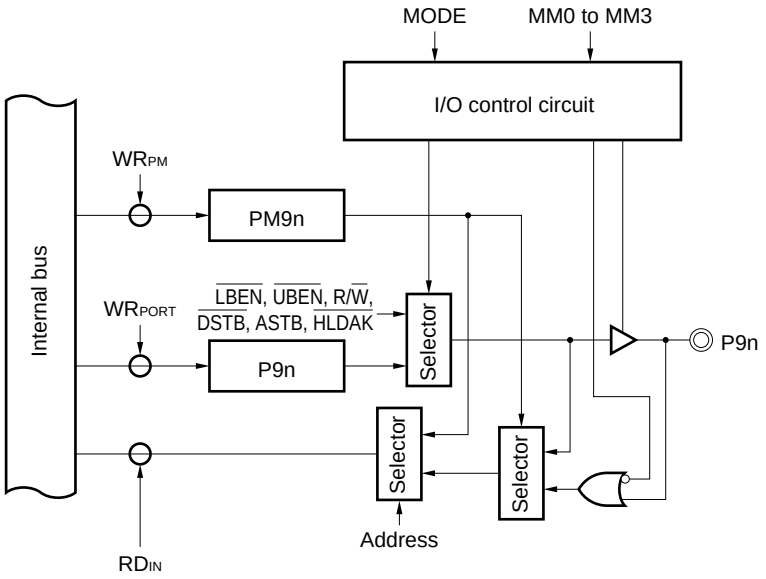
Remark n = 0 to 3

Figure 13-20. Block Diagram of P70 to P77 (Port 7)



Remark n = 0 to 7

Figure 13-21. Block Diagram of P90 to P95 (Port 9)



Remark n = 0 to 5

Figure 13-22. Block Diagram of P96 (Port 9)

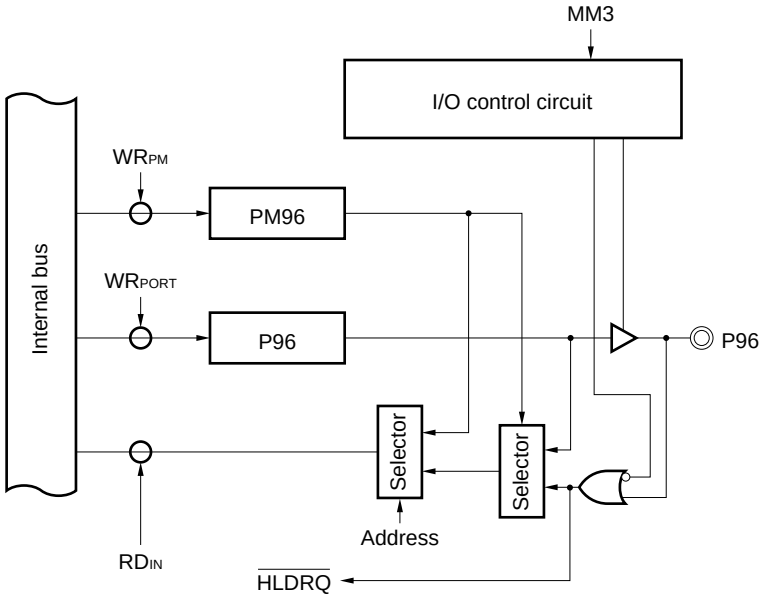
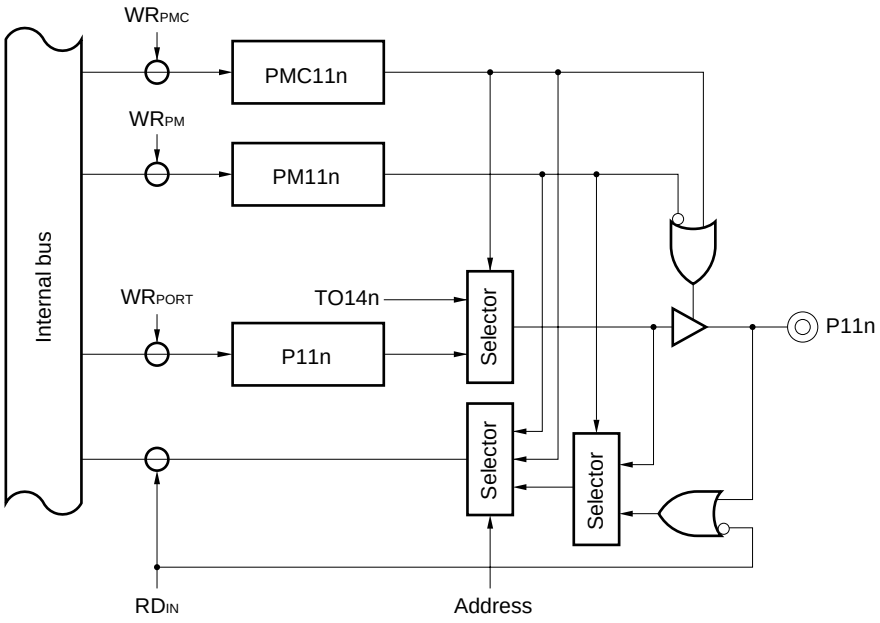
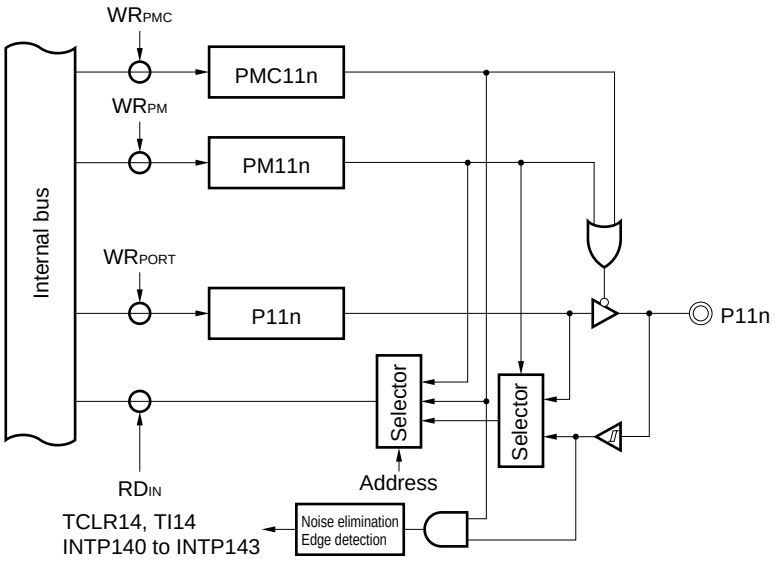


Figure 13-23. Block Diagram of P110 and P111 (Port 11)



Remark n = 0, 1

Figure 13-24. Block Diagram of P112 to P117 (Port 11)



Remark n = 2 to 7

14. RESET FUNCTIONS

When low-level input occurs at the $\overline{\text{RESET}}$ pin, a system reset is performed and the various on-chip hardware devices are reset to their initial settings.

When the input at the $\overline{\text{RESET}}$ pin changes from low level to high level, the reset status is canceled and the CPU resumes program execution. The contents of the various registers should be initialized within the program as necessary.

The feature of the reset functions is shown below.

- On-chip noise elimination circuit which uses analog delay (≅ 60 ns) for the RESET pin

15. INSTRUCTION SET

- **How to read instruction set tables**

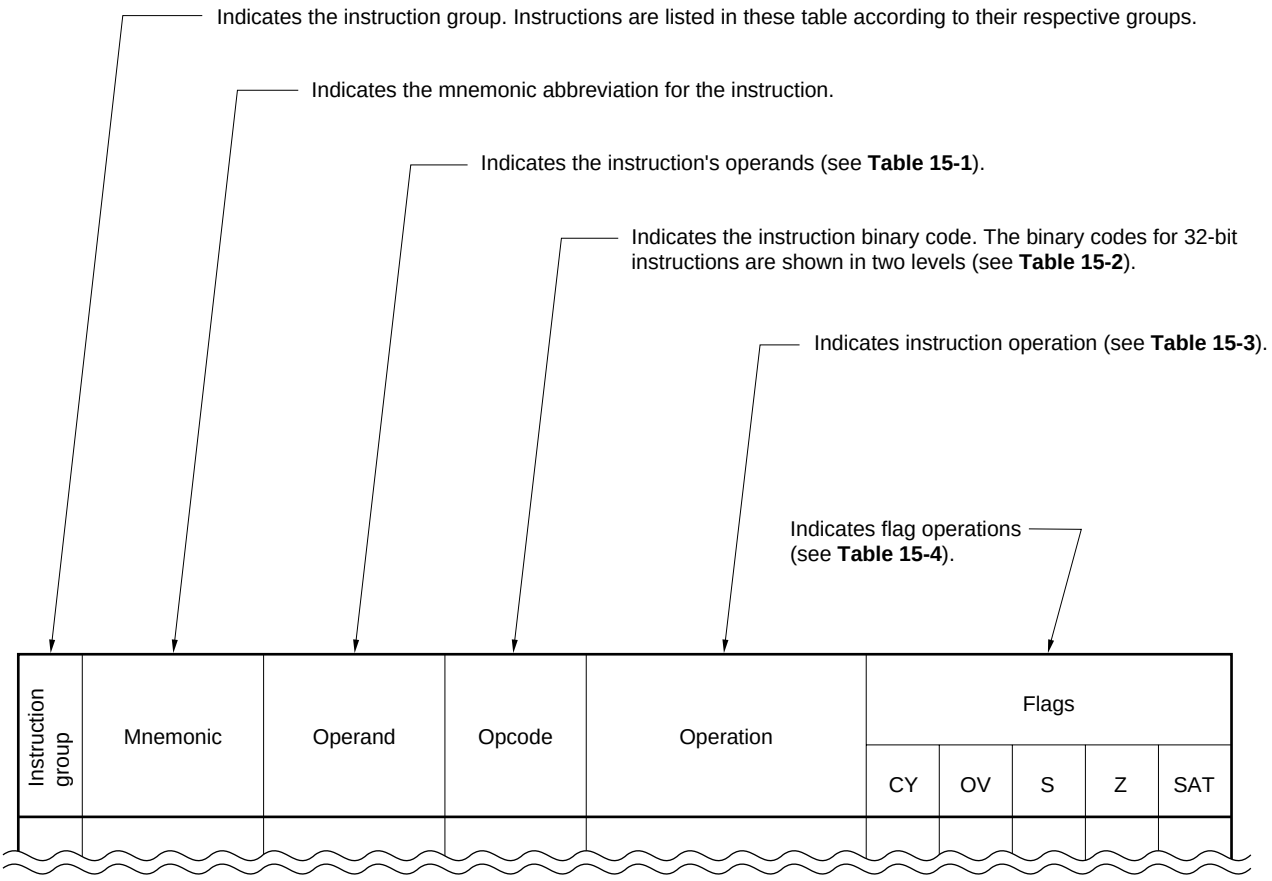


Table 15-1. Symbols Used to Indicate Operands

Symbol	Description
reg1	General registers (r0 to r31): used as source registers
reg2	General registers (r0 to r31): mainly used as destination registers
ep	Element pointer (r30)
bit#3	3-bit data used to specify bit number
immX	X bits immediate
dispX	X bits displaced
regID	System register number
vector	5-bit data used to specify trap vector (00H to 1FH)
cccc	4-bit data used to indicate condition code

Table 15-2. Symbols Used to Indicate Opcodes

Symbol	Description
R	1-bit data of code specifying reg1 or regID
r	1-bit data of code specifying reg2
d	1 bit of displaced data
i	1 bit of immediate data
cccc	4-bit data used to indicate condition code
bbb	3-bit data used to specify bit number

Table 15-3. Symbols Used to Indicate Operations

Symbol	Description
←	Assign
GR [ ]	General register
SR [ ]	System register
zero-extend (n)	Zero-extend n up until word length
sign-extend (n)	Sign-extend n up until word length
load-memory (a, b)	Read data having size b from address a
store-memory (a, b, c)	Replace data b at address a with data having size c
load-memory-bit (a, b)	Read bit b from address a
store-memory-bit (a, b, c)	Write c to bit b from address a
saturated (n)	Execute saturation processing for n (n = complement to 2) Calculation of n: When n ≥ 7FFFFFFFH, result is 7FFFFFFFH. When n ≤ 80000000H, result is 80000000H.
result	Result is indicated by flag operations
Byte	Byte (8 bits)
Halfword	Half word (16 bits)
Word	Word (32 bits)
+	Add
–	Subtract
||	Bit linkage
×	Multiply
÷	Divide
AND	Logical AND
OR	Logical OR
XOR	Exclusive OR
NOT	Logical NOT
logically shift left by	Logical shift left
logically shift right by	Logical shift right
arithmetically shift right by	Arithmetic shift right

Table 15-4. Flag Operations

Identifier	Description
(Blank)	No change
0	Clear to zero
×	Set or clear according to result
R	Restore previously saved value(s)

Table 15-5. Condition Codes

Condition name (cond)	Condition code (cccc)	Conditional expression	Description
V	0000	OV = 1	Overflow
NV	1000	OV = 0	No overflow
C/L	0001	CY = 1	Carry Lower (Less than)
NC/NL	1001	CY = 0	No carry No lower (Greater than or equal)
Z/E	0010	Z = 1	Zero Equal
NZ/NE	1010	Z = 0	Not zero Not equal
NH	0011	(CY OR Z) = 1	Not higher (Less than or equal)
H	1011	(CY OR Z) = 0	Higher (Greater than)
N	0100	S = 1	Negative
P	1100	S = 0	Positive
T	0101	–	Always (unconditional)
SA	1101	SAT = 1	Saturated
LT	0110	(S XOR OV) = 1	Less than signed
GE	1110	(S XOR OV) = 0	Greater than or equal signed
LE	0111	((S XOR OV) OR Z) = 1	Less than or equal signed
GT	1111	((S XOR OV) OR Z) = 0	Greater than signed

Instruction Set List

Instruction group	Mnemonic	Operand	Opcode	Operation	Flags				
					CY	OV	S	Z	SAT
Load/store instructions	SLD.B	disp7[ep], reg2	r r r r r 0 1 1 0 d d d d d d d	adr ← ep + zero-extend (disp7) GR[reg2] ← sign-extend (Load-memory (adr, Byte))					
	SLD.H	disp8[ep], reg2	r r r r r 1 0 0 0 d d d d d d d **Note 1**	adr ← ep + zero-extend (disp8) GR[reg2] ← sign-extend (Load-memory (adr, Halfword))					
	SLD.W	disp8[ep], reg2	r r r r r 1 0 1 0 d d d d d d 0 **Note 2**	adr ← ep + zero-extend (disp8) GR[reg2] ← Load-memory (adr, Word)					
	LD.B	disp16[reg1], reg2	r r r r r 1 1 1 0 0 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← sign-extend (Load-memory (adr, Byte))					
	LD.H	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d d 0 **Note 3**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← sign-extend (Load-memory (adr, Halfword))					
	LD.W	disp16[reg1], reg2	r r r r r 1 1 1 0 0 1 R R R R R d d d d d d d d d d d d d d d 1 **Note 3**	adr ← GR[reg1] + sign-extend (disp16) GR[reg2] ← Load-memory (adr, Word)					
	SST.B	reg2, disp7[ep]	r r r r r 0 1 1 1 d d d d d d d	adr ← ep + zero-extend (disp7) Store-memory (adr, GR[reg2], Byte)					
	SST.H	reg2, disp8[ep]	r r r r r 1 0 0 1 d d d d d d d **Note 1**	adr ← ep + zero-extend (disp8) Store-memory (adr, GR[reg2], Halfword)					
	SST.W	reg2, disp8[ep]	r r r r r 1 0 1 0 d d d d d d 1 **Note 2**	adr ← ep + zero-extend (disp8) Store-memory (adr, GR[reg2], Word)					
	ST.B	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 0 R R R R R d d d d d d d d d d d d d d d d	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Byte)					
	ST.H	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d d 0 **Note 3**	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Halfword)					
	ST.W	reg2, disp16[reg1]	r r r r r 1 1 1 0 1 1 R R R R R d d d d d d d d d d d d d d d 1 **Note 3**	adr ← GR[reg1] + sign-extend (disp16) Store-memory (adr, GR[reg2], Word)					
Arithmetic operation instructions	MOV	reg1, reg2	r r r r r 0 0 0 0 0 0 R R R R R	GR[reg2] ← GR[reg1]					
	MOV	imm5, reg2	r r r r r 0 1 0 0 0 0 i i i i i	GR[reg2] ← sign-extend (imm5)					
	MOVHI	imm16, reg1, reg2	r r r r r 1 1 0 0 1 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + (imm16 || 0^{16})					
	MOVEA	imm16, reg1, reg2	r r r r r 1 1 0 0 0 1 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + sign-extend (imm16)					
	ADD	reg1, reg2	r r r r r 0 0 1 1 1 0 R R R R R	GR[reg2] ← GR[reg2] + GR[reg1]	×	×	×	×	
	ADD	imm5, reg2	r r r r r 0 1 0 0 1 0 i i i i i	GR[reg2] ← GR[reg2] + sign-extend (imm5)	×	×	×	×	
	ADDI	imm16, reg1, reg2	r r r r r 1 1 0 0 0 0 R R R R R i i i i i i i i i i i i i i i i	GR[reg2] ← GR[reg1] + sign-extend (imm16)	×	×	×	×	
	SUB	reg1, reg2	r r r r r 0 0 1 1 0 1 R R R R R	GR[reg2] ← GR[reg2] – GR[reg1]	×	×	×	×	
	SUBR	reg1, reg2	r r r r r 0 0 1 1 0 0 R R R R R	GR[reg2] ← GR[reg1] – GR[reg2]	×	×	×	×	

Notes 1. ddddddd = high-order 7 bits of disp8

2. dddddd = high-order 6 bits of disp8

3. dddddddddddddddd = high-order 15 bits of disp16

Instruction group	Mnemonic	Operand	Opcode	Operation	Flags				
					CY	OV	S	Z	SAT
Arithmetic operation instructions	MULH	reg1, reg2	rrrrr000111RRRRR	GR[reg2] ← GR[reg2]Note × GR[reg1]Note (signed multiplication)					
	MULH	imm5, reg2	rrrrr010111iiiii	GR[reg2] ← GR[reg2]Note × sign-extend (imm5) (signed multiplication)					
	MULHI	imm16, reg1, reg2	rrrrr110111RRRRR iiiiiiiiiiiiiiii	GR[reg2] ← GR[reg1]Note × imm16 (signed multiplication)					
	DIVH	reg1, reg2	rrrrr000010RRRRR	GR[reg2] ← GR[reg2] ÷ GR[reg1]Note (signed division)		×	×	×	
	CMP	reg1, reg2	rrrrr001111RRRRR	result ← GR[reg2] – GR[reg1]	×	×	×	×	
	CMP	imm5, reg2	rrrrr010011iiiii	result ← GR[reg2] – sign-extend (imm5)	×	×	×	×	
	SETF	cccc, reg2	rrrrr1111110cccc 0000000000000000	if conditions are satisfied then GR[reg2] ← 00000001H else GR[reg2] ← 00000000H					
Saturated operation instructions	SATADD	reg1, reg2	rrrrr000110RRRRR	GR[reg2] ← saturated (GR[reg2] + GR[reg1])	×	×	×	×	×
	SATADD	imm5, reg2	rrrrr010001iiiii	GR[reg2] ← saturated (GR[reg2] + sign-extend (imm5))	×	×	×	×	×
	SATSUB	reg1, reg2	rrrrr000101RRRRR	GR[reg2] ← saturated (GR[reg2] – GR[reg1])	×	×	×	×	×
	SATSUBI	imm16, reg1, reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2] ← saturated (GR[reg1] – sign-extend (imm16))	×	×	×	×	×
	SATSUBR	reg1, reg2	rrrrr000100RRRRR	GR[reg2] ← saturated (GR[reg1] – GR[reg2])	×	×	×	×	×
Logical operation instruction	TST	reg1, reg2	rrrrr001011RRRRR	result ← GR[reg2]AND GR[reg1]		0	×	×	
	OR	reg1, reg2	rrrrr001000RRRRR	GR[reg2] ← GR[reg2]OR GR[reg1]		0	×	×	
	ORI	imm16, reg1, reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2] ← GR[reg1]OR zero-extend (imm16)		0	×	×	
	AND	reg1, reg2	rrrrr001010RRRRR	GR[reg2] ← GR[reg2]AND GR[reg1]		0	×	×	
	ANDI	imm16, reg1, reg2	rrrrr110110RRRRR iiiiiiiiiiiiiiii	GR[reg2] ← GR[reg1]AND zero-extend (imm16)		0	0	×	
	XOR	reg1, reg2	rrrrr001001RRRRR	GR[reg2] ← GR[reg2]XOR GR[reg1]		0	×	×	
	XORI	imm16, reg1, reg2	rrrrr110101RRRRR iiiiiiiiiiiiiiii	GR[reg2] ← GR[reg1]XOR zero-extend (imm16)		0	×	×	
	NOT	reg1, reg2	rrrrr00001RRRRR	GR[reg2] ← NOT (GR[reg1])		0	×	×	
	SHL	reg1, reg2	rrrrr111111RRRRR 0000000011000000	GR[reg2] ← GR[reg2]logically shift left by GR[reg1]	×	0	×	×	
	SHL	imm5, reg2	rrrrr010110iiiii	GR[reg2] ← GR[reg2]logically shift left by zero-extend (imm5)	×	0	×	×	
	SHR	reg1, reg2	rrrrr111111RRRRR 0000000010000000	GR[reg2] ← GR[reg2]logically shift right by GR[reg1]	×	0	×	×	
	SHR	imm5, reg2	rrrrr010100iiiii	GR[reg2] ← GR[reg2]logically shift right by zero-extend (imm5)	×	0	×	×	
	SAR	reg1, reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2] ← GR[reg2]arithmetically shift right by GR[reg1]	×	0	×	×	
	SAR	imm5, reg2	rrrrr010101iiiii	GR[reg2] ← GR[reg2]arithmetically shift right by zero-extend (imm5)	×	0	×	×	

Note Only the low-order half word is valid.

Instruction group	Mnemonic	Operand	Opcode	Operation	Flags				
					CY	OV	S	Z	SAT
Branch instructions	JMP	[reg1]	0000000001 1RRRRR	PC ← GR[reg1]					
	JR	disp22	0000011110 ddddddd ddddddddddddddd0 **Note 1**	PC ← PC + sign-extend (disp22)					
	JARL	disp22, reg2	rrrrr11110 ddddddd ddddddddddddddd0 **Note 1**	GR[reg2] ← PC + 4 PC ← PC + sign-extend (disp22)					
	Bcond	disp9	ddddd1011 dddcccc **Note 2**	if conditions are satisfied then PC ← PC + sign-extend (disp9)					
Bit manipulation instructions	SET1	bit#3, disp16[reg1]	00bbb111110 RRRRR ddddddddddddddd	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, 1)				×	
	CLR1	bit#3, disp16[reg1]	10bbb111110 RRRRR ddddddddddddddd	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, 0)				×	
	NOT1	bit#3, disp16[reg1]	01bbb111110 RRRRR ddddddddddddddd	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3)) Store-memory-bit (adr, bit#3, Z flag)				×	
	TST1	bit#3, disp16[reg1]	11bbb111110 RRRRR ddddddddddddddd	adr ← GR[reg1] + sign-extend (disp16) Z flag ← Not (Load-memory-bit (adr, bit#3))				×	

Notes 1. ddddddddddddddddddddddd = high-order 21 bits of disp22

2. dddddddd = high-order 8 bits of disp9

Instruction group	Mnemonic	Operand	Opcode	Operation		Flags				
						CY	OV	S	Z	SAT
Special instructions	LDSR	reg2, regID	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 **Note**	SR[regID] ← GR[reg2]	regID = EIPC, FEPC					
					regID = EIPSW, FEPSW					
					regID = PSW	×	×	×	×	×
	STSR	regID, reg2	r r r r r 1 1 1 1 1 1 R R R R R 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	GR[reg2] ← SR[regID]						
	TRAP	vector	0 0 0 0 0 1 1 1 1 1 1 i i i i i 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	EIPC ← PC + 4 (restored PC) EIPSW ← PSW ECR.EICC ← Interrupt code PSW.EP ← 1 PSW.ID ← 1 PC ← 00000040H (when vector is 00H to 0FH) 00000050H (when vector is 10H to 1FH)						
	RETI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0	if PSW.EP = 1 then PC ← EIPC PSW ← EIPSW else if PSW.NP = 1 then PC ← FEPC PSW ← FEPSW else PC ← EIPC PSW ← EIPSW		R	R	R	R	R
	HALT		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0	Stops						
	DI		0 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID ← 1 (maskable interrupt prohibit)						
	EI		1 0 0 0 0 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0 0 0 0	PSW.ID ← 0 (maskable interrupt enable)						
	NOP		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	No operation, uses at least one clock						

Note In this instructions, “reg2” is the mnemonic abbreviation for the source register, but the reg1 field is used for the opcode. Consequently, these instructions differ from other instructions in a way registers are specified in mnemonics description and opcodes.

rrrrr = regID specification

RRRRR = reg2 specification

16. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition		Rating	Units
Power supply voltage	V_{DD}	V_{DD} pin		–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin		–0.5 to V_{DD} + 0.3	V
	CV_{SS}	CV_{SS} pin		–0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		–0.5 to V_{DD} + 0.3	V
	AV_{SS}	AV_{SS} pin		–0.5 to +0.5	V
Input voltage	V_{I1}	**Note**, V_{DD} = 5.0 V ±10 %		–0.5 to V_{DD} + 0.3	V
Clock input voltage	V_K	X1 pin, V_{DD} = 5.0 V ±10 %		–0.5 to V_{DD} + 1.0	V
Low-level output current	I_{OL}	1 pin		4.0	mA
		Total for all pins		100	mA
High-level output current	I_{OH}	1 pin		–4.0	mA
		Total for all pins		–100	mA
Output voltage	V_O	V_{DD} = 5.0 V ±10 %		–0.5 to V_{DD} + 0.3	V
Analog input voltage	V_{IAN}	P70/ANI0 to P77/ANI7	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.3	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.3	V
Analog reference input voltage	AV_{REF}	AV_{REF1} to AV_{REF3}	$AV_{DD} > V_{DD}$	–0.5 to V_{DD} + 0.3	V
			$V_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.3	V
Operating temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note X1, P70/ANI0 to P77/ANI7, and AV_{REF1} to AV_{REF3} are excluded.

Cautions 1. Be sure to avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, open-drain pins and open collector pins can be directly connected. A direct connection to an external circuit can be made to avoid conflicting output from high-impedance pins if the external circuit is designed for the correct timing.

2. If the absolute maximum rating for any of the above parameters is exceeded even momentarily, it may adversely affect the quality of this product. In other words, these absolute maximum ratings have been set to prevent physical damage to the product. Do not use the product in such a way as to exceed any of these ratings.

The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Units
Input capacitance	C_I	f_C = 1 MHz			15	pF
I/O capacitance	C_{IO}	All pins are 0 V except for testing pin.			15	pF
Output capacitance	C_O				15	pF

★ **Recommended Operating Conditions**

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD})
Direct mode	0 to 33 MHz[Note 1]	–40 to +85°C	5.0 V ±10%
	5 to 33 MHz[Note 2]	–40 to +85°C	5.0 V ±10%
PLL mode	Free-running oscillation frequency to 33 MHz	–40 to +85°C	5.0 V ±10%

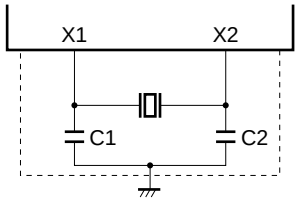
Notes 1. When not using A/D converter

2. When using A/D converter

Remark The range of internal operating clock frequency in PLL mode is the assured range of function operation. PLL locked frequency is specified by t_{CYX}.

★ **Recommended Oscillator**

(a) Ceramic oscillation resonator connection (T_A = –40 to +85°C)



★

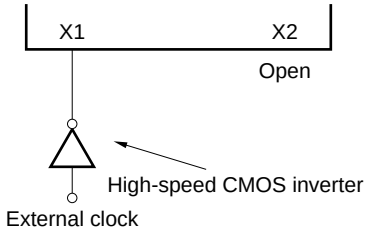
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant C1 (pF)	Recommended Circuit Constant C2 (pF)	Oscillation Voltage Range MIN. (V)	Oscillation Voltage Range MAX. (V)	Oscillation Stabilization Time (MAX.) T_{OST} (ms)
TDK	CCR5.0MC3	5.0	On-chip	On-chip	4.5	5.5	0.36
	FCR5.0MC5	5.0	On-chip	On-chip	4.5	5.5	0.32
	CCR6.6MC3	6.6	On-chip	On-chip	4.5	5.5	0.28
Murata Mfg.	CSA5.00MG040	5.0	100	100	4.5	5.5	0.46
	CST5.00MGW040	5.0	On-chip	On-chip	4.5	5.5	0.46
	CSA6.60MTZ040	6.6	100	100	4.5	5.5	0.42
	CST6.60MTW040	6.6	On-chip	On-chip	4.5	5.5	0.42

Cautions 1. Set the oscillator as close to the X1 and X2 pins as possible.

2. No other signal lines should be wired in the area enclosed by broken lines.

3. When matching μPD703003 with a resonator, be sure to perform sufficient evaluation.

(b) External clock input



Cautions 1. Set high-speed CMOS inverter as close as possible to the X1 pin.

2. When matching μPD703003 and a high-speed CMOS inverter, be sure to perform sufficient evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Units
High-level input voltage	V_{IH}	Except for X1 and pins listed in **Note**	2.2		V_{DD} + 0.3	V
		Note	0.8 V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	Except for X1 and pins listed in **Note**	–0.5		+0.8	V
		Note	–0.5		0.2 V_{DD}	V
High-level clock input voltage	V_{XH}	X1	0.8 V_{DD}		V_{DD} + 0.5	V
Low-level clock input voltage	V_{XL}	X1	–0.5		+0.6	V
Schmitt trigger input Threshold voltage	V_T^+	**Note**, rising edge		3.0		V
	V_T^-	**Note**, falling edge		2.0		V
Schmitt trigger input hysteresis width	$V_T^+ - V_T^-$	**Note**	0.5			V
High-level output voltage	V_{OH}	I_{OH} = –2.5 mA	0.7 V_{DD}			V
★		I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	I_{OL} = 2.5 mA			0.45	V
High-level input leak current	I_{LIH}	V_I = V_{DD}			10	μA
Low-level input leak current	I_{LIL}	V_I = 0 V			–10	μA
High-level output leak current	I_{LOH}	V_O = V_{DD}			10	μA
Low-level output leak current	I_{LOL}	V_O = 0 V			–10	μA
Software pull-up resistance	R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$	15	40	90	kΩ

Note P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/$\overline{SCK2}$, P23/RXD0/SI0, P24/$\overline{SCK0}$, P26/RXD1/SI1, P27/$\overline{SCK1}$, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, $\overline{RESET}$, NMI, MODE

Remarks 1. TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.

2. ϕ = Internal system clock frequency

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V) (2/2)**

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Units
Power supply current	When operating	I_{DD1}	Direct mode[Note]		2.4 × ϕ + 6	2.8 × ϕ + 19	mA
			PLL mode		2.5 × ϕ + 8	2.9 × ϕ + 22	mA
	During HALT mode	I_{DD2}	Direct mode[Note]		1.4 × ϕ + 5	1.5 × ϕ + 18	mA
			PLL mode		1.5 × ϕ + 7	1.6 × ϕ + 20	mA
	During IDLE mode	I_{DD3}	Direct mode[Note]		18.6 × ϕ + 100	22 × ϕ + 200	μA
			PLL mode		0.05 × ϕ + 4	0.1 × ϕ + 8	mA
	During STOP mode	I_{DD4}	–40°C ≤ T_A ≤ +50°C		2	50	μA
			50°C < T_A ≤ 85°C		2	200	μA

Note When using A/D converter: ϕ = 5 to 33 MHz
When not using A/D converter: ϕ = 0 to 33 MHz

Remarks 1. TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V. The power supply current does not include AV_{REF1} to AV_{REF3} or the current that flows across the software pull-up resistance.

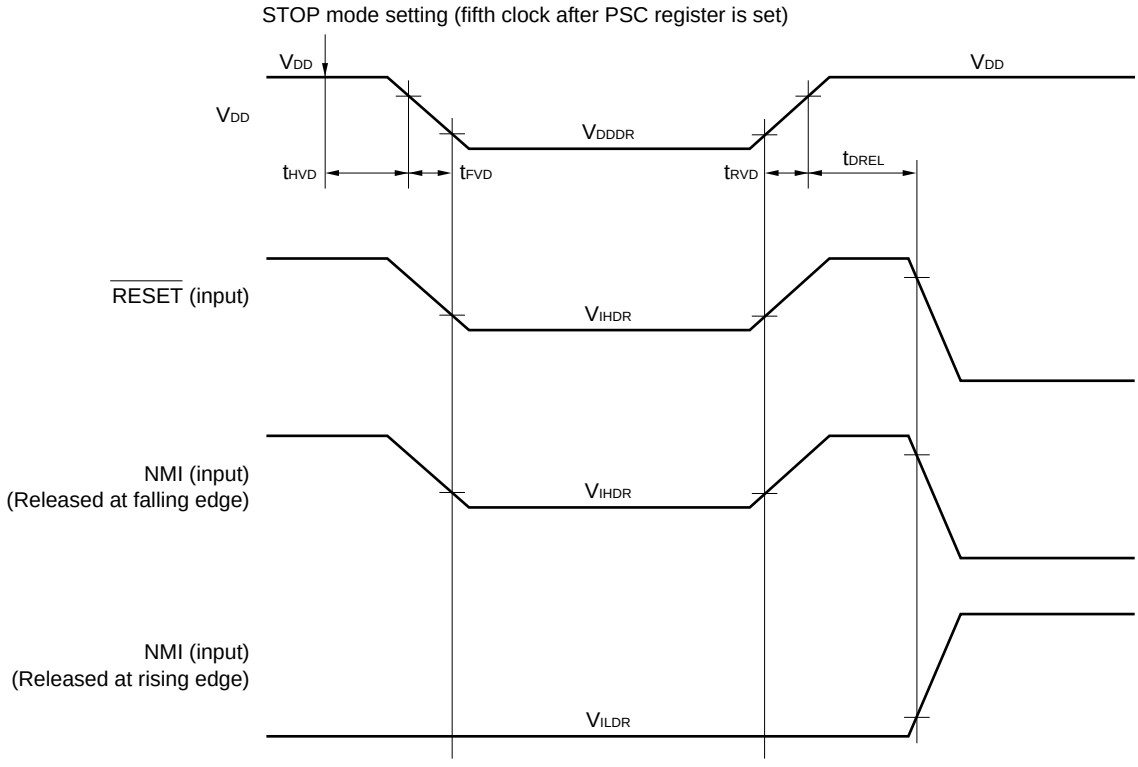
2. ϕ = Internal system clock frequency

Data Hold Characteristics (T_A = –40 to +85°C)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Units
	Data hold voltage	V_{DDDR}	STOP mode		1.5		5.5	V
★	Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$	–40°C ≤ T_A ≤ +50°C		0.2 V_{DDDR}	50	μA
				50°C < T_A ≤ 85°C		0.2 V_{DDDR}	200	μA
	Power supply voltage rise time	t_{RVD}			200			μs
	Power supply voltage fall time	t_{FVD}			200			μs
	Power supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
	STOP mode release signal input time	t_{DREL}			0			ns
	Data hold high-level input voltage	V_{IHDR}	**Note**		0.9 V_{DDDR}		V_{DDDR}	V
	Data hold low-level input voltage	V_{ILDR}	**Note**		0		0.1 V_{DDDR}	V

Note P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/$\overline{SCK2}$, P23/RXD0/SI0, P24/$\overline{SCK0}$, P26/RXD1/SI1, P27/$\overline{SCK1}$, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, $\overline{RESET}$, NMI, MODE, X1

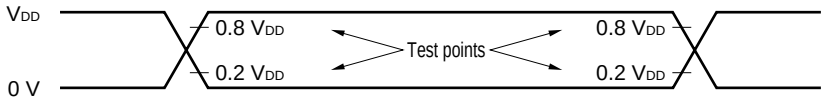
Remark TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.



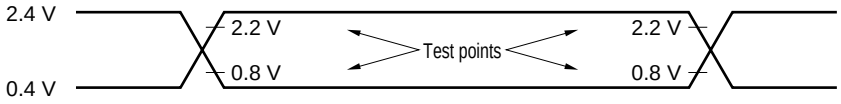
AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V)

AC test input waveform

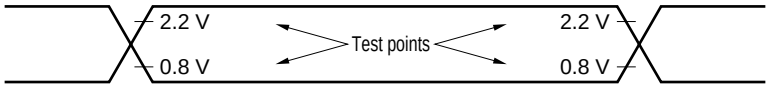
(a) P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/$\overline{SCK2}$, P23/RXD0/SI0, P24/$\overline{SCK0}$, P26/RXD1/SI1, P27/$\overline{SCK1}$, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, $\overline{RESET}$, NMI, MODE, X1



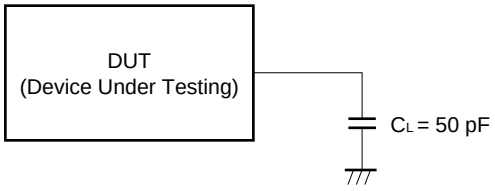
(b) Pins other than those listed in (a) above



AC test output test points



Load condition



Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to below 50 pF.

(1) Clock timing

	Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
★	X1 input cycle	<1>	t_{CYX}	Direct mode	20	**Note 1**	15	**Note 1**	ns
★				PLL mode (PLL locked)	200	250	150	250	ns
	X1 input high-level width	<2>	t_{WXH}	Direct mode	7		6		ns
				PLL mode	80		60		ns
	X1 input low-level width	<3>	t_{WXL}	Direct mode	7		6		ns
				PLL mode	80		60		ns
	X1 input rise time	<4>	t_{XR}	Direct mode		7		7	ns
				PLL mode		15		10	ns
	X1 input fall time	<5>	t_{XF}	Direct mode		7		7	ns
				PLL mode		15		10	ns
★	CPU operating frequency	—	ϕ	Direct mode	**Note 2**	25	**Note 2**	33	MHz
★				PLL mode	**Note 3**	25	**Note 3**	33	MHz
★	CLKOUT output cycle	<6>	t_{CYK}		40	**Note 4**	30	**Note 4**	ns
	CLKOUT input high-level width	<7>	t_{WKH}		0.5T – 5		0.5T – 5		ns
	CLKOUT input low-level width	<8>	t_{WKL}		0.5T – 5		0.5T – 5		ns
	CLKOUT input rise time	<9>	t_{KR}			5		5	ns
	CLKOUT input fall time	<10>	t_{KF}			5		5	ns
	X1 ↓ → CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	17	3	17	ns

★ **Notes 1.** When using A/D converter : 100 ns
When not using A/D converter : DC

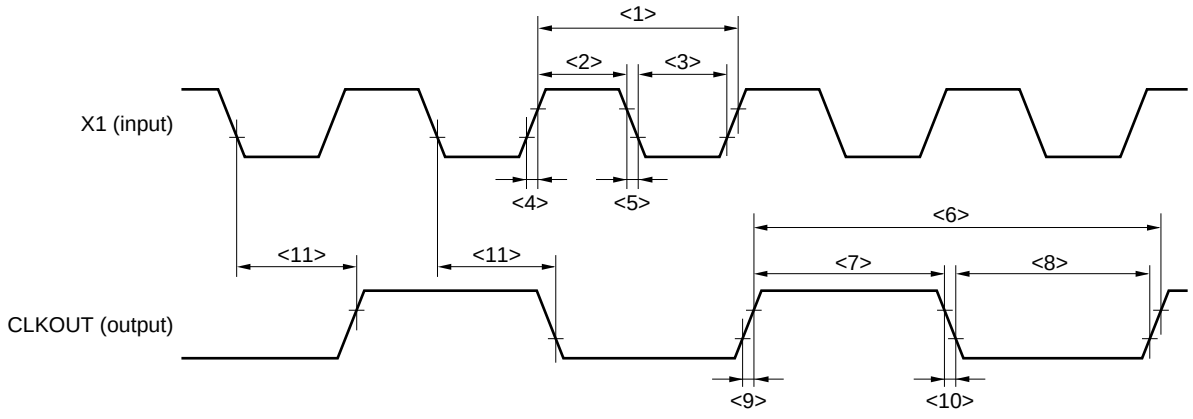
★ **2.** When using A/D converter : 5 MHz
When not using A/D converter : 0 MHz

★ **3.** Free-running oscillation frequency

★ **4.** When using A/D converter : 200 ns
When not using A/D converter : DC

Remark T = t_{CYK}

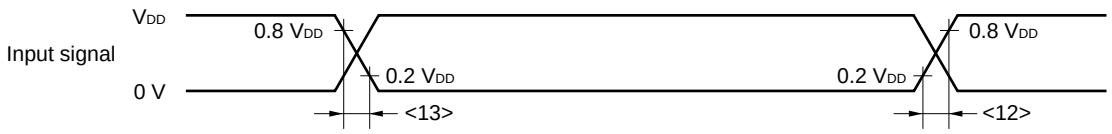
Parameter	Symbol		Conditions	TYP.	Units
Free-running oscillation frequency	—	ϕ_P	PLL mode	5	MHz



(2) Input waveform

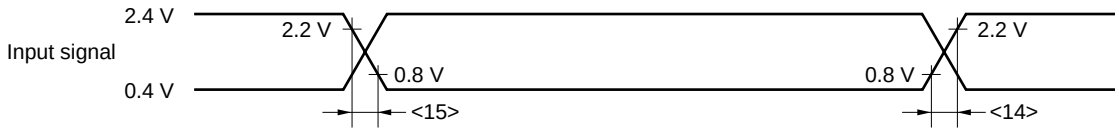
(a) P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/$\overline{SCK2}$, P23/RXD0/SI0, P24/$\overline{SCK0}$, P26/RXD1/SI1, P27/$\overline{SCK1}$, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/$\overline{SCK3}$, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, $\overline{RESET}$, NMI, MODE

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<12>	t_{IR2}			20		20	ns
Input fall time	<13>	t_{IF2}			20		20	ns



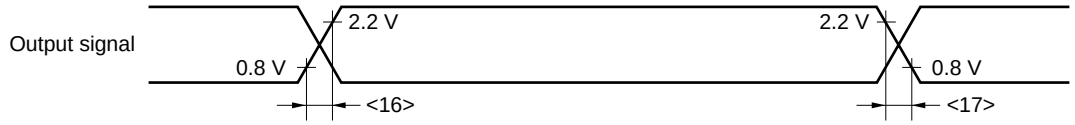
(b) Pins other than those listed in (a) above

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<14>	t_{IR1}			10		10	ns
Input fall time	<15>	t_{IF1}			10		10	ns



★ **(3) Output waveform (other than CLKOUT)**

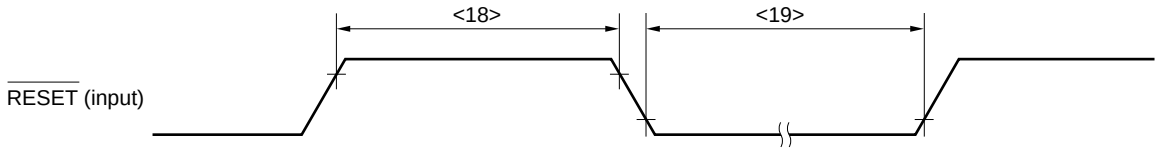
Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
Output rise time	<16>	t_{OR}			12		12	ns
Output fall time	<17>	t_{OF}			12		12	ns



(4) Reset timing

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{RESET}}$ high-level width	<18>	t_{WRSH}		500		500		ns
$\overline{\text{RESET}}$ low-level width	<19>	t_{WRSL}	When power supply is ON and STOP mode has been released	500 + T_{OST}		500 + T_{OST}		ns
			Other than when power supply is ON and STOP mode has been released	500		500		ns

Remark T_{OST}: Oscillation stabilization time



[MEMO]

(5) Read timing (1/2)

	Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
	CLKOUT↑ → address delay time	<20>	t_{DKA}		3	20	3	20	ns
★	CLKOUT↑ → R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$ delay time	<78>	t_{DKA2}		–2	+13	–2	+13	ns
	CLKOUT↑ → address float delay time	<21>	t_{FKA}		3	15	3	15	ns
★	CLKOUT↓ → ASTB delay time	<22>	t_{DKST}		–2	+13	–2	+13	ns
★	CLKOUT↑ → $\overline{DSTB}$ delay time	<23>	t_{DKD}		–2	+13	–2	+13	ns
★	Data input setup time (to CLKOUT↑)	<24>	t_{SIDK}		7		7		ns
	Data input hold time (from CLKOUT↑)	<25>	t_{HKID}		5		5		ns
★	$\overline{WAIT}$ setup time (to CLKOUT↓)	<26>	t_{SWTK}		8		8		ns
	$\overline{WAIT}$ hold time (from CLKOUT↓)	<27>	t_{HKWT}		5		5		ns
	Address hold time (from CLKOUT↑)	<28>	t_{HKA}		0		0		ns
	Address setup time (to ASTB↓)	<29>	t_{SAST}		0.5T – 10		0.5T – 10		ns
	Address hold time (from ASTB↓)	<30>	t_{HSTA}		0.5T – 10		0.5T – 10		ns
	$\overline{DSTB}$↓ → address float delay time	<31>	t_{FDA}			0		0	ns
	Data input setup time (to address)	<32>	t_{SAID}			(2 + n)T – 20		(2 + n)T – 20	ns
	Data input setup time (to $\overline{DSTB}$↓)	<33>	t_{SDID}			(1 + n)T – 20		(1 + n)T – 20	ns
	ASTB↓ → $\overline{DSTB}$↓ delay time	<34>	t_{DSTD}		0.5T – 10		0.5T – 10		ns
	Data input hold time (from $\overline{DSTB}$↑)	<35>	t_{HDID}		0		0		ns
★	$\overline{DSTB}$↑ → address output delay time	<36>	t_{DDA}		(1 + i)T – 3		(1 + i)T – 3		ns
	$\overline{DSTB}$↑ → ASTB↑ delay time	<37>	t_{DDSTH}		0.5T – 10		0.5T – 10		ns
	$\overline{DSTB}$↑ → ASTB↓ delay time	<38>	t_{DDSTL}		(1.5 + i)T – 10		(1.5 + i)T – 10		ns
	$\overline{DSTB}$ low-level width	<39>	t_{WDL}		(1 + n)T – 10		(1 + n)T – 10		ns
	ASTB high-level width	<40>	t_{WSTH}		T – 10		T – 10		ns
	$\overline{WAIT}$ setup time (to address)	<41>	t_{SAWT1}	n ≥ 1		1.5T – 20		1.5T – 20	ns
		<42>	t_{SAWT2}			(1.5 + n)T – 20		(1.5 + n)T – 20	ns
	$\overline{WAIT}$ hold time (from address)	<43>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		(0.5 + n)T		ns
		<44>	t_{HAWT2}		(1.5 + n)T		(1.5 + n)T		ns
	$\overline{WAIT}$ setup time (to ASTB↓)	<45>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
		<46>	t_{SSTWT2}			(1 + n)T – 15		(1 + n)T – 15	ns
	$\overline{WAIT}$ hold time (from ASTB↓)	<47>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
		<48>	t_{HSTWT2}		(1 + n)T		(1 + n)T		ns

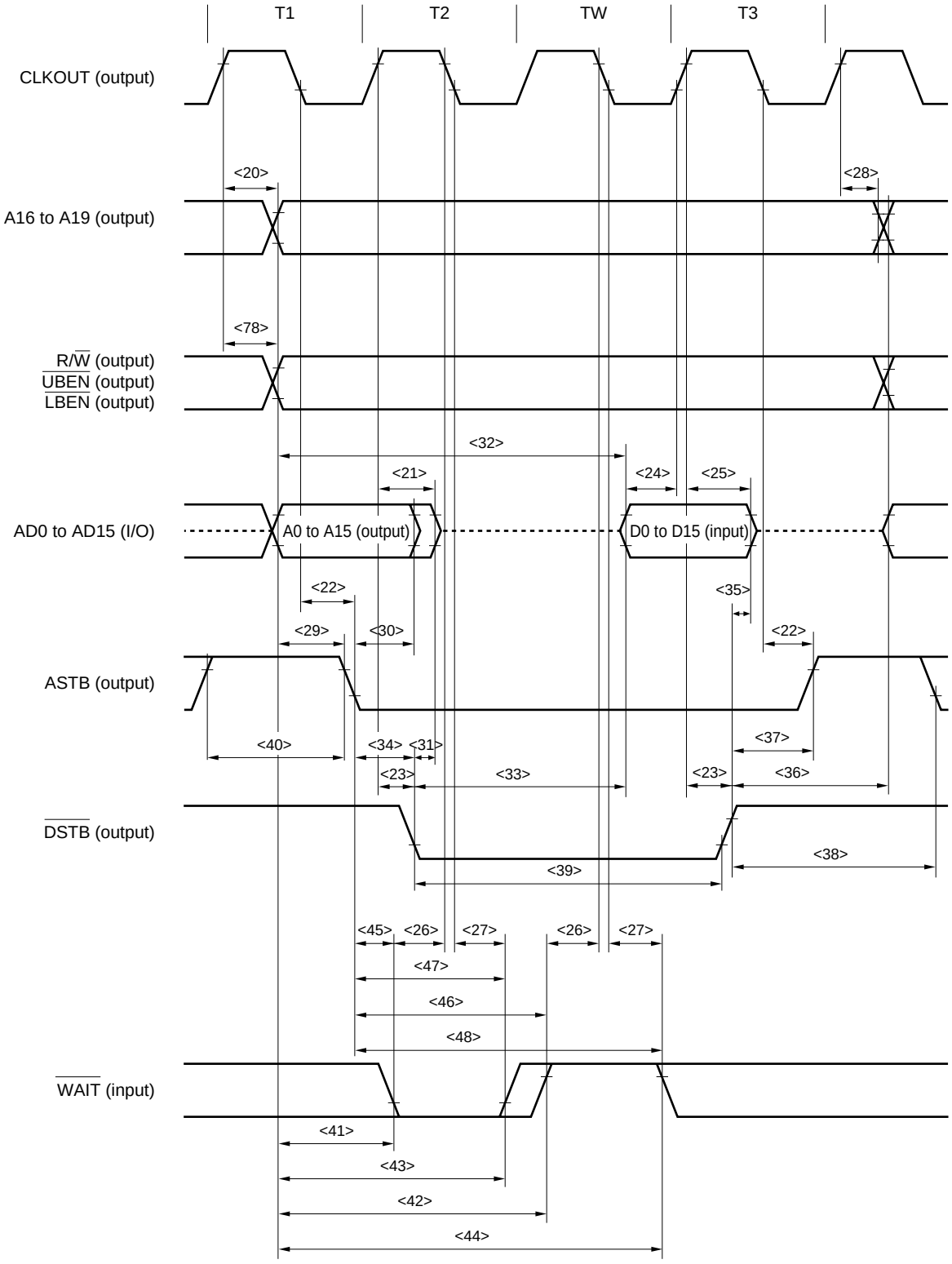
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

3. i indicates the number of idle states (0 or 1) that are inserted after a read cycle.

4. Maintain at least one of the two data input hold times, either t_{HKID} (<25>) or t_{HDID} (<35>).

(5) Read timing (2/2): 1 wait



★

Remark Broken line indicates high impedance.

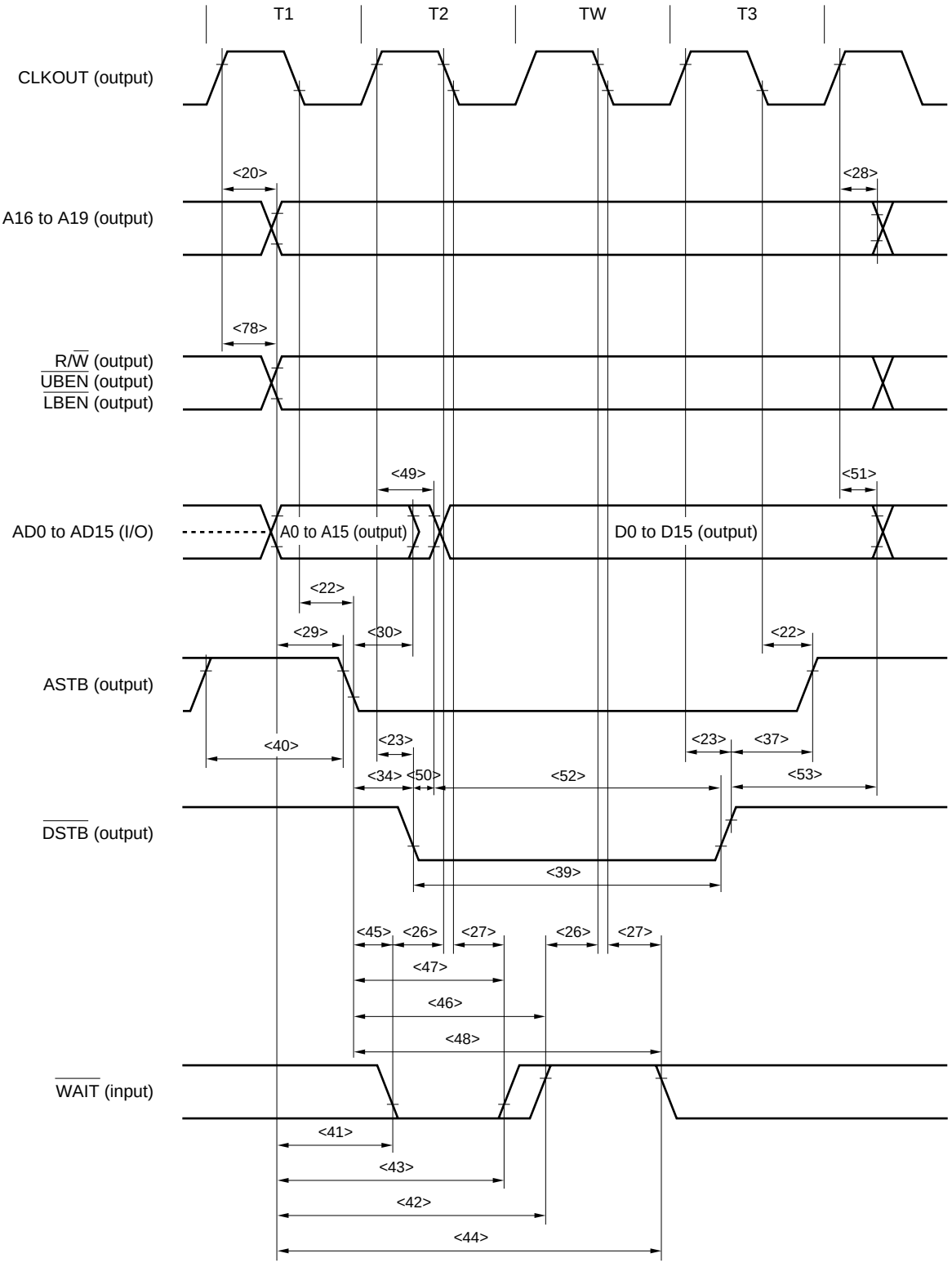
(6) Write timing (1/2)

	Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
	CLKOUT↑ → address delay time	<20>	t_{DKA}		3	20	3	20	ns
★	CLKOUT↑ → R/$\overline{W}$, $\overline{UBEN}$, $\overline{LBEN}$ delay time	<78>	t_{DKA2}		–2	+13	–2	+13	ns
★	CLKOUT↓ → ASTB delay time	<22>	t_{DKST}		–2	+13	–2	+13	ns
★	CLKOUT↑ → $\overline{DSTB}$ delay time	<23>	t_{DKD}		–2	+13	–2	+13	ns
★	$\overline{WAIT}$ setup time (to CLKOUT↓)	<26>	t_{SWTK}		8		8		ns
	$\overline{WAIT}$ hold time (from CLKOUT↓)	<27>	t_{HKWT}		5		5		ns
	Address hold time (from CLKOUT↑)	<28>	t_{HKA}		0		0		ns
	Address setup time (to ASTB↓)	<29>	t_{SAST}		0.5T – 10		0.5T – 10		ns
	Address hold time (from ASTB↓)	<30>	t_{HSTA}		0.5T – 10		0.5T – 10		ns
	ASTB↓ → $\overline{DSTB}$↓ delay time	<34>	t_{DSTD}		0.5T – 10		0.5T – 10		ns
	$\overline{DSTB}$↑ → ASTB↑ delay time	<37>	t_{DDSTH}		0.5T – 10		0.5T – 10		ns
	$\overline{DSTB}$ low-level width	<39>	t_{WDL}		(1 + n)T – 10		(1 + n)T – 10		ns
	$\overline{ASTB}$ high-level width	<40>	t_{WSTH}		T – 10		T – 10		ns
	$\overline{WAIT}$ setup time (to address)	<41>	t_{SAWT1}	n ≥ 1		1.5T – 20		1.5T – 20	ns
		<42>	t_{SAWT2}			(1.5 + n)T – 20		(1.5 + n)T – 20	ns
	$\overline{WAIT}$ hold time (from address)	<43>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		(0.5 + n)T		ns
		<44>	t_{HAWT2}		(1.5 + n)T		(1.5 + n)T		ns
	$\overline{WAIT}$ setup time (to ASTB↓)	<45>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
		<46>	t_{SSTWT2}			(1 + n)T – 15		(1 + n)T – 15	ns
	$\overline{WAIT}$ hold time (from ASTB↓)	<47>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
		<48>	t_{HSTWT2}		(1 + n)T		(1 + n)T		ns
	CLKOUT↑ → data output delay time	<49>	t_{DKOD}			20		20	ns
	$\overline{DSTB}$↓ → data output delay time	<50>	t_{DDOD}			10		10	ns
	Data output hold time (from CLKOUT↑)	<51>	t_{HKOD}		0		0		ns
	Data output setup time (to $\overline{DSTB}$↑)	<52>	t_{SODD}		(1 + n)T – 15		(1 + n)T – 15		ns
	Data output hold time (from $\overline{DSTB}$↑)	<53>	t_{HDOD}		T – 10		T – 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

(6) Write timing (2/2): 1 wait



Remark Broken line indicates high impedance.

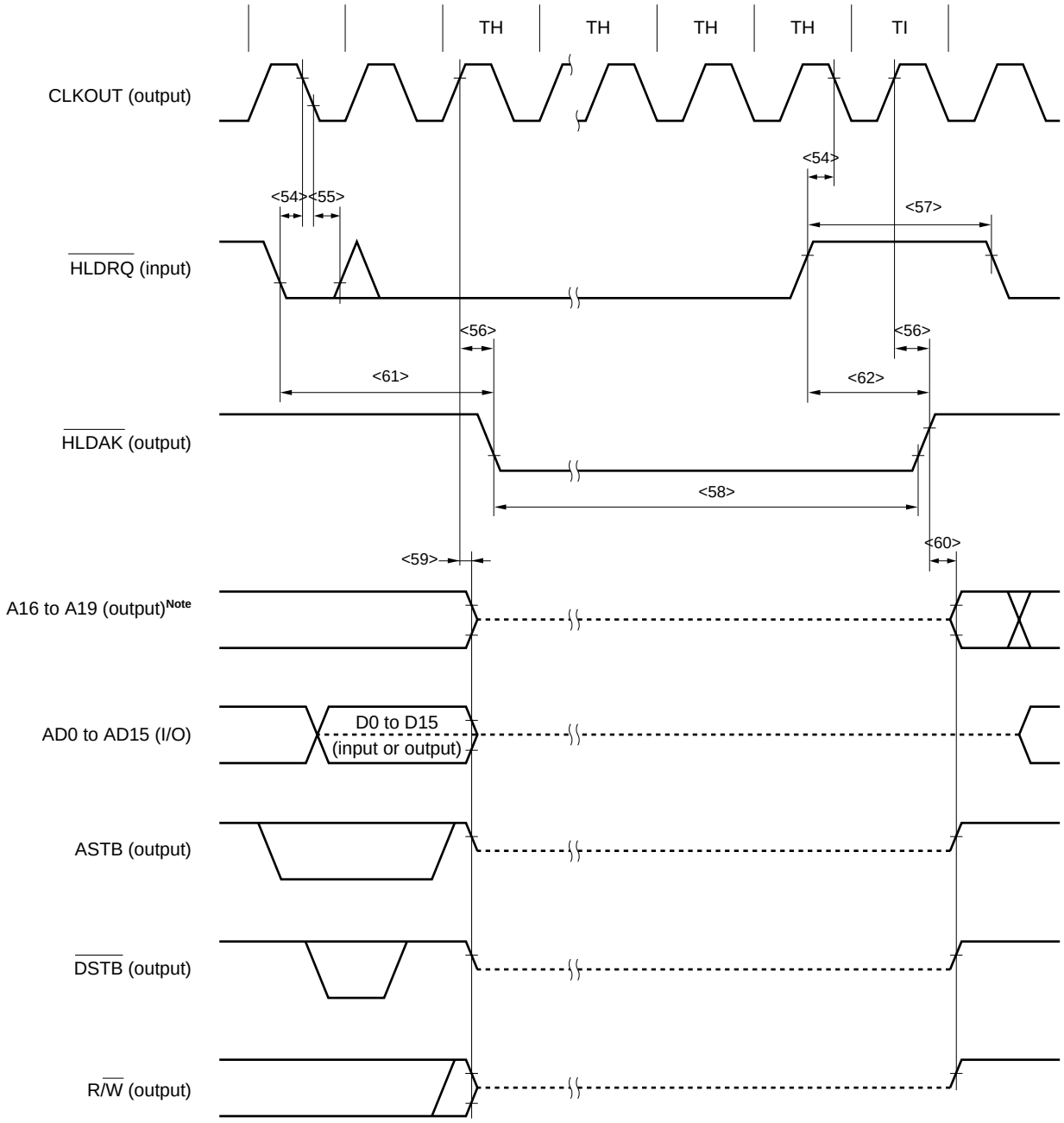
(7) Bus hold timing (1/2)

	Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
★	$\overline{HLDRQ}$ setup time (to CLKOUT↓)	<54>	t_{SHQK}		8		8		ns
	$\overline{HLDRQ}$ hold time (from CLKOUT↓)	<55>	t_{HKHQ}		5		5		ns
	CLKOUT↑ → $\overline{HLDAK}$ delay time	<56>	t_{DKHA}			20		20	ns
	$\overline{HLDRQ}$ high-level width	<57>	t_{WHQH}		T + 10		T + 10		ns
	$\overline{HLDAK}$ low-level width	<58>	t_{WHAL}		T – 10		T – 10		ns
★	CLKOUT↑ → bus float delay time	<59>	t_{DKF}			20		20	ns
	$\overline{HLDAK}$↑ → bus output delay time	<60>	t_{DHAC}		–3		–3		ns
	$\overline{HLDRQ}$↓ → $\overline{HLDAK}$↓ delay time	<61>	t_{DHQHA1}			(2n + 7.5)T + 20		(2n + 7.5)T + 20	ns
	$\overline{HLDRQ}$↑ → $\overline{HLDAK}$↑ delay time	<62>	t_{DHQHA2}		0.5T	1.5T + 20	0.5T	1.5T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

(7) Bus hold timing (2/2)



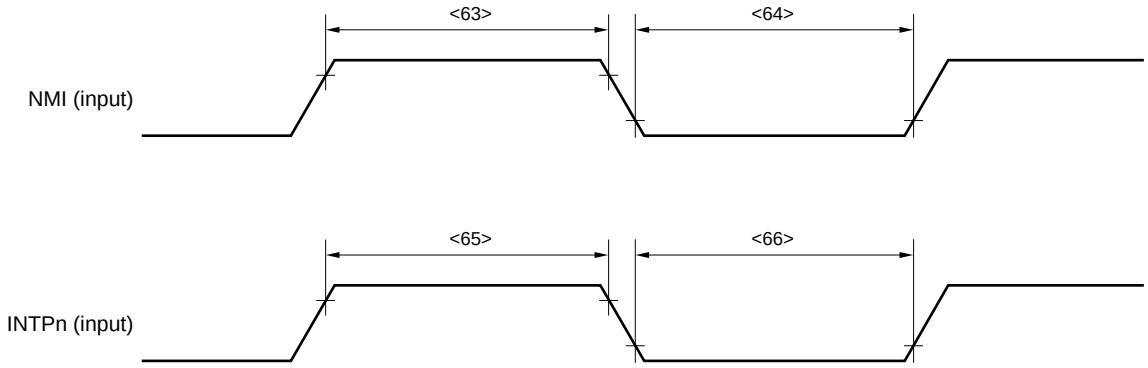
Note UBEN (output), LBEN (output)

Remark Broken line indicates high impedance.

(8) Interrupt timing

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
NMI high-level width	<63>	t_{WNIH}		500		500		ns
NMI low-level width	<64>	t_{WNIL}		500		500		ns
INTPn high-level width	<65>	t_{WITH}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		3T + 10		ns
INTPn low-level width	<66>	t_{WITL}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		3T + 10		ns

Remark T = t_{CYK}



Remark n = 110 to 113, 120 to 123, 130 to 133, 140 to 143

[MEMO]

(9) CSI timing (1/2)

(a) Master mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCKn}$ cycle	<67>	t_{CYSK1}	Output	160		120		ns
$\overline{SCKn}$ high-level width	<68>	t_{WSKH1}	Output	$0.5t_{CYSK1} - 20$		$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<69>	t_{WSKL1}	Output	$0.5t_{CYSK1} - 20$		$0.5t_{CYSK1} - 20$		ns
★ SIn setup time (to $\overline{SCKn}\uparrow$)	<70>	t_{SSISK1}		50		50		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<71>	t_{HSKSI1}		0		0		ns
SOn output delay time (to $\overline{SCKn}\downarrow$)	<72>	t_{DSKSO1}			18		18	ns
SOn output hold time (from $\overline{SCKn}\uparrow$)	<73>	t_{HSKSO1}		$0.5t_{CYSK1} - 5$		$0.5t_{CYSK1} - 5$		ns

Remark n = 0 to 2

★ (ii) Timing of CSI3

Parameter	Symbol		Conditions		25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
$\overline{SCK3}$ cycle	<67>	t_{CYSK3}	Output	R_L = 1.5 kΩ	500		500		ns
$\overline{SCK3}$ high-level width	<68>	t_{WSKH3}	Output	C_L = 50 pF	$0.5t_{CYSK3} - 150$		$0.5t_{CYSK3} - 150$		ns
$\overline{SCK3}$ low-level width	<69>	t_{WSKL3}	Output		$0.5t_{CYSK3} - 70$		$0.5t_{CYSK3} - 70$		ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	<70>	t_{SSISK3}			100		100		ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	<71>	t_{HSKSI3}			50		50		ns
SO3 output delay time (to $\overline{SCK3}\downarrow$)	<72>	t_{DSKSO3}	R_L = 1.5 kΩ			150		150	ns
SO3 output hold time (from $\overline{SCK3}\uparrow$)	<73>	t_{HSKSO3}	C_L = 50 pF		t_{WSKH3}		t_{WSKH3}		ns

Remark R_L and C_L are the load resistance and load capacitance of the output line for $\overline{SCK3}$ and SO3.

(b) Slave mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCKn}$ cycle	<67>	t_{CYSK2}	Input	160		120		ns
$\overline{SCKn}$ high-level width	<68>	t_{WSKH2}	Input	50		30		ns
$\overline{SCKn}$ low-level width	<69>	t_{WSKL2}	Input	50		30		ns
SIn setup time (to $\overline{SCKn}\uparrow$)	<70>	t_{SSISK2}		10		10		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<71>	t_{HSKSI2}		10		10		ns
★ SOn output delay time (to $\overline{SCKn}\downarrow$)	<72>	t_{DSKSO2}			45		45	ns
SOn output hold time (from $\overline{SCKn}\uparrow$)	<73>	t_{HSKSO2}		t_{WSKH2}		t_{WSKH2}		ns

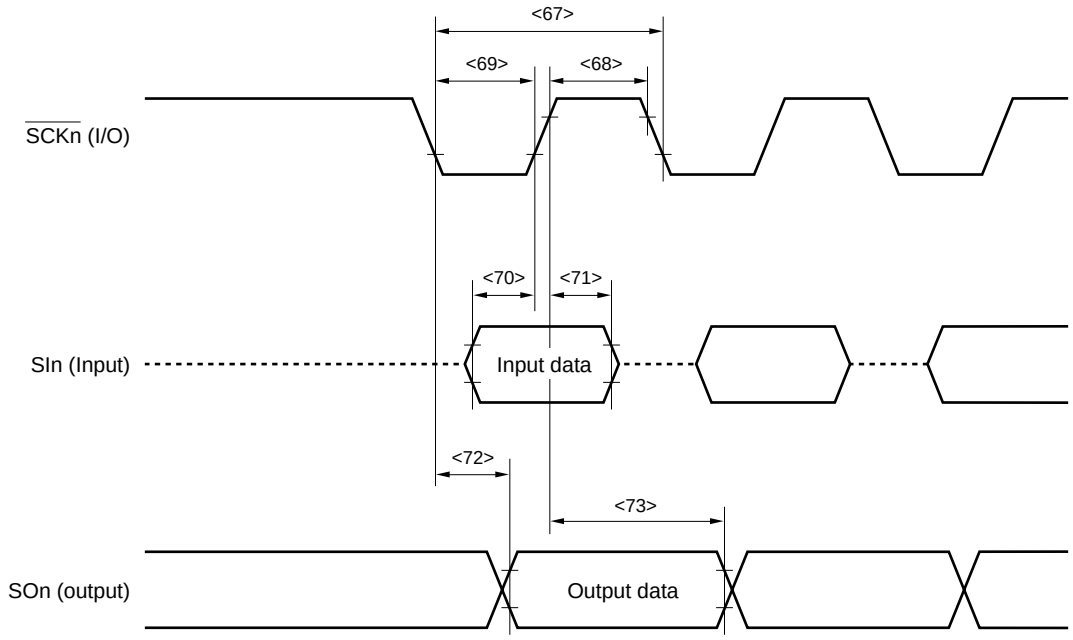
Remark n = 0 to 2

(9) CSI timing (2/2)

(ii) Timing of CSI3

	Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
					MIN.	MAX.	MIN.	MAX.	
	$\overline{SCK3}$ cycle	<67>	t_{CYSK4}	Input	500		500		ns
★	$\overline{SCK3}$ high-level width	<68>	t_{WSKH4}	Input	100		100		ns
	$\overline{SCK3}$ low-level width	<69>	t_{WSKL4}	Input	180		180		ns
	SI3 setup time (to $\overline{SCK3}$↑)	<70>	t_{SSISK4}		100		100		ns
	SI3 hold time (from $\overline{SCK3}$↑)	<71>	t_{HSKSI4}		50		50		ns
★	SO3 output delay time (to $\overline{SCK3}$↓)	<72>	t_{DSKSO4}	R_L = 1.5 kΩ		150		150	ns
	SO3 output hold time (from $\overline{SCK3}$↑)	<73>	t_{HSKSO4}	C_L = 50 pF	t_{WSKH4}		t_{WSKH4}		ns

Remark R_L is the load resistance and C_L is the load capacitance of the output line for $\overline{SCK3}$ and SO3.



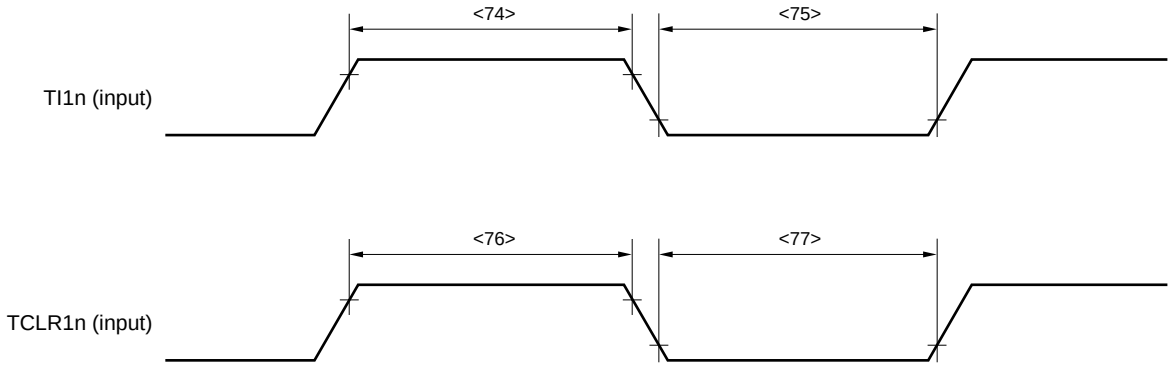
Remarks 1. Broken line indicates high impedance.

2. n = 0 to 3

(10) RPU timing

Parameter	Symbol		Conditions	25-MHz Version		33-MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
TI1n high-level width	<74>	t_{WTIH}		3T + 10		3T + 10		ns
TI1n low-level width	<75>	t_{WTIL}		3T + 10		3T + 10		ns
TCLR1n high-level width	<76>	t_{WTCH}		3T + 10		3T + 10		ns
TCLR1n low-level width	<77>	t_{WTCL}		3T + 10		3T + 10		ns

Remark T = t_{CYK}



Remark n = 1 to 4

★ **A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)**

Parameter	Symbol	Conditions	25-MHz Version			33-MHz Version			Units
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution	—		10			10			bit
Total error[Note 1]	—	4.5 V ≤ AV_{REF1} ≤ AV_{DD}			±0.55			±0.55	%FSR
	—	3.5 V ≤ AV_{REF1} ≤ AV_{DD}			±0.7			±0.7	%FSR
Quantization error	—				±1/2			±1/2	LSB
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF1} ≤ AV_{DD}	48			60			t_{CYK}
		3.5 V ≤ AV_{REF1} ≤ AV_{DD}	48			60			t_{CYK}
Sampling time	t_{SAMP}	4.5 V ≤ AV_{REF1} ≤ AV_{DD}	8			10			t_{CYK}
		3.5 V ≤ AV_{REF1} ≤ AV_{DD}	8			10			t_{CYK}
Zero scale error[Note 1]	—	4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±3.0	±4.5		±3.0	±4.5	LSB
	—	3.5 V ≤ AV_{REF1} ≤ AV_{DD}		±3.0	±5.5		±3.0	±5.5	LSB
Full scale error[Note 1]	—	4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±2.5		±1.5	±2.5	LSB
	—	3.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Nonlinearity error[Note 1]	—	4.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±3.5		±1.5	±3.5	LSB
	—	3.5 V ≤ AV_{REF1} ≤ AV_{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Analog input voltage[Note 2]	V_{IAN}		–0.3		AV_{DD} +0.3	–0.3		AV_{DD} +0.3	V
Reference voltage	AV_{REF1}		3.5		AV_{DD}	3.5		AV_{DD}	V
AV_{REF1} current	AI_{REF1}			1.2	3.0		1.2	3.0	mA
AV_{DD} power supply current	AI_{DD}			2.3	6.0		2.3	6.0	mA

Notes 1. Does not include quantization error.

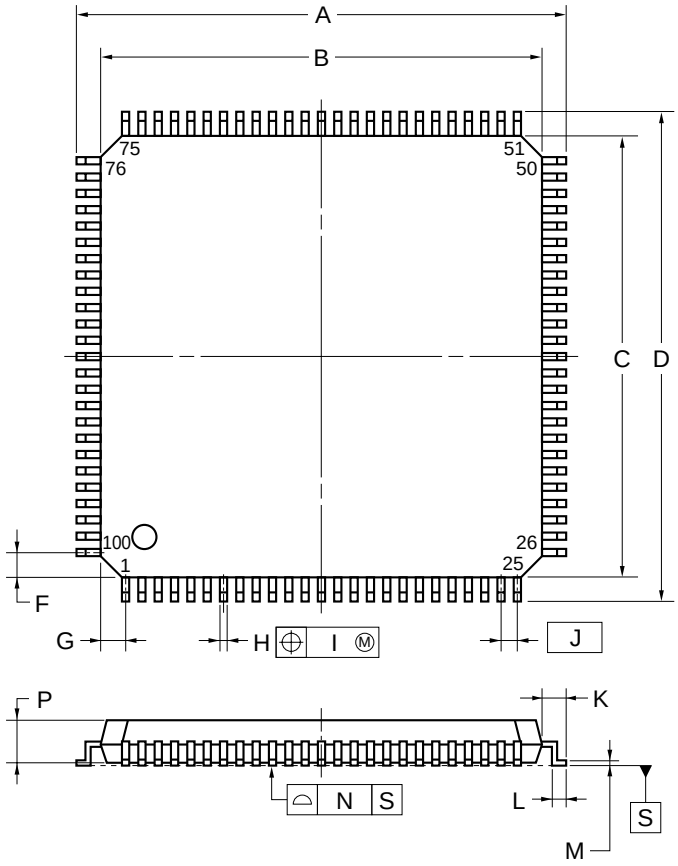
2. When V_{IAN} = 0, the conversion result becomes 000H.
When 0 < V_{IAN} < AV_{REF1}, conversion has 10-bit resolution.
When AV_{REF1} ≤ V_{IAN} ≤ AV_{DD}, the conversion result becomes 3FFH.

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

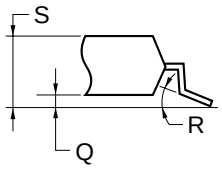
	Parameter	Symbol	Conditions	25-MHz Version			33-MHz Version			Units
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	Resolution	—				8			8	bit
	Total error	—	Load condition: 2 MΩ, 30 pF AV_{REF2} = V_{DD} AV_{REF3} = 0			0.8			0.8	%
		—	Load condition: 2 MΩ, 30 pF AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			1.0			1.0	%
		—	Load condition: 4 MΩ, 30 pF AV_{REF2} = V_{DD} AV_{REF3} = 0			0.6			0.6	%
		—	Load condition: 4 MΩ, 30 pF AV_{REF2} = 0.75 V_{DD} AV_{REF3} = 0.25 V_{DD}			0.8			0.8	%
	Settling time	—	Load condition: 2 MΩ, 30 pF			10			10	μs
	Output resistance	RO			10			10		kΩ
	AV_{REF2} input voltage	AV_{REF2}		0.75 V_{DD}		V_{DD}	0.75 V_{DD}		V_{DD}	V
	AV_{REF3} input voltage	AV_{REF3}		0		0.25 V_{DD}	0		0.25 V_{DD}	V
★	AV_{REF2} to AV_{REF3} resistance value	R_{AIREF}	DACS0, DACS1 = 55H	2	5		2	5		kΩ

★ 17. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



detail of lead end



NOTE

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45±0.05	$0.057^{+0.003}_{-0.002}$
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-3

★ 18. RECOMMENDED SOLDERING CONDITIONS

The μPD703003 should be soldered and mounted under the following recommended conditions.

For the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 18-1. Soldering Conditions

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (after that, prebaking is necessary at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device)	—

Note Exposure limit after dry-pack is opened. Storage conditions: temperature of 25°C and relative humidity of 65% or less.

Caution Do not use different soldering methods together (except for partial heating).

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Fax: 02-66 75 42 99

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Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

RELATED DOCUMENTS **μPD703003A, 703004A, 703025A Data Sheet (Under preparation)**
μPD70F3003 Data Sheet (U12036E)
μPD70F3003A, 70F3025A Data Sheet (U13189E)
V850 Family, Instruction Table (U10229J)[Note]

Note Japanese version

The related documents indicated in this publication may include preliminary version. However, preliminary versions are not marked as such.

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