NEC Electronics Inc.

μPD72002
Serial Communications Controller: Single-Channel, Advanced Multiprotocol, CMOS

June 1991

Description

The μPD72002 Serial Communications Controller is an advanced multiprotocol serial controller (AMPSC). The high-performance μPD72002 is a software-compatible, single-channel version of NEC's powerful μPD72001 AMPSC. Both the μPD72002 and the μPD72001 have a superset of the functions of the 8530 SCC.

The μPD72002 AMPSC contains a single full-duplex serial channel that can be configured to transmit and receive data in either asynchronous protocol or one of two synchronous protocols.

- Character-oriented protocol (COP), such as binary synchronous control (Bisync) and Monosync.
- Bit-oriented protocol (BOP), such as high-level data link control (HDLC) and synchronous data link control (SDLC).

The μPD72002 AMPSC, like its forerunner the μPD72001, provides vectored and non-vectored interrupt operation. Vectored operation allows multiple AMPSCs (both μPD72001s and μPD72002s) to be connected in an interrupt daisy chain configuration.

Separate direct memory access (DMA) request and acknowledge lines, available for both transmitter and receiver, provide a direct interface to the μPD71071 and 8237 DMA controllers, allowing for high-speed operation. The AMPSC is easily interfaced to most microprocessors with a minimum of additional logic.

Features that make the μPD72001 the right choice for today's advanced communications requirements are also present in the μPD72002. An on-chip digital phase-locked loop (DPLL) and two baud rate generator (BRG)/timers are available, one BRG for the transmitter and one for the receiver. The BRGs provide the flexibility of operation with asymmetrical data rates on the serial channel.

A crystal oscillator and a low-power standby mode of operation are also included. The standby mode reduces power consumption dramatically, preserving all register values while disabling the transmitter and receiver. The μPD72002's features simplify design requirements and make it an excellent choice for applications that require only one serial communications channel.

Features

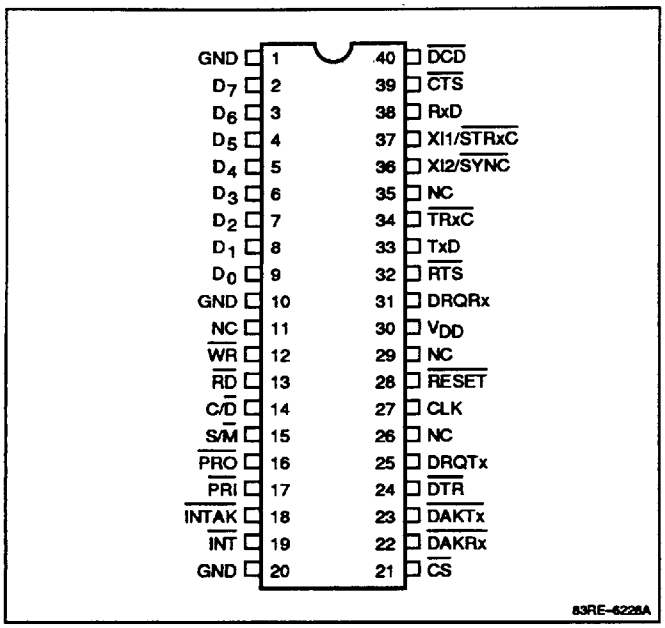
- Single-channel version of μPD72001
- Software compatible with μPD72001
- Functional superset of industry standard 8530
- CMOS technology
- Multiprotocol
  - —Asynchronous
  - —Synchronous
  - —Character-oriented (Bisync and Monosync)
  - —Bit-oriented (SDLC/HDLC)
- One full-duplex channel
- Versatile host-system interface
  - —Software polling
  - —Interrupt
  - —DMA
- Direct interface to μPD71071 and 8237 DMA controllers
- Interface to a majority of microprocessors (V-Series, 8080, 8085, 80x86/80x88, and others)
- Dc to 2.2-Mb/s data rate
- Modem control signals
- NRZ, NRZI, and FM encoding/decoding, Manchester decoding
- Digital phase-locked loop
- Two baud rate generator/timers (receive and transmit)
- Crystal oscillator
- SDLC loop mode
- Mark idle detection
- Short-frame detection
- Single + 5-volt power supply
- Standby mode for reduced power consumption
- 11-MHz, 12-MHz, or 12.5-MHz system and input data clocks
- Available in DIP, PLCC, and QFP packages

Ordering Information

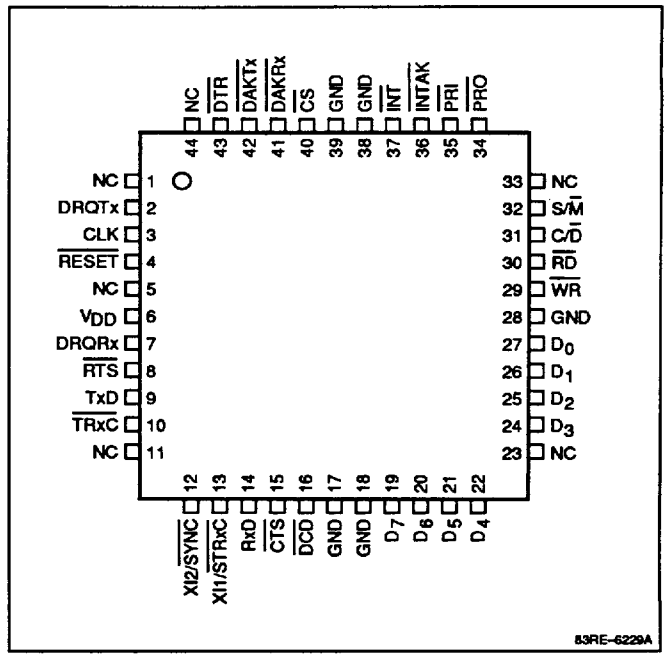
Part Number	Package	Max Clock Speed
μPD72002C	40-pin plastic DIP	12.5 MHz
μPD72002GB	44-pin plastic QFP	
μPD72002L	44-pin PLCC	

Pin Configurations

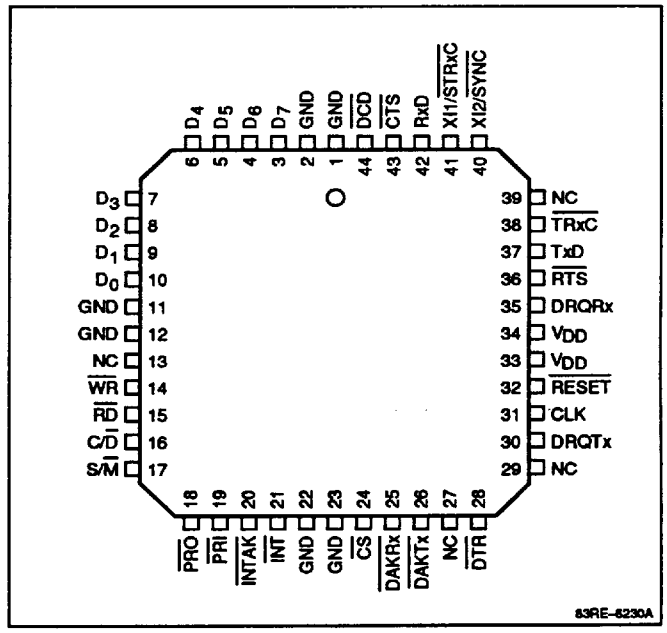
40-Pin Plastic DIP



44-Pin Plastic QFP



44-Pin Plastic Leaded Chip Carrier (PLCC)



Pin Identification

Symbol	I/O	Signal Function
C/$\overline{D}$	In	Control/data select from host computer
CLK	In	System clock from host computer
$\overline{CS}$	In	Chip select
$\overline{CTS}$	In	Clear-to-send
D_0-D_7	I/O	System data bus
$\overline{DAKR}$x	In	Receive DMA acknowledge
$\overline{DAKT}$x	In	Transmit DMA acknowledge
$\overline{DCD}$	In	Data carrier detect
DRQRx	Out	Receive DMA request
DRQTx	Out	Transmit DMA request
$\overline{DTR}$	Out	Data terminal ready
$\overline{INT}$	Out	Interrupt request to host computer
$\overline{INTAK}$	In	Interrupt acknowledge from host computer
$\overline{PRI}$	In	Priority interrupt daisy chain control
$\overline{PRO}$	Out	Priority interrupt daisy chain control
$\overline{RD}$	In	Read control from host computer
$\overline{RESET}$	In	System reset from host computer
$\overline{RTS}$	Out	Request-to-send
RxD	In	Receive data
S/$\overline{M}$	In	Secondary or main register select
$\overline{TRxC}$	I/O	Transmit-receive clock
TxD	Out	Transmit data
$\overline{WR}$	In	Write control from host computer
XI1/$\overline{STRxC}$	In	External crystal connection or transmit-receive clock source
XI2/$\overline{SYNC}$	I/O	External crystal connection or synchronization signal
NC		No connection
GND		System ground
V_{DD}		+5 V (typical)

PIN FUNCTIONS

CPU Interface

C/$\overline{D}$ (Control/Data Select). The input to this pin selects the type of data on the data bus during a write or read access. A low input selects data; a high input selects a control or status register.

CLK (System Clock). This input supplies the clock for the internal operation of the device. It is separate from the data clocks. The system clock input must be more than five times the serial data transfer rate.

$\overline{CS}$ (Chip Select). An active-low input signal at this pin selects the AMPSC for a read or write operation.

D_0-D_7 (Data Bus). These pins constitute a three-state, 8-bit, bidirectional data bus. The bus is connected to the host processor's data bus to transfer control words, status information, and send/receive data.

$\overline{INT}$ (Interrupt). The interrupt request output signal at this pin goes low if an interrupt source occurs within the AMPSC. The output is an open-drain transistor and requires a pull-up resistor.

$\overline{INTAK}$ (Interrupt Acknowledge). An active-low input signal at this pin is used in response to an interrupt request. In the vectored mode (CR2M bit D7 = 1), it causes the interrupt vector to be placed on the data bus. The output vector mode determines the number of cycles of $\overline{INTAK}$ toggling required for each interrupt acknowledge cycle (see CR2M bits D3-D5). In the nonvectored mode (D7 = 0), this pin must be pulled high. If unused, this pin must be pulled high also.

$\overline{PRI}$ (Priority Input). The $\overline{PRI}$ signal controls interrupt request generation and interrupt vector output. This pin is the input for the interrupt priority daisy chain that determines how interrupts from multiple devices are resolved. A high level prevents the AMPSC from presenting an interrupt vector during the INTAK sequence. A low level allows the vector to be presented. If unused, this pin must be tied low.

$\overline{PRO}$ (Priority Output). This is an output to the interrupt priority daisy chain. It controls interrupt requests from lower-priority devices. It indicates the existence of a higher-priority interrupt, either within the AMPSC or, if no internal interrupt exists, the condition of the $\overline{PRI}$ input.

$\overline{RD}$ (Read). The active-low $\overline{RD}$ input signal in conjunction with $\overline{CS}$ causes status or receive (Rx) data to be read out of the AMPSC. The data is presented on pins D_0-D_7. The values are dependent on the state of the S/$\overline{M}$ and C/$\overline{D}$ inputs and the internal state of the device.

$\overline{RESET}$ (Reset). Applying a low signal continuously for two or more clock cycles (t_{CYK}) to this pin resets the AMPSC (system reset) and places it in standby mode. A system reset disables the transmitter, receiver, interrupt, and DMA functions and sets the TxD and general-purpose output pins to high. It also resets all bits of the control registers.

S/$\overline{M}$ (Secondary/Main Select). The input to this pin selects either the main or secondary registers during a read or write operation. A low selects the main registers; a high selects the secondary registers.

$\overline{WR}$ (Write). The active-low $\overline{WR}$ input signal in conjunction with $\overline{CS}$ causes control words or transmit (Tx) data to be written into the AMPSC. The data written is input on D_0-D_7. The destination of the data is determined by the state of the S/$\overline{M}$ and C/$\overline{D}$ pins and the value of the internal register pointer.

Channel Interface

$\overline{DAKRx}$ (Receive DMA Acknowledge). This active-low input is a DMA acknowledge from the DMA controller. The pin is set low by the DMA controller in response to a receive DMA request from the AMPSC to indicate that DMA service has been granted to the AMPSC. This signal replaces the $\overline{CS}$ signal for DMA transfers

$\overline{DAKTx}$ (Transmit DMA Acknowledge). This active-low input is a DMA acknowledge from the DMA controller. The pin is set low by the DMA controller in response to a transmit DMA request from the AMPSC to indicate that DMA service has been granted to the AMPSC. This signal replaces the $\overline{CS}$ signal for DMA transfers.

DRQRx (Receive DMA Request). This active-high output is a DMA request to the DMA controller. The pin is set to high when the receiver enters the Rx Character Available state. It is reset when received data is read out of the channel.

DRQTx (Transmit DMA Request). This active-high output is a DMA request to the DMA controller. The pin is set to high when the Tx buffer is emptied. The conditions under which this occurs depend on the status of control register CR1 bit D2.

RxD (Receive Data). Receive data enters the AMPSC on this pin.

$\overline{STRxC}$ (Clock Source). This pin is the transmit or receive clock source input. It can be routed internally to the transmitter, receiver, the BRGs, or the DPLL. An alternative function as an external crystal connection point (XI1) is selected by CR15 bit D7.

$\overline{TRxC}$ (Transmit/Receive Clock). If bit D2 of CR15 is 0, this pin is a transmit or receive clock input. Also, it is an input if bits D5 and D6 or D3 and D4 of CR15 are set 1 and 0, respectively, overriding the state of bit D2.

If none of the conditions above are true, the pin functions as an output for either the crystal oscillator, the BRG, the DPLL, or the transmit clock. The clock source is selected by bits D0 and D1 of CR15.

TxD (Transmit Data). Transmit data exits the AMPSC on this pin.

XI1, XI2 (Crystal Connections). This pin pair may be connected to an external crystal that controls the internal oscillator.

Modem Control

$\overline{CTS}$ (Clear to Send). This is a general-purpose input usable, as an example, for modem control. A status change on $\overline{CTS}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{CTS}$ can be used with the Tx Enable bit (CR5 bit D3) to control transmitter operation.

$\overline{DCD}$ (Data Carrier Detect). This is a general-purpose input usable, as an example, for modem control. A status change on $\overline{DCD}$ affects E/S bit latch operation. If E/S INT is enabled (CR1 bit D0 set to 1), an E/S interrupt occurs. If the Auto Enable mode is selected (CR3 bit D5 set to 1), $\overline{DCD}$ can be used with the Rx Enable bit (CR3 bit D0) to control receiver operation.

$\overline{DTR}$ (Data Terminal Ready). This is a general-purpose active-low output controlled by CR5 bit D7.

$\overline{RTS}$ (Request to Send). This is a general-purpose output usable, as an example, for modem control. Pin status is set by CR5 bit D1 and Auto Enable bit status (CR3 bit D5).

$\overline{SYNC}$ (Sync Input or Output). In accordance with the settings of CR4 bits D7-D2, and with CR15 bit D7 = 0, the three functions of this pin are as follows.

(1) Asynchronous mode: general-purpose input that functions like $\overline{DCD}$ and $\overline{CTS}$.

(2) External sync mode: active-low input indicates to the AMPSC that synchronization has occurred.

(3) Internal sync mode: active low output indicates when synchronization is detected by the AMPSC.

An alternative function as an external crystal connection point (XI2) is selected by CR15 bit D7.

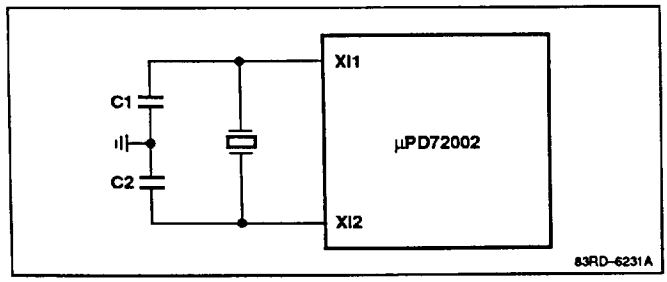
OSCILLATOR CRYSTAL

The crystal used with the μPD72002 internal crystal oscillator should be parallel resonant, fundamental mode, with an AT cut. For frequency stability, two capacitors can be added from the pins of the crystal to ground (figure 1). The value of the capacitors can be calculated by the following formula.

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

C_L is the load capacitance of the crystal and C_S is all stray capacitance in parallel with the crystal. The C_S value should include the input capacitance (C_{IO} and C_{IN}) of the μPD72002 and any wiring or socket capacitance.

Figure 1. Crystal Configuration Circuit



ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD} + 0.5 V
Output voltage, V_O	−0.5 to V_{DD} + 0.5 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Capacitance

T_A = +25°C; V_{DD} = 0 V; f_C = 1 MHz

Parameter	Symbol	Typ	Max	Unit	Conditions
Input capacitance	C_{IN}		10	pF	Unmeasured pins returned to 0 V
I/O capacitance	C_{IO}		20	pF	

DC Characteristics

T_A = −10 to +70°C; V_{DD} = +5 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input low voltage	V_{IL}	−0.5		+0.8	V	All pins except CLK
	V_{ILC}	−0.5		+0.6	V	CLK pins
Input high voltage	V_{IH}	+2.2		V_{DD} + 0.5	V	All pins except CLK
	V_{IHC}	+3.3		V_{DD} + 0.5	V	CLK pin
Output low voltage	V_{OL}			+0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	0.7 V_{DD}			V	I_{OH} = −400 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OUT} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OUT} = 0 V
Input leakage current, high	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IN} = 0 V
V_{DD} supply current	I_{DD}		20	40	mA	All outputs at high level; t_{CY} = 90 ns
Standby current	I_{DDI}		1	20	μA	f_{RxC} = f_{TxC} = f_{CLK} = DC
				1	mA	Standby mode

AC Characteristics

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	11 MHz Min	11 MHz Max	12 and 12.5 MHz Min	12 and 12.5 MHz Max	Unit	Conditions
Clock							
Clock cycle (Note 1)	t_{CYK}	90	2000	83 (12 MHz) 80 (12.5 MHz)	2000	ns	
Clock high-level width	t_{WKH}	40	1000	35	1000	ns	
Clock low-level width	t_{WKL}	40	1000	35	1000	ns	
Clock rise time, 1.5 to 3.0 V	t_{KR}		10		10	ns	
Clock fall time, 3.0 to 1.5 V	t_{KF}		10		10	ns	
Read Cycle							
Address setup time to $\overline{RD}$ ↓	t_{SAR}	0		0		ns	
Address hold time from $\overline{RD}$ ↑	t_{HRA}	0		0		ns	
$\overline{RD}$ pulse width	t_{WRL}	120		105		ns	
Data output delay time from address	t_{DAD}		100		100	ns	
Data output delay time from $\overline{RD}$ ↓	t_{DRD}		100		95	ns	
Data float delay time from $\overline{RD}$ ↑	t_{FRD}	10	40	10	40	ns	
Write Cycle							
Address setup time to $\overline{WR}$ ↓	t_{SAW}	0		0		ns	
Address hold time from $\overline{WR}$ ↑	t_{HWA}	0		0		ns	
$\overline{WR}$ pulse width	t_{WWL}	120		85		ns	
Data setup time to $\overline{WR}$ ↑	t_{SDW}	100		75		ns	
Data hold time from $\overline{WR}$ ↑	t_{HWD}	0		0		ns	
Read/Write Cycle							
$\overline{RD}$/$\overline{WR}$ recovery time (Note 2)	t_{RV}	140		125		ns	
Transmit or Receive Cycle							
Transmit/receive data cycle	t_{CYD}	5		5		t_{CYK}	
$\overline{STRxC}$, $\overline{TRxC}$ input clock cycle	t_{CYC}	90		83 (12 MHz), 80 (12.5 MHz)		ns	
$\overline{STRxC}$, $\overline{TRxC}$ input clock pulse							
High-level width	t_{WCH}	40		35		ns	
Low-level width	t_{WCL}	40		40		ns	
Transmit Cycle							
TxD delay time from $\overline{STRxC}$ ↓, $\overline{TRxC}$ ↓							
x1 mode	t_{DTCTD1}		100		90	ns	
x16, x32, x64 mode	t_{DTCTD2}		300		150	ns	
$\overline{INT}$ delay time from TxD	t_{DTDIQ}	4	6	4	6	t_{CYK}	Tx INT mode
DRQTx delay time from TxD	t_{DTDDQ}	4	6	4	6	t_{CYK}	Tx DMA mode
Receive Cycle							
RxD setup time to $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{SRDRC}	0		0		ns	
RxD hold time from $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{HRCRD}	120		90		ns	
INT delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCIQ}	7	11	7	11	t_{CYK}	Rx INT mode
DRQRx delay time from $\overline{RxC}$ ↑ (Note 3)	t_{DRCDQ}	7	11	7	11	t_{CYK}	Rx DMA mode

AC Characteristics (cont)

Parameter	Symbol	11 MHz Min	11 MHz Max	12 and 12.5 MHz Min	12 and 12.5 MHz Max	Unit	Conditions
DMA Request/Acknowledge Control							
DRQRx ↓ request delay time from $\overline{RD}$ ↓	t_{DRDQ}		120		100	ns	
DRQTx ↓ request delay time from $\overline{WR}$ ↓	t_{DWDQ}		120		100	ns	
$\overline{DAKRx}$ setup time to $\overline{RD}$ ↓	t_{DDAR}	0		0		ns	
$\overline{DAKTx}$ setup time to $\overline{WR}$ ↓	t_{DDAW}	0		0		ns	
$\overline{DAKRx}$ hold time from $\overline{RD}$ ↑	t_{DRDA}	0		0		ns	
$\overline{DAKTx}$ hold time from $\overline{WR}$ ↑	t_{DWDA}	0		0		ns	
Interrupt Control							
$\overline{INTAK}$ low-level width	t_{WIAL}	120		75		ns	
$\overline{PRO}$ delay time from $\overline{PRI}$	t_{DPIPO}		50		30	ns	
$\overline{PRI}$ setup time to $\overline{INTAK}$ ↓	t_{SPIIA}	0		0		ns	When vector output is selected
$\overline{PRI}$ hold time from $\overline{INTAK}$ ↑	t_{HIAPI}	20		10		ns	
Data output delay time from $\overline{INTAK}$ ↓	t_{DIAD}		120		80	ns	
Data float delay time from $\overline{INTAK}$ ↑	t_{FIAD}	10	40	10	40	ns	
Modem Control							
$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ pulse							
High-level width	t_{WMH}	2		2		t_{CYK}	
Low-level width	t_{WML}	2		2		t_{CYK}	
$\overline{INT}$ delay time from $\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$	t_{DMIQ}		2		2	t_{CYK}	
Sync Control							
$\overline{SYNC}$ delay time from $\overline{STRxC}$ ↑, $\overline{TRxC}$ ↑	t_{DTRCSY}	0	2	0	2	t_{CYK}	COP external synchronization
Crystal Oscillator							
XI1 input cycle time	t_{CYX}	90	2000	83 (12 MHz), 80 (12.5 MHz)	2000	ns	
Reset							
$\overline{RESET}$ pulse width	t_{WRSL}	2		2		t_{CYK}	

Notes:

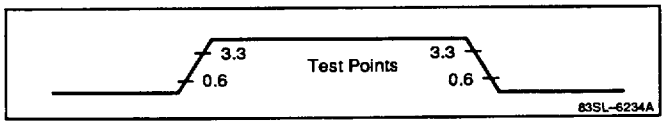
(1) In all modes, the system clock frequency must be more than five times the maximum data rate.

(2) For all operations except Tx/Rx data transfer.

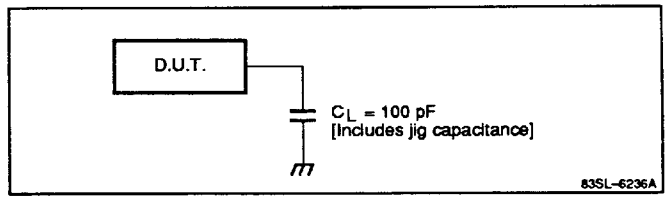
(3) $\overline{RxC}$ = $\overline{STRxC}$ or $\overline{TRxC}$.

Timing Waveforms

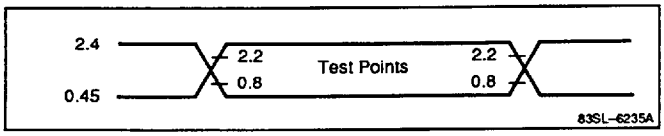
Clock Input Test Points



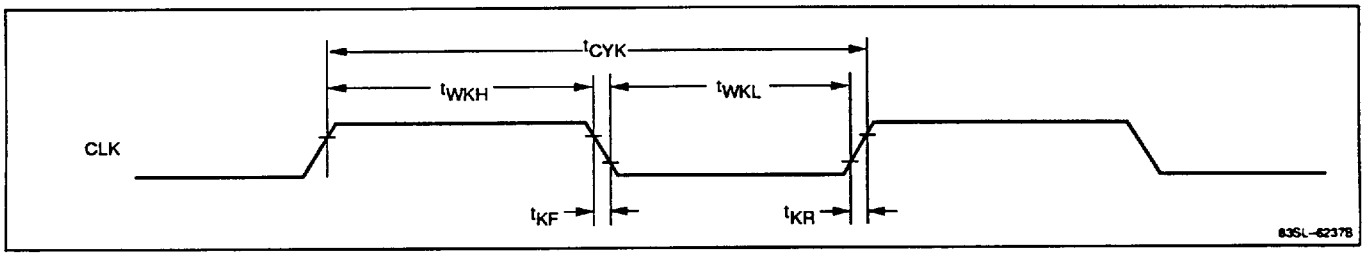
AC Test Load Circuit



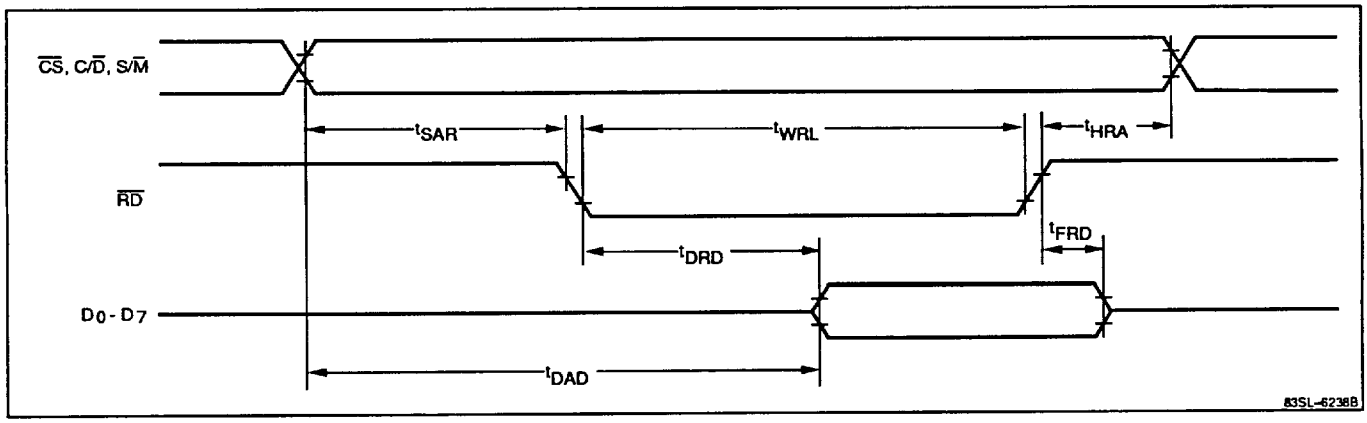
I/O Waveform Test Points



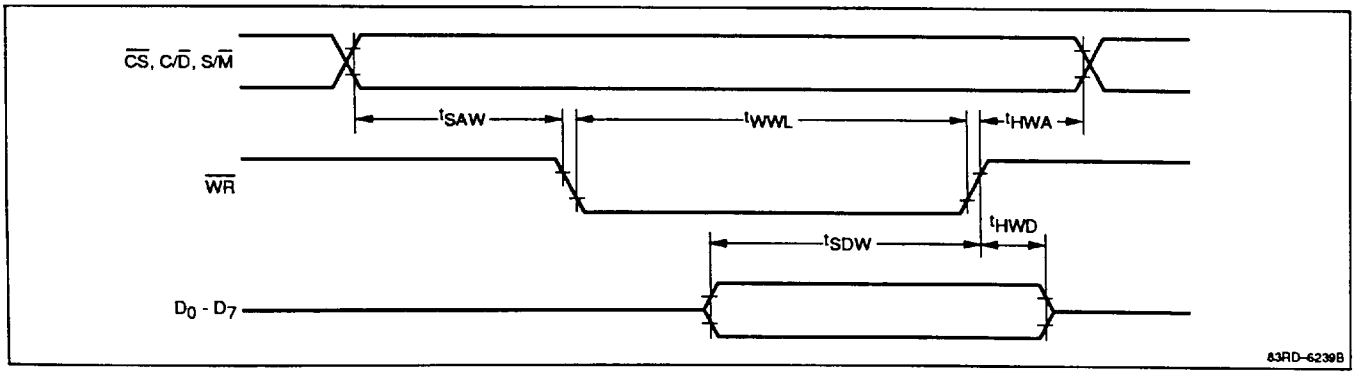
Clock Timing



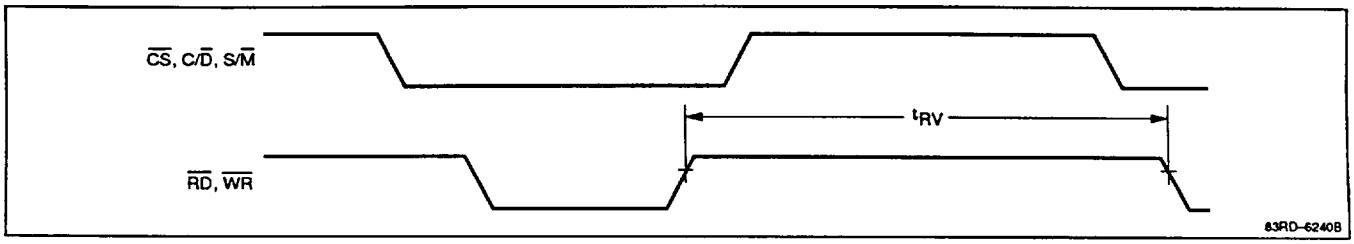
Read Cycle



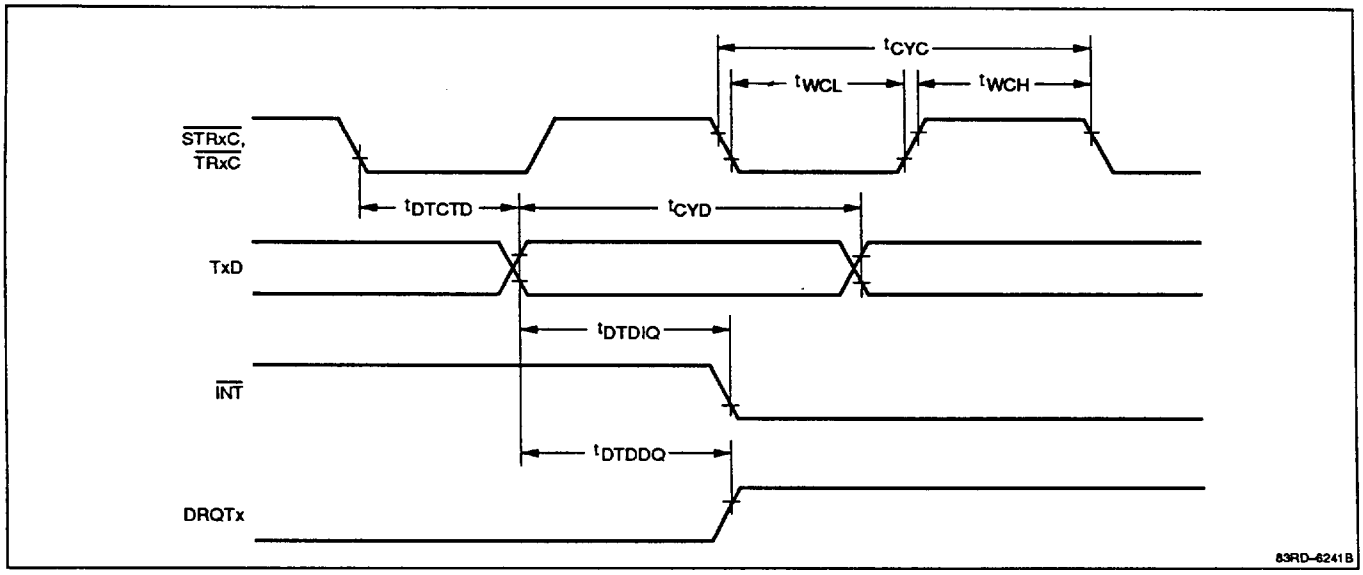
Write Cycle



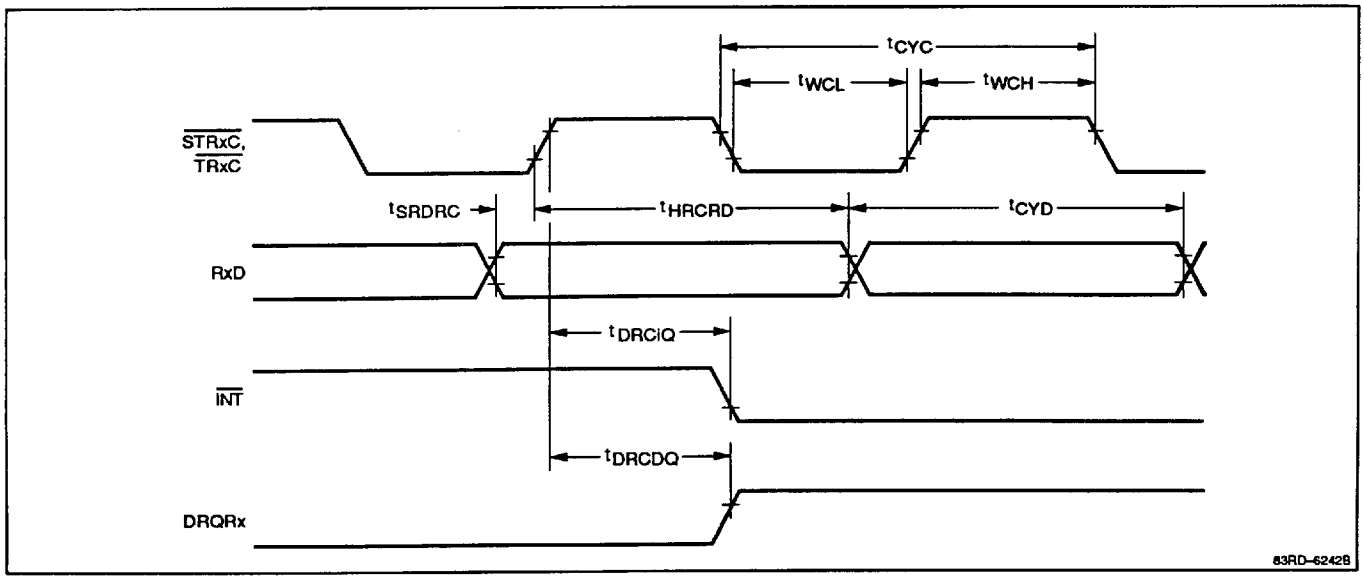
Read/Write Cycle (for all operations except Tx/Rx data transfer)



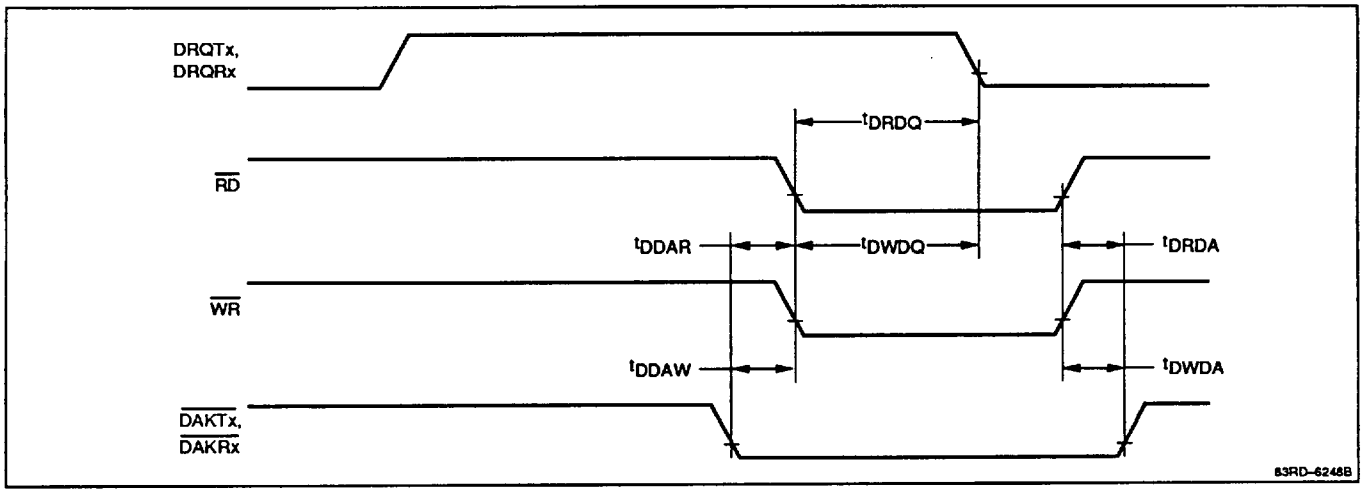
Transmit Cycle



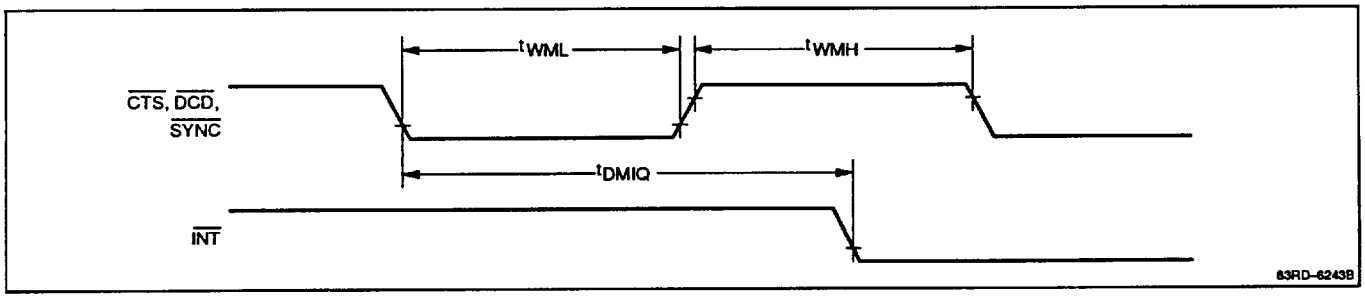
Receive Cycle



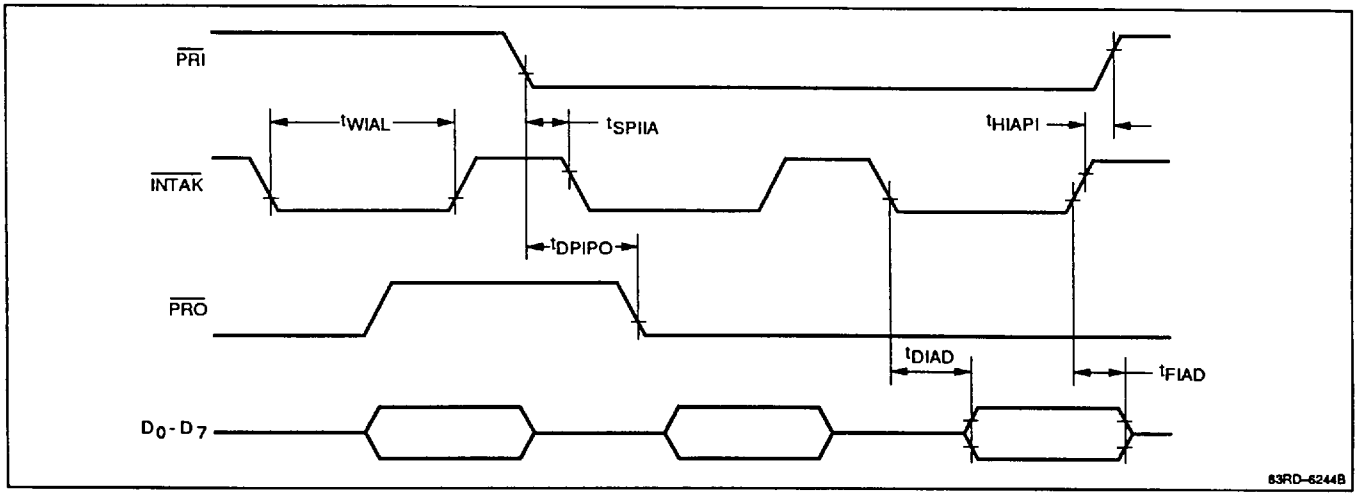
DMA Request/Acknowledge Control



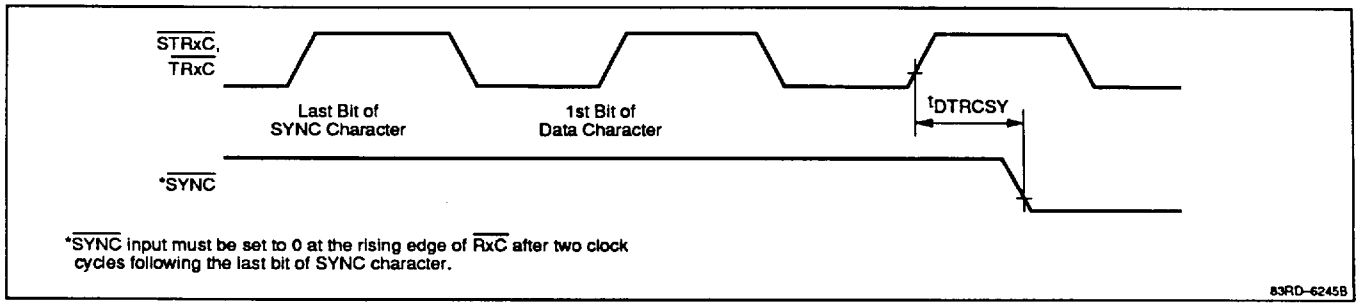
Modem Control



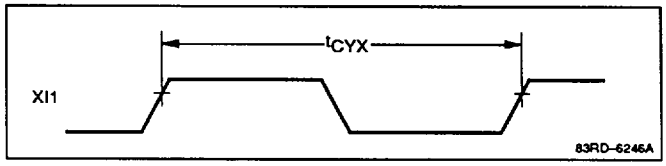
Interrupt Control



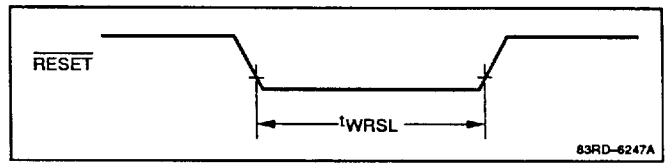
Sync Control



Crystal Oscillator



Reset



FUNCTIONAL OPERATION

Refer to the μPD72002 AMPSC block diagram (figure 2) for an overview of the four major functional blocks of logic listed below.

- System clock control
- Interface control
- Transmitter
- Receiver

System Clock Control

The system clock control logic receives and manages the system clock (CLK), which operates the internal circuitry of the μPD72002. The system clock and internal circuitry must be operating for the transmitters and receivers of the μPD72002 to function. In standby mode, the system clock is blocked by the clock control circuitry and the transmitters and receivers cannot operate. In clocked operation, the system clock can be used as the source for the data clock required by the transmitters and receivers.

The internal registers of the μPD72002 are static in nature and do not require the system clock to retain their contents.

Interface Control

The interface control logic contains the signals used to control the transfer of data and status information between the host CPU and the AMPSC. This logic block has four types of interface lines. The read/write and control lines ($\overline{RD}$, $\overline{WR}$, C/$\overline{D}$, S/$\overline{M}$, $\overline{CS}$) select the data to be transferred and the direction of transfer.

The reset line ($\overline{RESET}$), which is part of this group, resets the internal state of the μPD72002 when held active. The interrupt control line ($\overline{INT}$) sends a signal to the host CPU when the AMPSC requires attention. The interrupt acknowledge line ($\overline{INTAK}$) signals the μPD72002 when the host CPU is ready to service its request for attention. The interrupt priority lines ($\overline{PRI}$, $\overline{PRO}$) are used to form the interrupt priority daisy chain, which arbitrates the interrupt service priority.

The DMA control lines (DRQRx, DRQTx, $\overline{DAKRx}$, $\overline{DAKTx}$) inform the DMA controller when a data transfer is ready and when DMA service has been granted to the AMPSC. The data bus buffer provides temporary storage of the data (D_0-D_7) being transferred from the internal registers of the μPD72002 to the host CPU.

Transmitter

The transmitter accepts parallel byte data and sends it out serially. The data is sent out at a rate determined by the transmit data clock (TxCLK). The source of this clock is determined by the clock control multiplexer. Bytes are loaded into the transmit buffer. When the transmit shift register is empty, the contents of the transmit buffer are loaded into the transmit shift register.

The transmitter is also responsible for the transmit CRC calculation and the sending of flags and SYNC characters. The transmitter can be made to send breaks and aborts using commands from the host CPU.

The internal loopback feature connects the transmitter to the receiver and disconnects the receiver from the RxD pin. The echo loop feature connects the receiver to the TxD pin and disconnects the transmitter.

The baud rate generators (BRGs) divide down the selected clock source to produce data clocks that can be used for the transmitter and receiver. The clock multiplexer selects the clock sources for them. By selecting the correct value for the BRG count, the BRG can be used as a timer with a wide dynamic range. The clock source for the timer can be selected from the system clock, the data clock, an external source, or a crystal.

Receiver

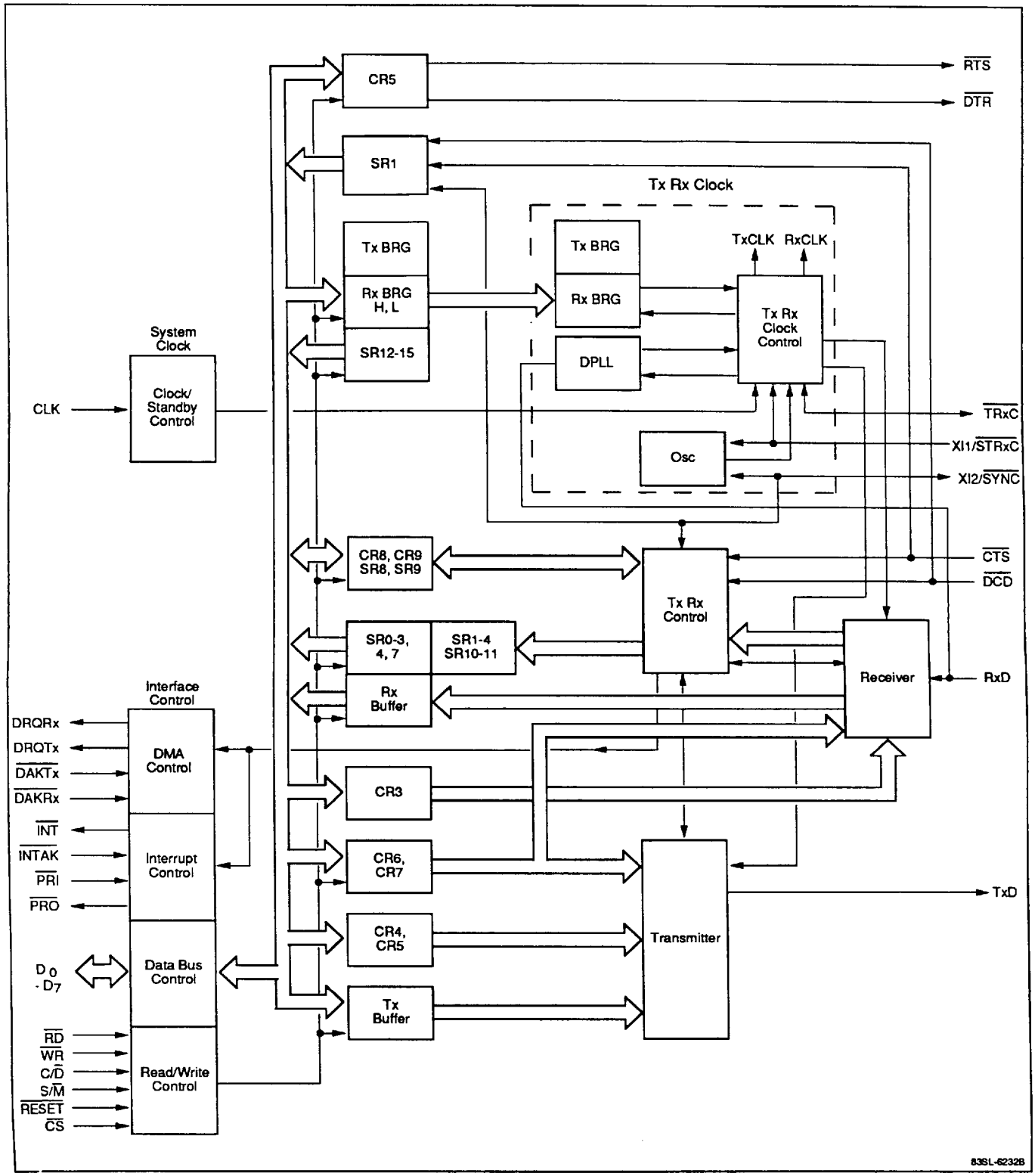
The receiver in the AMPSC accepts serial data into the receive shift register, which in turn assembles this serial data into parallel characters (byte). The assembled byte is transferred into the receive buffer (FIFO), which can contain up to three bytes. The receive status of each byte is transferred along with it through the receive buffer. In this way, the status reported by the μPD72002 is always current for the byte that is about to be removed from the FIFO.

The receive shift register also checks for flags and SYNC characters in the synchronous modes. Flags are automatically removed from the data stream, while SYNC characters have the option of being retained. This is determined by a CPU command.

The receiver in synchronous modes calculates the received CRC and checks it against the CRC received with the data. A difference is reported to the host processor.

The digital phase-locked loop (DPLL) is used to separate the data from the clocking information in the NRZI, FM, and Manchester-encoded bit streams. It locks in on the received data and provides an accurate and stable clock for the receiver.

Figure 2. μPD72002 AMPSC Block Diagram



Standby Mode

The μPD72002 enters the standby mode after a hardware reset or by issuing the standby command (CR13 bit D0). In standby mode, the system and data clocks are blocked internally by the clock multiplexer. This shuts down the AMPSC and reduces power consumption greatly. System power requirements can be further reduced by externally stopping the input clock transitions.

In standby mode, the μPD72002 retains all register values, but no internal functions operate and read operations of the AMPSC will not transfer any data. The transmitter and receiver remain disabled once standby mode is released, even if they were enabled when the AMPSC was placed in standby mode.

To release the standby mode, a write cycle must be performed to CR0. To resume normal operation without affecting the internal state of the device, a 0 can be written to CR0.

SYSTEM CONFIGURATION

In the system configuration example (figure 3), the μPD72002 is used as a high-speed interface to a modem. It controls the modem interface and serial data flow. The AMPSC is used with a direct memory access controller (DMAC) such as μPD71071 to speed data transfer and reduce host CPU overhead.

The μPD72002 directly interfaces the host CPU without requiring an interrupt controller, such as the μPD71059. Extra hardware is not required since the AMPSC can generate its own interrupt vectors.

The interface between the μPD72002 and the host CPU is not very complex. It requires only address decoding logic for I/O operations. The μPD72002 provides a direct DMA interface to the μPD71071 DMA controller by providing both DMA request and DMA acknowledge lines. The only additional signals required during DMA operation are $\overline{RD}$ and $\overline{WR}$; $\overline{CS}$ is not used during DMA data transfer.

The AMPSC's flexible interface simplifies connection to a variety of host processors.

PROGRAMMING

Software programming the AMPSC utilizes separate data and command/status paths. The data path uses an 8-bit register. The command/status path has a set of 8-bit registers structured for efficient and complete control with a minimum of interaction from the host processor.

The internal registers (table 1) are divided into control registers (CRs) and status registers (SRs).

To maintain compatibility with μPD72001:

(1) Registers CR2A and CR2B of the 72001 are replaced in the 72002 by CR2M (main) and CR2S (secondary).

(2) Register SR2B of the 72001 is replaced in the 72002 by SR2S.

The control and status registers for a given register bank are all accessed through the same I/O address. The different registers are selected by the register pointer in CR0 (bits D0-D2). The register pointer is reset to 0 after each register operation. For example,to write to CR2, a 2 is initially written to the control address ($C/\overline{D}$ pin set high). After this the value to be written into CR2 is also written to the control address.

To read from SR2, a 2 is written to the control address, and then a read cycle at the control address reads the value in SR2. A 0 is not required to be written before CR0 and SR0 are accessed. Control registers (figure 4) set up the device operation mode or control device operations. The host processor writes control words into these registers.

Status registers (figure 5) hold device status information. The host processor can sense the AMPSC device status by reading these registers.

Frequently used information is retained in control register CR0 and status register SR0. This information can be sent or received by writing or reading a single byte. In normal operation, CR0 is initially loaded with a command to reset the AMPSC. Next, CR2M is loaded to set the interface mode. This is followed by the remaining registers, beginning with CR4 to set the protocol type.

Figure 3. System Configuration Example

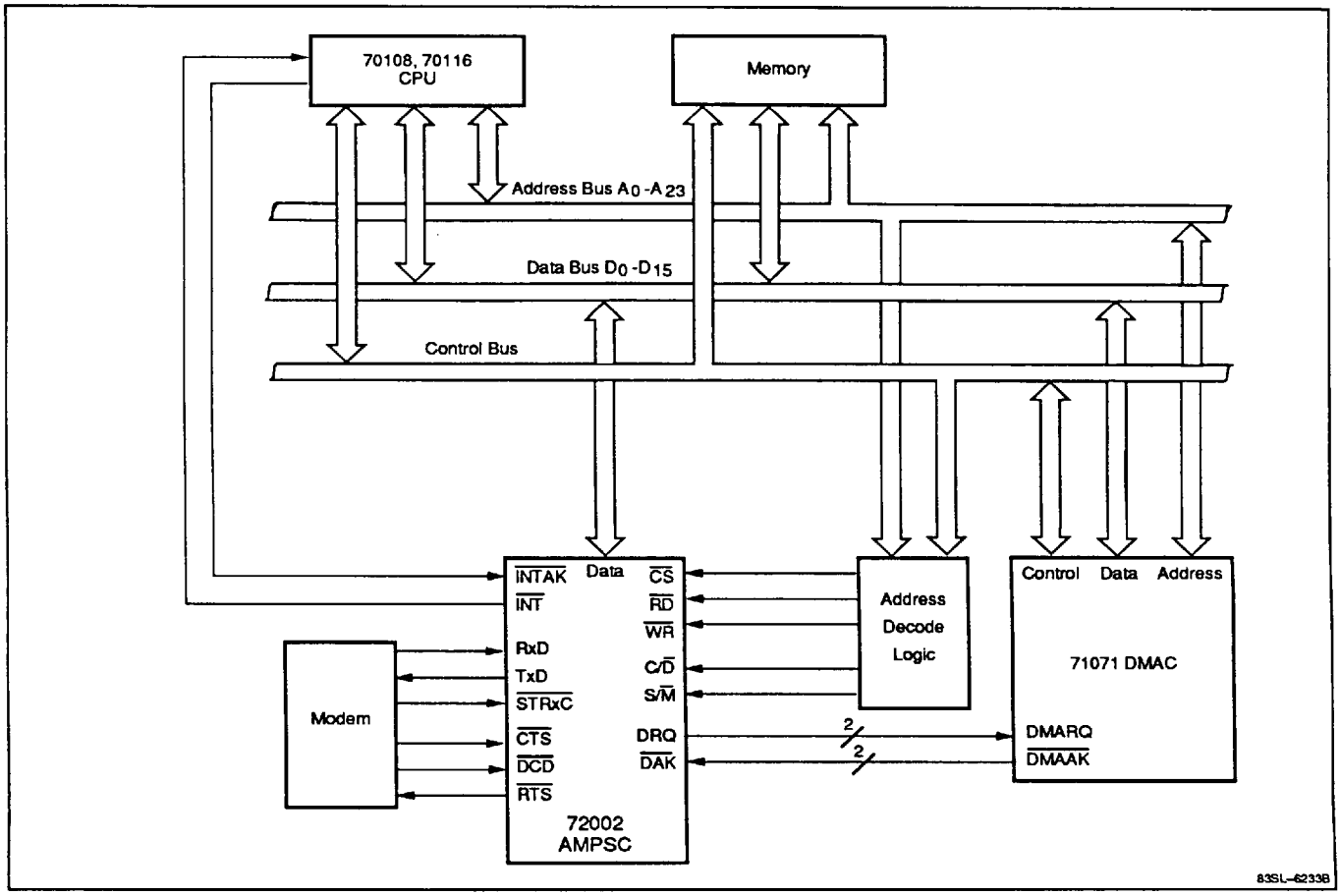


Figure 4. Control Register Bit Functions

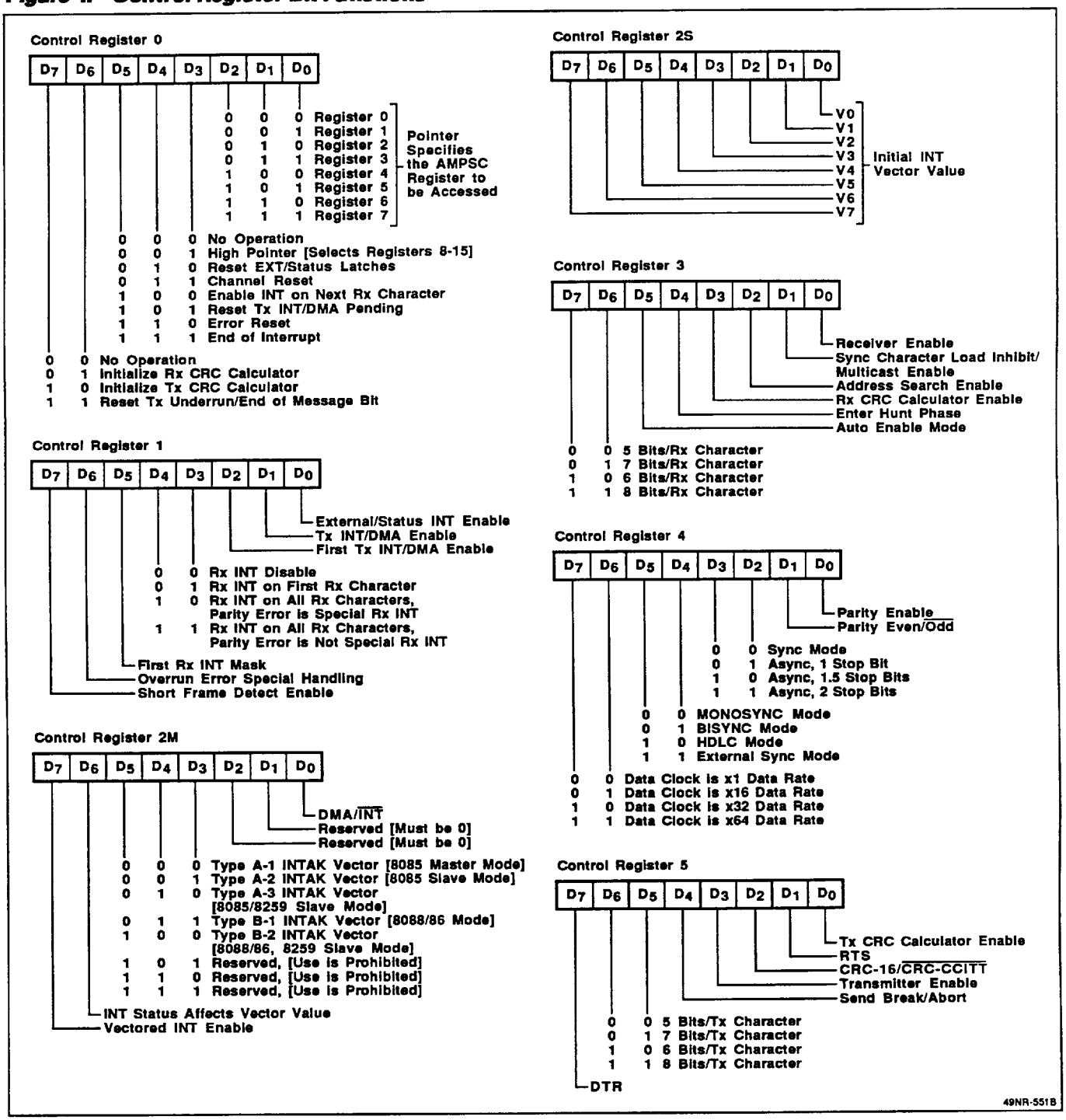


Figure 4. Control Register Bit Functions (cont)

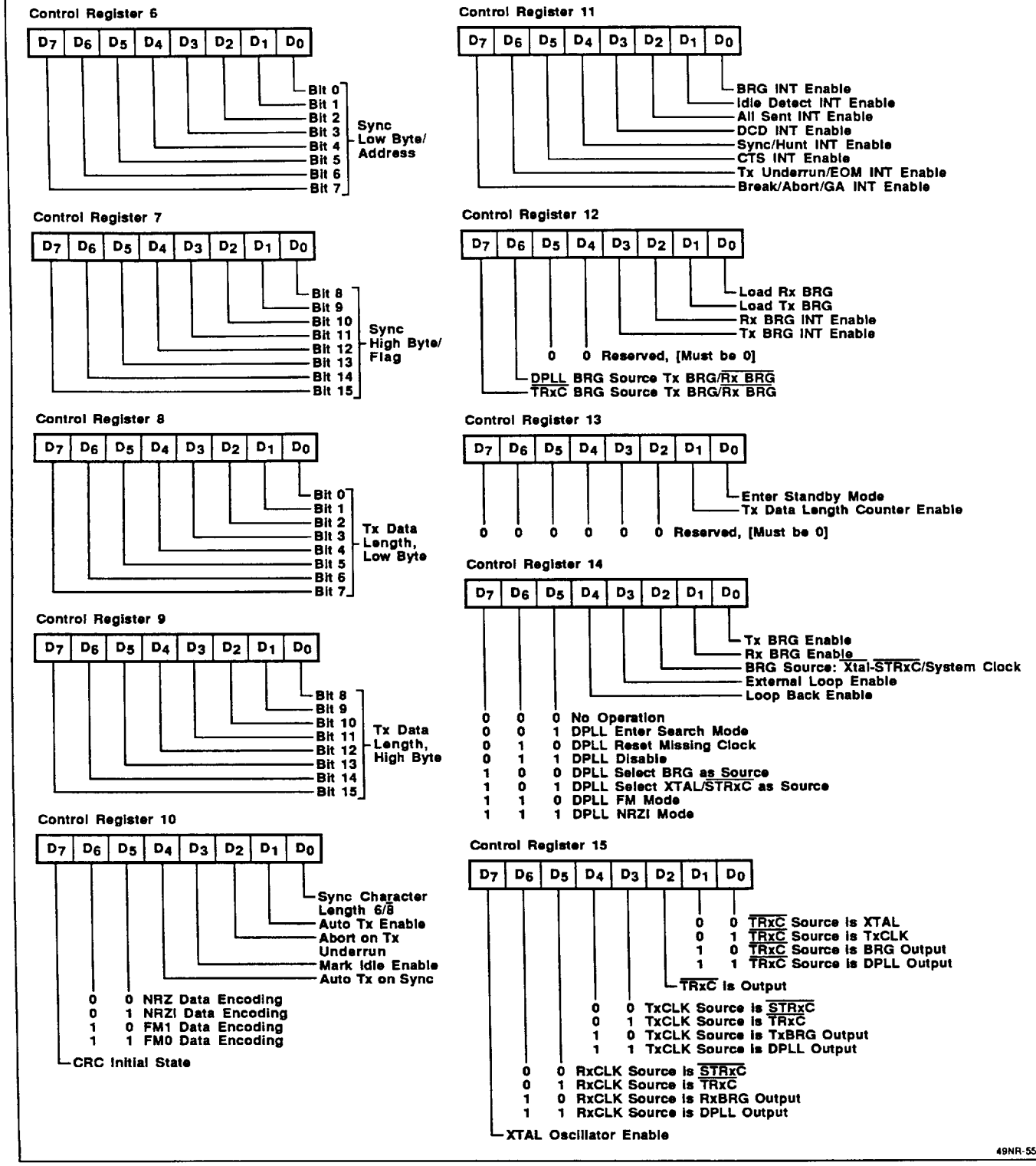


Figure 5. Status Register Bit Functions

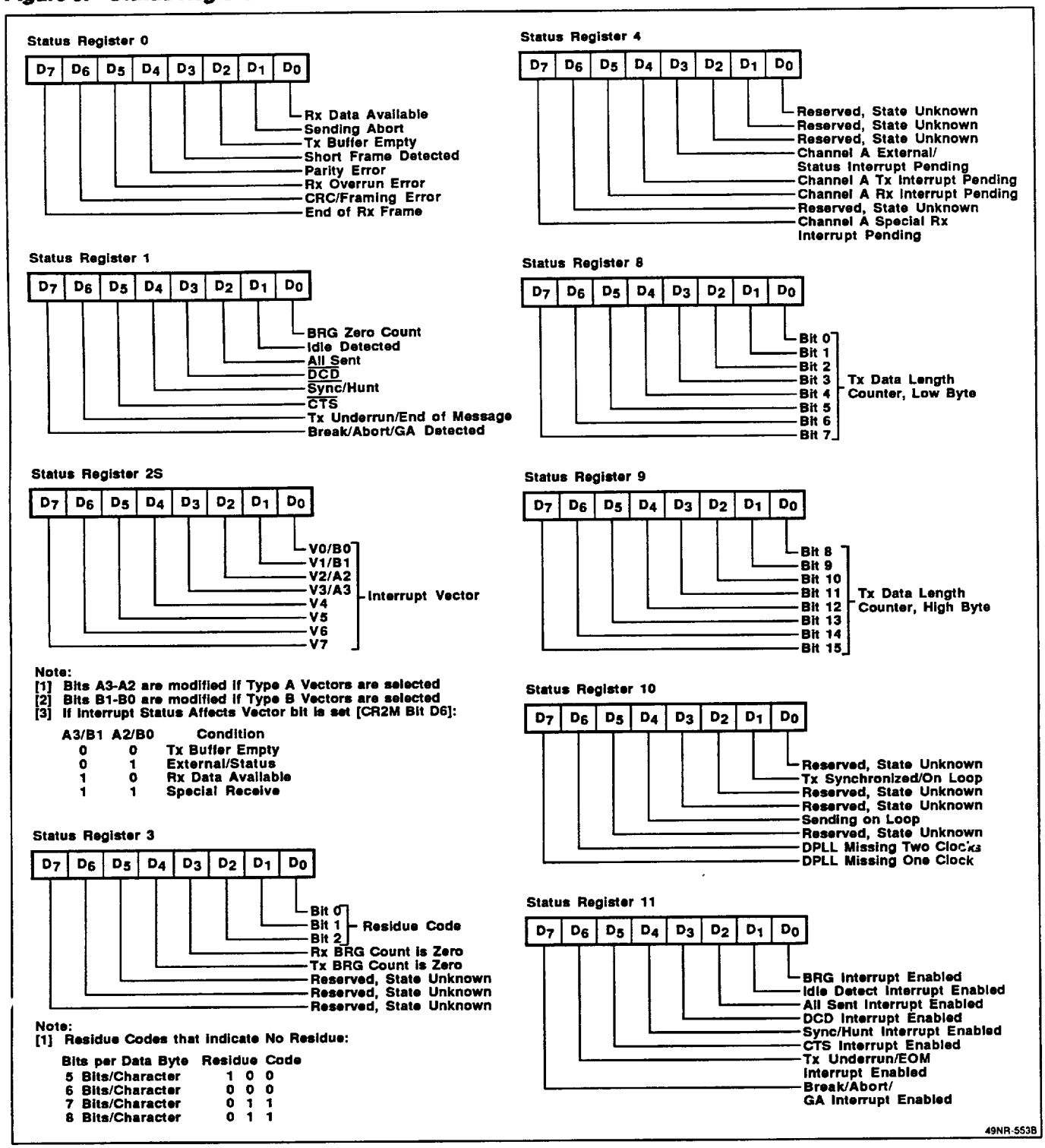


Figure 5. Status Register Bit Functions (cont)

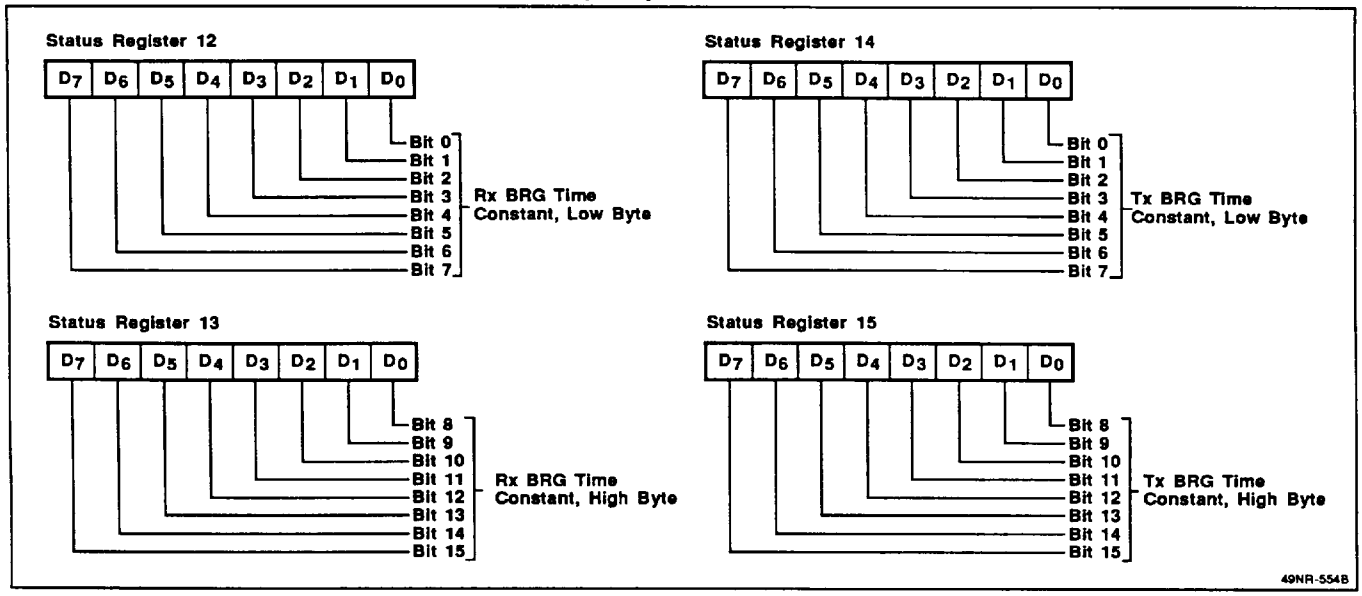


Table 1. AMPSC Internal Registers

Control Registers	CR0M, CR0S	
	CR1	
	CR2M	
	CR2S	Initial value of an interrupt vector
	CR3	
	CR4	
	CR5	
	CR6	
	CR7	
	CR8, CR9	Used as a pair
	CR10	
	CR11	
	CR12	Tx/Rx BRG registers are loaded by setting bits 0 and 1 of CR12
	CR13	
	CR14	
	CR15	

Status Registers	SR0	
	SR1	
	SR2M	No register
	SR2S	Value of interrupt vector
	SR3	
	SR4	
	SR5, SR6, SR7	No registers
	SR8	
	SR9	
	SR10	
	SR11	
	SR12, SR13	Used as a pair
	SR14, SR15	Used as a pair

CONTROL REGISTER CR0

CRC Control (D7-D6)

These bits are valid when the COP or BOP mode is selected. They are not used in the asynchronous mode.

No Operation (00). This command has no effect.

Initialize Rx CRC Calculator (01). This command initializes the receive (Rx) CRC calculator. The command should be issued before data reception starts. However, before this command is issued, the initial value of the Rx CRC calculator must be set by the value of CR10 bit D7.

This command is not required in the BOP mode, since the CRC calculator is automatically initialized upon receipt of a flag according to the value of CR10 bit D7.

Initialize Tx CRC Calculator (10). This command initializes the transmit (Tx) CRC calculator. It should be issued before data transmission is started. However, before the command is issued, the initial value of the Tx CRC calculator must be set by the value of CR10 bit D7.

In the BOP mode, if CR10 bit D7 is set to 1, the Tx CRC calculator is automatically initialized to 1 when a flag is loaded into the transmit shift register within the AMPSC.

Reset Tx Underrun/EOM Bit (11). This command resets SR1 bit D6 (transmit underrun/end-of-message bit) from 1 to 0. If data is not loaded into the transmit buffer before the transmit shift register begins transmitting its last bit, the AMPSC enters the Tx Underrun/EOM state. At this point, the AMPSC checks to see if a CRC or SYNC/Flag is to be sent—which depends on the value of SR1 bit D6 and the operating mode. Therefore, SR1 bit D6 must be reset before transmission of the last byte starts to enable transmission of the CRC. At the occurrence of a Tx Underrun, the CRC or the SYNC character/flag is sent when SR1 bit D6 is a 0 or 1, respectively. SR1 bit D6 is set when the CRC byte is written to the Tx shift register by the AMPSC.

In the BOP mode, bit D6 of SR1 is automatically set to 0 when the first data byte of a frame is written into the AMPSC.

Command (D5-D3)

These bits control the state of the device.

No Operation (000). This command has no effect.

High Pointer (001). This command is used in conjunction with CR0 bits D2-D0 (register pointer) to access status registers 8 through 15. For example, to access SR11, bits D5-D0 of CR0 are set to 001011.

Reset E/S Bit Latches (010). The Reset External Status Bit Latch command is issued when an E/S bit (any bit of SR1) latch operation has occurred. It opens the E/S latches and prepares for the latching of a new E/S bit status change. If the E/S interrupt is enabled, an E/S interrupt will occur and the latches will latch when an E/S bit's status changes. Not all state transitions will cause latching and an interrupt to occur. See the description of SR1 for details. New status will not be available in SR1 until this command is issued.

Channel Reset (011). This command resets the serial channel. It performs a function similar to the $\overline{\text{RESET}}$ pin. Executing the channel reset command halts channel operation. After a channel reset, three system clock periods (t_{CY}) should elapse before any further commands or data are sent to the channel.

Enable Next Rx Character Interrupt (100). This command is valid only when the First Rx Character mode (CR1 bits D4-D3 = 01) is selected. It is issued at the end of a message to request an additional Rx interrupt for the first received byte of the next message. The additional Rx interrupt occurs when the next data byte is received after the command is issued.

This command has no effect when the First Rx INT mask is on (CR1 bit D5 = 1), even if the First Rx INT mode is selected.

Reset Tx Interrupt/DMA Pending (101). This command is used to clear a pending Tx interrupt request or Tx DMA request while the Tx buffer is empty (SR0 bit D2 = 1). It is typically used to clear a Tx interrupt or Tx DMA request caused by the Tx buffer empty state that occurs after the last byte is written into the AMPSC.

Error Reset (110). This command is used to reset the pertinent bits (SR0 bits D7-D3) if a Special Rx Condition has occurred. If it occurs when the First Rx INT mode is selected, any data that is subsequently received is not transferred to the last stage of the AMPSC internal Rx buffer, but will remain in the first and second stages until this command is issued.

End of Interrupt (111). This command is used so that the AMPSC can recognize the end of interrupt service processing. It should be issued when interrupt service for the AMPSC is completed. Command execution resets the internal interrupt service latch and reenables lower priority interrupt requests. This command is required when the start of interrupt service has been indicated by either conducting an $\overline{\text{INTAK}}$ cycle, or by reading SR2S.

Register Pointer (D2-D0)

These bits specify which AMPSC register number is to be accessed. The bits are reset to 000 when system reset is executed or when the AMPSC is accessed after a register pointer value is specified. For registers numbered 8 and above, the High Pointer command (D5-D3 = 001) is used in conjunction with the register pointer to access them.

CONTROL REGISTER CR1

Short Frame Detect (D7)

Valid only in BOP mode, this bit detects short HDLC frames (frames shorter than 32 bits).

Short Frame Detect Disabled (0). Short frame detection is disabled.

Short Frame Detect Enabled (1). Short frame detection is enabled. If a short frame is received, SR0 bit D3 (Short Frame Detect) is set to 1, and a Special Rx Condition interrupt is generated.

Overrun Error (D6)

This bit selects the timing of overrun error detection.

Normal Mode (0). In this mode, a Special Rx Condition interrupt indicating Rx Overrun Error occurs when the received data that caused the error is transferred to the last stage of the Rx FIFO.

Special Mode (1). In this mode, a Special Rx Condition interrupt indicating Rx Overrun Error occurs immediately when the AMPSC detects the overrun error. The received data that caused the overrun error may not be the byte at the last stage of the Rx FIFO.

Receive Interrupt on First Character Mask (D5)

This bit is enabled only if the First Rx INT mode (CR1 bits D4-D3 = 01) is selected. It is used to mask Rx interrupts caused by received data. Setting this bit to 1 causes all first receive interrupts to be masked. It does not mask Special Rx Condition interrupts. It is used in data transfers when no interrupt service is desired or required, such as DMA only data transfer.

Receive Interrupt Mode (D4-D3)

These bits set the Rx INT mode. They specify the way received data is managed.

Disable Mode (00). This mode is used to accept received data using status polling, or to disable the receive interrupt request.

First Rx Character Mode (01). In this mode, which is typically used with DMA data transfer, an Rx interrupt occurs only when the first byte is received. This interrupt occurs when the receiver is enabled after initialization or after the Enable Next Received Character interrupt command is issued.

All Receive-1 Mode (10). This mode causes a receive interrupt to be generated for each byte received. In this mode, a parity error causes a Special Rx Condition interrupt.

All Receive-2 Mode (11). This mode is the same as All Receive-1 mode, except that a parity error does not cause a Special Rx Condition interrupt.

First Transmit Interrupt/DMA Enable (D2)

This bit determines whether a transmit interrupt or DMA request is generated immediately after the transmitter is enabled. It is valid when Tx INT/DMA is enabled (CR1 bit D1 = 1).

A transmit interrupt or DMA request is issued if bit D2 is 1 when the transmitter is enabled, but not if it is 0. Regardless of the state of bit D2, an interrupt or DMA request is generated when the Tx buffer makes the full-to-empty transition.

Transmit Interrupt/DMA Enable (D1)

This bit enables the transmit interrupt or DMA request. Each time a Tx Buffer Empty condition exists and provided bit D1 is set, an interrupt or DMA request is generated.

External/Status Interrupt Enable (D0)

If bit D0 is set, a change in state of the external/status bits causes an interrupt to occur. The current state of the external/status bits is latched. The latches must be reset with the Reset External/Status Bit Latches command (CR0 bits D5-D3) before subsequent interrupts can occur.

CONTROL REGISTER CR2M

Vectored Interrupt Enable (D7)

This bit determines the handling of the interrupt vector. If the bit is set, the interrupt vector is placed on the data bus during the $\overline{\text{INTAK}}$ cycle by the AMPSC. If the bit is reset, the vector is not placed on the bus; it can be read by the host processor from status register SR2S. In this mode, the $\overline{\text{INT}}$ signal is released after the host processor reads SR2S or clears the interrupt condition.

Interrupt Status Affects Vector (D6)

This bit determines if the value of an interrupt vector is modified according to the source of the interrupt. If the bit is set, the vector is modified as specified by bits D5-D3. If the bit is reset, the vector is not modified and the cause of the interrupt must be determined by reading SR0 and SR1.

Interrupt Vector Mode (D5-D3)

These bits determine the interrupt vector operation and select which bits of an interrupt vector are to be changed when the Interrupt Status Affects Vector bit is set (CR2M bit D6 = 1). For details of how the vector is modified, refer to the description of register SR2S. Table 4 shows the vector operation determined by bits D5-D3.

Interrupt/DMA Mode (D0)

This bit selects the data transfer mode: interrupt (D0 = 0) or DMA (D0 = 1). The E/S, Rx, and Special Rx Condition interrupts can be enabled in both modes. The Tx interrupts are disabled in DMA mode.

CONTROL REGISTER CR2S

Bits D7-D0 of CR2S set the initial value of an interrupt vector.

CONTROL REGISTER CR3

Receive Character Bit Length (D7-D6)

These bits determine the number of bits per character in the received data.

Bits D7-D6	Bits per Character
00	5
01	7
10	6
11	8

In COP mode, the number of bits in the SYNC character must be equal to the bit length of the received character. Parity is enabled or disabled accordingly (CR4 bit D0) depending on the selection of the received character bit length to match the SYNC character bit length.

Auto Enable Mode (D5)

Bit D5 enables and disables the auto enable mode. In this mode, the $\overline{CTS}$ and $\overline{DCD}$ pins control operation of the transmitter and receiver, respectively. If the input pin is high, the transmitter or receiver is disabled. In asynchronous mode with bit D5 = 1, the $\overline{RTS}$ pin outputs the current transmitter status. The pin remains low during transmission and returns high only after all characters have been sent.

The auto enable mode is enabled by setting bit D5 to 1 and disabled by resetting bit D5 to 0. With bit D5 = 0, $\overline{CTS}$, $\overline{DCD}$, and $\overline{RTS}$ function as normal inputs and outputs.

In auto enable mode, any status change on the $\overline{CTS}$ or $\overline{DCD}$ pins is latched and an external/status interrupt is generated.

Enter Hunt Phase (D4)

Valid in COP or BOP mode, bit D4 set to 1 forces the AMPSC to enter the hunt phase. In the hunt phase, the AMPSC searches the received data stream for either a SYNC character or Flag before it begins loading data into the Rx FIFO. When synchronization is established, bit D4 is set to 0 automatically.

Receive CRC Calculator Enable (D3)

Valid only in COP or BOP mode, bit D3 determines whether a CRC calculation is to be performed on the received data. In COP mode, the CRC is calculated 8 bit times after a byte is transferred into the receive FIFO. If bit D3 is reset before this time, the byte will not be included in the CRC calculation. D3 must be set again after the next byte is received to resume the CRC calculation.

Address Search Mode Enable (D2)

Valid only in BOP mode, bit D2 determines whether the address field value of a received frame is to be compared with the value set in CR6. If the bit is set to 1, Address Search is enabled and the AMPSC checks the first byte of the frame. If the byte matches CR6 or the global address (FFH), the frame is received. If the byte does not match, the AMPSC enters the Hunt mode again, and the byte and the rest of the frame are blocked and not received. If Multicast mode is enabled (CR3 bit D1), only the 4 most significant bits (CR6 bits D7-D4) of the address byte are compared.

Sync Character Load Inhibit/Multicast Enable (D1)

Valid only in COP or BOP mode, bit D1 has a different meaning in each mode. In COP mode, setting bit D1 to 1 enables the Sync Character Load Inhibit function. This prevents any byte that matches the value in CR6 from being loaded into the Rx FIFO and from being included in the CRC calculation.

In COP mode, this bit is used in conjunction with the Enter Hunt Phase bit (CR3 bit D4) to begin receive operation by the AMPSC. Once synchronization has been established, SYNC characters included in the received data stream are not transferred into the Rx buffer and are not included in the CRC calculation. However, if the Rx FIFO is full and the SYNC character causes an overrun, this function is invalidated. The SYNC character will be transferred into the first stage of the Rx FIFO, but no overrun error is reported by the AMPSC.

In BOP mode, bit D1 enables the Multicast function. In this mode, which is a modified form of the address search mode, only the most significant 4 bits of the received address are compared with the identical bits of CR6. Frame acceptance will function in the same way as in the address search mode.

If Multicast mode is enabled, no Abort detection is performed unless the address that matches the value in CR6 is detected. Once address detection is performed, Abort detection is subsequently performed unconditionally.

Receiver Enable (D0)

This bit enables and disables the receiver. Setting bit D0 enables the receiver; resetting it disables the receiver. If the Auto Enable mode is selected (CR3 bit D5 = 1), the signal applied to the $\overline{DCD}$ pin controls receiver operation.

Table 4. Interrupt Vector Operation Throughout INTAK Sequence

CR2M						Data Bus Status (INTAK response of AMPSC)							
D5	D4	D3	Mode	$\overline{PRI}$	$\overline{INTAK}$ Cycle	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	A1	Low	1st	1	1	0	0	1	1	0	1
				Low	2nd	V7	V6	V5	V4	M3	M2	V1	V0
				Low	3rd	0	0	0	0	0	0	0	0
				X	1st	1	1	0	0	1	1	0	1
				High	2nd	High Impedance							
				High	3rd	High Impedance							
0	0	1	A2	Low	1st	High Impedance							
				Low	2nd	V7	V6	V5	V4	M3	M2	V1	V0
				Low	3rd	0	0	0	0	0	0	0	0
				X	1st	High Impedance							
				High	2nd	High Impedance							
				High	3rd	High Impedance							
0	1	0	A3	X	1st	High Impedance							
				Low	2nd	V7	V6	V5	V4	M3	M2	V1	V0
				Low	3rd	0	0	0	0	0	0	0	0
				X	1st	High Impedance							
				High	2nd	High Impedance							
				High	3rd	High Impedance							
0	1	1	B1	Low	1st	High Impedance							
				Low	2nd	V7	V6	V5	V4	V3	V2	M1	M0
				X	1st	High Impedance							
				High	2nd	High Impedance							
1	0	0	B2	X	1st	High Impedance							
				Low	2nd	V7	V6	V5	V4	V3	V2	M1	M0
				X	1st	High Impedance							
				High	2nd	High Impedance							

Notes:

(1) X = Don't care

(2) When the Interrupt Status Affects Vector (Bit D6 of CR2M) is set, the M data bits are modified to indicate the interrupt source.

(3) Modes A3 and B2 ignore the state of $\overline{PRI}$. They are slave modes for use with an interrupt controller such as the μPD71059.

CONTROL REGISTER CR4

Clock Rate (D7-D6)

Bits D7 and D6 select the clock rate divisor. They are ignored in the internal synchronous modes. In the external synchronous mode, only the x1 and x16 selections are valid.

In asynchronous mode, the following values apply.

Bits D7-D6	Divisor
00	x1
01	x16
10	x32
11	x64

The divisor value is the factor by which the supplied data clock is greater than the data rate for the transmitter and receiver. The data clock source is selected by the clock multiplexer. It can be set to any of the BRG, DPLL, or external clock sources. The divisor determines the number of times that the received data is sampled per bit time by the receiver. Also, it determines the composition of the transmitter output.

Protocol Mode (D5-D4)

Bits D5-D4 select the synchronous protocol, which is used when the synchronous mode is selected with bits D3-D2.

Bits D5-D4	Mode
00	Monosync, character synchronous
01	Bisync, character synchronous
11	External sync, character synchronous
10	HDLC, bit synchronous

Tx Stop Bits/Sync Mode (D3-D2)

Bits D3-D2 select the number of stop bits sent after each byte in asynchronous mode, or they select the synchronous mode.

Bits D3-D2	Mode
00	Sync mode
01	Async mode, 1 stop bit
10	Async mode, 1.5 stop bits
11	Async mode, 2 stop bits

Parity Select (D1)

Valid in asynchronous and COP modes, bit D1 selects the parity type: 0 = odd and 1 = even. It is used only when the Parity Enable bit D0 of CR4 is set to 1.

Parity Enable (D0)

Bit D0 enables the parity bit calculation on transmitted data and parity checking on received data. Setting bit D0 enables parity; resetting bit D0 disables parity. If the length of the received character is 7 bits or less, the parity bit can be read in the received data byte. If parity is disabled, no parity bit is transmitted and none is expected on receipt.

CONTROL REGISTER CR5

$\overline{\text{DTR}}$ Control (D7)

This bit controls the $\overline{\text{DTR}}$ pin status: 0 = high and 1 = low.

Transmit Character Bit Length (D6-D5)

These bits specify the bit count per character in transmitted data.

Bits D6-D5	Bits/Character
00	5 or fewer
01	7
10	6
11	8

If the bit count per character is 6 or 7, only the low-order bits of the byte are valid and the most significant bit(s) are ignored. If the count is 5 bits or lower when writing into the transmit data register, refer to the data format in table 5.

Table 5. Parallel Data Format for 1 to 5 Bits per Character

Bits	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	0	0	D0
2	1	1	1	0	0	0	D1	D0
3	1	1	0	0	0	D2	D1	D0
4	1	0	0	0	D3	D2	D1	D0
5	0	0	0	D4	D3	D2	D1	D0

Dn = Valid data bit

Send Break/Abort (D4)

Bit D4 controls the break or abort transmission according to the selected mode. In asynchronous mode, bit D4 controls sending the break signal (TxD set to spacing (0) condition). Setting bit D4 to 1 begins sending the break signal; resetting it to 0 returns the transmitter to normal operation.

In BOP mode, setting bit D4 to 1 causes eight 1-bits (Abort sequence) to be sent. Depending on the preceding serial data, a total of up to 13 1-bits can be transmitted by the AMPSC when this command is issued. When the abort is transmitted, the data in the Tx buffer is invalidated. After completion of the message, bit D4 is reset automatically and the transmitter returns to the idle state.

Transmitter Enable (D3)

Disable. Setting bit D3 to 0 disables the transmitter. If the transmitter is currently sending a character, the AMPSC waits until the character is completed before setting TxD to the marking (1) state. If bit D3 is reset during transmission of a CRC character, a SYNC character or Flag is sent in place of the CRC character.

If D3 is reset in the COP or BOP mode, the Tx Underrun/EOM bit (SR1 bit D6) is set.

If the AMPSC is in the SDLC Loop mode (refer to CR10) or the Echo Loop Test mode (refer to CR14), the TxD pin is connected to RxD and is not set to marking.

Enable. Setting bit D3 to 1 enables the transmitter to start transmission. If the Auto Enable mode is selected (CR3 bit D5 = 1), the signal applied to the $\overline{CTS}$ pin controls transmitter operation.

CRC Polynomial (D2)

This bit selects the polynomial used for CRC calculation. It is valid only in COP or BOP mode. Only the CCITT polynomial is used in BOP mode. Bit D7 of CR10 sets the initial value of the CRC calculator.

D2 = 0 (CRC-CCITT): The generating polynomial expression is $X^{16} + X^{12} + X^5 + 1$.

D2 = 1 (CRC-16): The generating polynomial expression is $X^{16} + X^{15} + X^2 + 1$.

$\overline{RTS}$ Control (D1)

Bit D1 controls the $\overline{RTS}$ pin. Setting bit D1 to 0 causes $\overline{RTS}$ to be high; setting it to 1 causes it to go low.

If Auto Enable mode is selected in asynchronous mode, $\overline{RTS}$ operates differently. If bit D1 remains at 0 from the start of transmission through to the end, $\overline{RTS}$ will stay high. If it is set to 1 from the start of a transmission, $\overline{RTS}$ remains low. If it starts set to 1 and is then set to 0 while transmitting, $\overline{RTS}$ will not go high until all data is transferred out of the Tx shift register (All Sent bit D2 of SR1 = 1).

Transmit CRC Calculator Enable (D0)

Valid only in the COP or BOP mode, bit D0 determines whether transmitted data is included in the CRC calculation. If bit D0 is set when the byte is transferred into the Tx shift register, the byte is included in the Tx CRC calculation. Bit D0 should be set or reset before loading a data byte into the AMPSC.

In BOP mode, since all transmit data is included in the CRC calculation, this bit should remain set to 1.

CONTROL REGISTER CR6

Valid only in the COP or BOP mode, this byte (bits D7-D0) specifies the SYNC character pattern or address value.

In Monosync or External Sync mode, D7-D0 holds the Tx SYNC character. In Bisync mode, the low-order byte of the SYNC character is set in D7-D0.

In Monosync or External Sync mode with the SYNC character length selected as 6 bits (CR10 bit D0 = 1), bits D1 and D0 are repeated in bit positions D7 and D6 of CR6.

In BOP mode with the Address Search Enable mode set (CR3 bit D2 = 1), this byte is the secondary address. With the Multicast bit set (CR3 bit D1 = 1), only the 4 most significant bits are used.

CONTROL REGISTER CR7

Valid only in the COP or BOP mode, these bits specify the SYNC character or Flag.

In Monosync mode, D7-D0 hold the Rx SYNC character. In Bisync mode, the high-order byte of the SYNC character is set in D7-D0. These bits are not used in External Sync mode.

In Monosync mode with the SYNC character length selected as 6 bits, the 6 uppermost bits of CR7 contain the Rx SYNC character.

In BOP mode, the flag pattern (01111110) is set in bits D7-D0.

CONTROL REGISTER CR8

Valid only in the BOP mode, CR8 bits D7-D0 hold the low byte (bits 7-0) of the transmit data length. Register pair CR8 and CR9 must be loaded before the Tx Data Length Counter Enable bit (CR13 bit D1) and Tx Enable bit (CR5 bit D3) are set. The transmit data length register (TxDLR) is used to automate the sending of HDLC frames. See the description of CR13 bit D1 for detailed information.

CONTROL REGISTER CR9

Valid only in the BOP mode, CR9 bits D7-D0 hold the high byte (bits 15-8) of the transmit data length. Register CR9 is paired with CR8.

CONTROL REGISTER CR10

Initial CRC State (D7)

Valid only in the COP or BOP mode, bit D7 specifies the initial state of the CRC calculator. Setting this bit to 0 causes the CRC to be initialized to 0 when the Initialize Tx/Rx CRC command (CR0 bits D7-D6) is performed. Setting this bit to 1 causes the CRC to be set to all 1s.

Data Format (D6-D5)

These bits specify the serial data format and enable the corresponding encoder/decoder.

Bits D6-D5	Format
00	NRZ
01	NRZI
10	FM1
11	FM0

With NRZ format, it is possible to decode Manchester encoded data by setting the DPLL mode to FM (CR14 bits D7-D5 = 110).

Auto Tx on Sync/Tx on Loop (D4)

Bit D4 is valid only in the COP or BOP mode. In COP mode, bit D4 provides the Auto Tx on Sync function to synchronize receiver and transmitter operation as follows.

(1) D4 = 0. The Auto Tx on Sync function (CR10 bit D1 = 1) is disabled.

(2) D4 = 1. If CR10 bit D1 is also set to 1, the transmitter is disabled and the receiver enters the Hunt Phase. When the SYNC character is detected, character synchronization is established, the transmitter is enabled, and data transmission can begin. The state of character synchronization can be determined from the state of the Tx Sync/On Loop bit (SR10 bit D1).

Once synchronization is established after D4 is set to 1, resetting the bit to 0 does not affect synchronization.

In BOP mode, bit D4 controls SDLC Loop operation. This bit is valid only when CR10 bit D1 (Auto Tx/Loop Enable) is set to 1. Bit D4 should be set before the transmitter or receiver is enabled.

The Tx on Loop function is used for data transmission during SDLC Loop operations. Bit D4 set to 0 (1) disables (enables) the function.

(1) D4 = 0. The Tx on Loop function is disabled (CR10 bit D1 = 1). In SDLC Loop mode of operation, once the AMPSC forms a loop (and starts transmission), bit D4 must be reset to 0. This allows the CRC and flag to be automatically transmitted if a Tx Underrun/EOM condition occurs and allows the AMPSC to be subsequently placed in Loop mode with a 1-bit delay. Bit D4 must be reset before the CRC transmission is completed.

(2) D4 = 1. SDLC Loop operation is selected (CR10 bit D1 = 1). In SDLC Loop mode, the RxD input is connected to the TxD output within the AMPSC to form a loop. GA (Go Ahead) pattern detection is initiated. If the GA pattern (11111110 = FEH) is detected, 1-bit delay is inserted between RxD and TxD and the GA pattern detection is continued. At this point the transmitter remains disabled, but the receiver can be enabled. Subsequently, if the GA pattern is detected, the transmitter is enabled; the GA pattern is automatically transformed into a flag so that any data in the Tx buffer may be transmitted following the flag. Once transmission is started, bit D4 must be reset before the CRC transmission is completed.

Idle Condition (D3)

Valid only in BOP mode, bit D3 determines the type of information to be transmitted following a closing flag or completion of the Send Abort command. If bit D3 is 0, flags will be sent; if it is a 1, continuous marks (1s) will be sent.

Transmit Condition on Underrun (D2)

Valid only in the BOP mode, bit D2 determines transmitter action when a Tx Underrun condition occurs. If bit D2 is reset, either the CRC followed by a flag or just a flag is transmitted depending on the state of the Tx Underrun/EOM bit (SR1 bit D6) and the Tx CRC Enable

bit (CR5 bit D0). If the CRC is disabled or the Tx Underrun bit is a 1, only flags are sent. Otherwise, the CRC is sent followed by flags. If bit D2 is set, the Abort message is sent followed by flags regardless of the state of the Tx Underrun/EOM bit or the Tx CRC Enable bit.

Auto Tx/Loop Enable (D1)

Valid only in the COP or BOP mode, bit D1 enables the operation that is set with bit D4. This bit should be set before the transmitter or receiver is enabled.

In COP mode, if D1 is set to 0, the Auto Tx on Sync function is disabled; if D1 is set to 1, the Auto Tx on Sync function is enabled.

In BOP mode, bit D1 controls SDLC Loop operation. If D1 is set to 0, Loop operation is disabled. If this bit is set to 0 after the AMPSC has entered loop operation, the RxD pin is disconnected from the TxD output in the AMPSC as soon as the GA pattern has been received, disabling SDLC Loop mode. If bit D1 is set to 1, Loop operation is enabled.

SYNC Character Length (D0)

Valid only in the COP mode, bit D0 determines the number of bits per SYNC character. Setting bit D0 to 0 gives a character length of 8 bits in Monosync and 16 bits in Bisync. With bit D0 = 1, the character length is 6 bits for Monosync mode. Bit D0 must not be set to 1 in Bisync mode.

CONTROL REGISTER CR11

Each bit of CR11 controls E/S interrupt request generation by the AMPSC due to the E/S interrupt sources. An interrupt is generated if the E/S interrupts are enabled (CR1 bit D0 = 1). For the causes of interrupts assigned to each, refer to the description of SR1. Setting each bit to 1 enables it as a source of interrupts.

Break/Abort/Go Ahead Interrupt Enable (D7)

In Asynchronous and COP modes, bit D7 enables interrupts at the beginning and end of each detected break condition (a null character plus a framing error).

In BOP mode, when not in SDLC loop, bit D7 enables interrupts at the beginning and end of each received abort condition (7 or more consecutive 1-bits). In SDLC loop mode, bit D7 also enables interrupts for detecting the GA pattern (11111110 = FEH).

Transmitter Underrun/End of Message Interrupt Enable (D6)

Valid only in the COP or BOP mode, bit D6 enables interrupts caused by Tx Underrun and Tx End of Message detection.

Clear to Send Interrupt Enable (D5)

Bit D5 enables interrupts caused by a change of state on the $\overline{CTS}$ pin.

SYNC/Hunt Interrupt Enable (D4)

Bit D4 enables interrupts caused by a change in the $\overline{SYNC}$/Hunt state.

Data Carrier Detect Interrupt Enable (D3)

Bit D3 enables interrupts caused by a change of state on the $\overline{DCD}$ pin.

All Sent Interrupt Enable (D2)

Valid only in the Asynchronous or BOP mode, bit D2 enables interrupts generated by the All Sent condition.

Idle Detect Interrupt Enable (D1)

Valid only in the BOP mode, bit D1 enables interrupts caused by a change in the Idle Detection condition.

BRG Interrupt Enable (D0)

Bit D0 enables interrupts caused by one of the baud rate generator/timers (BRG) counting down from 1 to 0. Also, each of the BRGs must be enabled (CR12 bits D3-D2).

CONTROL REGISTER CR12

BRG Select for $\overline{TRxC}$ (D7)

When BRG is selected as the source of the clock at the $\overline{TRxC}$ pin (CR15 bits D1-D0 = 10), and the $\overline{TRxC}$ pin is set to output (CR15 bit D2 = 1), bit D7 selects TxBRG (D7 = 1) or RxBRG (D7 = 0).

BRG Select for DPLL (D6)

Bit D6 selects the source (TxBRG or RxBRG) for the DPLL. It is valid when the BRG is selected as the source for the DPLL circuit (CR14 bits D7-D5 = 100). Setting bit D6 to 1 selects TxBRG and setting it to 0 selects RxBRG.

Transmit BRG Interrupt Enable (D3)

Bit D3 enables an E/S interrupt when the TxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Receive BRG Interrupt Enable (D2)

Bit D2 enables an E/S interrupt when the RxBRG counts down from 1 to 0. It is valid only when the BRG IE bit is set (CR11 bit D0 = 1).

Transmit BRG Register Set (D1)

Bit D1 is used to write the time constant value into the TxBRG register. When D1 is set to 1, the next two bytes written to the AMPSC are assumed to be the time constant value. The lower byte is written in the first write cycle and the upper byte in the second write cycle. Bit D1 is automatically reset after the register is loaded.

The time constant is calculated by the following formula.

$$\text{Time constant} = \frac{\text{Source clock frequency (Hz)}}{2 \times (\text{Data clock rate (b/s)})} - 2$$

The data clock rate is the transmitted or received data rate multiplied by the clock factor specified in CR4 bits D7-D6. For example, if the system clock is selected as the BRG source (CR14 bit D2 = 1) at 8 MHz and the BRG is the transmitter source (CR15 bits D4-D3 = 10) with a clock factor of x16 (CR4 bits D7-D6 = 01) and data rate of 9600 bits per second, the calculation would be as follows.

$$\frac{8 \times 10^6}{2 \times (9600 \times 16)} - 2 = 24.04 = 0018 \text{ (hex)}$$

The loading sequence in hexadecimal for the TxBRG would be 0C, 02, 18, and 00.

If data is being written while the BRG is running, the value will not be loaded into the BRG until it counts down to 0.

Receive BRG Register Set (D0)

Bit D0 is used to write the time constant value into the RxBRG register. It operates in the same manner as bit D1 for the TxBRG register.

CONTROL REGISTER CR13

Transmit Data Length Counter Enable (D1)

Bit D1 enables the transmit data length counter(TxDLC) that determines the end of a transmitted frame and is valid only in BOP mode. When bit D1 is set to 1, the TxDLC (SR8-SR9) is incremented each time a Tx interrupt or DMA request is generated, and the value is compared with the value in the transmit length register (TxLR CR8-CR9). If the two values are equal, the subsequent Tx Buffer Empty status is masked and no interrupt or DMA request is made. This results in a transmitter underrun condition. The AMPSC then generates an External/Status interrupt with the Tx Underrun/EOM bit set. Next, the AMPSC sends the CRC followed by a closing flag; once the closing flag has been sent, an E/S interrupt with the All Sent bit set is generated.

If the transmitter underruns and the TxDLC and TxLR values do not match, then the AMPSC generates an E/S interrupt with the Tx Underrun/EOM bit set. The AMPSC then sends an Abort followed by a flag; the Sending Abort bit (SR0 bit D1) will be set. Once the flag is sent, an E/S interrupt with the All Sent bit set is generated.

The TxLC value (SR8-SR9) can also be compared with the frame length to determine if correct transmission occurred. In either case the TxDLC enable bit must be set to 1 again in order to generate new Tx interrupts/DMA requests.

Standby Mode Set (D0)

Setting bit D0 to 1 places the AMPSC in the Standby mode. This mode consumes very little power but saves all internal register values. The transmitter and receiver remain disabled once standby mode is released even if both were enabled when the AMPSC was placed in standby mode. Greater power reduction is possible by not toggling any of the AMPSC inputs. In this mode, the system clock (CLK) and the data clocks are not circulated within the AMPSC.

The AMPSC enters the standby mode automatically after RESET. Writing 00H to CR0 restores normal operation. Table 6 lists the status of the pins in standby mode. During standby mode, the $\overline{WR}$ and $\overline{RD}$ pins must be held high and the $\overline{CTS}$, $\overline{DCD}$, and $\overline{SYNC}$ pins cannot be toggled. Read cycles that are conducted will not result in data being driven onto the bus.

Table 6. Pin Status in Standby Mode

Symbol	I/O	Pin Status
C/$\overline{D}$	In	Unchanged
$\overline{CS}$	In	Unchanged
$\overline{CTS}$	In	Unchanged
D_0-D_7	I/O	High-Impedance
$\overline{DAKR}$x	In	Unchanged
$\overline{DAKT}$x	In	Unchanged
$\overline{DCD}$	In	Unchanged
DRQRx	Out	Retains current state
DRQTx	Out	Retains current state
$\overline{DTR}$	Out	Retains current state
$\overline{INT}$	Out	Retains current state
$\overline{INTAK}$	In	Unchanged

Table 6. Pin Status in Standby Mode (cont)

Symbol	I/O	Pin Status
$\overline{PRI}$	In	Unchanged
$\overline{PRO}$	Out	Depends on $\overline{PRI}$
$\overline{RD}$	In	Unchanged
$\overline{RTS}$	Out	Retains current state
RxD	In	Unchanged
S/$\overline{M}$	In	Unchanged
$\overline{TRxC}$	I/O	High-Impedance
TxD	Out	Retains current state
$\overline{WR}$	In	Unchanged/
XI1/ $\overline{STRxC}$	In	Unchanged
XI2/ $\overline{SYNC}$	I/O	High-Impedance

CONTROL REGISTER CR14

DPLL Command (D7-D5)

These bits control the digital phase-locked loop(DPLL). After reset, the DPLL is disabled, the $\overline{STRxC}$ pin is selected as the source clock, and the NRZI mode is selected. The DPLL commands corresponding to the eight states of bits D7-D5 are described below.

No Operation (000). This command causes no operation.

Enter Search (001). This command causes the DPLL to start the detection of edges in received data. Circuit operation depends on the data format.

Reset Missing Clock (010). Valid when FM mode is selected, this command resets the Missing Clock bits (SR10 bits D7-D6).

Disable (011). This command stops DPLL operation and resets the Missing Clock bits.

Source BRG Select (100). This command selects a BRG as the clock source for the DPLL. Selection of TxBRG or RxBRG is determined by CR12 bit D6 (BRG Select for DPLL).

Source Xtal/$\overline{STRxC}$ Select (101). This command is used when the crystal-controlled oscillator or a clock applied to the $\overline{STRxC}$ pin is to be the source clock for the DPLL. Selection between the crystal oscillator and the $\overline{STRxC}$ input is specified by CR15 bit D7 (Crystal Select).

FM Mode (110). This command is used when received data is to be treated as FM format. Setting the data format to NRZ (CR10 bits D6-D5 = 00) allows the AMPSC to decode Manchester encoded data.

NRZI Mode (111). This command is used when received serial data is to be treated as NRZI format.

Local Self Test (D4)

When bit D4 is set to 1, the transmitter output is directly connected to the input of the receiver within the AMPSC. Signals applied to the RxD pin will be ignored. In this mode, Auto Enable cannot be used to control the transmitter or receiver.

Echo Loop Test (D3)

When bit D3 is set to 1, the RxD input pin is connected to the TxD output pin in the AMPSC so that the received data is echoed back to the remote sender for line testing. The AMPSC transmitter is disabled. In this mode, Auto Enable cannot be used to control the transmitter.

BRG Source Select (D2)

Bit D2 selects the source clock for the BRGs. The selected source clock is shared by the TxBRG and the RxBRG. If D2 is set to 1, the system clock is used as the source clock. If D2 is set to 0, the source clock can either be the crystal oscillator (CR15 bit D7 = 1) or the $\overline{STRxC}$ input (CR15 bit D7 = 0).

Receive BRG Enable (D1)

Setting bit D1 to 1 starts the RxBRG, which takes two clocks to begin operating.

Transmit BRG Enable (D0)

Setting bit D0 to 1 starts the TxBRG, which takes two clocks to begin operating.

CONTROL REGISTER CR15

Crystal Select (D7)

If bit D7 is set to 1, the on-chip crystal oscillator is enabled and a crystal can be connected across pins XI1 and XI2. If bit D7 is 0, the oscillator is disabled and the pins become $\overline{SYNC}$ and $\overline{STRxC}$.

Receive Clock Select (D6-D5)

These bits select the source for the receive data clock.

Bits D6-D5	Receive Clock Source
00	Clock applied to $\overline{STRxC}$ pin
01	Clock applied to $\overline{TRxC}$ pin (CR15 bits D2-D0 are invalid)
10	RxBRG output
11	DPLL output

Transmit Clock Select (D4-D3)

These bits select the source for the transmit data clock.

Bits D4-D3	Transmit Clock Source
00	Clock applied to $\overline{STRxC}$ pin
01	Clock applied to $\overline{TRxC}$ pin (CR15 bits D2-D0 are invalid)
10	TxBRG output
11	DPLL output

$\overline{TRxC}$ Input/Output (D2)

Bit D2 determines whether the $\overline{TRxC}$ pin will be an input or an output. It is an input if bit D2 = 0 or if the pin is specified as an input by bits CR15 D6-D5 or D4-D3.

$\overline{TRxC}$ Source Select (D1-D0)

When the $\overline{TRxC}$ pin is selected as an output, these bits determine the output source. Refer to the preceding descriptions for D6-D5, D4-D3, and D2 to determine when the $\overline{TRxC}$ pin is an output.

Bits D1-D0	Output at Pin $\overline{TRxC}$
00	On-chip crystal oscillator (if enabled)
01	Transmit data clock
10	TxBRG or RxBRG as selected by CR12 bit D7
11	DPLL output

STATUS REGISTER SR0

End of Frame (D7)

Valid only in the BOP mode, bit D7 indicates if reception of a single frame is complete. When this bit is 1, a complete frame has been received and the CRC Error bit (SR0 bit D6) and Residue Code (SR3 bits D2-D0) are valid. The EOF condition causes a Special Rx Condition interrupt. The Error Reset command resets this bit.

CRC/Framing Error (D6)

In the asynchronous mode, bit D6 indicates a framing error. It is set to 1 if a zero is detected at the stop bit position. It generates a Special Rx Condition interrupt. Bit D6 is reset by an Error Reset command or reception of a normal data byte.

In the COP or BOP mode, bit D6 set to 1 indicates a CRC error. Bit D6 set to 0 indicates no CRC error.

In the COP mode, bit D6 is valid 20 bit times subsequent to the last bit of the second CRC byte that is input at the RxD pin, or 16 bit times after the second CRC byte is transferred to the Rx buffer.

In the BOP mode, bit D6 is valid when the End of Frame bit (SR0 bit D7) is set to 1.

A CRC error does not generate a Special Rx Condition interrupt.

Receive Overrun Error (D5)

A 1 in bit D5 indicates an Rx Overrun error. This error occurs each time the AMPSC attempts to transfer an additional byte from the Rx shift register to the Rx FIFO and the FIFO is already full.

An Rx Overrun error causes a Special Rx Condition interrupt. The timing of the Rx Overrun Error and the resulting Special Rx Condition interrupt will differ depending on the setting of the Overrun Error INT bit (CR1 bit D6). For more details, refer to the description of control register CR1.

The Rx Overrun Error bit is reset by the Error Reset command.

Parity Error (D4)

Valid only in the Asynchronous or COP mode when parity is enabled (CR4 bit D0 = 1). A 1 in bit D4 indicates that a parity error occurred in a received byte. The Parity Error bit is reset by the Error Reset command.

In the All Receive INT-1 mode (CR1 bits D4-D3 = 10), a parity error causes a Special Rx Condition interrupt.

Short Frame Detect (D3)

Valid only in the BOP mode when Short Frame Detect Enable is selected (CR1 bit D7 = 1), bit D3 is set when a short frame is received and is reset by the Error Reset command. A short frame has fewer than 32 bits between two flags.

Detection of a short frame causes a Special Rx Condition interrupt.

Transmit Buffer Empty (D2)

A 1 in bit D2 indicates that the Tx buffer is empty and can be loaded with the next Tx byte. Bit D2 is 0 when the Tx buffer contains a byte that has not been transferred to the Tx shift register. Bit D2 is also 0 in the COP or BOP mode during CRC transmission.

Sending Abort (D1)

Valid only in the BOP mode, a 1 in bit D1 indicates that the AMPSC is sending an abort sequence.

Bit D1 is reset by the Error Reset command. Status changes in bit D1 do not cause an interrupt.

Receive Data Available (D0)

A 1 in bit D0 indicates the presence of valid received data in the Rx buffer of the AMPSC.

STATUS REGISTER SR1

This register consists of external status bits that indicate the causes of E/S interrupts. If the E/S INT is enabled (CR1 bit D0 = 1) and an interrupt by a specific E/S bit is enabled, the changes in the pertinent E/S bit states are latched and cause an E/S interrupt. If the E/S interrupt is disabled, changes in the E/S bit status will not be latched.

Break/Abort/Go Ahead Detect (D7)

Bit D7 is valid only in the Asynchronous or BOP mode. In the Asynchronous mode, a 1 in bit D7 indicates that a Break (character in which the start, stop, and data bits are all 0s) has occurred. Data received during the Break (all 0s) is not loaded into the Rx FIFO.

In the BOP mode, bit D7 indicates the reception of an Abort (seven or more consecutive 1s). In SDLC Loop mode, bit D7 indicates reception of the Go Ahead (GA) pattern (11111110 = FEH) or the reception of an Abort.

Transmit Underrun/End of Message (D6)

Valid only in the COP or BOP mode, a 1 in bit D6 indicates that all transmit data has been transferred to the Tx shift register. CRC transmission, when the transmitter underruns, can be controlled by manipulating this bit.

If CRC transmission is desired when the transmitter underruns, bit D6 must be reset to 0 by the Reset Tx Underrun/EOM command bit (CR0 bits D7-D6 = 11). Before this command is issued, the transmitter must be enabled and at least one byte must have been transferred to the Tx buffer.

In the BOP mode, bit D6 is automatically reset to 0 when the first byte is transferred after transmission is enabled. A status change from 1 to 0 in this bit does not cause an E/S interrupt.

Clear To Send (D5)

Bit D5 indicates the inverted state of the $\overline{CTS}$ pin. Any change causes an interrupt.

Sync/Hunt (D4)

In the Asynchronous or External Sync mode, bit D4 indicates the inverted state of the $\overline{SYNC}$ pin.

In the internal sync COP or BOP mode, bit D4 indicates the AMPSC synchronization state. A 0 in bit D4 indicates that synchronization is established. A 1 indicates the AMPSC is in the Hunt Phase or the receiver is disabled.

Any change in state generates an interrupt.

Data Carrier Detect (D3)

Bit D3 indicates the inverted state of the $\overline{DCD}$ pin. Any change generates an interrupt.

All Sent (D2)

Valid only in the Asynchronous or BOP mode. Bit D2 set to 1 indicates that all the transmit data within the AMPSC has left the Tx shift register. The 1 to 0 state transition of this bit does not generate an interrupt.

Idle Detect (D1)

Bit D1 set to 1 indicates detection of the Idle state (15 or more consecutive 1s) in BOP mode. The 1 to 0 state transition of this bit does not generate an interrupt.

BRG Zero Count (D0)

Bit D0 set to 1 indicates that one of the BRGs has counted down to zero. Bits D4-D3 of SR3 determine which BRG counted out. The 1 to 0 state transition of this bit does not generate an interrupt.

STATUS REGISTER SR2S

This register indicates the value of the interrupt vector. It can only be read from the secondary channel. The value depends on the state of CR2M bit D6 (Interrupt Status Affects Vector bit). If bit D6 is 0, SR2S will always equal CR2S. If bit D6 is 1, the value of SR2S is modified by the cause of the highest priority interrupt source within the AMPSC.

The bits of SR2S that are affected depend on the Output Vector Type setting. Bits V3-V2 are affected for Type A vectors, and bits V1-V0 for Type B vectors. All other bits remain unchanged. Table 7 gives the value returned for the various types of interrupts.

Table 7. Vector Values in SR2S

V3, V1	V2, V0	Condition
0	0	Tx buffer empty
0	1	External/status
1	0	Rx data available
1	1	Special Rx condition

When interrupts are available in the Nonvectored mode (CR2A bit D7 = 0), SR2S is read in order to indicate to the

AMPSC that interrupt service has started. This clears the interrupt request (INT) and prevents lower priority interrupts from being generated until the End of Interrupt command (CR0) is issued.

STATUS REGISTER SR3

TxBRG Zero Count (D4)

Bit D4 is valid when TxBRG is enabled (CR14 bit D0 = 1). A 1 in bit D0 indicates that the TxBRG counted down to zero. This bit in conjunction with the SR1 bit D0 causes an External/Status interrupt and is latched on a transition from 0 to 1. The transition from 1 to 0 does not cause an interrupt.

RxBRG Zero Count (D3)

Bit D3 is valid when RxBRG is enabled (CR14 bit D1 = 1). A 1 in bit D3 indicates that the RxBRG counted down to zero. This bit functions in the same manner as bit D4.

Residue Code (D2-D0)

Valid only in the BOP mode, bits D2-D0 indicate the number of valid bits in the last data byte received in a frame. The meaning of these bits depends on the number of bits per data byte. The previous character refers to the last character read before the end of frame, and so on. See table 8. Figure 6 is an example of a residue code of 000 and a character length of 8 bits. It indicates that bits 0 and 1 in the last byte are valid.

Figure 6. Example of Valid Bits in the I-Field (Residue = 000)

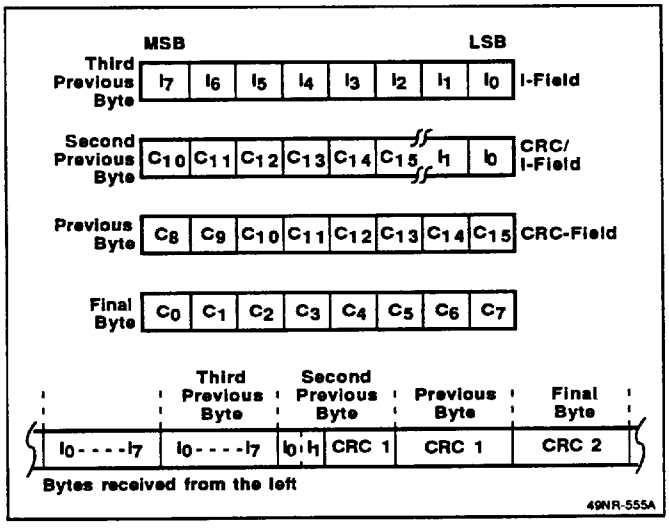


Table 8. Residue Codes

D2	D1	D0	Previous Character MSB							LSB	2nd Previous Character MSB							LSB
8 Bits per Character																		
0	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D
0	0	1	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D
0	1	0	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D
0	1	1*	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D
1	0	0	C	C	C	C	C	C	C	C	C	C	C	C	C	D	D	D
1	0	1	C	C	C	C	C	C	C	C	C	D	D	D	D	D	D	D
1	1	0	C	C	C	C	C	C	C	C	C	C	C	D	D	D	D	D
1	1	1	C	C	C	C	C	C	C	D	D	D	D	D	D	D	D	D
7 Bits per Character																		
0	0	0	X	C	C	C	C	C	C	D	X	D	D	D	D	D	D	D
0	0	1	X	C	C	C	C	C	C	C	X	C	C	D	D	D	D	D
0	1	0	X	C	C	C	C	C	C	C	X	C	C	C	C	D	D	D
0	1	1*	X	C	C	C	C	C	C	C	X	D	D	D	D	D	D	D
1	0	0	X	C	C	C	C	C	C	C	X	C	C	C	C	C	D	D
1	0	1	X	C	C	C	C	C	C	C	X	C	D	D	D	D	D	D
1	1	0	X	C	C	C	C	C	C	C	X	C	C	C	D	D	D	D
6 Bits per Character																		
0	0	0*	X	X	C	C	C	C	C	C	X	X	D	D	D	D	D	D
0	0	1	X	X	C	C	C	C	C	C	X	X	C	C	D	D	D	D
0	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	D	D
1	0	0	X	X	C	C	C	C	C	C	X	X	C	C	C	C	C	D
1	0	1	X	X	C	C	C	C	C	C	X	X	C	D	D	D	D	D
1	1	0	X	X	C	C	C	C	C	C	X	X	C	C	C	D	D	D
5 Bits per Character																		
0	0	0	X	X	X	C	C	C	C	C	X	X	X	C	D	D	D	D
0	0	1	X	X	X	C	C	C	C	C	X	X	X	C	C	D	D	D
0	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	D
1	0	0*	X	X	X	C	C	C	C	C	X	X	X	C	C	C	C	C
1	1	0	X	X	X	C	C	C	C	C	X	X	X	C	C	C	D	D

C = CRC bit
D = Valid data
X = Invalid
* = No residue (boundary of the last received data matches the boundary between one byte and the CRC).

STATUS REGISTER SR4

Each bit of this register indicates whether a corresponding cause of interrupt exists within the AMPSC. A bit is set to 1 when its matching interrupt is being serviced or if a lower-priority interrupt is pending during the servicing of a higher-priority interrupt. Otherwise, it is 0.

Bit	Description
D7	Special Rx Condition INT pending
D5	Rx INT pending
D4	Tx INT pending
D3	E/S INT pending

STATUS REGISTER SR8

Valid only in the BOP mode, bits D7-D0 of SR8 are the low-order byte of the Tx Data Length counter. Register SR8 is normally used to determine if frame transmission completed correctly. If the value of CR8/CR9 does not equal the value of SR8/SR9 when the transmitter underruns, the AMPSC automatically transmits an Abort. Registers SR8 and SR9 are cleared by a reset or when the TxDLC enable bit (CR13 bit D8) is set to 1.

STATUS REGISTER SR9

Valid only in the BOP mode, bits D7-D0 of SR9 are the high-order byte of the Tx Data Length counter. Registers SR8 and SR9 are used in conjunction with each other.

STATUS REGISTER SR10

One Clock Missing (D7)

This bit indicates whether a transition has been detected in the received data. It is valid when the FM data format is selected and the DPLL is in operation. With FM data format, a transition (rising or falling) must occur within one bit time at a bit boundary or center. The DPLL uses this transition as a reference for clock generation.

If no transitions occur, the DPLL clock generation may not operate properly. The DPLL detects transitions every 2 bits.

A 1 in bit D7 indicates no transition was detected in the received data. This bit is latched, and is reset by the Reset Missing Clock command (CR14 bits D7-D5 = 010) or the Enter Search command (CR14 bits D7-D5 = 001).

Two Clocks Missing (D6)

Bit D6 indicates that two consecutive transitions in the received data were missed.

Sending on Loop (D4)

Bit D4 set to 1 indicates that the AMPSC is in the SDLC Loop connection and is transmitting. It is valid only in the BOP mode when the SDLC Loop mode is selected (CR10 bits D4, D1 = 1).

Tx Sync/On Loop (D1)

Bit D1 is valid only in the COP or BOP mode. A 1 in bit D1 indicates the transmitter and receiver are synchronized (SYNC character detection on the receiver has been completed) and transmission is enabled for the device after both the Auto Tx on Sync and the bit D4 Enable bits (CR10 bits D4, D1) were set. This bit is also set to 0 when the Auto Tx on Sync bit (CR10 bit D4) or the D4 Enable bit (CR10 bit D1) is reset. A 0 in bit D1 indicates that the receiver is not synchronized with the transmitter.

In the BOP mode, a 1 in bit D1 indicates that a GA pattern was detected and a 1-bit delay was inserted between the RxD input and TxD output. Bit D1 remains a 1 during the time the SDLC Loop is formed.

When bit D1 is 0, the TxD and RxD lines are connected without the delay in Loop mode. Bit D1 is also 0 when the AMPSC is not in the Loop mode.

STATUS REGISTER SR11

This register directly indicates the value set in CR11 for interrupt enables. The host processor can use SR11 to read the interrupt enable states for the various interrupt sources within the AMPSC.

STATUS REGISTERS SR12-SR13

Register SR12 indicates the lower 8 bits (bits 7-0) of the value set in the Rx BRG.

Register SR13 indicates the upper 8 bits (bits 15-8) of the value set in the Rx BRG.

STATUS REGISTERS SR14-SR15

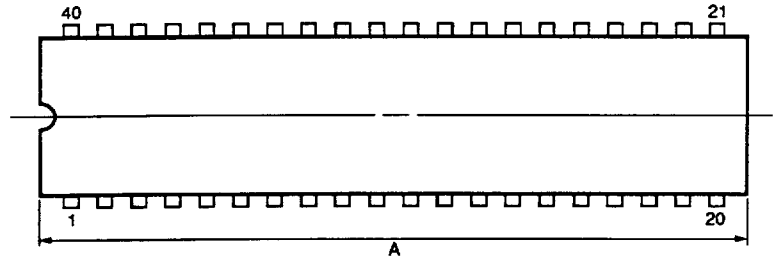
Register SR14 indicates the lower 8 bits (bits 7-0) of the value set in the Tx BRG.

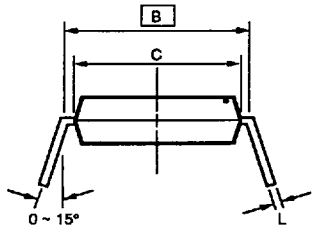
Register SR15 indicates the upper 8 bits (bits 15-8) of the value set in the Tx BRG.

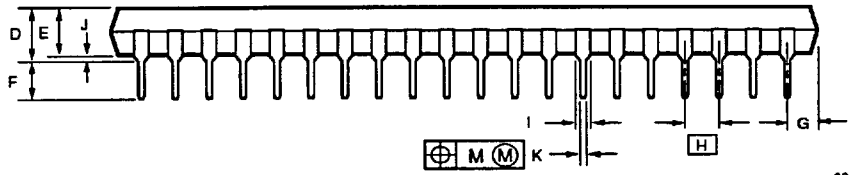
PACKAGE DRAWINGS

40-Pin Plastic DIP

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	15.24 [TP]	.600 [TP]
C	13.2	.520
D	5.72 max	.225 max
E	4.31 max	.170 max
F	3.6 ±0.3	.142 ±.012
G	2.54 max	.100 max
H	2.54 [TP]	.100 [TP]
I	1.2 min	.047 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	$0.25\ ^{+0.10}_{-0.05}$	$.010\ ^{+.004}_{-.002}$
M	0.25	.010





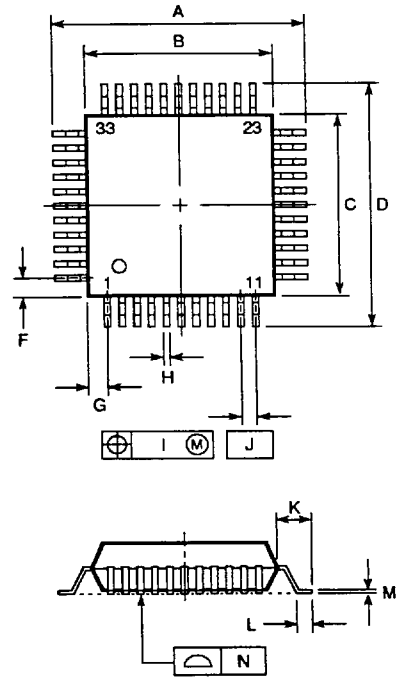


P40C-100-600A

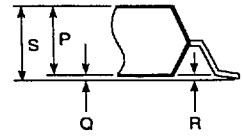
83vO-6140B (6/89)

44-Pin Plastic QFP

Item	Millimeters	Inches
A	13.6 ±0.4	.535 $^{+.017}_{-.016}$
B	10.0 ±0.2	.394 $^{+.008}_{-.009}$
C	10.0 ±0.2	.394 $^{+.008}_{-.009}$
D	13.6 ±0.4	.535 $^{+.017}_{-.016}$
F	1.0	.039
G	1.0	.039
H	0.35 ±0.10	.014 $^{+.004}_{-.005}$
I	0.15	.006
J	0.8 (TP)	.031 (TP)
K	1.8 ±0.2	.071 $^{+.008}_{-.009}$
L	0.8 ±0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ±0.1	.004 ±.004
R	0.1 ±0.1	.004 ±.004
S	3.0 max	.119 max



Enlarged detail of lead end

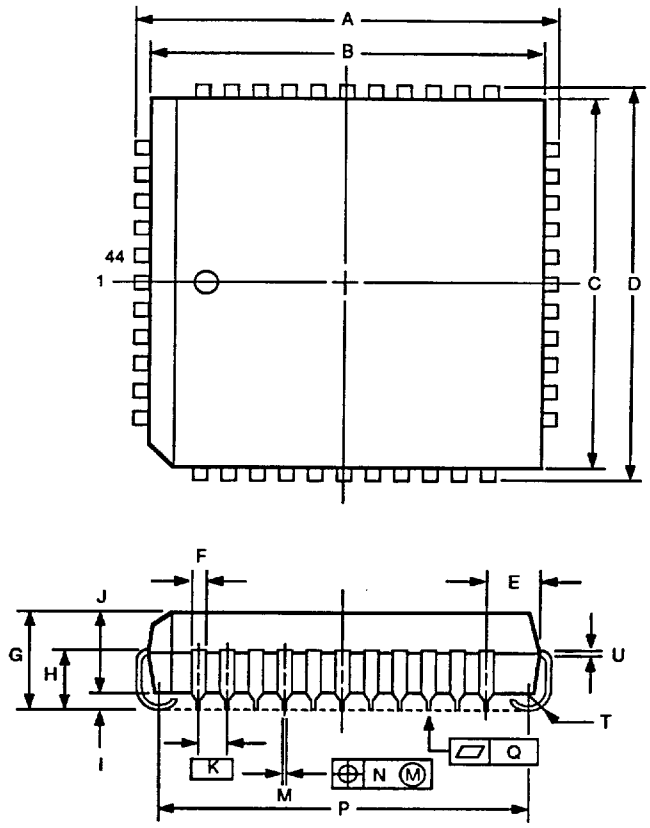


P44GB-80-3B4

49NR-556B (7/89)

44-Pin Plastic Leaded Chip Carrier (PLCC)

Item	Millimeters	Inches
A	17.5 ±0.2	.689 ±.008
B	16.58	.653
C	16.58	.653
D	17.5 ±0.2	.689 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	15.50 ±0.20	.610 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$



P44L-50A1

6/89 83YL-5804B

NEC

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