

### Description

The  $\mu$ PD7507 and  $\mu$ PD7508 4-bit, single-chip CMOS microcomputers have the  $\mu$ PD7500 series architecture. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Thirty-two I/O lines are organized into eight 4-bit ports: input port/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, 6, and 7.

The  $\mu$ PD7507 and  $\mu$ PD7508 execute 92 instructions of the  $\mu$ PD7500 series A instruction set with a 5- $\mu$ s instruction cycle time.

Maximum power consumption is 900  $\mu$ A at 5 V, less in the HALT and STOP low-power modes.

The  $\mu$ PD75CG08E is a piggyback EPROM prototyping chip that is pin-compatible with  $\mu$ PD7507 and  $\mu$ PD7508. A 2716 inserted into the top of the  $\mu$ PD75CG08E emulates the  $\mu$ PD7507's ROM. A 2732 emulates the  $\mu$ PD7508's ROM. When emulating the  $\mu$ PD7507, the user must take care to use only the first 128 RAM locations. Although the  $\mu$ PD7507 and  $\mu$ PD7508 can operate over a range of 2.5 to 6.0 V,  $\mu$ PD75CG08E operation is limited to 5 V  $\pm$ 10%.

Table 1 summarizes the differences among  $\mu$ PD7507,  $\mu$ PD7508 and  $\mu$ PD75CG08E.

**Table 1. Features Comparison**

	$\mu$ PD75CG08E	$\mu$ PD7507/7508
Program memory	2K x 8 EPROM (2716) 4K x 8 EPROM (2732)	2K x 8 masked ROM (7507) 4K x 8 masked ROM (7508)
Data memory	224 x 4	128 x 4 (7507) 224 x 4 (7508)
Data retention mode	No	Yes
Power supply	5 V $\pm$ 10%	2.7 to 6.0 V
Package types	40-pin ceramic piggyback DIP	40-pin plastic DIP 40-pin plastic shrink DIP 52-pin plastic QFP

### Features

- Single chip microcomputer
- Program ROM
  - $\mu$ PD7507: 2048 x 8-bit
  - $\mu$ PD7508: 4096 x 8-bit
  - $\mu$ PD75CG08: piggyback EPROM
- Data RAM
  - $\mu$ PD7507: 128 x 4-bit
  - $\mu$ PD7508: 224 x 4-bit
  - $\mu$ PD75CG08: 224 x 4-bit
- 8-bit timer/event counter
- Four 4-bit general purpose registers
- Four vectored, prioritized interrupts
- Executes 92 instructions of  $\mu$ PD7500 series A instruction set
- 5  $\mu$ s instruction cycle/400 kHz external clock
- Two standby modes
- 32 I/O lines
- Low-power HALT and STOP modes

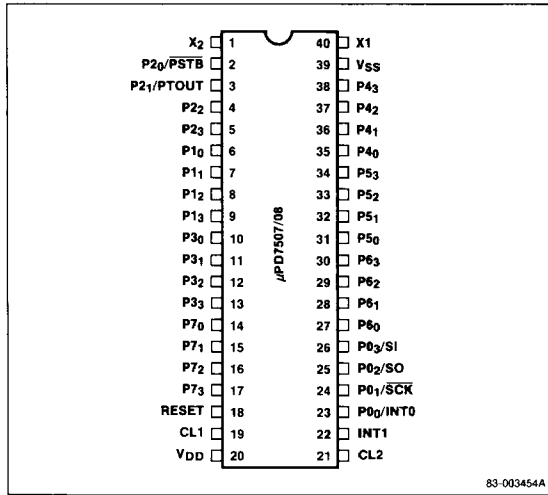
### Ordering Information

*Part Number	Package Type	Max Frequency of Operation
$\mu$ PD7507C	40-pin plastic DIP	410 kHz
$\mu$ PD7507CU	40-pin plastic shrink DIP	410 kHz
$\mu$ PD7507GC-00	52-pin plastic QFP	410 kHz
$\mu$ PD7508C	40-pin plastic DIP	410 kHz
$\mu$ PD7508CU	40-pin plastic shrink DIP	410 kHz
$\mu$ PD7508GC-00	52-pin plastic QFP	410 kHz
$\mu$ PD75CG08E	40-pin ceramic piggyback DIP	410 kHz

\* A 3-digit mask identification code is added to the part number by NEC at the time of code verification.

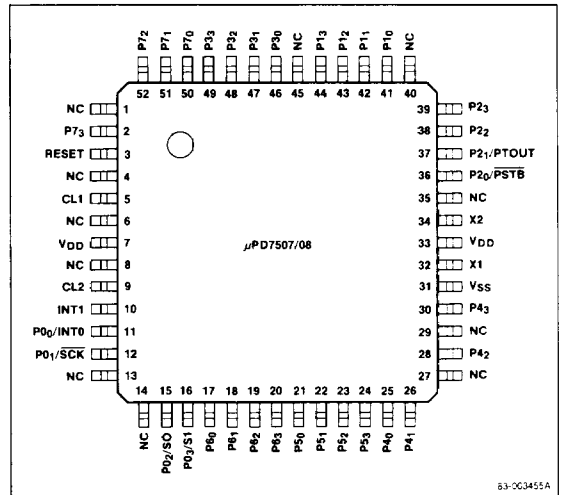
### Pin Configurations

#### 40-Pin Plastic DIP and Plastic Shrink DIP



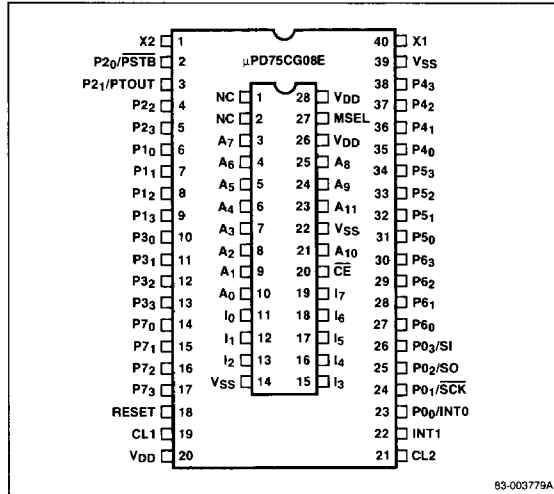
83-003454A

#### 52-Pin Plastic QFP



83-003455A

#### 40-Pin Ceramic Piggyback DIP



83-003779A

### Pin Identification

#### 40-Pin DIP, Shrink DIP and Piggyback DIP

No.	Symbol	Function
1, 40	X2, X1	Crystal clock/external event input port
2-5	P20/PSTB, P21/PTOUT, P22, P23	Output port 2/output strobe pulse, timer out F/F signal
6-9	P10-P13	I/O port 1
10-13	P30-P33	Output port 3
14-17	P70-P73	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	VDD	Positive power supply
22	INT1	External interrupt
23-26	P00/INT0, P01/SCK, P02/SO, P03/SI	Input port 0/external interrupt, serial I/O interface
27-30	P60-P63	I/O port 6
31-34	P50-P53	I/O port 5
35-38	P43-P40	I/O port 4
39	VSS	Ground

## Pin Identification (cont)

### 28-Pin EPROM Socket on Piggyback DIP

No.	Symbol	Function
1, 2	NC	Not connected
3-10	A <sub>7</sub> -A <sub>0</sub>	Address bits 7-0
11-13	I <sub>0</sub> -I <sub>2</sub>	Data bits 0-2
14, 22	V <sub>SS</sub>	Ground
15-19	I <sub>3</sub> -I <sub>7</sub>	Data bits 3-7
20	$\overline{CE}$	Chip enable
21, 23	A <sub>10</sub> -A <sub>11</sub>	Address bits 10, 11
24, 25	A <sub>9</sub> , A <sub>8</sub>	Address bits 9, 8
26, 28	V <sub>DD</sub>	Positive power supply
27	MSEL	Memory select

### 52-Pin QFP

No.	Symbol	Function
1, 4, 6, 8, 13, 14, 27, 29, 35, 40, 45	NC	Not connected
2, 50-52	P <sub>70</sub> -P <sub>73</sub>	I/O port 7
3	RESET	RESET input
5, 9	CL1, CL2	System clock inputs
7	V <sub>DD</sub>	Positive power supply
10	INT1	External interrupt
11, 12, 15, 16	P <sub>00</sub> /INT <sub>0</sub> , P <sub>01</sub> /SCK, P <sub>02</sub> /SO, P <sub>03</sub> /SI	Input port 0/external interrupt, serial I/O interface
17-20	P <sub>60</sub> -P <sub>63</sub>	I/O port 6
21-24	P <sub>50</sub> -P <sub>53</sub>	I/O port 5
25, 26 28, 30	P <sub>43</sub> -P <sub>40</sub>	I/O port 4
31	V <sub>SS</sub>	Ground
32, 34	X1, X2	Crystal clock/external event input
33	V <sub>DD</sub>	Positive power supply
36-39	P <sub>20</sub> /PSTB, P <sub>21</sub> /PTOUT, P <sub>22</sub> , P <sub>23</sub>	4-bit output port 2/output strobe pulse, timer out F/F signal
41-44	P <sub>10</sub> -P <sub>13</sub>	I/O port 1
46-49	P <sub>30</sub> -P <sub>33</sub>	Output port 3

## Pin Functions

### P<sub>00</sub>/INT<sub>0</sub>, P<sub>01</sub>/SCK, P<sub>02</sub>/SO, P<sub>03</sub>/SI [Port 0/ External Interrupt, Serial Interface]

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO (active low), and the serial clock SCK (active low), used for synchronizing data transfer, make up the 8-bit serial I/O interface. Line P<sub>00</sub> is always shared with external interrupt INT<sub>0</sub>, a rising edge-triggered interrupt. If P<sub>00</sub>/INT<sub>0</sub> is unused, it should be connected to V<sub>SS</sub>. If P<sub>01</sub>/SCK, P<sub>02</sub>/SO, or P<sub>03</sub>/SI are unused, connect them to V<sub>SS</sub> or V<sub>DD</sub>.

### P<sub>10</sub>-P<sub>13</sub> [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a P<sub>20</sub>/PSTB pulse. Connect unused pins to V<sub>SS</sub> or V<sub>DD</sub>.

### P<sub>20</sub>/PSTB, P<sub>21</sub>/PTOUT, P<sub>22</sub>, P<sub>23</sub> [Port 2]

4-bit latched three-state output port. Line P<sub>20</sub> is shared with PSTB, the port 1 output strobe pulse. Line P<sub>21</sub> is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

### P<sub>30</sub>-P<sub>33</sub> [Port 3]

4-bit latched three-state output port. Leave unused pins open.

### P<sub>40</sub>-P<sub>43</sub> [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V<sub>DD</sub> or GND. In output mode, leave unused pins open.

### P<sub>53</sub>-P<sub>50</sub> [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V<sub>SS</sub> or V<sub>DD</sub>. In output mode, leave unused pins open.

### P<sub>63</sub>-P<sub>60</sub> [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V<sub>SS</sub> or V<sub>DD</sub>. In output mode, leave unused pins open.

### P70-P73 [Port 7]

4-bit input/latched three state output port. In input mode, connect unused pins to V<sub>SS</sub> or V<sub>DD</sub>. In output mode, leave unused pins open.

### X2, X1 [Crystal Clock/External Event Input]

Connect a crystal oscillator circuit to input X1 and output X2 for crystal clock operation. Alternatively, connect external event pulses to input X1 and leave output X2 open for external event counting. If X1 is not used, connect it to ground. If X2 is not used, leave it open.

### CL1, CL2 [System Clock Input]

Connect a 82 kΩ resistor across CL1 and CL2, and connect a 33 pF capacitor from CL1 to V<sub>SS</sub>. Alternatively, connect an external clock source to CL1 and leave CL2 open.

### RESET [Reset]

A high level input to this pin initializes the μPD7507/08 after power up.

### INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V<sub>SS</sub> if unused.

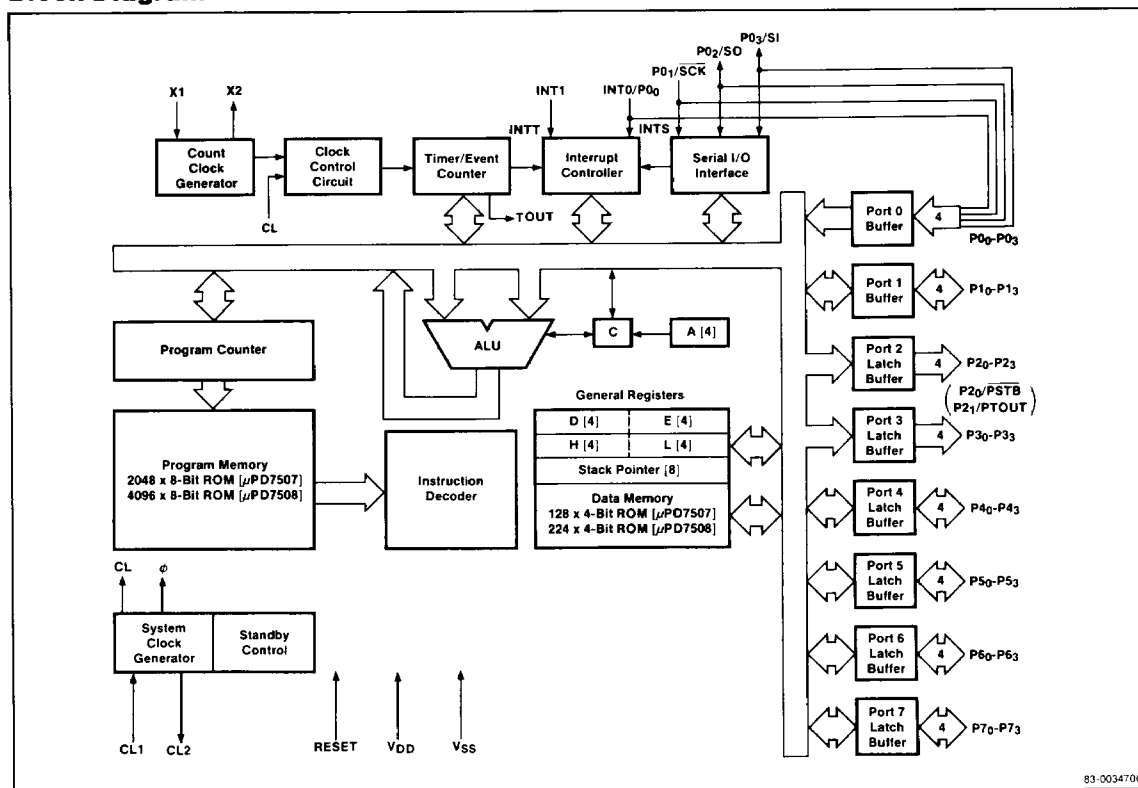
### VDD [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

### VSS [Ground]

Ground.

## Block Diagram

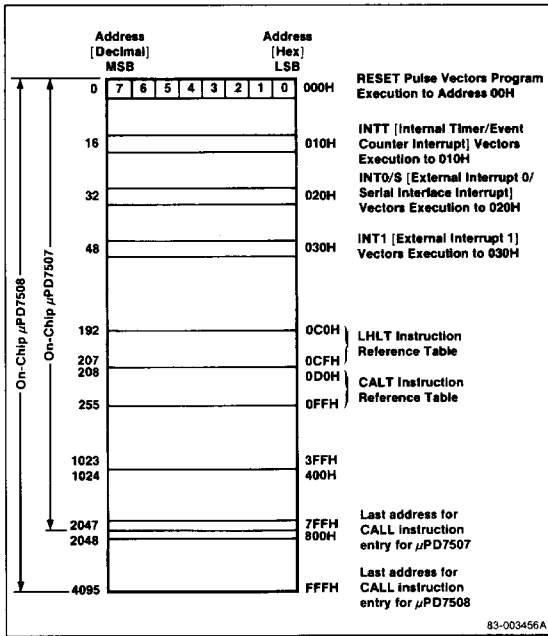


83-003470C

## Memory Map

Figure 1 shows the ROM memory map of the μPD7507/08.

Figure 1. ROM Map



## Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM<sub>1</sub> and CM<sub>2</sub>), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and count clock generator circuit (X). It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter. Figure 2 shows the clock control circuit.

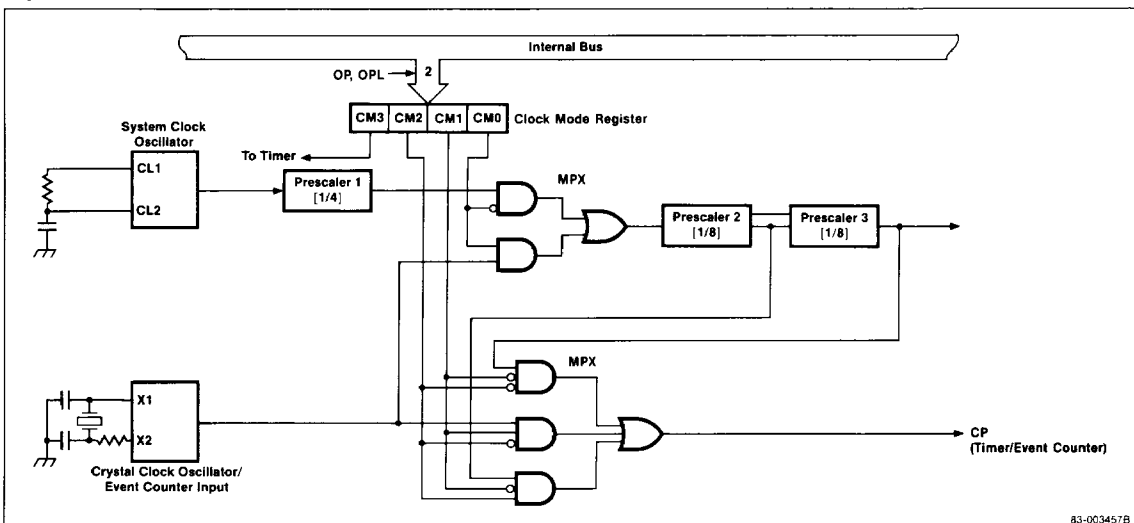
Table 2 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency.

Table 2. Selecting the Count Pulse Frequency

CM <sub>2</sub>	CM <sub>1</sub>	CM <sub>0</sub>	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM <sub>3</sub>	TOUT Signal
0	Disabled
1	Enabled

Figure 2. Clock Control Circuit



**Timer/Event Counter**

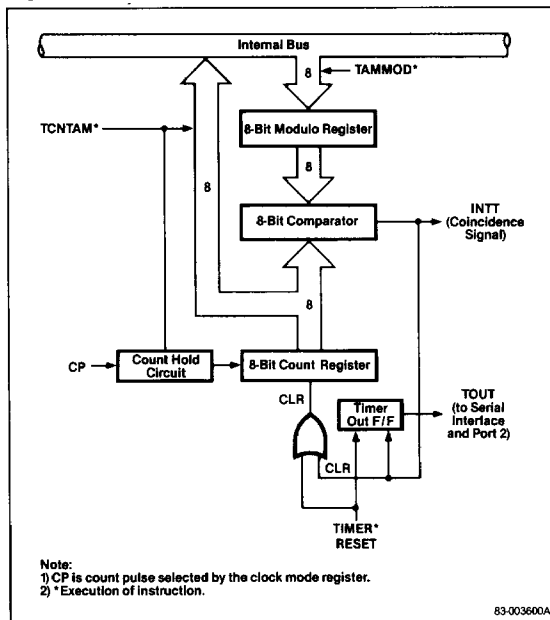
The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip-flop as shown in figure 3.

The 8-bit count register is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and the modulo register and outputs an INTT when they are equal.

**Figure 3. Timer/Event Counter**

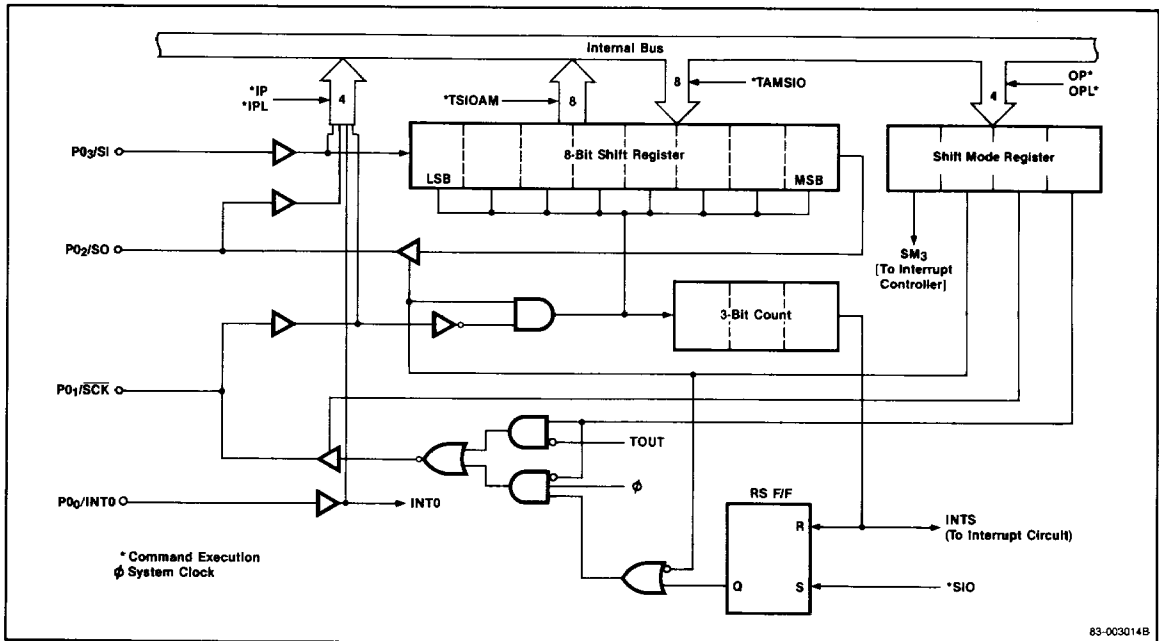


## Serial Interface

The 8-bit serial interface allows the μPD7507/08 to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or micro-computers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit SCK pulse counter, the SI input port, the SO output port, the SCK serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

**Figure 4. Serial Interface**



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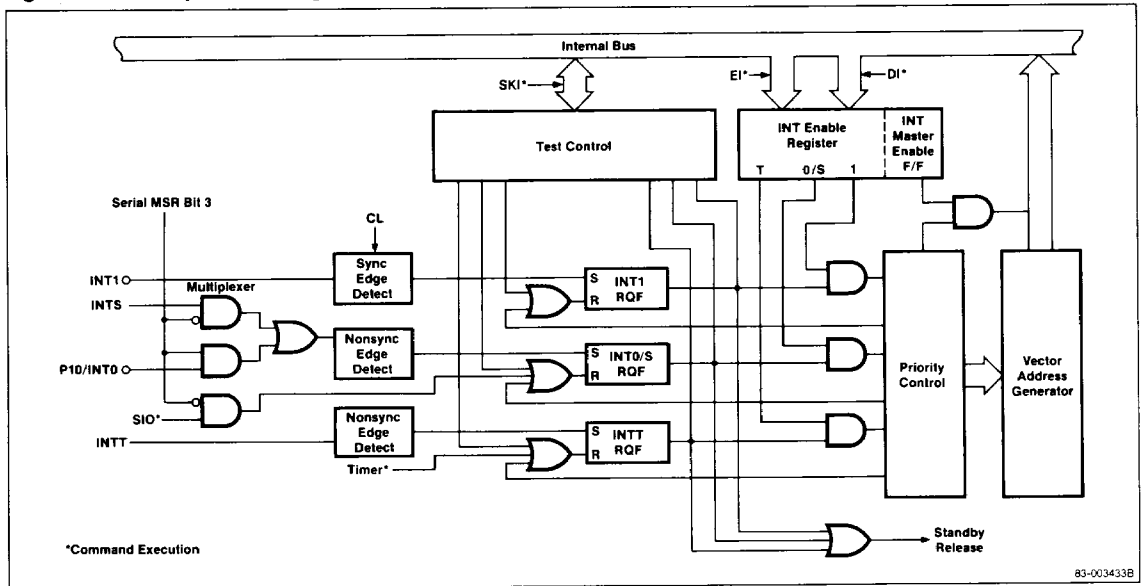
### Interrupts

The μPD7507/08 has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 3 is a summary of the four interrupts. Figure 5 is the block diagram.

**Table 3. μPD7507/08 Interrupts**

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

**Figure 5. Interrupt Block Diagram**





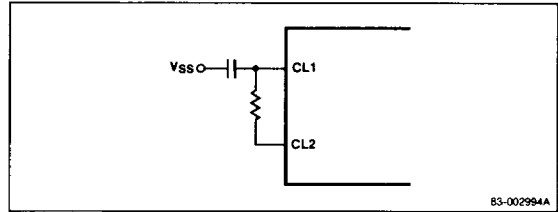
## System Clock and Timing Circuitry

Timing for the μPD7507/08 is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase shift required for oscillation. Figure 6 shows the connection for an RC circuit. Figure 7 shows the connection for an external clock source.

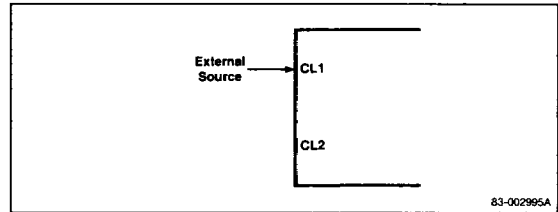
The internal oscillator generates a frequency in the range 60 kHz to 300 kHz depending on the frequency reference. For example, at  $V_{DD} = 5\text{ V}$ , an 82-kΩ resistor and a 33-pF capacitor generate a frequency of 200 kHz. The oscillation frequency is fed to the clock control circuit. It is divided by two and the resulting signal is fed to the CPU and serial interface as shown in figure 8.

Table 4 shows the operating status of the various logic blocks under the three power down-modes.

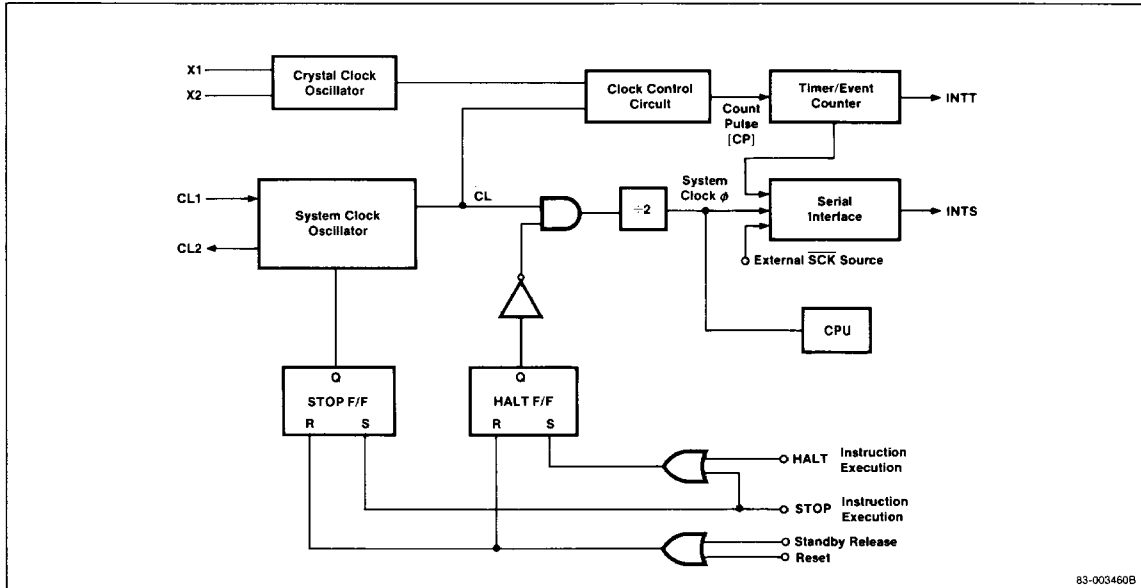
**Figure 6. RC Circuit Connection**



**Figure 7. External Clock Source Connection**



**Figure 8. System Clock Circuitry**



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**Table 4. Power-Down Operating Status**

Logic Block	Power-Down Mode		Data Retention Mode
	HALT	STOP	
System clock	(Note 1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(Note 3)	Disabled
Serial interface	(Note 2)	(Note 2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(Note 4)

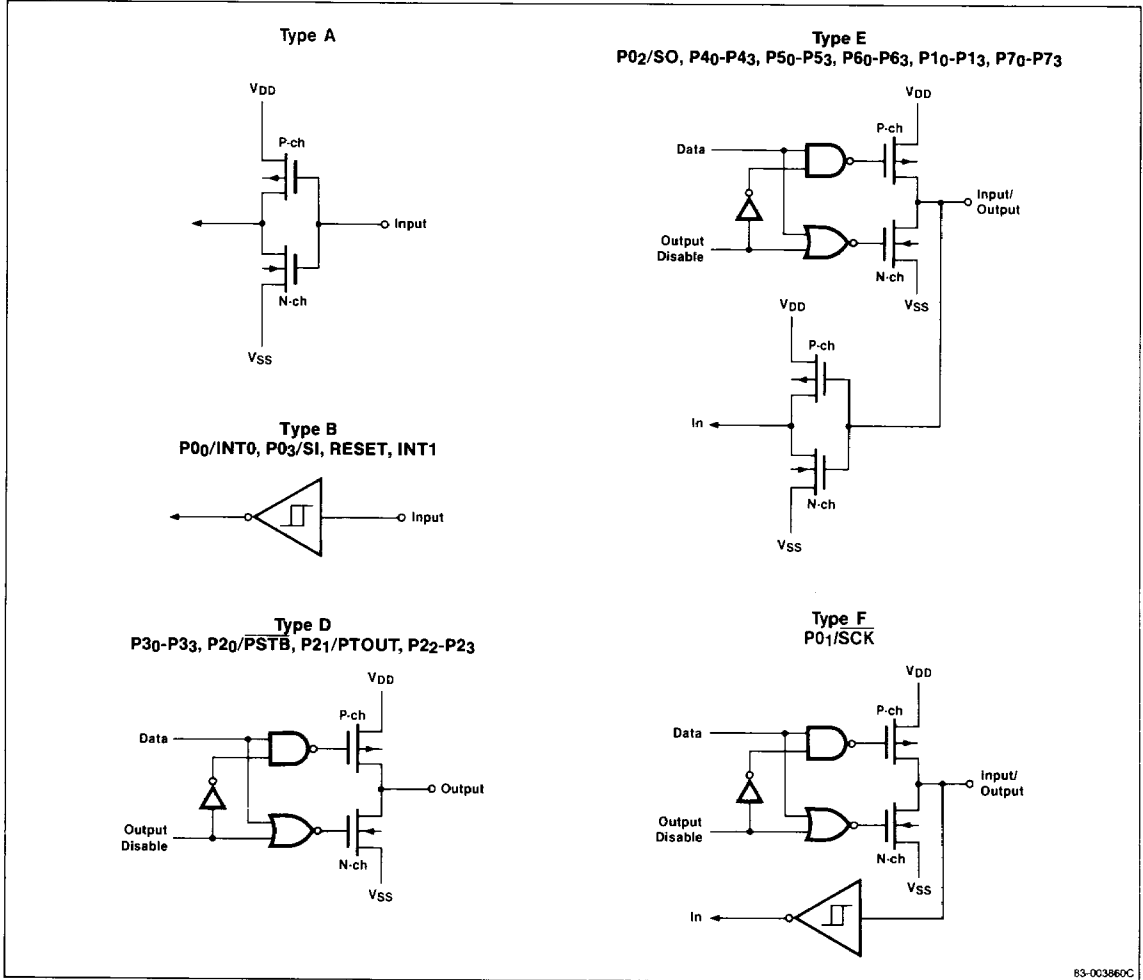
**Note:**

- (1) Supplied to timer/event counter but not to CPU or serial interface.
- (2) Can function normally if the serial MSR is set to get the  $\overline{SCK}$  signal externally or from the TOUT signal.
- (3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.
- (4) To enter the data retention mode, raise RESET while  $V_{DD}$  is lowered. To end the data retention mode, raise RESET when  $V_{DD}$  is raised, then lower it. INTT, INT0, INTS or RESET releases the STOP mode. RESET or any interrupt releases the HALT mode.

## I/O Port Interfaces

Figure 9 shows the internal circuit configurations at the I/O ports.

**Figure 9. Interface at Input/Output Ports**



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### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$

Operating temperature, $T_{\text{OPT}}$	-10 to +70°C
Storage temperature, $T_{\text{STG}}$	-65 to +150°C
Power supply voltage, $V_{\text{DD}}$	-0.3 to +7.0 V
All input and output voltages	-0.3 to $V_{\text{DD}} + 0.3$ V
Output current high, $I_{\text{OH}}$	
One pin	-17 mA
All pins, total	-30 mA
Output current low, $I_{\text{OL}}$	
One pin	17 mA
Ports 1, 2, 3, 7	25 mA
Ports 4, 5, 6	25 mA

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### DC Characteristics 1

For  $V_{\text{DD}} = 2.5$  to  $3.3$  V (7507, 7508 only)

$T_A = -10$  to  $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage, high	$V_{\text{IH1}}$	$0.8 V_{\text{DD}}$		$V_{\text{DD}}$	V	Except CL1, X1
	$V_{\text{IH2}}$	$V_{\text{DD}} - 0.3$		$V_{\text{DD}}$	V	CL1, X1
	$V_{\text{IHDR}}$	$0.9 V_{\text{DDDR}}$		$V_{\text{DDDR}} + 0.2$	V	RESET, data retention mode
Input voltage, low	$V_{\text{IL1}}$	0		$0.2 V_{\text{DD}}$	V	Except CL1, X1
	$V_{\text{IL2}}$	0		0.3	V	CL1, X1
Output voltage, high	$V_{\text{OH}}$	$V_{\text{DD}} - 0.5$			V	$I_{\text{OH}} = -80 \mu\text{A}$
Output voltage, low	$V_{\text{OL}}$			0.5	V	$I_{\text{OL}} = 350 \mu\text{A}$
Input leakage current, high	$I_{\text{LIH1}}$			3	$\mu\text{A}$	Except CL1, X1; $V_i = V_{\text{DD}}$
	$I_{\text{LIH2}}$			10	$\mu\text{A}$	CL1, X1
Input leakage current, low	$I_{\text{LIL1}}$			-3	$\mu\text{A}$	Except CL1, X1; $V_i = 0$ V
	$I_{\text{LIL2}}$			-10	$\mu\text{A}$	CL1, X1
Output leakage current, high	$I_{\text{LOH}}$			3	$\mu\text{A}$	$V_0 = V_{\text{DD}}$
Output leakage current, low	$I_{\text{LOL}}$			-3	$\mu\text{A}$	$V_0 = 0$ V
Supply voltage	$V_{\text{DDDR}}$	2.0			V	Data retention mode
Supply current	$I_{\text{DD1}}$		50	250	$\mu\text{A}$	Normal operation, $V_{\text{DD}} = 3$ V $\pm 10\%$ ; $R = 240$ k $\Omega$ $\pm 2\%$ , $C = 33$ pF $\pm 5\%$
			35	230	$\mu\text{A}$	Normal operation, $V_{\text{DD}} = 2.5$ V; $R = 240$ k $\Omega$ $\pm 2\%$ , $C = 33$ pF $\pm 5\%$
	$I_{\text{DD2}}$		0.3	10	$\mu\text{A}$	Stop mode, $X1 = 0$ V; $V_{\text{DD}} = 3$ V $\pm 10\%$
			0.2	10	$\mu\text{A}$	Stop mode, $X1 = 0$ V; $V_{\text{DD}} = 2.5$ V
	$I_{\text{DDDR}}$		0.2	10	$\mu\text{A}$	Data retention mode, $V_{\text{DDDR}} = 2.0$ V

### Capacitance

$T_A = 25^\circ\text{C}$ ,  $V_{\text{DD}} = 0$  V

Parameter	Symbol	Limits		Unit	Test Conditions
		Typ	Max		
Input capacitance	$C_i$		15	pF	$f = 1$ MHz;
Output capacitance	$C_o$		15	pF	unmeasured pins returned to $V_{\text{SS}}$
I/O capacitance	$C_{\text{IO}}$		15	pF	

## DC Characteristics 2 *1.6473*

For  $V_{DD} = 2.7$  to  $6.0$  V (75CG08E, 5 V  $\pm 10\%$ )

$T_A = -10$  to  $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input voltage, high	$V_{IH1}$	$0.7 V_{DD}$		$V_{DD}$	V	Except CL1, X1
	$V_{IH2}$	$V_{DD} - 0.5$		$V_{DD}$	V	CL1, X1
	$V_{IHDR}$	$0.9 V_{DDDR}$		$V_{DDDR} + 0.2$	V	RESET, data retention mode, 7507/08 only
Input voltage, low	$V_{IL1}$	0		$0.3 V_{DD}$	V	Except CL1, X1
	$V_{IL2}$	0		0.5	V	CL1, X1
Output voltage, high	$V_{OH}$	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only
		$V_{DD} - 0.5$			V	$I_{OH} = -100$ $\mu\text{A}$ , 7507/08 only
	$V_{OH1}$	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA, 75CG08E only
	$V_{OH2}$	$V_{DD} - 0.75$			V	$I_{OH} = -5.0$ mA, 75CG08E only
Output voltage, low	$V_{OL}$			0.4	V	$I_{OL} = 1.6$ mA; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only
				0.5	V	$I_{OL} = 400$ $\mu\text{A}$ , 7507/08 only
				0.4	V	$I_{OL} = -1.6$ mA, 75CG08E only
Input current, high	$I_{IH}$			300	$\mu\text{A}$	75CG08E only, $V_I = V_{DD}$ , MSEL
Input current, low	$I_{IL}$			-200	$\mu\text{A}$	75CG08E only, $V_I = 0$ V, $I_0$ -17
Input leakage current, high	$I_{LIH1}$			3	$\mu\text{A}$	Except CL1, X1; $V_I = V_{DD}$
	$I_{LIH2}$			10	$\mu\text{A}$	CL1, X1
Input leakage current, low	$I_{LIL1}$			-3	$\mu\text{A}$	Except CL1, X1; $V_I = 0$ V
	$I_{LIL2}$			-10	$\mu\text{A}$	CL1, X1
Output leakage current, high	$I_{LOH}$			3	$\mu\text{A}$	$V_O = V_{DD}$
Output leakage current, low	$I_{LOL}$			-3	$\mu\text{A}$	$V_O = 0$ V
Supply voltage	$V_{DDDR}$	2.0			V	Data retention mode, 7507/08 only
Supply current	$I_{DD1}$		300	900	$\mu\text{A}$	Normal operation, $V_{DD} = 5$ V $\pm 10\%$ ; $R = 82$ k $\Omega$ $\pm 2\%$ , $C = 33$ pF $\pm 5\%$
			70	300	$\mu\text{A}$	Normal operation, $V_{DD} = 3$ V $\pm 10\%$ ; $R = 160$ k $\Omega$ $\pm 2\%$ , $C = 33$ pF $\pm 5\%$ , 7507/08 only
	$I_{DD2}$		1.0	20	$\mu\text{A}$	Stop mode, $X1 = 0$ V; $V_{DD} = 5$ V $\pm 10\%$ , 7507/08 only
			0.3	10	$\mu\text{A}$	Stop mode, $X1 = 0$ V; $V_{DD} = 3$ V $\pm 10\%$ , 7507/08 only
			2	20	$\mu\text{A}$	Stop mode, $X1 = 0$ V; $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
	$I_{DDDR}$		0.2	10	$\mu\text{A}$	Data retention mode $V_{DDDR} = 2.0$ V, 7507/08 only

**AC Characteristics 1**

For  $V_{DD} = 2.7$  to  $6.0$  V (75CG08, 5 V  $\pm 10\%$ )

$T_A = -10$  to  $+70$  °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
System clock frequency	$f_{CC}$	150	200	240	kHz	$V_{DD} = 5.0$ V $\pm 10\%$ ; R = 82 k $\Omega$ $\pm 2\%$ (Note 1)
		75	100	120	kHz	$V_{DD} = 3.0$ $\pm 10\%$ ; R = 160 k $\Omega$ $\pm 2\%$ (Note 1), 7507/08 only
		75		135	kHz	$V_{DD} = 3.0$ $\pm 10\%$ ; R = 160 k $\Omega$ $\pm 2\%$ (Note 1), 7507/08 only
	$f_C$	10		410	kHz	CL1, external clock, 50% duty; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only, $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
		10		125	kHz	CL1, external clock, 50% duty; $V_{DD} = 2.7$ V, 7507/08 only
		10		300	kHz	CL1, external clock, 50% duty; 75CG08E only
System clock rise and fall times	$t_{CR}, t_{CF}$			0.2	$\mu$ s	CL1, external clock
System clock pulse width	$t_{CH}, t_{CL}$	1.2		50	$\mu$ s	CL1, external clock; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only
		4.0		50	$\mu$ s	CL1, external clock; $V_{DD} = 2.7$ V, 7507/08 only
		1.5		50	$\mu$ s	CL1, external clock, 75CG08E only
		1.2		50	$\mu$ s	CL1, external clock; $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
Counter clock frequency	$f_{XX}$	25	32	50	kHz	X1, X2, crystal oscillator
		$f_X$	0		410	kHz
		0		125	kHz	X1, external pulse input, 50% duty; $V_{DD} = 2.7$ V, 7507/08 only
		0		300	kHz	X1, external pulse input; 50% duty, 75CG08 only
		0		410	kHz	X1, external pulse input; 50% duty; $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
Counter clock rise and fall times	$t_{XR}, t_{XF}$			0.2	$\mu$ s	X1, external pulse input
Counter clock pulse width	$t_{XH}, t_{XL}$	1.2			$\mu$ s	X1, external pulse input; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only
		4.0			$\mu$ s	X1, external pulse input; $V_{DD} = 2.7$ V, 7507/08 only
		1.5			$\mu$ s	X1, external pulse input, 75CG08E only
		1.2			$\mu$ s	X1, external pulse input; $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
SCK cycle time	$t_{KCY}$	3.0			$\mu$ s	SCK as input; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
		8.0			$\mu$ s	SCK as input, 7507/08 only
		4.9			$\mu$ s	SCK as output; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
		16.0			$\mu$ s	SCK as output, 7507/08 only
		4.0			$\mu$ s	SCK as input, 75CG08E only
		6.7			$\mu$ s	SCK as output, 75CG08E only
SCK pulse width	$t_{KH}, t_{KL}$	1.3			$\mu$ s	SCK as input; $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 5\%$ , 75CG08E only
		4.0			$\mu$ s	SCK as input

## AC Characteristics 1 (cont)

For  $V_{DD} = 2.7$  to  $6.0$  V (75CG08, 5 V  $\pm 10\%$ )

$T_A = -10$  to  $+70^\circ\text{C}$

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
SCK pulse width	$t_{KH}, t_{KL}$	2.2			$\mu\text{s}$	SCK as output, $V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
		8.0			$\mu\text{s}$	SCK as output, 7507/08 only
		1.8			$\mu\text{s}$	SCK input, 75CG08E only
		3.0			$\mu\text{s}$	SCK as output, 75CG08E only
SI setup time to $\overline{\text{SCK}} \uparrow$	$t_{SIK}$	300			ns	
SI hold time after $\overline{\text{SCK}} \uparrow$	$t_{KSI}$	450			ns	
SO delay time after $\overline{\text{SCK}} \downarrow$	$t_{KSO}$			850	ns	$V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
				1200	ns	7507/08 only
Port 1 output setup time to $\overline{\text{PSTB}} \uparrow$	$t_{PST}$	(Note 2)			$\mu\text{s}$	$V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
		(Note 3)			$\mu\text{s}$	7507/08 only
Port 1 output setup time to $\overline{\text{PSTB}} \uparrow$	$t_{STP}$	100			ns	$V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
		100			ns	7507/08 only
$\overline{\text{PSTB}}$ pulse width	$t_{STL}$	(Note 2)			$\mu\text{s}$	$V_{DD} = 4.5$ to $6.0$ V, 7507/08 only $V_{DD} = 5$ V $\pm 10\%$ , 75CG08E only
		(Note 3)			$\mu\text{s}$	7507/08 only
INT0 pulse width	$t_{I0H}, t_{I0L}$	10			$\mu\text{s}$	
INT1 pulse width	$t_{I1H}, t_{I1L}$			$2/f_{CC}$ or $2/f_C$	$\mu\text{s}$	
RESET pulse width	$t_{RSH}, t_{RSL}$	10			$\mu\text{s}$	
RESET setup time	$t_{SRS}$	0			ns	7507/08 only
RESET hold time	$t_{HRS}$	0			ns	7007/08 only

### Note:

(1) RC network at CL1 and CL2;  $C = 33$  pF  $\pm 5\%$ ,  $|\Delta C/^\circ\text{C}| \leq 60$  ppm.

(2)  $(10^3) \div 2(f_{CC}$  or  $f_C$  in kHz) - 0.8  $\mu\text{s}$ .

(3)  $(10^3) \div 2(f_{CC}$  or  $f_C$  in kHz) - 2.0  $\mu\text{s}$ .

3

### AC Characteristics 2

For  $V_{DD} = 2.5$  to  $3.3$  V (7507, 7508 only)

$T_A = -10$  to  $+70$  °C

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
System clock frequency	$f_{CC}$	50		80	kHz	R = 240 kΩ ±2% (Note 1)
		50	64	77		$V_{DD} = 2.5$ V; R = 240 kΩ ±2% (Note 1)
	$f_C$	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	$t_{CR}, t_{CF}$			0.2	μs	CL1, external clock
System clock pulse width	$t_{CH}, t_{CL}$	6.25		50	μs	CL1, external clock
Counter clock frequency	$f_{XX}$	25	32	50	kHz	X1, X2, crystal oscillator
	$f_X$	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	$t_{XR}, t_{XF}$			0.2	μs	X1, external pulse input
Counter clock pulse width	$t_{XH}, t_{XL}$	6.25			μs	X1, external pulse input
SCK cycle time	$t_{KCY}$	12.5			μs	SCK as input
		25.0			μs	SCK as output
SCK pulse width	$t_{KH}, t_{KL}$	6.25			μs	SCK as input
		11.5			μs	SCK as output
SI setup time to SCK ↑	$t_{SIK}$	1			μs	
SI hold time after SCK ↑	$t_{KSI}$	1			μs	
SO delay time after SCK ↓	$t_{KSO}$			2	μs	
Port 1 output setup time to $\overline{PSTB}$ ↑	$t_{PST}$	(Note 2)			μs	
Port 1 output hold time after $\overline{PSTB}$ ↑	$t_{STP}$	100			ns	
$\overline{PSTB}$ pulse width	$t_{STL}$	(Note 2)			μs	
INT0 pulse width	$t_{I0H}, t_{I0L}$	30			μs	
INT1 pulse width	$t_{I1H}, t_{I1L}$	(Note 3)			μs	
RESET pulse width	$t_{RSH}, t_{RSL}$	30			μs	
RESET setup time	$t_{SRS}$	0			ns	
RESET hold time	$t_{HRS}$	0			ns	

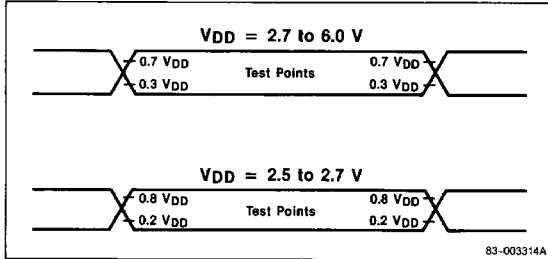
**Notes:**

- (1) RC network at CL1 and CL2; C = 33 pF ±5%,  $|\Delta C/^\circ C| \leq 60$  ppm.
- (2)  $10^3 \div 2$  ( $f_{CC}$  or  $f_C$  in kHz) - 2.0.
- (3)  $10^3 \div 2$  ( $f_{CC}$  or  $f_C$  in kHz).

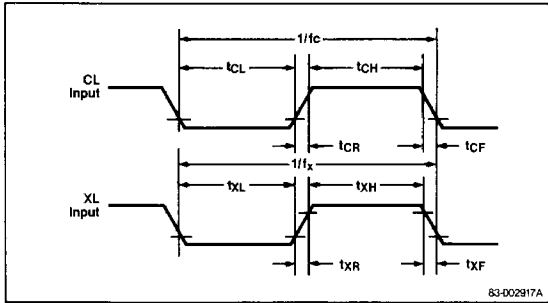


## Timing Waveforms

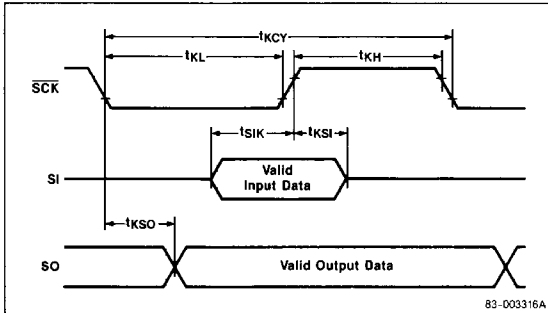
### Timing Measurement Points



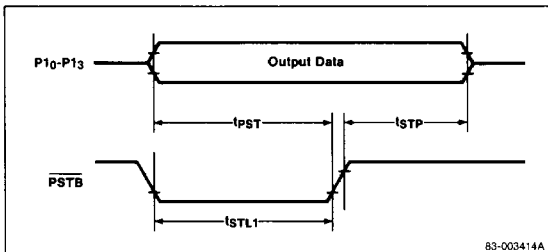
### Clocks



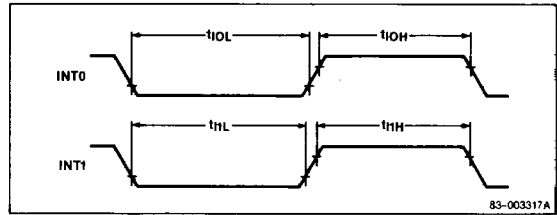
### Serial Interface



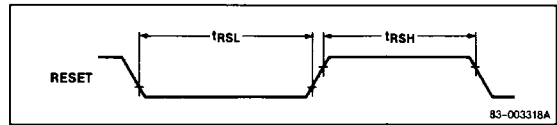
### Output Strobe



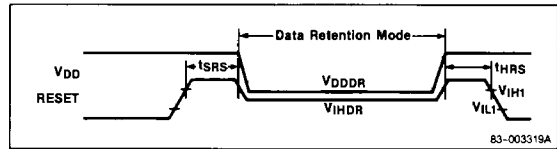
### External Interrupts



### RESET



### Data Retention Mode

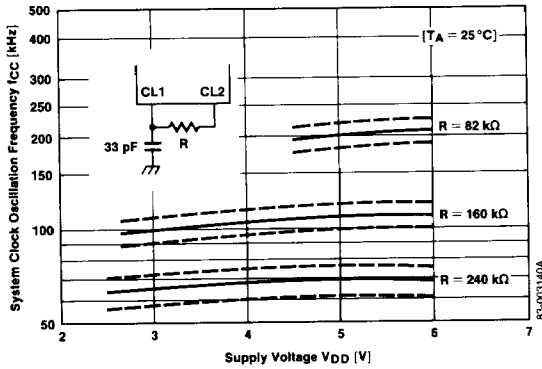


3

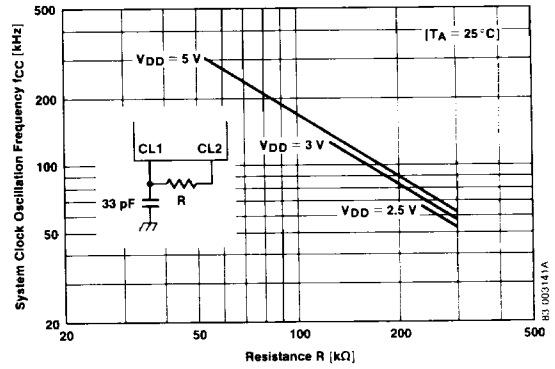
### Operating Characteristics

T<sub>A</sub> = 25°C

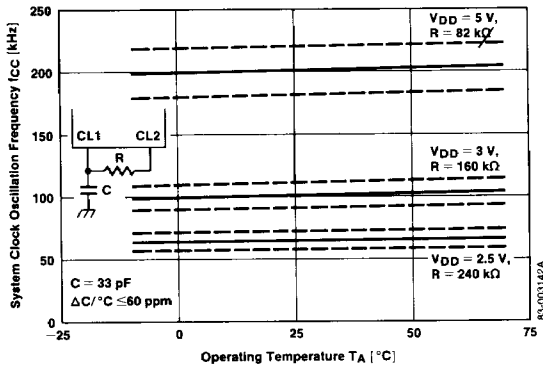
f<sub>CC</sub> vs V<sub>DD</sub>



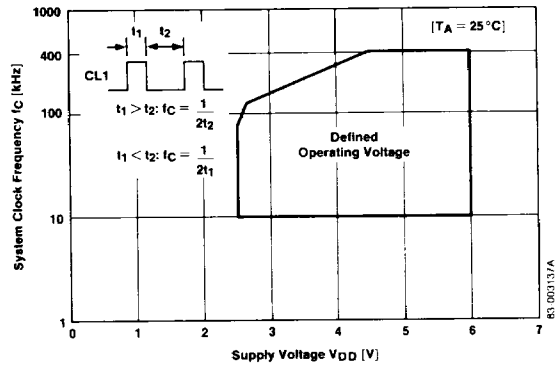
f<sub>CC</sub> vs R



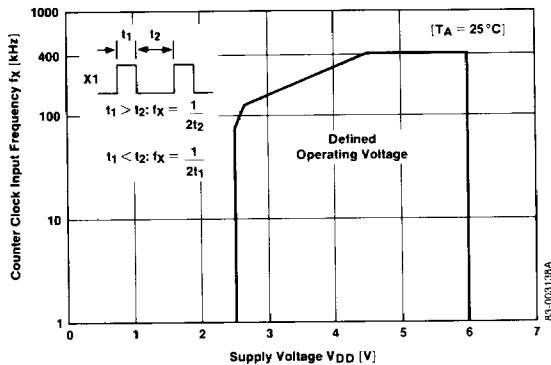
f<sub>CC</sub> vs T<sub>A</sub>



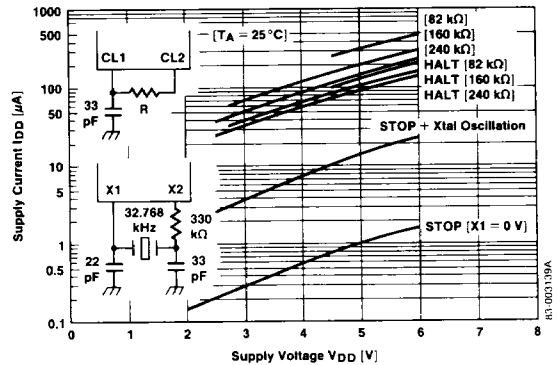
f<sub>C</sub> vs V<sub>DD</sub> [External Clock]



f<sub>X</sub> vs V<sub>DD</sub> [External Clock]



I<sub>DD</sub> vs V<sub>DD</sub>



## Operating Characteristics (cont)

$T_A = 25^\circ\text{C}$

