NEC

Application Note

μPD780988 Subseries

8-Bit Single-Chip Microcontrollers

Inverter control

μPD780982
μPD780983
μPD780984
μPD780986
μPD780988
μPD78F0988A

Document No. U13119EJ4V0AN00 (4th edition)
Date Published July 2001 J CP(K)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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J01.2

Major Revisions in This Edition

Page	Description
Throughout	The following product name has been modified: μPD78F0988 → μPD78F0988A
P. 43	**CHAPTER 3 CONTROL** **Figure 3-8 TM7 Operation Timing** has been modified.
P. 46	**CHAPTER 4 NOTES ON TIME REQUIRED FOR TIMING SET INTERRUPT PROCESSING** The interrupt processing time has been modified accordingly under the following conditions: • TM7 is used as an 8-bit timer. • TM7 is used as a 10-bit timer.

The mark ⋆ shows major revised points.

INTRODUCTION

Target Readers

This application note is intended for users who wish to understand the functions of the μPD780988 Subseries, and to design application programs using these products. This manual describes only the μPD780988 hereafter.

- μPD780988 Subseries: μPD780982, μPD780983, μPD780984, μPD780986, μPD780988, and μPD78F0988A[Note] ★

Note Under development

Purpose

The purpose of this application note is to help users understand the inverter control functions of the μPD780988 Subseries by using a sample application.
The program and hardware configurations published here are just examples and are not intended for mass production.

Organization

This application note is divided into the following sections:

- Overview of functions
- Hardware configuration
- Control
- Cautions
- Flowcharts
- Program list

Conventions

In this application note, symbols and notation are used as follows:

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numerical representation:	Binary: ××××××××B
	Decimal: ××××
	Hexadecimal: ××××H
Characters that are easily confused:	0 (zero), O (uppercase of o)
	1 (one), l (lowercase of L), I (uppercase of i)

Related Documents

- **Documents Related to Devices**

Document Name	Document Number
★ μPD780982, 780983, 780984, 780986, 780988, 780982(A), 780983(A), 780984(A), 780986(A), 780988(A) Data Sheet	U12804E
★ μPD78F0988A Data Sheet	To be prepared
μPD780988 Subseries User's Manual	U13029E
μPD780988 Subseries Application Note Inverter Control	This manual
78K/0 Series User's Manual Instruction	U12326E
78K/0 Series Application Note Fundamental (I)	IEA-1288
78K/0, 78K/0S Series Application Note Flash Memory Write	U14458E

- **Documents Related to Development Tools**

Document Name		Document Number
★ RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
PG-FP3 Flash Memory Programmer		U13502E
IE-78K0-NS In-circuit Emulator		U13731E
IE-78001-R-A In-circuit Emulator		U14142E
IE-780988-NS-EM4 In-circuit Emulator		To be prepared
EP-78240 Emulation Probe		U10332E
SM78K0S, SM78K0 System Simulator Ver.2.10 or Later Windows™ Based	Operation	U14611E
SM78K Series System Simulator Ver.2.10 or Later	External Parts User Open Interface Specification	To be prepared
ID78K0-NS Integrated Debugger Ver.2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
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- **Documents Related to Embedded Software (User's Manuals)**

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Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW OF FUNCTIONS

As a sample application for the real-time pulse unit (RPU) of the μPD780988, this chapter introduces an application for three-phase inverter control according to PWM output.

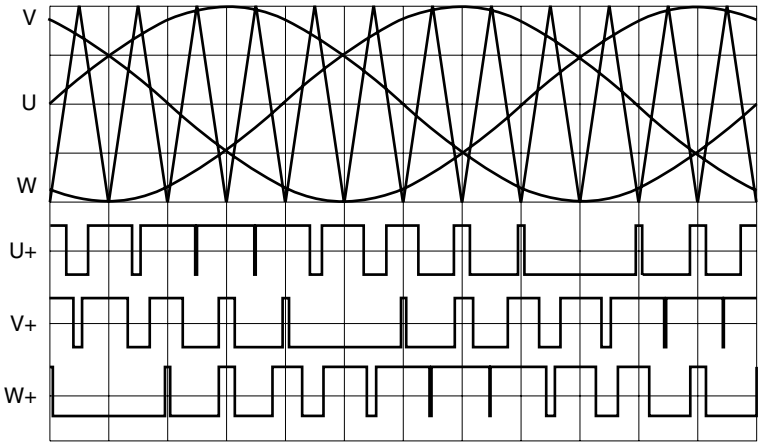
The operating environment is shown below.

CPU:	μPD780988
Operating clock:	System clock 8 MHz (Internal: 8 MHz)
Operating voltage:	5 V
Internal ROM:	60 Kbytes
Internal RAM:	2 Kbytes
External expansion memory:	Not used

1.1 PWM Signal Generation

As shown in Figure 1-1, the PWM signal is generated by using a sawtooth (carrier) wave to modulate a sine wave.

Figure 1-1. Use of Sawtooth Wave to Generate PWM Sine Waveform

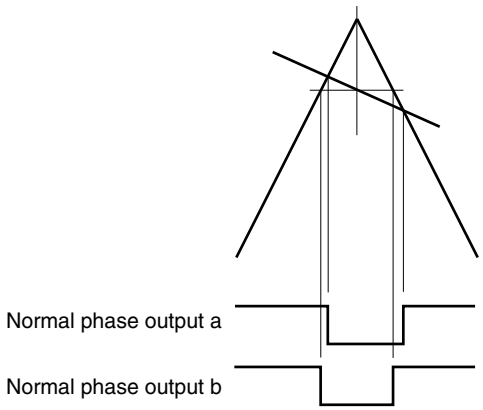


Remark The U–, V–, and W– phases are obtained by inverting the high and low levels of the waveforms of the U+, V+, and W+ phases.

Figure 1-2 shows the switching timing of the normal phase output.

When switching occurs at the intersection of the sawtooth and sine waves, a waveform like that indicated by "a" below is generated. However, depending on the complexity of the processing and the number of settings, the sample application simulates switching at the timing indicated by "b."

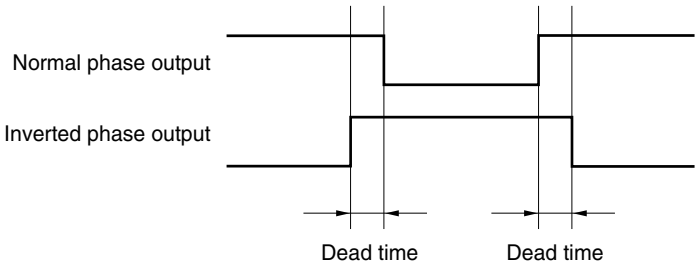
Figure 1-2. Switching Timing



1.2 Dead Time

To prevent the positive and negative transistors of each phase from going on together, dead time is inserted into the PWM output. The dead time can be set, by key input, to a value of between 1 μs and 32 μs, the output of the PWM signal being driven low after the elapse of the previously set delay.

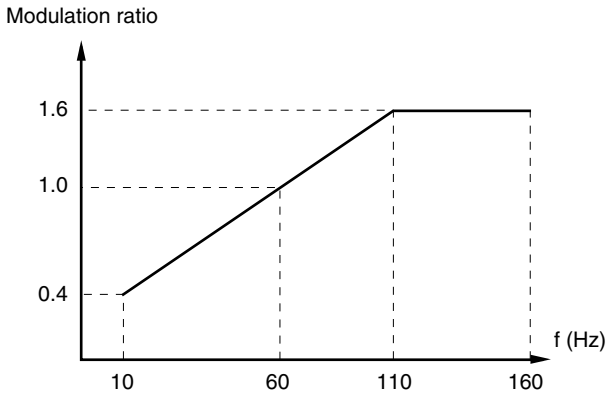
Figure 1-3. Dead Time



1.3 V/f Control

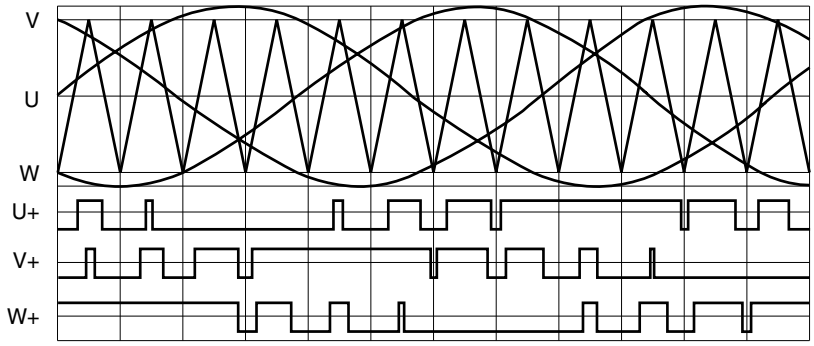
To adjust the torque of the motor, V/f control is used to adjust the voltage (V) in line with the output frequency (f). Figure 1-4 shows how the characteristic modulation ratio of the sample program varies with the output frequency. The modulation ratio (sine wave amplitude)/(sawtooth wave amplitude) is such that, when equal to 1, the sawtooth wave amplitude is equal to that of the sine wave.

Figure 1-4. Variation of Characteristic Modulation Ratio with Output Frequency



After V/f modulation, if the sawtooth and sine waves do not intersect, as shown in Figure 1-5, switching is not performed.

Figure 1-5. Generation of PWM Sine Waveform under V/f Control



Remark The U–, V–, and W– phases are obtained by inverting high- and low-level waveforms of the U+, V+, and W+ phases.

1.4 Inverter Output Setting Range

Table 1-1 indicates the inverter output setting range for the sample application.

Table 1-1. Inverter Output Setting Range

Carrier Frequency (Hz)	Output Frequency Setting Range (Hz)	Dead Time Setting Range (μs)
200	4 to 25	1 to 32
400	4 to 50	
600	4 to 75	
800	4 to 100	
1,000	4 to 120	
1,200 to 3,800	4 to 160	
4,000		1 to 31
4,200		1 to 29
4,400		1 to 28
4,600		1 to 27
4,800		1 to 26
5,000		1 to 25
5,200		1 to 24
5,400		1 to 23
5,600		1 to 22
5,800		1 to 21
6,000 to 6,200		1 to 20
6,400		1 to 19
6,600 to 6,800		1 to 18
7,000 to 7,200		1 to 17
7,400 to 7,800		1 to 16
8,000 to 8,200		1 to 15
8,400 to 8,800		1 to 14
9,000 to 9,600		1 to 13
9,800 to 10,400		1 to 12
10,600 to 11,200		1 to 11
11,400 to 12,400		1 to 10
12,600 to 13,800		1 to 9
14,000 to 15,600		1 to 8
15,800 to 17,800		1 to 7
18,800 to 20,000		1 to 6

1.5 Frequency Shifting

The current frequency is compared with the set frequency (target frequency) every 5 ms.

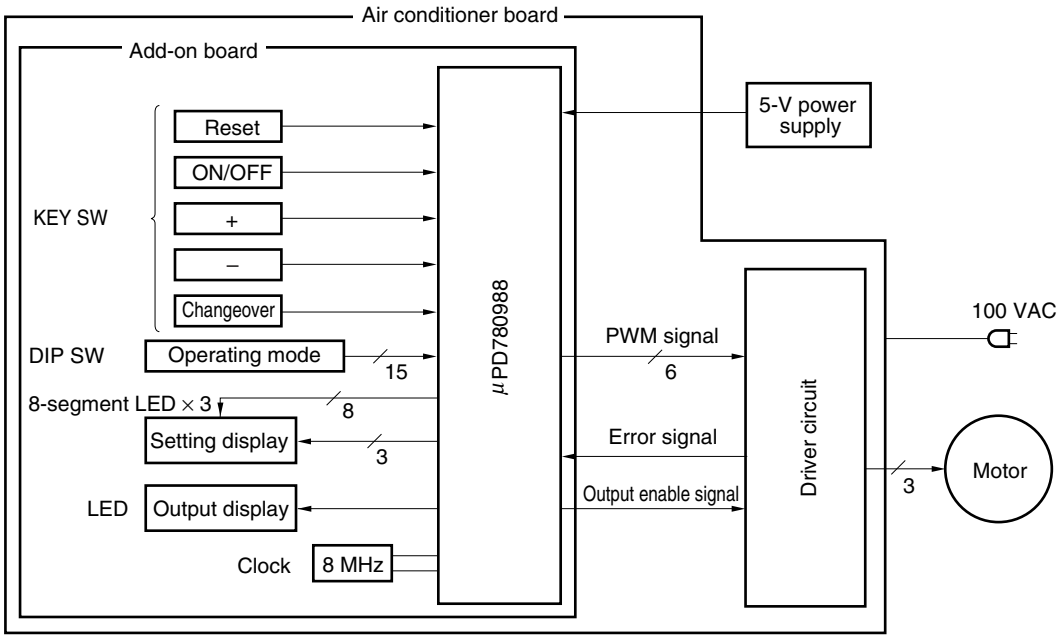
When the current and target frequencies are found to differ, the output frequency is adjusted in 1-Hz steps, at the specified rate of change.

CHAPTER 2 HARDWARE CONFIGURATION

2.1 System Configuration

Figure 2-1 shows the hardware configuration.

Figure 2-1. Hardware Configuration

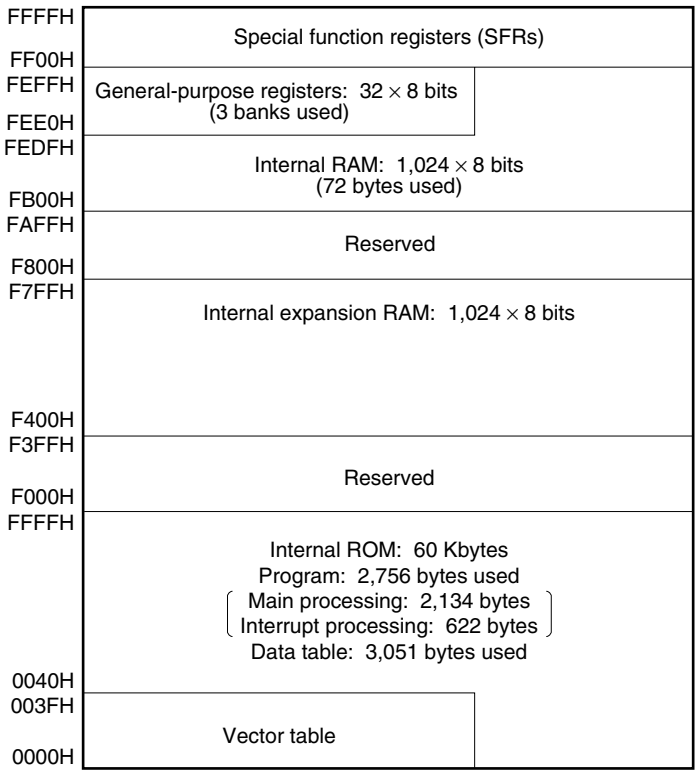


2.2 CPU Block

2.2.1 Memory map

Figure 2-2 shows the memory map.

Figure 2-2. Memory Map



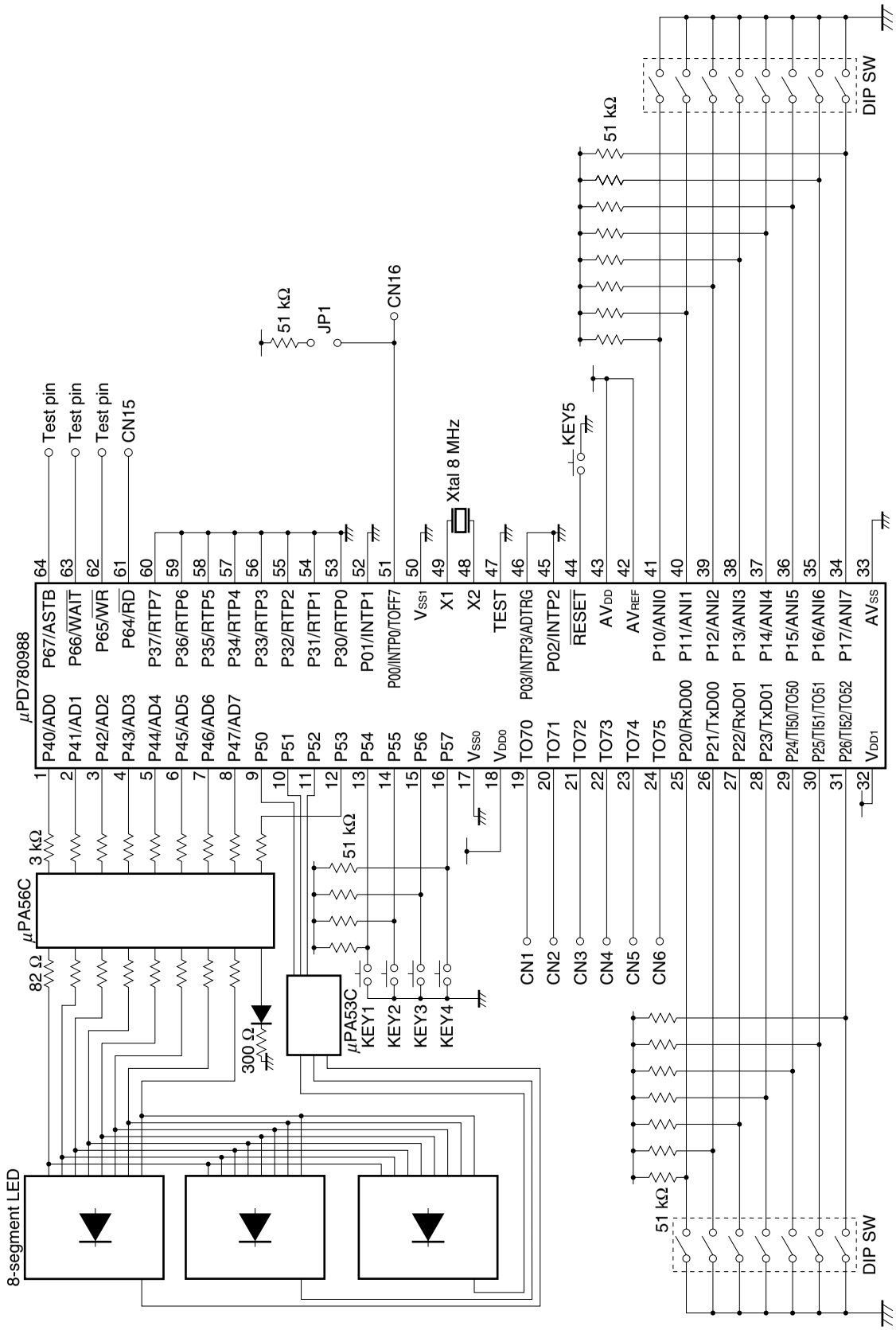
2.2.2 Pin mapping

Table 2-1. Pin Mapping

Pin No.	Pin Name	I/O	Signal Name	A	R	Setting	Pin No.	Pin Name	I/O	Signal Name	A	R	Setting
1	P40	I/O	SEG LED (a) output	H	I	L	33	AV_{SS}	—	(Connect to V_{SS})	—	—	—
2	P41	I/O	SEG LED (b) output	H	I	L	34	P17	I	Changeover between 8 and 10 bits	—	I	I
3	P42	I/O	SEG LED (c) output	H	I	L	35	P16	I	V/f control on/off	—	I	I
4	P43	I/O	SEG LED (d) output	H	I	L	36	P15	I	TM7 count clock selection	—	I	I
5	P44	I/O	SEG LED (e) output	H	I	L	37	P14	I		—	I	I
6	P45	I/O	SEG LED (f) output	H	I	L	38	P13	I		—	I	I
7	P46	I/O	SEG LED (g) output	H	I	L	39	P12	I	INTTM7 occurrence frequency selection	—	I	I
8	P47	I/O	SEG LED (h) output	H	I	L	40	P11	I		—	I	I
9	P50	I/O	SEG LED digit 3 output	H	I	H	41	P10	I		—	I	I
10	P51	I/O	SEG LED digit 2 output	H	I	L	42	AV_{REF}	—	Not used	—	—	—
11	P52	I/O	SEG LED digit 1 output	H	I	L	43	AV_{DD}	—	(Connect to V_{DD})	—	—	—
12	P53	I/O	Operation indicator LED	H	I	L	44	$\overline{\text{RESET}}$	I	Reset input	L	I	I
13	P54	I/O	[ON/OFF] input	L	I	I	45	P02	I/O	(Connect to V_{SS})	—	I	I
14	P55	I/O	[+] input	L	I	I	46	P03	I/O	(Connect to V_{SS})	—	I	I
15	P56	I/O	[–] input	L	I	I	47	IC	—	(Connect to V_{SS})	—	—	—
16	P57	I/O	[Changeover] input	L	I	I	48	X2	—	System clock	—	—	—
17	V_{SS0}	—	Ground	—	—	—	49	X1	I	System clock	—	I	—
18	V_{DD0}	—	Supply voltage	—	—	—	50	V_{SS1}	—	Ground	—	—	—
19	TO70	O	U+ output	L	O	H	51	P00	I/O	Error signal input	L	I	I
20	TO71	O	U– output	L	O	H	52	P01	I/O	(Connect to V_{SS})	—	I	I
21	TO72	O	V+ output	L	O	H	53	P30	I/O	Not used	—	I	I
22	TO73	O	V– output	L	O	H	54	P31	I/O	(Connect to V_{DD})	—	I	I
23	TO74	O	W+ output	L	O	H	55	P32	I/O		—	I	I
24	TO75	O	W– output	L	O	H	56	P33	I/O		—	I	I
25	P20	I/O	V/f table selection	L	I	I	57	P34	I/O		—	I	I
26	P21	I/O		L	I	I	58	P35	I/O		—	I	I
27	P22	I/O		L	I	I	59	P36	I/O		—	I	I
28	P23	I/O	Not used	L	I	I	60	P37	I/O		—	I	I
29	P24	I/O		L	I	I	61	P64	I/O	Enable signal output	L	I	H
30	P25	I/O		L	I	I	62	P65	I/O	Test pin output	—	I	L
31	P26	I/O		L	I	I	63	P66	I/O	Test pin output	—	I	L
32	V_{DD1}	—	Supply voltage	—	—	—	64	P67	I/O	Test pin output	—	I	L

Remark I/O: Input/output (I: Input, O: Output)
A: Active level (H: High level, L: Low level)
R: Pin status at reset (I: Input, O: Output)
Setting: Setting made at initialization (I: Input, H: High-level output, L: Low-level output)

2.3 Circuit Diagram



CHAPTER 3 CONTROL

3.1 State Transition Table

Table 3-1 lists the state transitions. During the execution of the mode handling indicated by **<1>** to **<5>** under "State," if any of the events indicated under "Factor" should occur, transition to the mode having the number shown is performed.

An "*" in a column indicates that mode transition is not performed. Input is valid, however.

A "—" in a column indicates that input is not valid.

Table 3-1. State Transition

State[Note 1] \ Factor[Note 2]		Reset Input	ON/OFF Input	+ Input	– Input	Changeover Input	Stop Signal	Synchronous/ Asynchronous Input	Processing End
<1>	Initialize	*	—	—	—	—	—	*	<5>
<2>	Output frequency change	<1>	<5>	<4>	<4>	*	<5>	—	<3>
<3>	Fixed output frequency	<1>	<5>	<4>	<4>	*	<5>	—	—
<4>	Setting	<1>	#1	*	*	#1	<5>	—	—
<5>	Signal output stop	<1>	#2	<4>	<4>	*	*	—	—

#1: Transition to mode <2>, <3>, or <5> is performed depending on the output state.

#2: Transition to mode <2> is performed when no stop signal is input.

Notes 1. States

Initialize:	Initially set processing state after a reset start
Output frequency change:	Frequency change processing state, when the target frequency differs from the output frequency
Fixed frequency output:	Fixed frequency output state, when the target frequency matches the output frequency
Setting:	Setting of change pattern to be selected by key input, target frequency, carrier frequency, dead time, and rate of frequency change
Signal output stop:	State existing when frequency output is stopped

2. Factors

Reset input:	When key switch connected to reset pin is pressed
ON/OFF input:	When [ON/OFF] key is pressed
+ input:	When [+] key is pressed
– input:	When [–] key is pressed
Changeover input:	When [Changeover] key is pressed
Stop signal:	When input of the stop signal is detected
DIP SW input:	V/f table selection setting input
	Input to select the size (8/10 bits) of timer 7 (TM7)
	Input to specify whether to turn V/f control on/off
	Input to specify the TM7 count clock
	Input to specify the INTTM7 occurrence frequency
Processing end:	When initialization ends, transition to the signal output stopped state is performed. When output frequency change processing ends, transition to fixed frequency output is performed.

3.2 Program Configuration

Table 3-2 lists the configured subroutines and interrupt processing performed by the sample application.

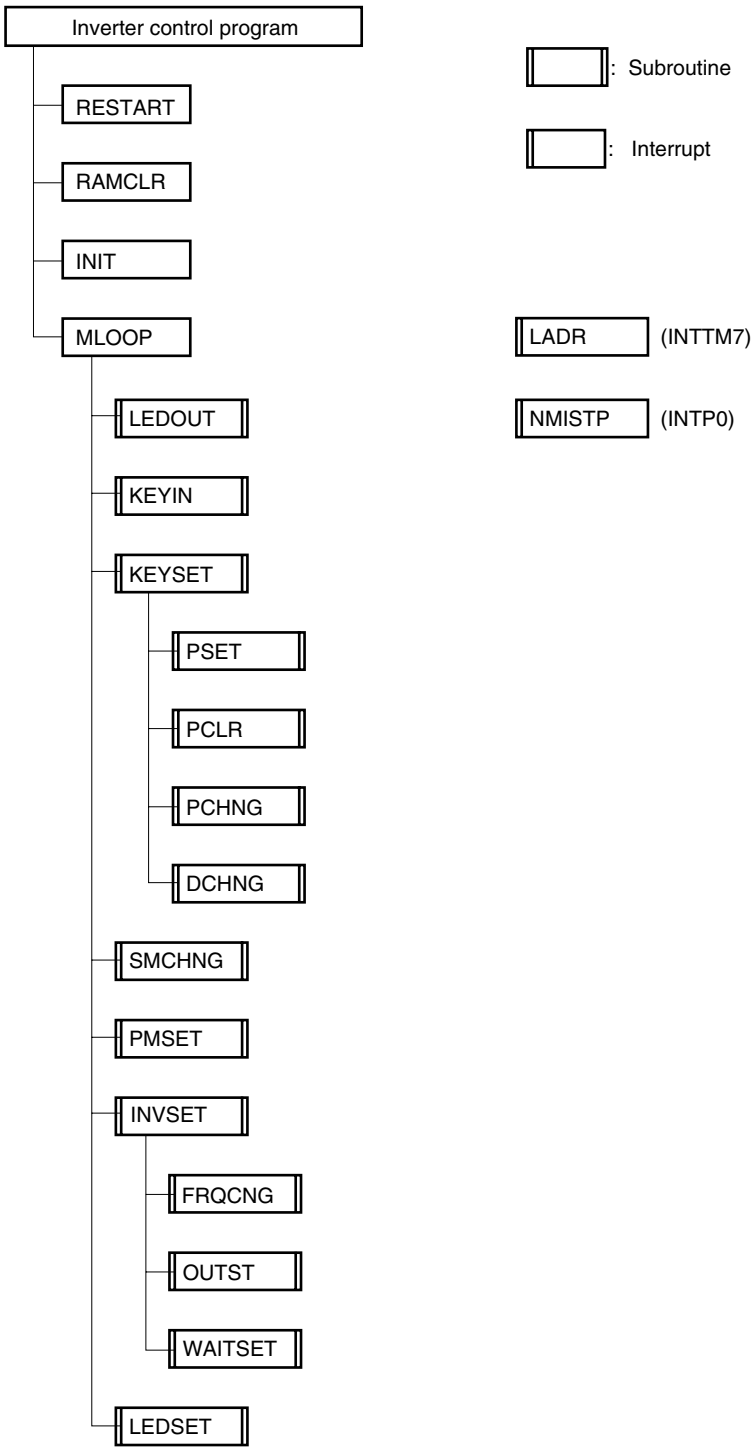
Table 3-2. Subroutines and Interrupt Processing

Symbol	Processing
RESTART	Setting of control register and port mode
RAMCLR	RAM area clear
INIT	Initial setting of variables, DIP SW input (setting of operating mode)
MAINLP	Set by key input Setting of inverter output variable Setting of LEDs and test pin output
— LEDOUT	Output processing for LEDs and 8-segment LEDs
— KEYIN	Key input processing
— KEYSET	Key input setting
— — PSET	Determination of set value according to [ON/OFF] key input
— — PCLR	Clearing of set value according to [Changeover] key input
— — PCHNG	Change of set value according to [+] or [–] key input
— — DCHNG	Change of 8-segment LED display according to [Changeover] key input
— SMCHNG	Setting mode transition processing
— PMSET	Main mode transition processing
— INVSET	Inverter output setting processing
— — FRQCNG	Setting of inverter output variable when changing output frequency
— — OUTST	Setting of inverter output start
— — WAITSET	Setting of wait when changing output frequency
— LEDSET	Setting of LED and 8-segment LED indications
LADR	Timing set interrupt (context switching)
INTP0	Safety stop set interrupt (vectored interrupt)

Figure 3-1 illustrates the program configuration.

As shown in the figure, processing begins from RESTART. MLOOP processing is performed after the completion of RESTART and INIT processing.

Figure 3-1. Program Configuration



3.3 RAM and Flags

Tables 3-3 to 3-6 list the variables and flags used by the sample application.

Depending on the linker, variables and flags are allocated such that they can be relocated. To allocate 2-byte variables to an even-numbered address, however, it is necessary to specify the relocatable attribute.

Table 3-3. Variables Used for Inverter Control (1/2)

Symbol	Bytes	Use, Setting, Reference	Set Value
PMODE	1	PWM output mode Set by mode transition	Stop mode: 0 Fixed output mode: 1 Output change mode: 2
NFOUT	1	Output frequency Set by inverter output setting	During output: (Target frequency) **Example** 10 Hz: 0AH (10) While stopped: 0FFH
RFOUT	1	Target frequency Set by key setting Referenced by inverter output setting	Output setting: (Target frequency) Stop setting: 0FFH
NCRRY	1	Carrier frequency number Set by key setting Referenced by inverter output setting	Argument at CRRYTBL[] reference 1 to 64H (100)
NDEAD	1	Dead time number Set by key setting Referenced by inverter output setting	Argument at DEADTBL[] reference 1 to 20H (32)
NCHNG	1	Frequency change rate number Set by key setting Referenced by inverter output setting	Argument at CHNGTBL[] reference 0 to 3
WAITCNT	2	Frequency change wait counter Set by inverter output setting	After being set, the CHNGTBL[] reference value is decremented by 1 until 0 is reached.
VFP	2	V/f modulation ratio pointer Referenced and set by inverter output setting	Argument at VFTBL[] reference 0 to 9DH (157)
SADR	2	Value added to sine wave reference phase Referenced and set by INTTM7 processing	Transfer of BSADR set value
BSADR	2	Transfer buffer used for SADR change Set by inverter output setting	Value added to sine wave reference phase $\frac{\text{(Output frequency)}}{\text{(Carrier frequency)}} \times n$ where n = number of sine wave data items × number of interrupt occurrences
OFFSET	2	Offset revision determined by V/f modulation Referenced and set by INTTM7 processing	Transfer BOFFSET set value

Table 3-3. Variables Used for Inverter Control (2/2)

Symbol	Bytes	Use, Setting, Reference	Set Value
BOFFSET	2	Transfer buffer used for OFFSET change Set by inverter output setting	Offset revision determined by V/f modulation $\left\lvert \frac{BVF}{2} - \frac{BCM03}{2} \right\rvert$
VF	2	V/f modulation multiplier Referenced and set by INTTM7 processing	Transfer BVF set value
BVF	2	Transfer buffer used for VF change Set by inverter output setting	V/f modulation multiplier $\frac{\text{TM7 operation clock}}{2 \times fc} \times \frac{VFTBL[\ ]}{80H}$
BCM03	2	Transfer buffer used for CM03 change Set by inverter output setting	CM03 set value $\frac{\text{TM7 operation clock}}{2 \times fc}$
VFTBLNO	2	V/f table address Set in variable initialization Referenced by inverter output setting	Start address of VFTBL1 to VFTBL8
TM7CLK	1	TM7 count clock Set in variable initialization Referenced by inverter output setting	0 to 7 **Example** fx/2: 1
TM7CNT	1	Number of INTTM7 occurrences Set in variable initialization Referenced by the inverter output setting	1 to 8 **Example** One occurrence per two TM7 underflow occurrences: 2

fc: Carrier frequency

Explanation of major symbols

(1) VFP

The argument at VFTBL1[] to VFTBL8[] reference is set. In VFTBL1[] to VFTBL8[], to describe the 157 words of the V/f modulation ratio corresponding to 4 to 160 Hz, VFP can be set to a value within the range of 0 to 9DH (157).

(2) SADR, BSADR

The sine wave reference phase increment is set. To equally divide the sine wave table data count (512/256 words) by the carrier wave count for one sine wave cycle, calculation is performed as follows:

$$\frac{\text{(Output frequency)}}{\text{(Carrier frequency)}} \times \text{(Sine wave data count)} \times \text{(Number of INTTM7 interrupt occurrences)}$$

(3) VF, BVF

Multiplying the V/f modulation multiplier by the SINTBL1[] to SINTBL8[] reference value (0 to 0FFH)/SINTBL1[] reference value (0 to 3FFH) gives a sine wave having an amplitude equal to that of the carrier wave multiplied by the modulation ratio.

The value of VFTBL1[] to VFTBL8[] described in the modulation ratio table is equal to (modulation ratio) × 80H.

Therefore, the value set for VF is as follows:

$$\text{(Carrier wave amplitude)} \times \text{(Modulation ratio)} = \frac{\text{TM7 operation clock}^{\text{Note}}}{2 \times \text{fc}} \times \frac{\text{VFTBL[ ]}}{\text{80H}}$$

Note The carrier wave amplitude is obtained by dividing the carrier wave half-cycle (1/(2 × fc)) by the timer count (1/TM7 operation clock), as follows:

$$\frac{1/(2 \times \text{fc})}{1/\text{TM7 operation clock}} = \frac{\text{TM7 operation clock}}{2 \times \text{fc}}$$

(4) OFFSET, BOFFSET

Value set for offset revision determined by V/f modulation.

Within the V/f modulated sine wave data, because the CM3/2 data exists together with much other data, it is necessary to perform offset revision determined by V/f modulation.

(a) When the V/f modulation ratio is greater than or equal to 1, the offset value is decremented.

(b) When the V/f modulation ratio is less than 1, the offset value is incremented.

The value set for the offset determined by V/f modulation is calculated as follows:

$$\left| \frac{\text{VF}}{2} - \frac{\text{CM3}}{2} \right|$$

Table 3-4. Flags Used for Inverter Control

Symbol	Use, Setting	Set Value
_CHNGST	Interrupt variable transfer request Set in inverter output setting Reset by INTTM7 processing	Reset: No transfer request Set: Transfer request
_MINIT	Selection of mode initialization processing Set/reset by mode transition processing	Reset: Mode initialization unnecessary Set: Mode initialization necessary
_PCHNG	Determination of output setting change Set by key setting Reset by inverter output setting	Reset: No setting change Set: Setting changed
_BSVF	Transfer flag for _SVF change Set by inverter output setting	Reset: V/f modulation ratio < 1 Set: V/f modulation ratio ≥ 1
_SVF	Indicates V/f modulation ratio. Set and referenced by INTTM7 processing	Transfers _BSVF value.
_10BIT	TM7 timer size (8/10 bits) selection Set by variable initialization Referenced by inverter output setting	Reset: TM7 is 8 bits long. Set: TM7 is 10 bits long.
_VFON	V/f control on/off selection Set by variable initialization Referenced by inverter output setting	Reset: V/f control not exerted Set: V/f control exerted

Table 3-5. Variables Used for Other Than Inverter Control (1/3)

Symbol	Bytes	Use, Setting, Reference	Set Value	
NSET	1	Value set by key input Set and referenced by key setting	DMODE	Meaning of set value
			10H	Target frequency
			11H	Carrier frequency number
			12H	Dead time number
			03H	Frequency change rate number
NSETMN	1	Minimum NSET value Set and referenced by key setting	DMODE	Meaning of minimum value
			10H	Target frequency
			11H	Carrier frequency number
			12H	Dead time number
			03H	Frequency change rate number
NSETMX	1	Maximum NSET value Set and referenced by key setting	DMODE	Meaning of maximum value
			10H	Target frequency
			11H	Carrier frequency number
			12H	Dead time number
			03H	Frequency change rate number
SFOUT	1	Buffer used for setting target frequency Set by key setting Referenced by inverter output setting	Target frequency set by key setting **Example** 10 Hz: 0AH (10)	

Table 3-5. Variables Used for Other Than Inverter Control (2/3)

Symbol	Bytes	Use, Setting, Reference	Set Value	
KIN	1	Key input Set and referenced by key setting	Port (P5) input value	
SMODE	1	Key setting mode Set by setting mode transition processing	00H	PWM output setting
			01H	Setting off
DMODE	1	8-segment LED display mode Set and referenced by key setting	10H	Display of output frequency
			11H	Display of carrier frequency
			12H	Display of dead time
			03H	Display of frequency change rate
SEGBUF	3	8-segment LED display buffer Set and referenced by key setting	Character codes displayed by three 8-segment LEDs	
SEGCNT	1	8-segment LED flash counter Set and referenced by LED display setting	Decremented (–1) from 0E4H (initial value) to 1CH. SEG LED is lit when the most significant bit = 1.	
LEDCNT	1	LED flash counter Set and referenced by LED display setting	Decremented (–1) from 0E4H (initial value) to 1CH. LED is lit when the most significant bit = 1.	
KSMPCNT	1	Key input sampling counter Set and referenced by key input processing	Decremented (–1) from 2 (initial value) to 0.	
KONCNT	1	Hold-down counter Set and referenced by key input processing	Decremented (–1) from 13H (initial value) to 0.	
KCODE1	1	Key code buffer 1 Set and referenced by key input processing (Key codes are listed in **Table 3-11**.)	Previously input key code 0: Null 1: [Changeover] 2: [–] 3: [+] 4: [ON/OFF]	
KCODE2	1	Key code buffer 2 Set and referenced by key input processing	Input key code See above.	
MKAKE1	2	Multiplicand buffer Used in main processing	The multiplicand data stored in the buffer is 16 bits long.	
MKAKE2	2	Multiplier buffer Used in main processing	The multiplier data stored in the buffer is 16 bits long.	
MKOTAE	4	Calculation result storage buffer Used in main processing	Calculation result data stored in the buffer is 32 bits long.	
IKAKE1	2	Multiplicand buffer Used in INTTM7 interrupt processing	The multiplicand data stored in the buffer is 16 bits long.	
IKAKE2	2	Multiplier buffer Used in INTTM7 interrupt processing	The multiplier data stored in the buffer is 16 bits long.	
IKOTAE4	4	Calculation result storage buffer Used in INTTM7 interrupt processing	Calculation result data stored in the buffer is 32 bits long.	
WARU1	4	Dividend buffer Used in main processing	The dividend data stored in the buffer is 32 bits long. Calculation result data (quotient) stored in the buffer is 32 bits long.	

Table 3-5. Variables Used for Other Than Inverter Control (3/3)

Symbol	Bytes	Use, Setting, Reference	Set Value
WARU2	2	Divider buffer Used in main processing	The divider data stored in the buffer is 16 bits long.
AMARI	2	Remainder storage buffer Used in main processing	The remainder data stored in the buffer is 16 bits long.

Table 3-6. Flags Used for Other Than Inverter Control

Symbol	Use, Setting	Set Value
_LEDOUT	LED output setting Set/reset by LED display setting	Reset: LED not lit Set: LED lit

3.4 Tables

Table 3-7 lists the data tables used by the sample application.

Table 3-7. Data Tables

Symbol	Bytes	Value to Be Specified	Argument	Referencing
SINTBL[]	256	Sine wave data (1 cycle) ...sinθ × 7FH + 7FH	HL of RB1	INTTM7 interrupt processing
SINTBL1[]	512 × 2	Sine wave data (1 cycle) ...sinθ × 1FFH + 1FFH	HL of RB1	INTTM7 interrupt processing
VFTBL[]	4 × 8	V/f table address Start address of VFTBL1 to VFTBL8	P20 to P22	Variable initialization
VFTBL1[]	157	V/f modulation ratio (1) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL2[]	157	V/f modulation ratio (2) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL3[]	157	V/f modulation ratio (3) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL4[]	157	V/f modulation ratio (4) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL5[]	157	V/f modulation ratio (5) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL6[]	157	V/f modulation ratio (6) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL7[]	157	V/f modulation ratio (7) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
VFTBL8[]	157	V/f modulation ratio (8) ...(Modulation ratio) × 100H (256)	VFP	Inverter output setting
CRRYTBL[]	10 × 2	(Carrier frequency) **Example** 1,530 Hz: 5FAH (1530)	NCRRY	Inverter output setting
FMXTBL[]	10 × 2	(Maximum output frequency) × 10 **Example** 100 Hz: 3E8H (1000)	NCRRY	Key setting
DMXTBL[]	10	Argument at DEADTBL[] reference	NCRRY	Key setting
CHDSPTBL[]	4 × 2	Frequency change rate 8-segment LED display data	NCHNG	LED display setting
CHNGTBL[]	4 × 2	Frequency change rate for WAITCNT setting	NCHNG	Inverter output setting
LEDTBL[]	26	8-segment LED display pattern	Character code	LED display setting
TMCLKTBL[]	4 × 8	Clock for TM7 operation **Example** 8 MHz: 1200H, 007AH	TM7CLK	Inverter output setting
CMNTBL10[]	8	Minimum carrier frequency (TM7 is 10 bits long.) **Example** 4 kHz: 14H (20)	TM7CLK	Variable initialization Key setting
CMNTBL8[]	8	Minimum carrier frequency (TM7 is 8 bits long.) **Example** 16 kHz: 50H (80)	TM7CLK	Variable initialization Key setting

Explanation of major symbols

(1) Sine wave table SINTBL[]/SINTBL1[]

0 to 2π is divided by 256 or 512 to give the sine wave data for each phase.

Because the sine is a decimal value within the range between the minimum value –1 and the maximum value + 1, to enable setting as 8- and 10-bit integer data, the sine is multiplied by the values shown below for 8 and 10 bits, respectively.

$$\frac{0FEH}{(+1) - (-1)} = 7FH$$

$$\frac{3FEH}{(+1) - (-1)} = 1FFH$$

Also, to enable comparison based on a compare instruction, –1 is made to correspond to 0, and +1 is made to correspond to 0FEH/3FEH. Therefore, the value described in the sine wave table is equal to the either of the following values for 8 and 10 bits, respectively.

$7FH + 7FH \times \sin\theta$

$1FFH + 1FFH \times \sin\theta$

(2) V/f modulation ratio tables VFTBL1[] to VFTBL8[]

The V/f modulation ratio is defined for all output frequencies (157 frequencies from 4 to 160 Hz).

The modulation ratio is a decimal number in the range between 0 and 1.6. To enable the setting of the modulation ratio as 8-bit integer data, the values that appear in the table are obtained by multiplying the modulation ratio by 256.

Each V/f modulation ratio table contains the following modulation ratios:

	10 Hz	60 Hz	80 Hz	110 Hz
VFTBL1:	0.4	1.0		1.6
VFTBL2:	0.2	1.0		1.6
VFTBL3:	0.4	1.4		1.6
VFTBL4:	0.2	1.4		1.6
VFTBL5:	0.4	1.0	1.2	
VFTBL6:	0.2	1.0	1.2	
VFTBL7:	0.4	1.2	1.2	
VFTBL8:	0.2	1.2	1.2	

3.5 Registers

Table 3-8 lists the register banks used by the sample application, as well as those that are not used.

Table 3-8. Register Banks

Number	Use
0	Main processing
1	INTTM7 timing set interrupt processing
2	INTP0 safety stop interrupt processing
3	Not used

Table 3-9 lists the uses of the registers used in interrupt processing.

Table 3-9. Registers Used in Interrupt Processing

Register	Bank 5	Bank 7
rp0 (AX)	Not used	Accumulator
rp1 (BC)	Input wait	Not used
rp6 (DE)	Not used	Sine wave table reference argument
rp7 (HL)	Not used	Sine wave reference phase

(1) Sine wave reference phase

Indicates the sine wave phase of the output waveform, with 0 to 0FFH/3FFH corresponding to 0 to 2π.

At the start of interrupt processing, the previous sine wave reference phase is set. Every time interrupt processing is performed, the phase is advanced (by adding SADR) to give the current sine wave reference phase.

At the start of output, 0 is initially set.

(2) Sine wave table reference argument

This value is used as the argument for sine wave table reference.

The phase that is referenced is set in rp7 (HL). However, sine wave data consists of 256 bytes or 512 words, so only the higher 8 or 9 bits are valid.

Four bits in rp6 (DE) are shifted to the right to set a doubled value.

3.6 Program Description

3.6.1 Initialization (symbol name: RESTART, RAMCLR, INIT)

Initialization is performed at a reset start.
Initialization is explained below.

- The control register and stack pointer are set (RESTART).
  (As the stack area, 32 bytes of the saddr area, starting from 0FB00H, are secured.)
- Port initialization is performed (RESTART).
- Excluding SFR and register bank 0, all of internal RAM is cleared (RAMCLR).
- Initial setting of interrupts and the 10-bit inverter control timer (TM7) is performed (INIT).
- DIP SW is input (operating mode is set) (INIT).

(1) TM7 timer size (8/10 bits) selection

The size (8/10 bits) of TM7 is specified according to the setting of DIP SW2 bit 7 (P17).

A size of 10 bits is selected when _10BIT is set to 1.
A size of 8 bits is selected when _10BIT is set to 0.

(2) V/f control on/off selection

Whether to turn V/f control on or off is selected according to the setting of DIP SW2 bit 6 (P16).

V/f control is turned on when _VFON is set to 1.
V/f control is turned off when _VFON is set to 0.

(3) INTTM7 interrupt occurrence frequency selection

The frequency of INTTM7 interrupt occurrences is selected according to the input of DIP SW2 bits 0 to 2 (P10 to P12). TM7CNT will hold the value input from P10 to P12 plus 1.

(4) TM7 count clock selection

The count clock for TM7 is selected according to the input of DIP SW2 bits 3 to 5 (P13 to P15). The TM7CLK will hold the value input from P13 to P15.

(5) V/f table selection

The V/f table is selected according to the input of DIP SW1 bits 0 to 2 (P20 to P22). The VFTBLNO will hold the V/f table storage address obtained from VFTBL[] using the value input from P20 to P22 as an argument.

3.6.2 Main processing

In the main processing loop, the following processing is performed every 5 ms.

- LED, 8-segment LED output
- Key input
- Key setting
- Setting mode transition
- Main mode transition
- Inverter output setting
- LED, 8-segment LED display setting

(1) LED, 8-segment LED output

LED output is performed according to the LED display setting (_LEDOUT).

_LEDOUT: Set .....LED lit
_LEDOUT: Reset .....LED not lit

8-segment LED digit switching and segment output change are performed.

Figure 3-2. Digit Switching

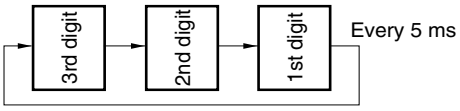


Table 3-10. Segment Display Pattern

Display	a	b	c	d	e	f	g	h
0	1	1	1	1	1	1	0	0
1	0	1	1	0	0	0	0	0
2	1	1	0	1	1	0	1	0
3	1	1	1	1	0	0	1	0
4	0	1	1	0	0	1	1	0
5	1	0	1	1	0	1	1	0
6	1	0	1	1	1	1	1	0
7	1	1	1	0	0	1	0	0
8	1	1	1	1	1	1	1	0
9	1	1	1	1	0	1	1	0
d	0	1	1	1	1	0	1	0
o	0	0	1	1	1	0	1	0
Off	0	0	0	0	0	0	0	0

Figure 3-3. Segment Arrangement

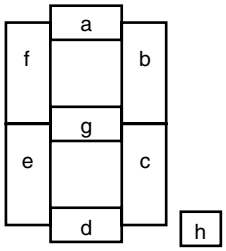
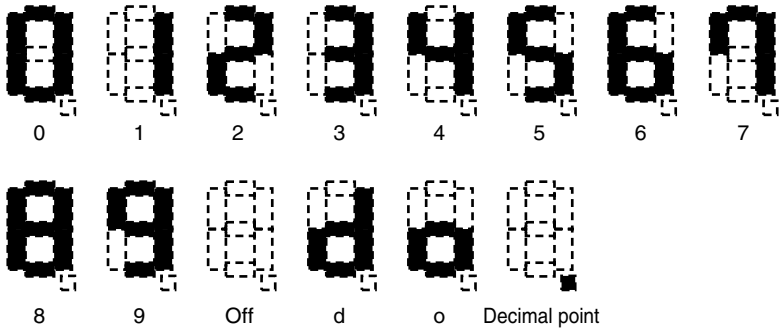


Figure 3-4. 8-Segment LED Display Pattern

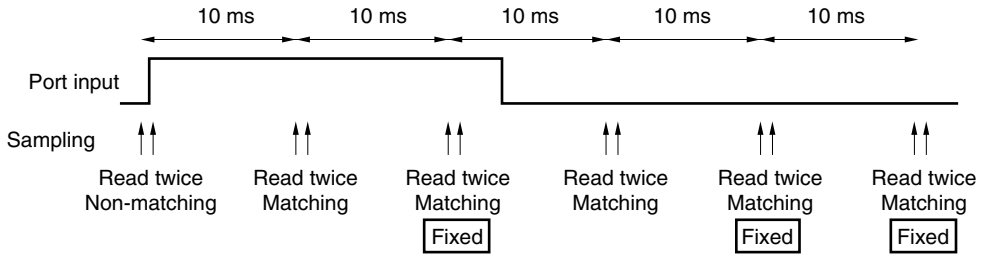


(2) Key input

As shown in Figure 3-5, key input port sampling is performed, and fixed key code KCODE2 is set.

Also, at the beginning of input processing, to transfer KCODE2 to KCODE1, KCODE1 is set to the key code fixed at the previous sampling.

Figure 3-5. Key Input Port Sampling



If the [ON/OFF], [+], [–], and [Changeover] keys are pressed simultaneously, only the key having the highest priority is effective.

Table 3-11. Key Input Priority

Key	Port	Code	Priority
[ON/OFF]	P54	04H	High
[+]	P55	03H	↑
[–]	P56	02H	↓
[Changeover]	P57	01H	Low

(3) Key setting

Processing for the key set by key input (KCODE2) is performed.

When KCODE1 ≠ KCODE2, new input is considered.

The processing performed for each input key is listed in Table 3-12.

Table 3-12. Processing Performed for Input Keys

Input Key	Processing Performed According to Mode	
	Output Setting Mode	OFF Mode
[ON/OFF]	Output setting value NSET fixed Set _PCHNG	Output start (during stop) RFOUT ← SFOUT Output stop (during output) RFOUT ← 0FFH
[+]	NSET increment (+1)	
[–]	NSET decrement (–1)	
[Changeover]	Output set value NSET clear	Display mode DMODE change

(4) Setting mode transition

Key input setting mode transition is performed. Table 3-13 lists the setting mode state transitions for key input.

During mode processing indicated by one of <1> to <3> in "Mode," upon the key input indicated in "Key," transition to the mode corresponding to the number shown is performed.

An "*" in a column indicates that the key is valid and that state transition is not performed.

A "—" in a column indicates that the key is invalid.

Table 3-13. Setting Mode State Transition

Mode \ Key		[ON/OFF]	[+]	[–]	[Changeover]
<1>	Table setting	<3>	*	*	—
<2>	Output setting	<3>	*	*	<3>
<3>	OFF	*	<2>	<2>	*

Remark Upon a reset start, table setting mode <1> is assumed.

(5) Main mode transition

As indicated in Table 3-1, inverter output mode MMODE is changed and _MINIT is set.

_MINIT is the flag used for mode initialize processing, and is set only when the state is changed (upon a reset start, depending on the initialize processing, stop mode is assumed). Table 3-14 lists the values set for MMODE.

Table 3-14. MMODE Set Values

Main Mode	MMODE
(Protection) stop mode	0
Fixed output mode	1
Output change mode	2

(6) Inverter output variable setting (subroutine: INVSET)

In output change mode (MMODE = 2), every time the wait counter (decremented by 1 every 5 ms) reaches 0, output frequency NFOUT is incremented or decremented by 1 such that it corresponds as closely as possible to set target frequency RFOUT.

When the output frequency is changed, and when the settings of the carrier frequency, dead time, and rate of frequency change are changed by key input (_PCHNG: set), the value of the transfer buffer for interrupt variable setting is calculated as indicated in Table 3-15 (the method of calculation is given in **Table 3-3**).

To reference the interrupt variable by means of interrupt processing, a value is set in the transfer buffer during main processing, and _CHNGST is set.

During interrupt processing _CHNGST is checked and, if set, the interrupt variable is set to the value in the transfer buffer and _CHNGST is reset (see **Figure 3-6**).

Table 3-15. Interrupt Variables and Transfer Buffer

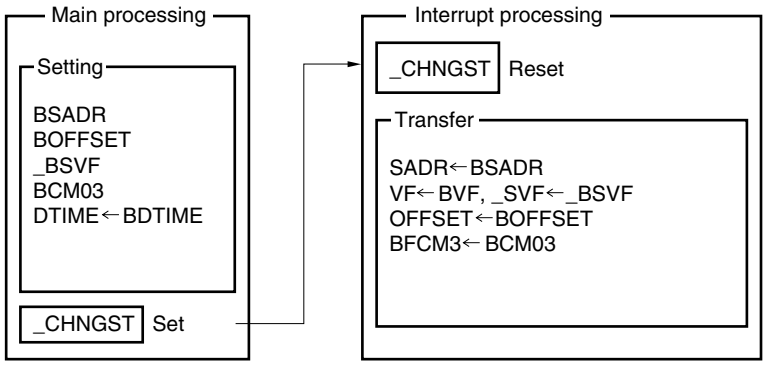
Transfer Buffer	Interrupt Variable
BSADR	SADR
BOFFSET	OFFSET
BVF	VF
_BSVF	_SVF
BCM03	
BDTIME	

Remark The values of BCM03 and BDTIME are transferred to CM3 and DTIME of sfr.

Table 3-16. Wait Counter Set Values

Rate of Frequency Change	Wait Counter Set Value	Remarks
0.5 Hz/s	400	Wait time
1.0 Hz/s	200	(Counter value) × 5 [ms]
1.5 Hz/s	133	
2.0 Hz/s	100	

Figure 3-6. Interrupt Variable Setting



While _MINIT is set, mode initialize processing (output start, stop setting) is performed (see **Table 3-17**).

Table 3-17. Output Start, Stop Setting

	Output Start Setting	Output Stop Setting	Subroutine
TM7 output	Enabled	Prohibited	OUTST
Interrupt processing	Enabled	Prohibited	OUTST
Output frequency	Set to 4 Hz	Stop setting	INVSET
Wait	Set	Not set	WAITSET
Interrupt variable	Set	Not set	FRQCNG

(7) LED and 8-segment LED display setting

The current PWM output signal state is set as shown below.

LED — At PWM output (MMODE ≠ 0) _LEDOUT is set.
At PWM output (MMODE = 0) _LEDOUT is reset.

8-segment LED — Depending on display mode DMODE, the character code to be displayed is set in 8-segment LED display buffer SEGBUF.

Table 3-18. Character Codes

Character	Code	Character	Code	Character	Code	Character	Code	Character	Code
0	00H	5	05H	d	0AH	0.	10H	5.	15H
1	01H	6	06H	o	0BH	1.	11H	6.	16H
2	02H	7	07H			2.	12H	7.	17H
3	03H	8	08H	" "	0DH	3.	13H	8.	18H
4	04H	9	09H			4.	14H	9.	19H

Remark There are no character codes above 0EH, 0FH and 1AH.

Table 3-19. 8-Segment LED Display in Each Mode

	When OFF Mode Is Set		When Other Than OFF Mode Is Set		Remarks
	LED	8-segment LED	LED	8-segment LED	
Change pattern selection			Not lit	P01 [Note]	When pattern 1 is set
Signal output stopped					
Target frequency	Not lit	65	Not lit	65[Note]	When 65 Hz is set
Carrier frequency	Not lit	10.0	Not lit	10.0[Note]	When 10,000 Hz is set
Dead time	Not lit	d10	Not lit	d10[Note]	When 10 μs is set
Rate of frequency change	Not lit	o2.0	Not lit	o2.0[Note]	When 2 Hz/s is set
Output frequency change					
Target/Output frequency	Flashing	65	Flashing	65[Note]	When 65 Hz is set
Carrier frequency	Flashing	10.0	Flashing	10.0[Note]	When 10,000 Hz is set
Rate of frequency change	Flashing	o2.0	Flashing	o2.0[Note]	When 2 Hz/s is set
Fixed frequency output					
Target/Output frequency	Lit	65	Lit	65[Note]	When 65 Hz is set
Carrier frequency	Lit	10.0	Lit	10.0[Note]	When 10,000 Hz is set
Rate of frequency change	Lit	o2.0	Lit	o2.0[Note]	When 2 Hz/s is set

Note Flashing display (50% duty, 1-s cycle). The flash cycle is reset every time key input is performed.

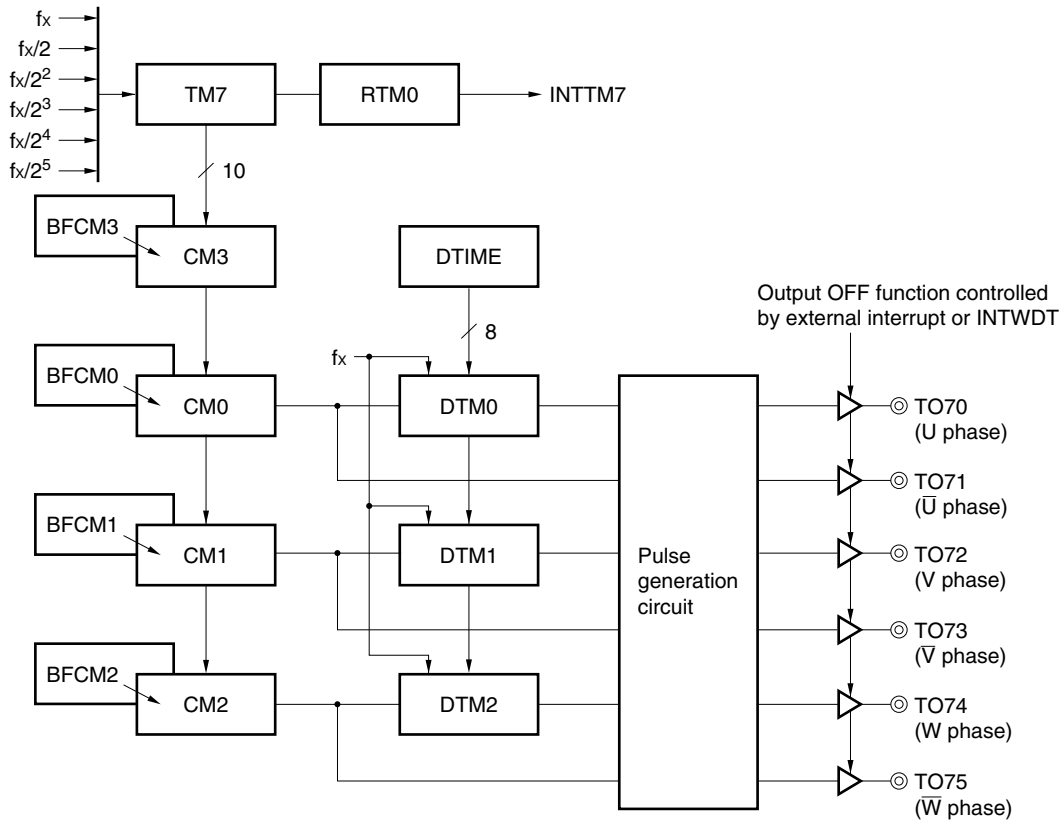
3.6.3 Setting PWM switching timing

Figure 3-7 shows the configuration of the 10-bit inverter control timer (TM7) when sawtooth wave modulation is performed with the μPD780988.

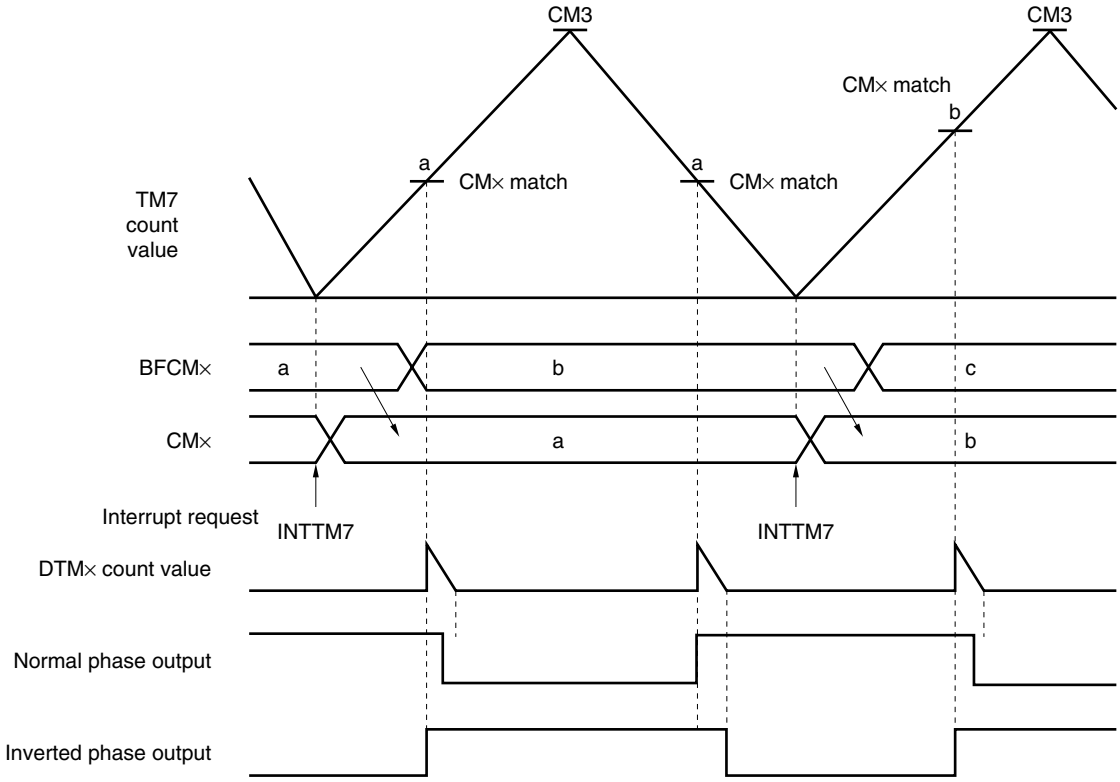
As shown in Figure 3-7, the carrier frequency is set in compare register CM3 and the dead time is set in dead time setting register DTIME. The timings at which switching is performed are set in transfer buffers BFCM0 to BFCM2.

Upon the occurrence of the INTTM7 interrupt, the values set in BFCM0 to BFCM2 are transferred to compare registers CM0 to CM2 (see **Figure 3-8**).

Figure 3-7. Block Diagram of 10-Bit Inverter Control Timer



★ **Figure 3-8. TM7 Operation Timing**



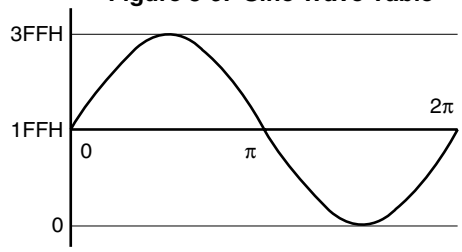
The setting of the timing for BFCM0 to BFCM2 is explained below.

(1) Sine wave data reference

Sine wave table reference is performed according to the output phase.

The range of the reference value is between 0 to 0FFH/1FFH, as shown in Figure 3-9.

Figure 3-9. Sine Wave Table

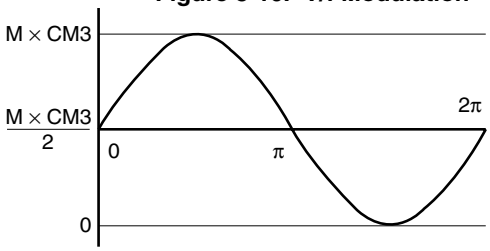


(2) V/f modulation

The sine wave data is multiplied by V/f modulation ratio VF.

The higher 8 or 10 bits correspond to the carrier frequency multiplied by the modulation ratio (see **Figure 3-10**).

Figure 3-10. V/f Modulation



(3) Offset revision according to V/f modulation

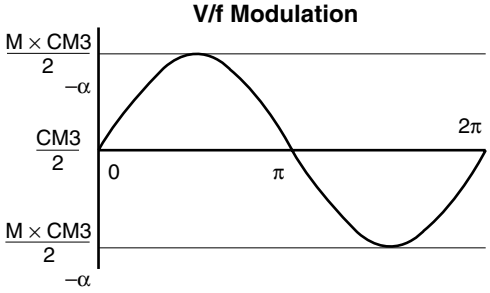
Within the V/f modulated sine wave data, because the CM3/2 data exists together with much other data, offset revision according to the V/f modulation is performed.

When the V/f modulation ratio is greater than or equal to 1, the offset value is decremented. When the V/f modulation ratio is less than 1, the offset value is incremented.

The value set for the offset determined by V/f modulation is calculated as follows:

$$\left| \frac{VF}{2} - \frac{CM3}{2} \right|$$

Figure 3-11. Offset Revision According to V/f Modulation



(4) Timing setting

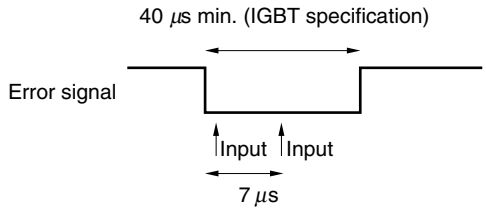
The value obtained by performing steps (1) to (3), above, is set in BFCM0X.

3.6.4 INTP0 safety stop processing

Processing starts at the falling edge of the external interrupt input to the INTP0 input pin.

To prevent the occurrence of a safety stop that is caused by noise, INTP0 pin sampling is repeated during interrupt processing. Stop setting processing is performed only when two consecutive reads of the active (low) level give the same value.

Figure 3-12. Safety Stop Conditions



During stop setting, output of the 10-bit inverter control timer (TM7) is prohibited and target frequency RFOUT is set to the stop setting (0FFH).

During main processing, when the target frequency is set to the stop setting, the main mode is also set to the stop setting. Also, timing set interrupt is prohibited.

3.6.5 Dead time input

During other than PWM output processing, to measure the dead time of the CPU, test pin (P66, P67) output is performed.

Test pin output consists of the processing shown below.

(1) Inverter output setting (subroutine: INVSET)

P67 is set immediately before the subroutine call of the main loop.

P67 is reset immediately after the subroutine call of the main loop.

(2) INTTM7 interrupt processing

At the beginning of interrupt processing, P66 is set.

After the completion of interrupt processing, P66 is restored.

CHAPTER 4 NOTES ON TIME REQUIRED FOR TIMING SET INTERRUPT PROCESSING

In the sample application, the switching timing for PWM output is calculated based on the interrupt processing for each carrier cycle.

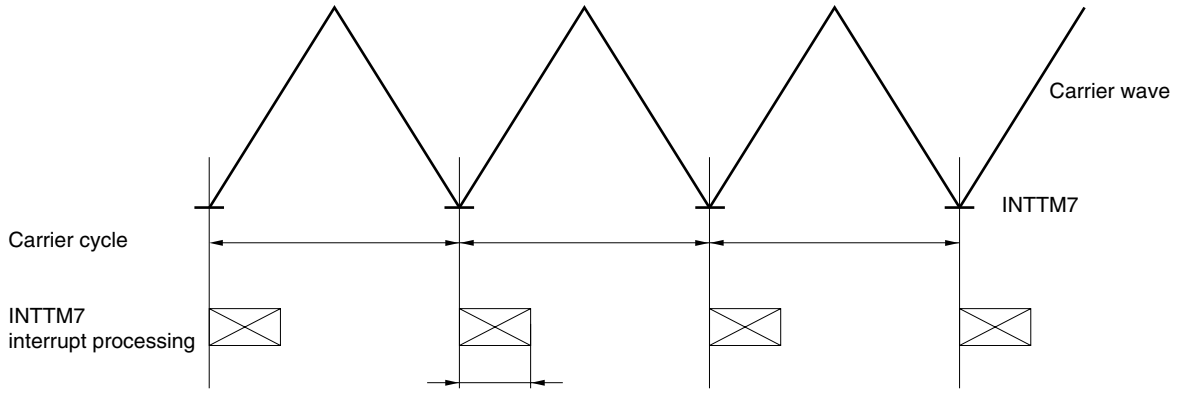
Therefore, the interrupt processing time that must be secured within the carrier cycle is as follows:

★ • 64 μs if TM7 is 8 bits long

★ • 256 μs if TM7 is 10 bits long

Remark TM7: 10-bit inverter control timer

Figure 4-1. Time Required for Timing Set Interrupt Processing



★ However, if TM7 is 8 bits long, a carrier frequency of 15.6 kHz or higher cannot be output. If TM7 is 10 bits long,
★ a carrier frequency of 3.9 kHz or higher cannot be output.

To solve this problem, it is necessary to select the frequency of INTTM7 interrupt occurrences and divide the frequency by an appropriate value.

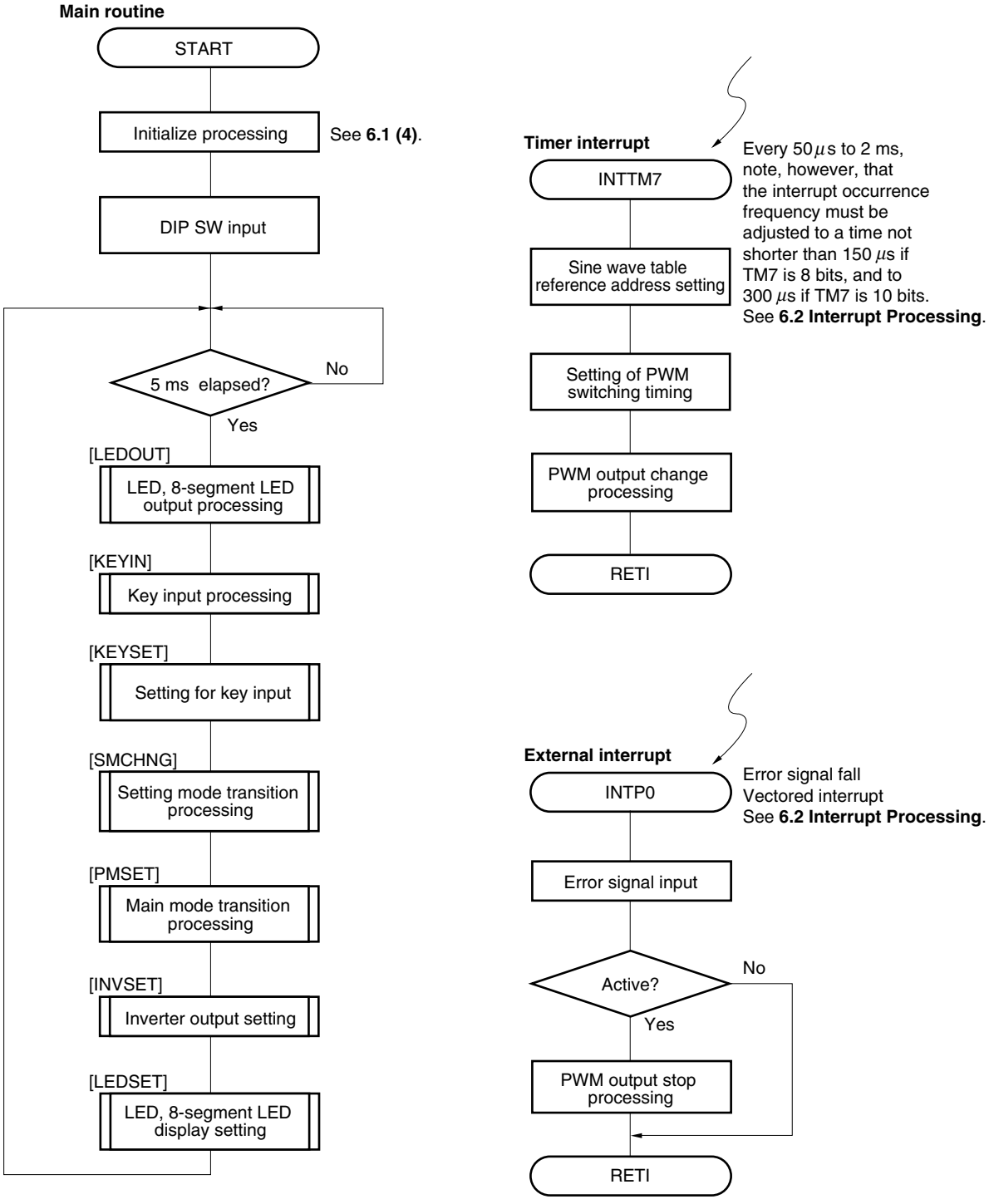
Therefore, the frequency of INTTM7 interrupt occurrences must be specified as listed below:

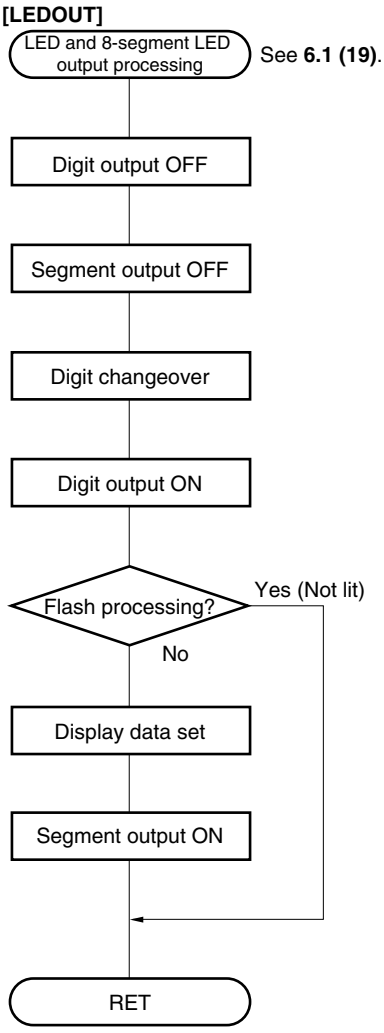
★ • **If TM7 is 8 bits long**

Carrier Frequency	Interrupt Occurrence Frequency
-15.6 kHz	Once
15.6 to 20 kHz	Twice

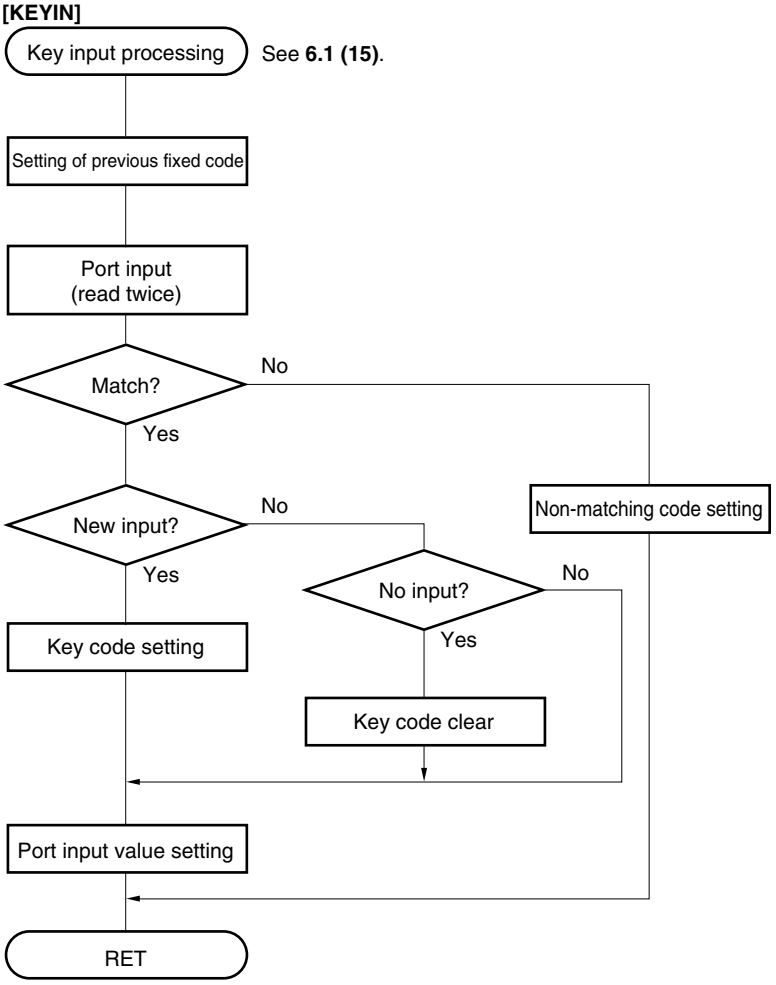
★ • **If TM7 is 10 bits long**

Carrier Frequency	Interrupt Occurrence Frequency
-3.9 kHz	Once
3.9 to 7.8 kHz	Twice
7.9 to 11.7 kHz	Three times
11.8 to 15.6 kHz	Four times
15.7 to 19.5 kHz	Five times

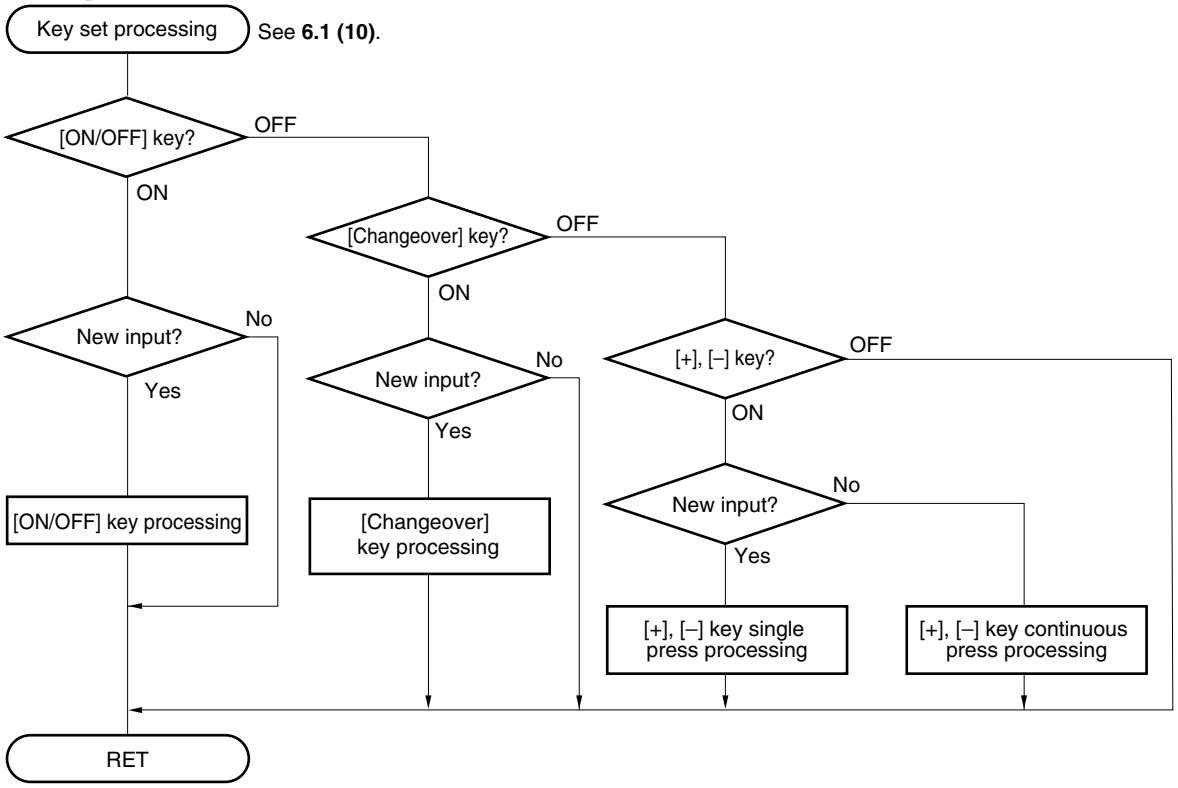

Main routine
START
Initialize processing
See 6.1 (4).
DIP SW input
5 ms elapsed?
No
Yes
[LEDOUT]
LED, 8-segment LED output processing
[KEYIN]
Key input processing
[KEYSET]
Setting for key input
[SMCHNG]
Setting mode transition processing
[PMSET]
Main mode transition processing
[INVSET]
Inverter output setting
[LEDSET]
LED, 8-segment LED display setting
Timer interrupt
INTTM7
Every 50 μs to 2 ms, note, however, that the interrupt occurrence frequency must be adjusted to a time not shorter than 150 μs if TM7 is 8 bits, and to 300 μs if TM7 is 10 bits.
See 6.2 Interrupt Processing.
Sine wave table reference address setting
Setting of PWM switching timing
PWM output change processing
RETI
External interrupt
INTP0
Error signal fall
Vectored interrupt
See 6.2 Interrupt Processing.
Error signal input
Active?
No
Yes
PWM output stop processing
RETI

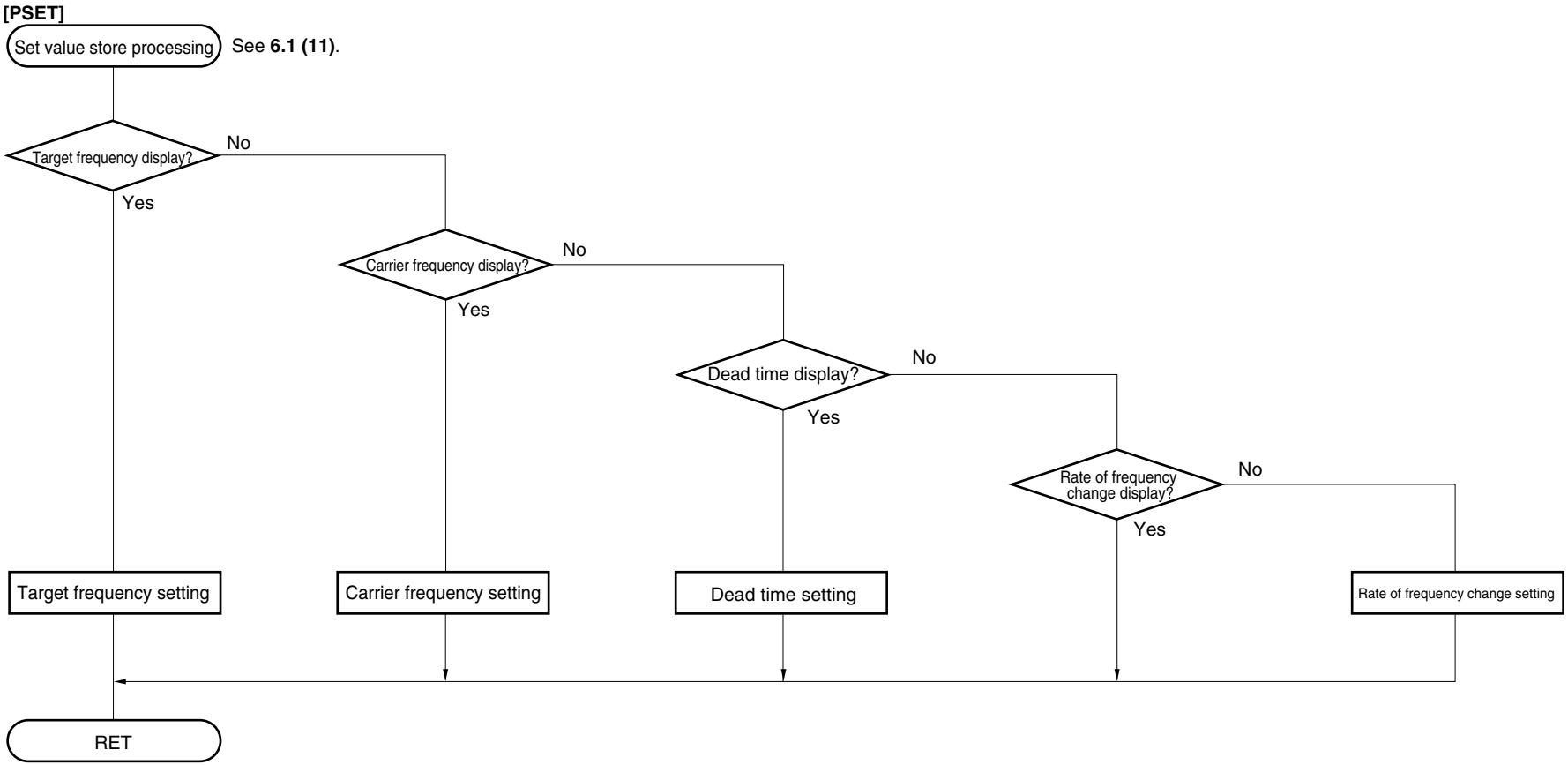

[LEDOUT]
LED and 8-segment LED output processing
See 6.1 (19).
Digit output OFF
Segment output OFF
Digit changeover
Digit output ON
Flash processing?
Yes (Not lit)
No
Display data set
Segment output ON
RET

[KEYIN]

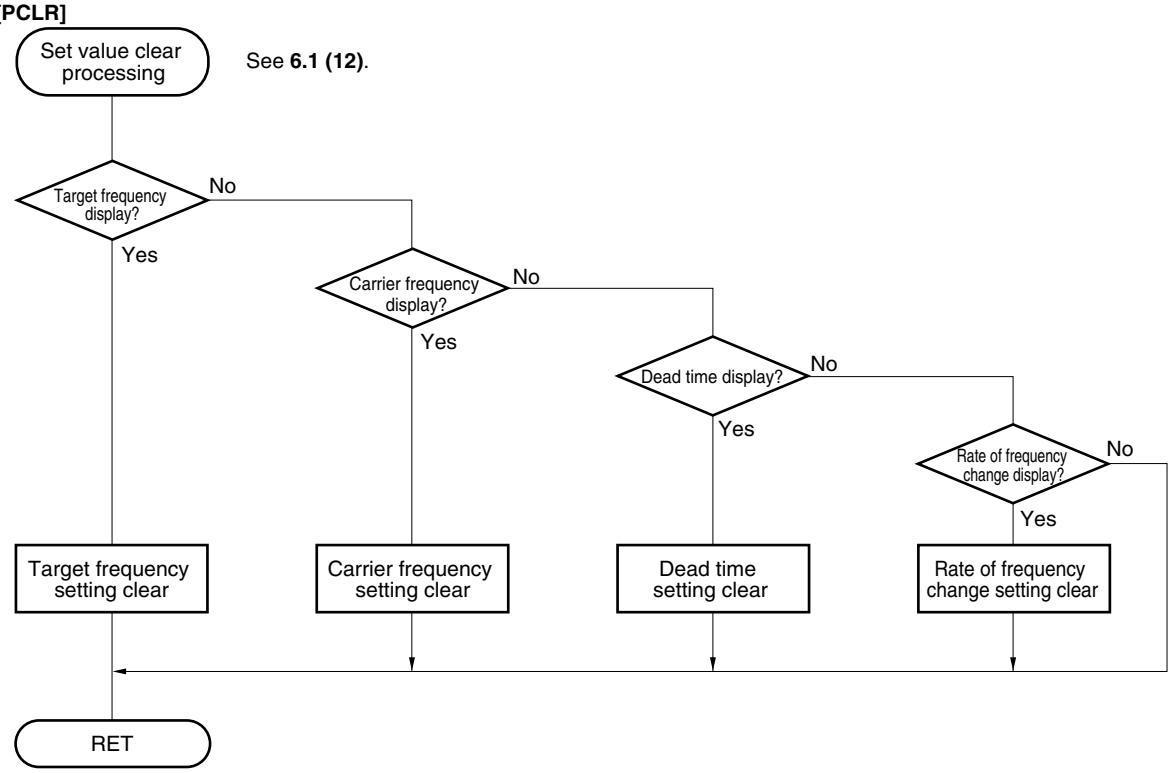

Key input processing
See 6.1 (15).
Setting of previous fixed code
Port input
(read twice)
Match?
No
Yes
New input?
No
Yes
Non-matching code setting
No input?
No
Yes
Key code setting
Key code clear
Port input value setting
RET

[KEYSET]

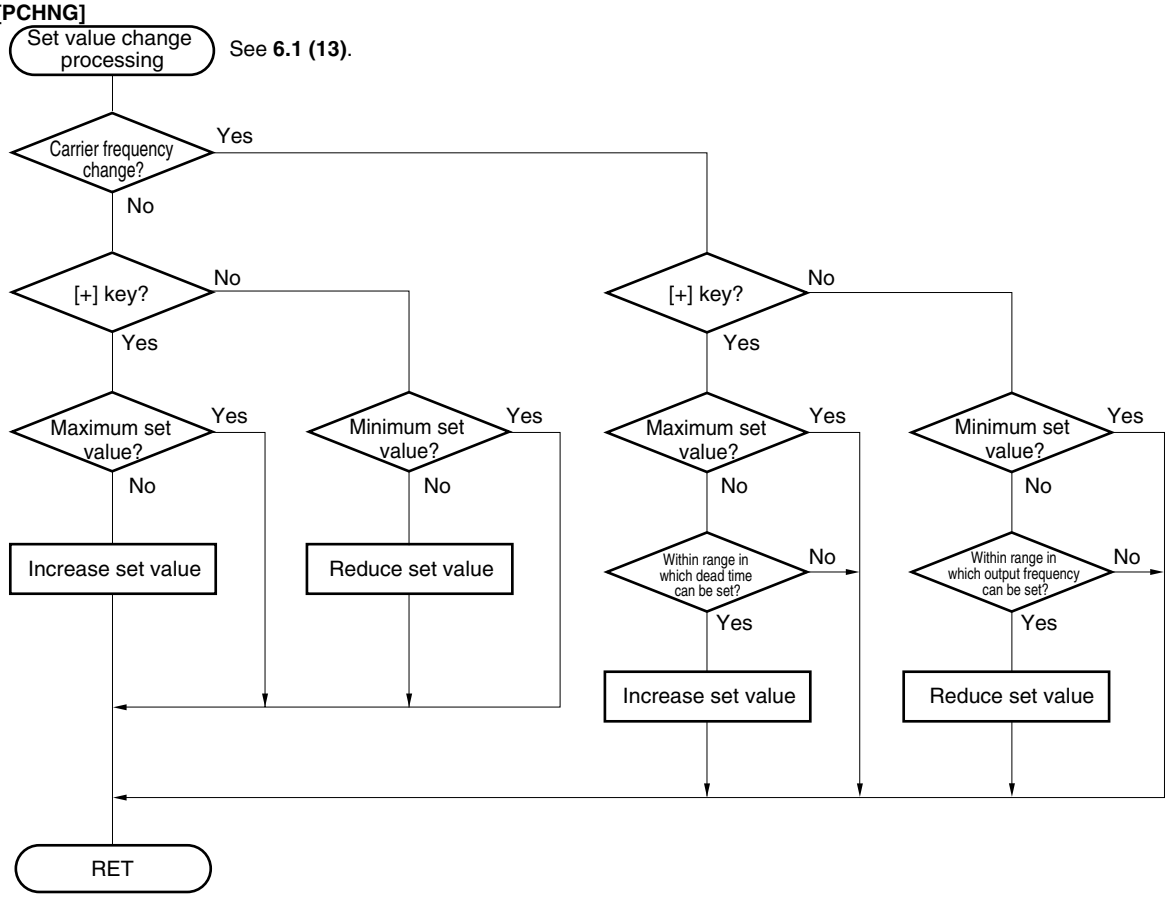

Key set processing
See **6.1 (10)**.
[ON/OFF] key?
OFF
ON
[Changeover] key?
OFF
ON
New input?
No
Yes
New input?
No
Yes
[+], [–] key?
OFF
ON
New input?
No
Yes
[ON/OFF] key processing
[Changeover] key processing
[+], [–] key single press processing
[+], [–] key continuous press processing
RET

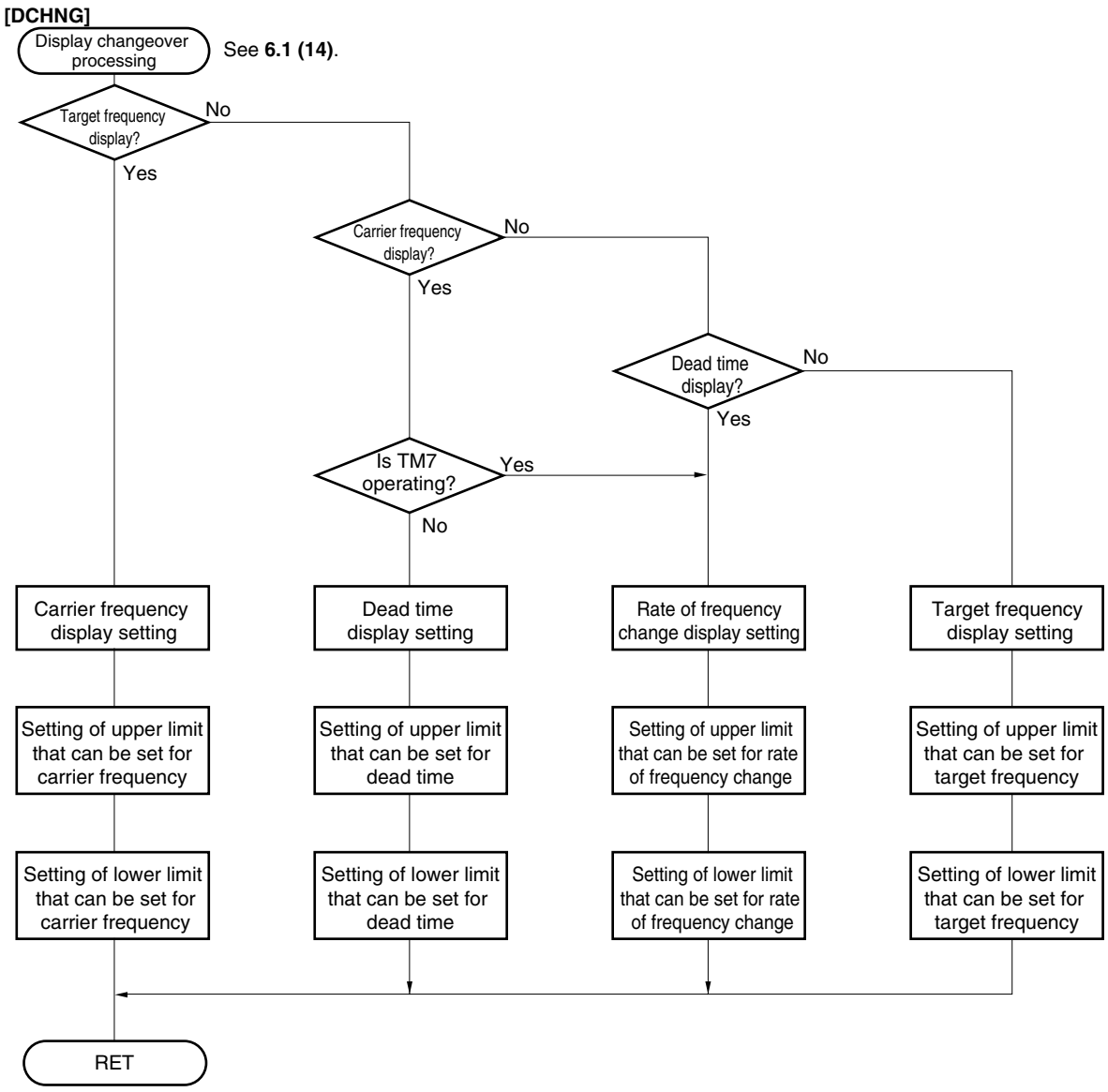

[PSET]
Set value store processing
See 6.1 (11).
Target frequency display?
No
Yes
Carrier frequency display?
No
Yes
Dead time display?
No
Yes
Rate of frequency change display?
No
Yes
Target frequency setting
Carrier frequency setting
Dead time setting
Rate of frequency change setting
RET

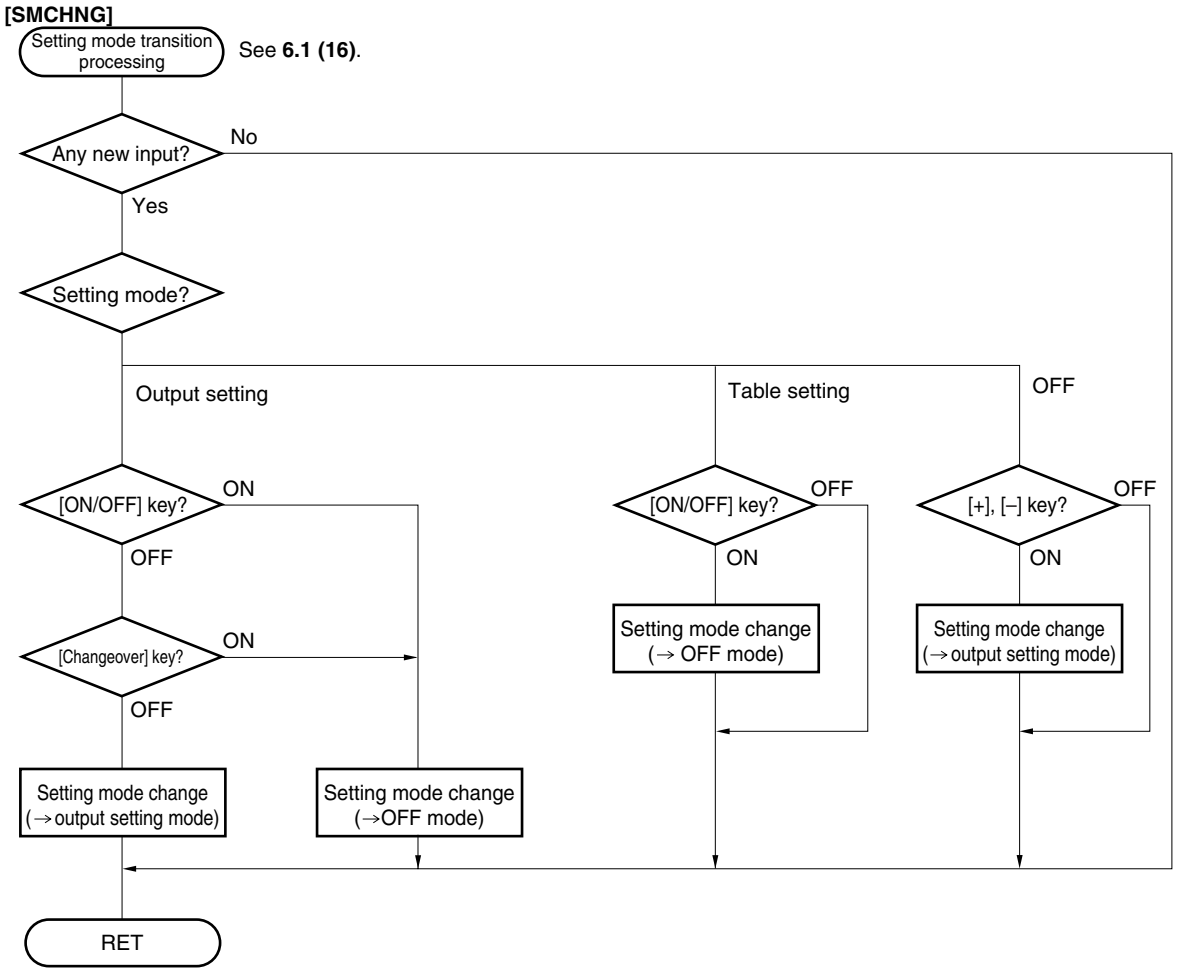
[PCLR]

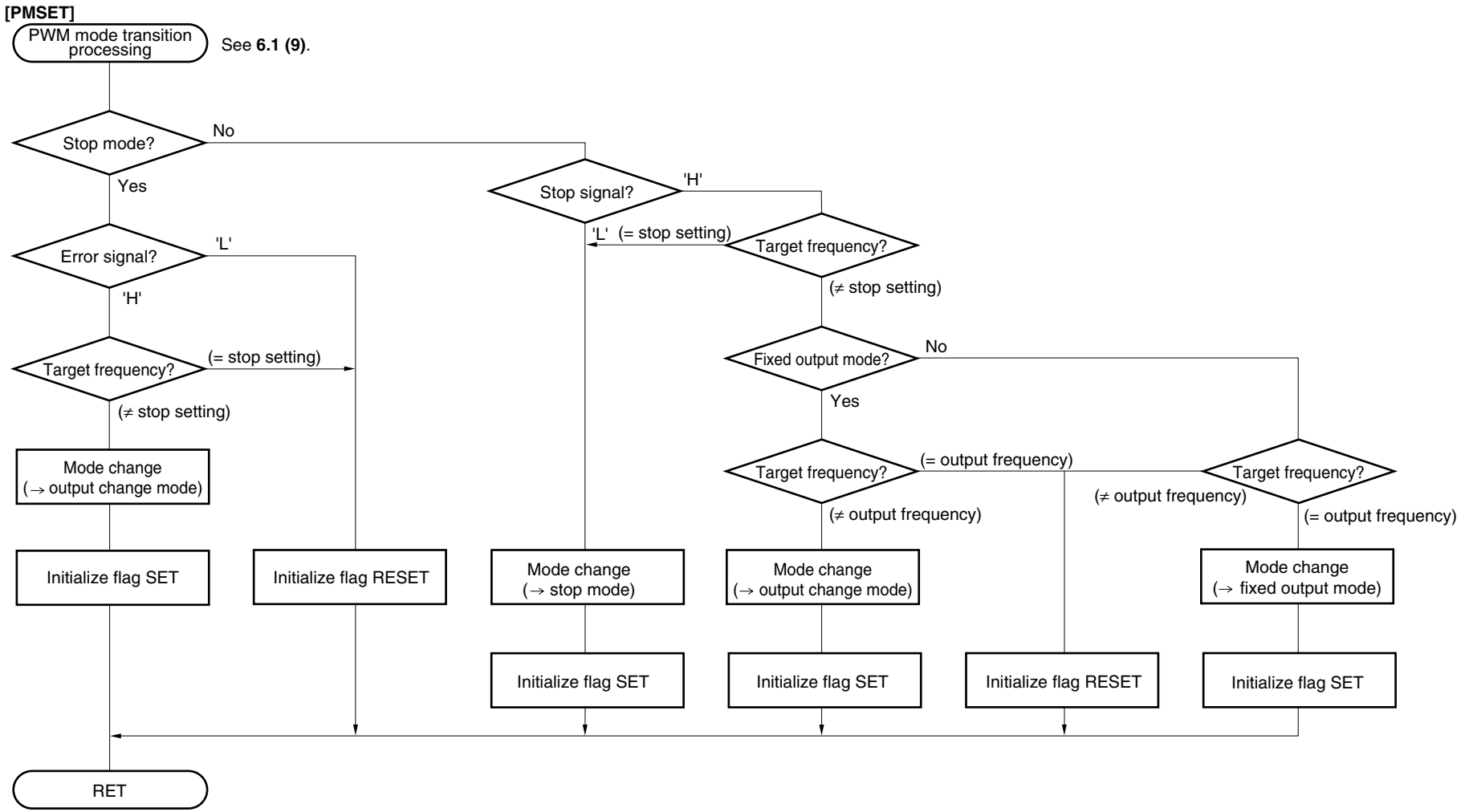

Set value clear processing
See **6.1 (12)**.
Target frequency display?
No
Yes
Carrier frequency display?
No
Yes
Dead time display?
No
Yes
Rate of frequency change display?
No
Yes
Target frequency setting clear
Carrier frequency setting clear
Dead time setting clear
Rate of frequency change setting clear
RET

[PCHNG]

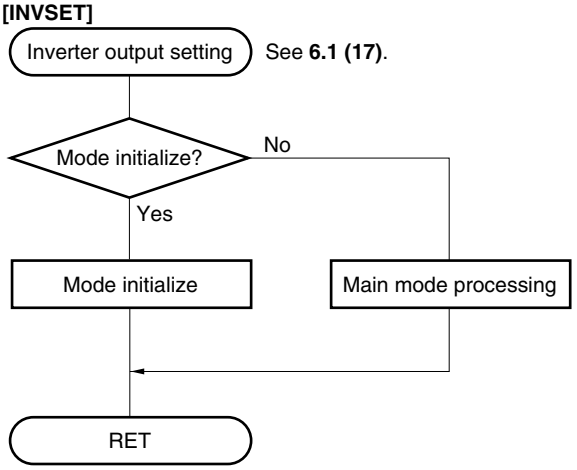

Set value change processing
See **6.1 (13)**.
Carrier frequency change?
Yes
No
[+] key?
No
Yes
Maximum set value?
Yes
No
Minimum set value?
Yes
No
Increase set value
Reduce set value
[+] key?
No
Yes
Maximum set value?
Yes
No
Minimum set value?
Yes
No
Within range in which dead time can be set?
No
Yes
Within range in which output frequency can be set?
No
Yes
Increase set value
Reduce set value
RET

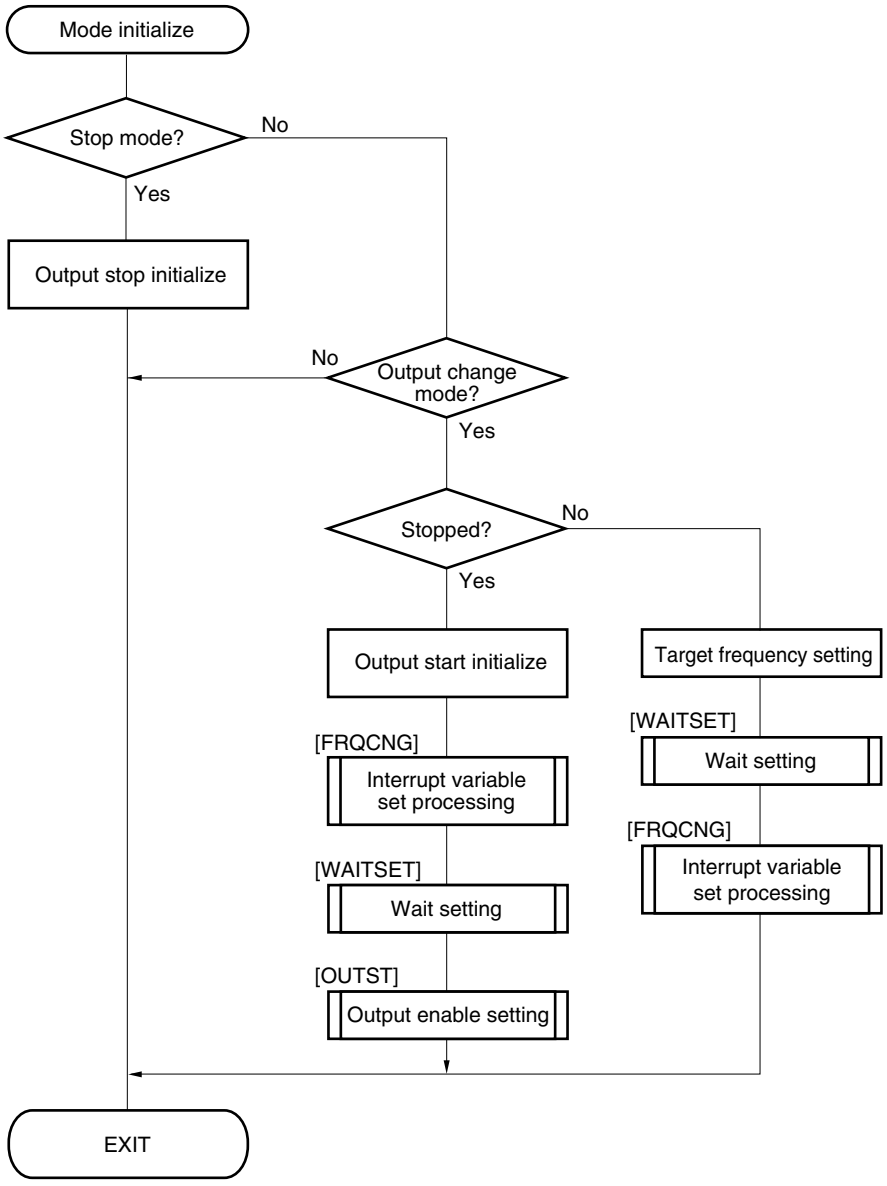

[DCHNG]
Display changeover processing
See 6.1 (14).
Target frequency display?
No
Yes
Carrier frequency display?
No
Yes
Dead time display?
No
Yes
Is TM7 operating?
Yes
No
Carrier frequency display setting
Dead time display setting
Rate of frequency change display setting
Target frequency display setting
Setting of upper limit that can be set for carrier frequency
Setting of upper limit that can be set for dead time
Setting of upper limit that can be set for rate of frequency change
Setting of upper limit that can be set for target frequency
Setting of lower limit that can be set for carrier frequency
Setting of lower limit that can be set for dead time
Setting of lower limit that can be set for rate of frequency change
Setting of lower limit that can be set for target frequency
RET

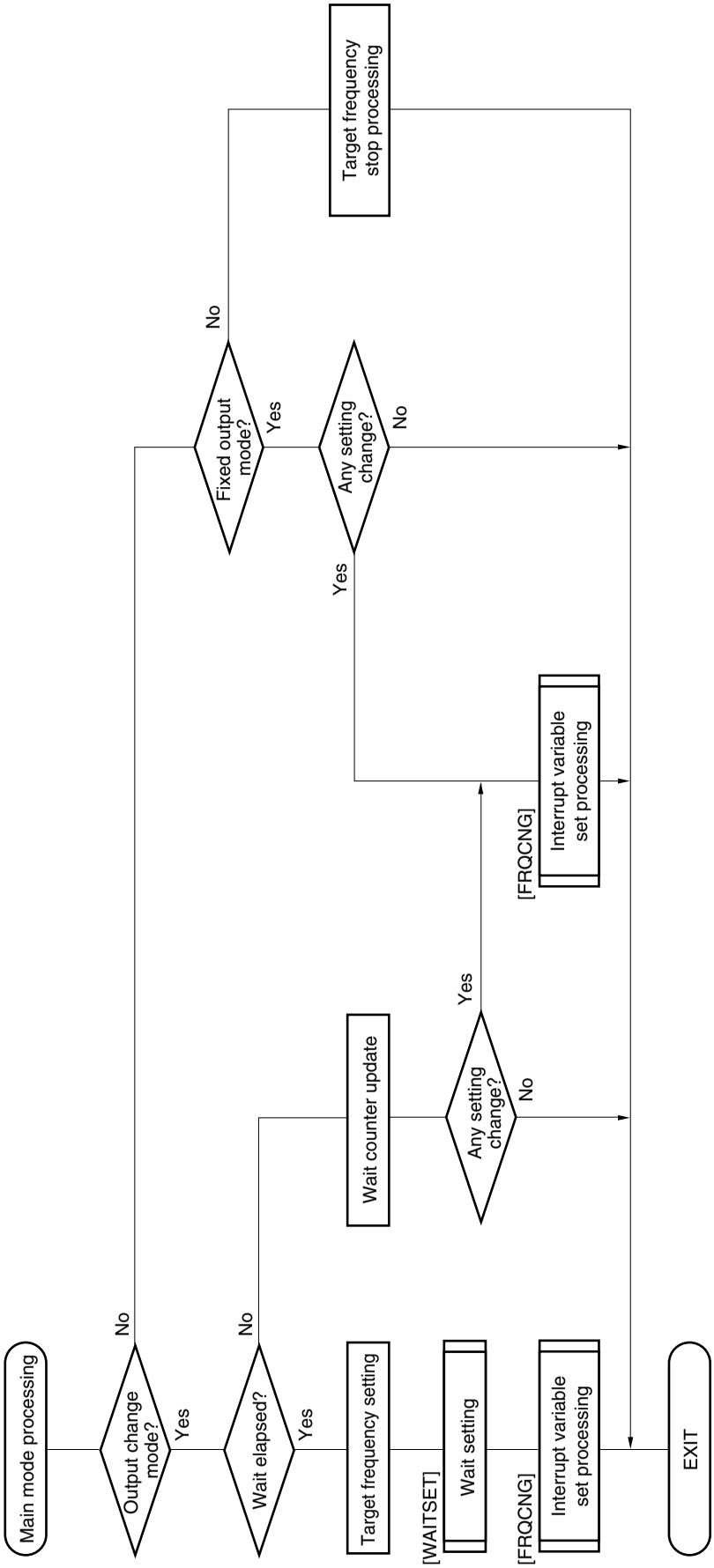

[SMCHNG]
Setting mode transition processing
See 6.1 (16).
Any new input?
No
Yes
Setting mode?
Output setting
Table setting
OFF
[ON/OFF] key?
ON
OFF
[Changeover] key?
ON
OFF
Setting mode change (→ output setting mode)
Setting mode change (→OFF mode)
[ON/OFF] key?
OFF
ON
Setting mode change (→ OFF mode)
[+], [–] key?
OFF
ON
Setting mode change (→output setting mode)
RET

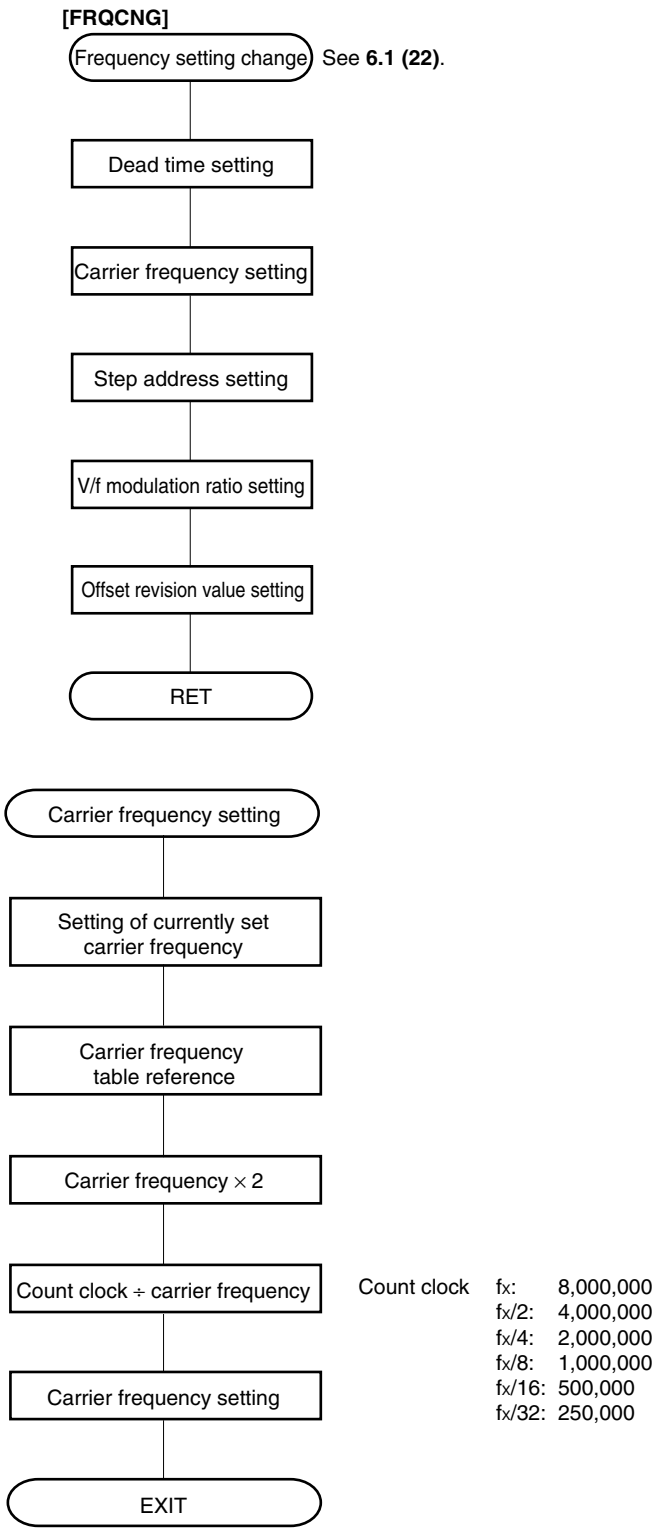

[PMSET]
PWM mode transition processing
See 6.1 (9).
Stop mode?
No
Yes
Stop signal?
'H'
'L' (= stop setting)
Target frequency?
(≠ stop setting)
Error signal?
'L'
'H'
Target frequency?
(= stop setting)
(≠ stop setting)
Fixed output mode?
No
Yes
Target frequency?
(= output frequency)
(≠ output frequency)
Target frequency?
(≠ output frequency)
(= output frequency)
Mode change (→ output change mode)
Initialize flag SET
Initialize flag RESET
Mode change (→ stop mode)
Mode change (→ output change mode)
Mode change (→ fixed output mode)
Initialize flag SET
Initialize flag SET
Initialize flag RESET
Initialize flag SET
RET

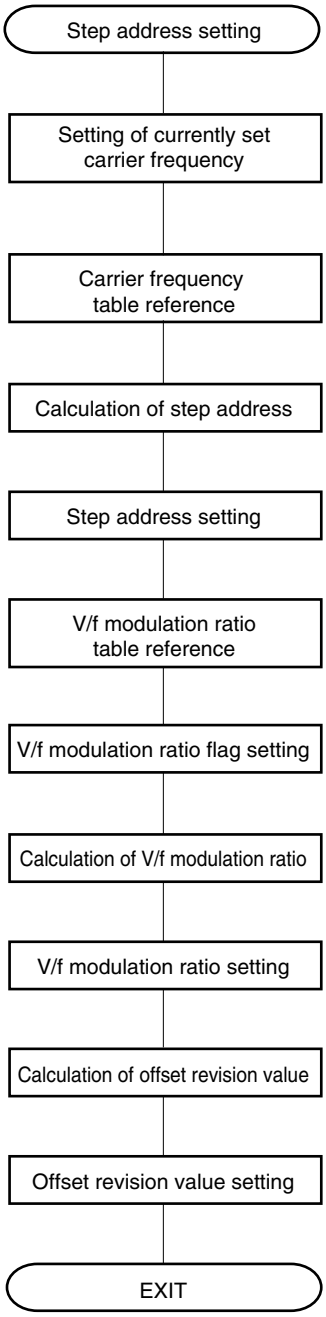
[INVSET]


Inverter output setting
See **6.1 (17)**.
Mode initialize?
No
Yes
Mode initialize
Main mode processing
RET

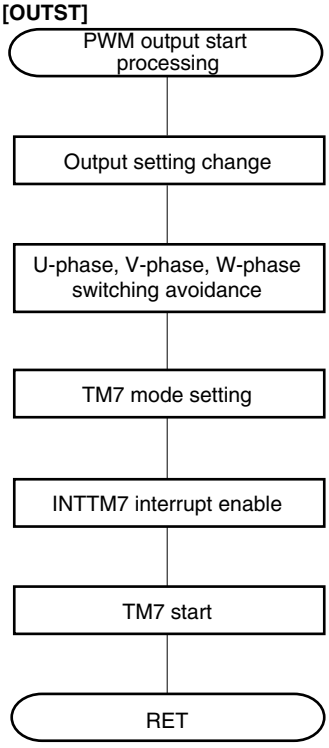

Mode initialize
Stop mode?
No
Yes
Output stop initialize
No
Output change mode?
Yes
Stopped?
No
Yes
Output start initialize
Target frequency setting
[WAITSET]
Wait setting
[FRQCNG]
Interrupt variable set processing
[FRQCNG]
Interrupt variable set processing
[WAITSET]
Wait setting
[OUTST]
Output enable setting
EXIT


Main mode processing
Output change mode?
Yes
No
Wait elapsed?
Yes
No
Target frequency setting
[WAITSET]
Wait setting
[FRQCNG]
Interrupt variable set processing
EXIT
Wait counter update
Any setting change?
Yes
No
[FRQCNG]
Interrupt variable set processing
Fixed output mode?
Yes
No
Any setting change?
Yes
No
Target frequency stop processing

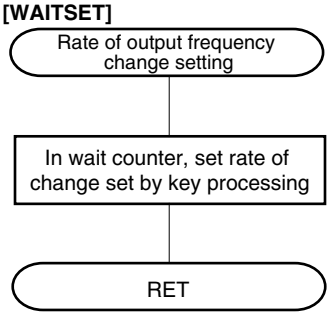

[FRQCNG]
Frequency setting change
See 6.1 (22).
Dead time setting
Carrier frequency setting
Step address setting
V/f modulation ratio setting
Offset revision value setting
RET
Carrier frequency setting
Setting of currently set carrier frequency
Carrier frequency table reference
Carrier frequency × 2
Count clock ÷ carrier frequency
Carrier frequency setting
EXIT
Count clock
fx: 8,000,000
fx/2: 4,000,000
fx/4: 2,000,000
fx/8: 1,000,000
fx/16: 500,000
fx/32: 250,000


Step address setting
Setting of currently set carrier frequency
Carrier frequency table reference
Calculation of step address
Step address setting
V/f modulation ratio table reference
V/f modulation ratio flag setting
Calculation of V/f modulation ratio
V/f modulation ratio setting
Calculation of offset revision value
Offset revision value setting
EXIT

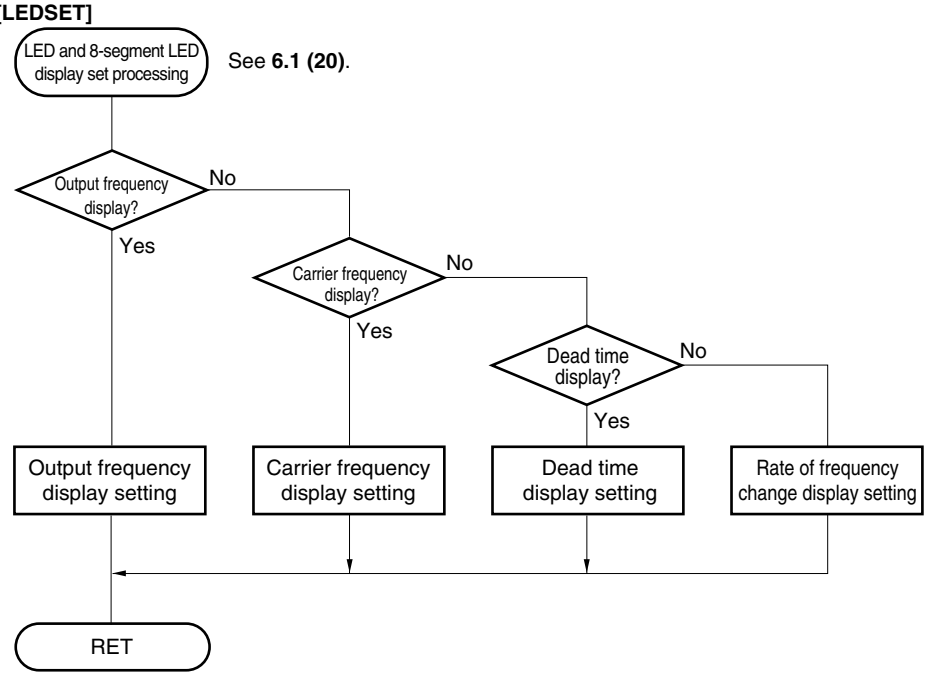
[OUTST]



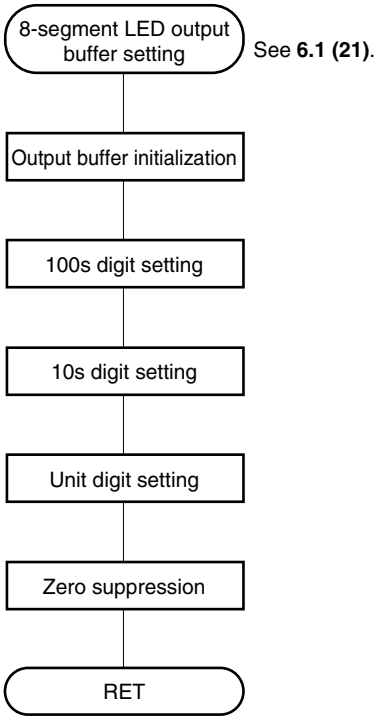
[WAITSET]

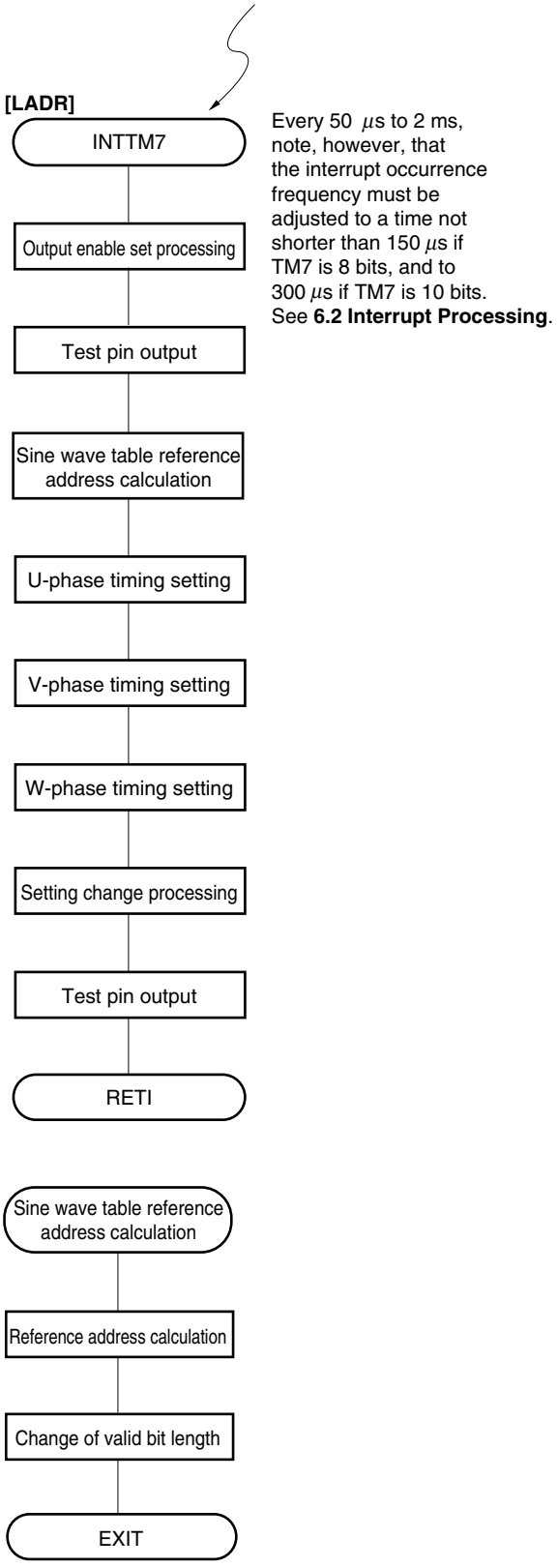


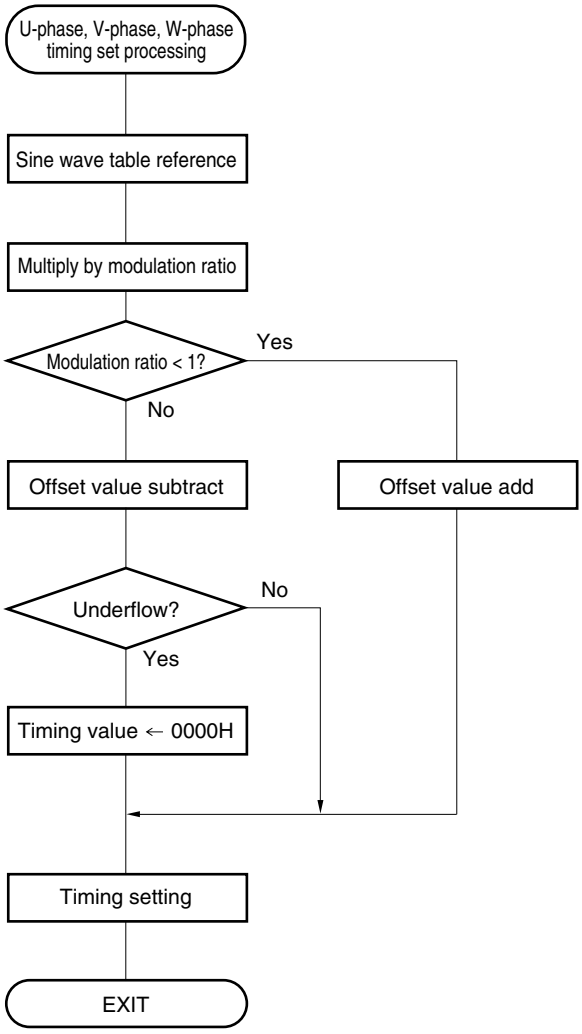
[LEDSET]



[BUFSET]




[LADR]
INTTM7
Output enable set processing
Test pin output
Sine wave table reference address calculation
U-phase timing setting
V-phase timing setting
W-phase timing setting
Setting change processing
Test pin output
RETI
Every 50 μs to 2 ms, note, however, that the interrupt occurrence frequency must be adjusted to a time not shorter than 150 μs if TM7 is 8 bits, and to 300 μs if TM7 is 10 bits. See 6.2 Interrupt Processing.
Sine wave table reference address calculation
Reference address calculation
Change of valid bit length
EXIT


U-phase, V-phase, W-phase timing set processing
Sine wave table reference
Multiply by modulation ratio
Modulation ratio < 1?
Yes
No
Offset value subtract
Offset value add
Underflow?
No
Yes
Timing value ← 0000H
Timing setting
EXIT

CHAPTER 6 PROGRAM LIST

This chapter lists the programs of this application software.

6.1 Main Processing

```
EXTRN   CRRYTBL,VFTBL                       ;  Table
EXTRN   VFTBL1, VFTBL2, VFTBL3, VFTBL4      ;  Table
EXTRN   VFTBL5, VFTBL6, VFTBL7, VFTBL8      ;  Table
EXTRN   CHNGTBL                             ;  Table
EXTRN   LEDTBL, FMXTBL, DMXTBL, CHDSPTBL    ;  Table
EXTRN   TMCLKTBL,CMNTBL10,CMNTBL08          ;  Table
EXTRN   LADR,   INTP0                       ;  Interrupt

PUBLIC  BVF,    VF,     BSADR,  SADR        ;  saddr variable
PUBLIC  BOFFSET,OFFSET, RFOUT               ;  saddr variable
PUBLIC  BCM03                               ;  saddr variable
PUBLIC  IKAKE1, IKAKE2, IKOTAE              ;  saddr variable
PUBLIC  _CHNGST,_BSVF,  _SVF,   _10BIT      ;  Flag
```

(1) Stack area allocation

```
STACK   DSEG AT 0FB00H  ;************ Stack definition
        DS      32
STKINI:
```

(2) Variable definition

```
SDAT    DSEG    SADDR  ;************ Variable definition

PMODE:  DS 1    ; Main mode
RFOUT:  DS 1    ; Target frequency
NFOUT:  DS 1    ; Output frequency
NCRRY:  DS 1    ; Carrier frequency
NDEAD:  DS 1    ; Dead time
NCHNG:  DS 1    ; Change rate
NSET:   DS 1    ; Setting number
NSETMN: DS 1    ; Maximum setting number
NSETMX: DS 1    ; Minimum setting number
SFOUT:  DS 1    ; Carrier frequency buffer
KIN:    DS 1    ; Port input pattern
SMODE:  DS 1    ; Key input setting mode
DMODE:  DS 1    ; SEG LED display mode
DUMMY:  DS 1

WAITCNT:DS 2    ; Wait counter
BSADR:  DS 2    ; Step address buffer
BVF:    DS 2    ; Modulation ratio buffer
BCM03:  DS 2    ; CM03 buffer
BOFFSET:DS 2    ; V/f offset revision value buffer

SADR:   DS 2    ; Step address
VF:     DS 2    ; Modulation ratio
VFP:    DS 2    ; V/f modulation ratio data pointer
OFFSET: DS 2    ; V/f offset revision value buffer

MKAKE1: DS 2    ; Multiplicand area (2 bytes) for main processing
MKAKE2: DS 2    ; Multiplier area (2 bytes) for main processing
MKOTAE: DS 4    ; Calculation result storage area (4 bytes) for main processing
IKAKE1: DS 2    ; Multiplicand area (2 bytes) for interrupt processing
IKAKE2: DS 2    ; Multiplier area (2 bytes) for interrupt processing
IKOTAE: DS 4    ; Calculation result storage area (4 bytes) for interrupt processing
WARU1:  DS 4    ; Dividend area (4 bytes)
WARU2:  DS 2    ; Divider area (2 bytes)
AMARI:  DS 2    ; Remainder storage area (2 bytes)

VFTBLNO:DS 2    ; V/f table selection
TM7CLK: DS 1    ; TM7 count clock selection
TM7CNT: DS 1    ; INTTM7 occurrence frequency selection

BDTIME: DS 1    ; Dead time counter
SEGBUF: DS 3    ; SEG LED display buffer
SEGCNT: DS 1    ; SEG LED flash counter
LEDCNT: DS 1    ; LED flash counter
KSMPCNT:DS 1    ; Key input sampling counter
KONCNT: DS 1    ; Hold-down counter
KCODE1: DS 1    ; Key code buffer 1
KCODE2: DS 1    ; Key code buffer 2
PSMPCNT:DS 1    ; Stop signal sampling counter
```

```
FLAG    BSEG UNIT
_CHNGST DBIT    ; Frequency change request
_LEDOUT DBIT    ; LED output
_MINIT  DBIT    ; PWM mode initialization
_PCHNG  DBIT    ; PWM variable change
_SVF    DBIT    ; V/f modulation ratio (0:  Modulation ratio < 1)
_BSVF   DBIT    ; V/f modulation buffer
_10BIT  DBIT    ; Flag to indicate whether timer 7 is 10 or 8 bits
_VFON   DBIT    ; V/f control selection flag
```

(3) Vector table

```
; ********************************************
; *                Vector table              *
; ********************************************

VERESET         CSEG    AT 0000H

        DW      RESTART                 ; Reset start
        DW      RESTART                 ;  Dummy
        DW      RESTART                 ;  0 INTWDT
        DW      INTP0                   ;  1 INTP0
        DW      RESTART                 ;  2 INTP1
        DW      RESTART                 ;  3 INTP2
        DW      RESTART                 ;  4 INTP3
        DW      LADR                    ;  5 INTTM7
        DW      RESTART                 ;  6 INTSER0
        DW      RESTART                 ;  7 INTSR0
        DW      RESTART                 ;  8 INTST0
        DW      RESTART                 ;  9 INTSER1
        DW      RESTART                 ; 10 INTSR1
        DW      RESTART                 ; 11 INTST1
        DW      RESTART                 ; 12 INTTM50
        DW      RESTART                 ; 13 INTTM51
        DW      RESTART                 ; 14 INTTM52
        DW      RESTART                 ; 15 INTAD0

VDIBRK          CSEG    AT 003EH

        DW      RESTART                 ; BRK

MAINRUT         CSEG    AT 80H          ; MAIN START Address 80H
```

(4) Initialization

```
; ***********************************************
; *              Initialization                 *
; ***********************************************

RESTART:
        DI                              ;

; ***  Stack pointer initialization  ***

        MOVW    SP,#STKINI              ;

; ***      Register bank setting     ***

        SEL     RB0                     ; Register bank = 0

; ***       CPU clock setting        ***

        MOV     PCC,#00000000B          ; CPU clock = fx (8 MHz:  0.25 μs)

; ***       Port initialization      ***

        ; ///// Expansion mode setting /////

        MOV     MM,#00000000B           ;
        MOV     MEM,#00000000B          ;

        ; ///// Port setting /////
                                        ; Port latch setting
        MOV     P0,#00000000B           ; Input port
        MOV     P2,#00000000B           ; Input port
        MOV     P3,#00000000B           ; Input port
        MOV     P4,#00000000B           ; P40 to P47:  Low output
        MOV     P5,#00000001B           ; P50:  High, P51 to P53:  Low
        MOV     P6,#00010000B           ; P64:  High, P65 to P67:  Low
                                        ; Port mode setting
        MOV     PM0,#11111111B          ; Input mode
        MOV     PM2,#11111111B          ; Input mode
        MOV     PM3,#11111111B          ; Input mode
        MOV     PM4,#00000000B          ; Output mode
        MOV     PM5,#11110000B          ; P50 to P53:  Output mode
        MOV     PM6,#00001111B          ; P64 to P67:  Output mode
                                        ; Pull-up resistor setting
        MOV     PU0,#00000000B          ; Not to be used
        MOV     PU2,#00000000B          ; Not to be used
        MOV     PU3,#00000000B          ; Not to be used
        MOV     PU4,#00000000B          ; Not to be used
        MOV     PU5,#00000000B          ; Not to be used
        MOV     PU6,#00000000B          ; Not to be used

        ; ///// Priority specification flag clearing /////

        MOV     PR0L,#0FFH              ;
        MOV     PR0H,#0FFH              ;
```

```
        ; ///// External interrupt valid edge setting /////

        MOV     EGP,#00000000B          ;
        MOV     EGN,#00000001B          ; INTP0 Low Active
```

(5) RAM initialization

```
; ********************************************
; *              RAM initialization          *
; ********************************************

; **********   RAM clearing   **********

RAMCLR:
        MOV     A,#00H
        MOVW    HL,#0FEF7H
RAMCLR0:
        MOV     [HL],A
        DEC     L
        BNZ     $RAMCLR0
```

(6) DIP SW input

```
; ***********************************************
; *                 DIP SW input                *
; ***********************************************

INIT:
        MOV     A,P1
        XOR     A,#0FFH

SW_IN_1:
        BF      A.7,$SW_IN_2
        SET1    _10BIT
SW_IN_2:
        BF      A.6,$SW_IN_3
        SET1    _VFON
SW_IN_3:
        AND     A,#00111111B
        MOV     B,A
        AND     A,#00000111B
        INC     A
        MOV     TM7CNT,A

        MOV     A,B
        ROR     A,1
        ROR     A,1
        ROR     A,1
        AND     A,#00000111B
        MOV     TM7CLK,A

; **********     Vf table selection SW input     **********

        MOV     A,P2
        XOR     A,#0FFH
        AND     A,#00000111B
        ROL     A,1                     ; A = A x 2
        MOV     C,A
        MOVW    HL,#VFTBL
        MOV     A,[HL+C]
        MOV     X,A
        INC     C
        MOV     A,[HL+C]
        MOVW    VFTBLNO,AX
```

(7) RAM initialization

```
; ********************************************
; *              RAM initialization          *
; ********************************************

        MOV     PMODE,#PMSTOP    ; Main mode:  Output stop
        MOV     DMODE,#DMFOUT    ; Display mode:  Output frequency
        MOV     SMODE,#SMOFF     ; Setting mode:  OFF
        MOV     NDEAD,#5         ; Dead time initialization
        MOV     NCHNG,#0         ; Frequency change rate initialization

        MOV     A,TM7CLK
        MOV     C,A
        MOVW    HL,#CMNTBL10
        BT      _10BIT,$RAMSET1
        MOVW    HL,#CMNTBL08
RAMSET1:
        MOV     A,[HL+C]
        MOV     NCRRY,A          ; Carrier frequency initialization
        MOV     C,A
        MOVW    HL,#FMXTBL
        MOV     A,[HL+C]
        MOV     NSET,A           ; Initialization display No.
        MOV     SFOUT,A          ; Target frequency initialization
        MOV     NSETMX,A         ; Target frequency upper limit setting
        MOV     NSETMN,#4        ; Target frequency lower limit setting

        MOV     NFOUT,#FRQSTOP   ; Output frequency:  Stop setting
        MOV     RFOUT,#FRQSTOP   ; Target frequency:  Stop setting
        MOV     KSMPCNT,#3       ; Key input sampling counter setting
        MOV     PSMPCNT,#1       ; Stop signal sampling counter setting
        MOV     SEGCNT,#80H+SEGINI   ; 8-segment LED flash counter setting
        MOV     LEDCNT,#80H+LEDINI   ; LED flash counter setting
        MOV     SEGBUF,#CHRSPC       ; 8-segment LED display buffer 1:  " "
        MOV     SEGBUF+1,#CHRSPC     ; 8-segment LED display buffer 2:  " "
        MOV     SEGBUF+2,#CHRSPC     ; 8-segment LED display buffer 3:  " "
```

(8) SFR initialization

```
; ***********************************************
; *              SFR initialization             *
; ***********************************************

        MOV     A,B
        MOV     TMC7,A

        MOV     TMM7,#00000000B  ;

        CLR1    PIF0
        CLR1    PMK0            ; INTP0 (motor failure detection) interrupt enable
        EI

MLOOP:          ;************ Main loop
        BTCLR   TMIF50,$MLOOP1   ; 5 ms elapsed (main processing execution)
        NOP
        NOP
        NOP
        BR      MLOOP
MLOOP1:
        CLR1    P6.7        ; Turn on LED for main processing time measurement output
        CALL    !LEDOUT     ; LED and 8-segment LED output processing
        CALL    !KEYIN      ; Key input processing
        CALL    !KEYSET     ; Key setting
        CALL    !SMCHNG     ; Setting mode transition processing
        CALL    !PMSET      ; Main mode transition processing
        CALL    !INVSET     ; Inverter output setting
        CALL    !LEDSET     ; LED and 8-segment LED display setting
        SET1    P6.7        ; Turn off LED for main processing time measurement output
        BR      MLOOP
```

(9) PWM mode transition processing

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS    PWM mode transition processing   SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
PMSET:          ;************    ; Branch for output stop mode
        CMP     PMODE,#PMSTOP
        BNZ     $PMSET2
PMSET0:
        MOV1    CY,P0.0          ; Stop signal input (first time)
        MOV1    A.0,CY
        MOV     B,#1
PMSETW1:
        DBNZ    B,$PMSETW1
        XOR1    CY,P0.0          ; Stop signal input (second time)
        BC      $PMSET0
        BF      A.0,$PMSET1      ; Stop signal active?
        CMP     RFOUT,#FRQSTOP   ; Frequency stop setting?
        BZ      $PMSET1
        MOV     PMODE,#PMCHNG
        SET1    _MINIT
        BR      $PMSET6
PMSET1:
        CLR1    _MINIT
        BR      $PMSET6
PMSET2:         ;************ Branch for output
        MOV1    CY,P0.0          ; Stop signal input (first time)
        MOV1    A.0,CY
        MOV     B,#1
PMSETW2:
        DBNZ    B,$PMSETW2
        XOR1    CY,P0.0          ; Stop signal input (second time)
        BC      $PMSET2
        BT      A.0,$PMSET4
PMSET3:         ;************ Stop directed by stop signal
        MOV     PMODE,#PMSTOP    ; Stop mode setting
        SET1    _MINIT
        BR      $PMSET6
PMSET4:
        CMP     RFOUT,#FRQSTOP   ; Stop setting?
        BZ      $PMSET3
        CMP     PMODE,#PMFOUT
        BNZ     $PMSET5
        MOV     A,RFOUT
        CMP     A,NFOUT
        BZ      $PMSET1
        MOV     PMODE,#PMCHNG
        SET1    _MINIT
        BR      $PMSET6
PMSET5:
        MOV     A,RFOUT
        CMP     A,NFOUT
        BNZ     $PMSET1
        MOVW    WAITCNT,#0
        BNZ     $PMSET1
        MOV     PMODE,#PMFOUT
        SET1    _MINIT
PMSET6:
        RET
```

(10) Key setting

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS             Key setting             SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
KEYSET:         ;************ [ON/OFF] key setting
        CMP     KCODE2,#KONOF    ; [ON/OFF] key pressed?
        BNZ     $KEYSET1
        MOV     A,KCODE1
        CMP     A,KCODE2
        BZ      $KEYSET6
        CMP     SMODE,#SMOFF
        BZ      $KEYSET7
        CALL    !PSET            ; Set value store subroutine
        BR      $KEYSET6
KEYSET7:
        CMP     PMODE,#PMSTOP
        BZ      $KEYSET10
        MOV     RFOUT,#FRQSTOP
        BR      $KEYSET6
KEYSET10:
        MOV     A,SFOUT
        MOV     RFOUT,A
        CMP     DMODE,#DMDEAD
        BNZ     $KEYSET6
        MOV     DMODE,#DMFOUT
        MOV     NSET,A
        MOV     A,NCRRY
        ;@MOV   A,FMXTBL[A]
         MOV    C,A
         MOVW   HL,#FMXTBL
         MOV    A,[HL+C]
        MOV     NSETMX,A         ; Upper limit setting
        MOV     NSETMN,#4        ; Lower limit setting
        BR      $KEYSET6
KEYSET1:        ;************ [Changeover] key setting
        CMP     KCODE2,#KCHNG    ; [Changeover] key pressed?
        BNZ     $KEYSET3
        MOV     A,KCODE1
        CMP     A,KCODE2
        BZ      $KEYSET6
        CMP     SMODE,#SMOFF
        BZ      $KEYSET2
        CALL    !PCLR            ; Set value clear subroutine
        BR      $KEYSET6
KEYSET2:
        CALL    !DCHNG
        BR      $KEYSET6
KEYSET3:        ;************ [+], [-] key setting
        BF      KCODE2.1,$KEYSET6
        MOV     A,KCODE1
        CMP     A,KCODE2
        BZ      $KEYSET4
        MOV     KONCNT,#KONINI
        BR      $KEYSET5
```

```
KEYSET4:
        BF      DMODE.4,$KEYSET6
        DBNZ    KONCNT,$KEYSET6
        MOV     KONCNT,#KONRES
KEYSET5:
        MOV     SEGCNT,#80H+SEGINI
        CALL    !PCHNG          ; Set value change subroutine
KEYSET6:
        RET
```

(11) Set value store subroutine

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss      Set value store subroutine     ss
        ;sssssssssssssssssssssssssssssssssssssss
PSET:           ;************ Target frequency setting
        CMP     DMODE,#DMFOUT   ; Target frequency display?
        BNZ     $PSET1
        MOV     A,NSET
        MOV     SFOUT,A         ; Target frequency setting
        CMP     PMODE,#PMSTOP
        BZ      $PSET5
        MOV     A,NSET
        MOV     RFOUT,A
        BR      $PSET5
PSET1:          ;************ Carrier frequency setting
        CMP     DMODE,#DMCRRY   ; Carrier frequency display?
        BNZ     $PSET2
        MOV     A,NSET
        MOV     NCRRY,A         ; Carrier frequency setting
        BR      $PSET5
PSET2:          ;************ Dead time setting
        CMP     DMODE,#DMDEAD   ; Dead time display?
        BNZ     $PSET3
        MOV     A,NSET
        MOV     NDEAD,A         ; Dead time setting
        BR      $PSET5
PSET3:          ;************ Setting of rate of frequency change
        MOV     A,NSET
        MOV     NCHNG,A         ; Setting of rate of frequency change
PSET5:
        CMP     PMODE,#PMSTOP
        BZ      $PSET6
        SET1    _PCHNG
PSET6:
        RET
```

(12) Set value clear subroutine

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss      Set value clear subroutine     ss
        ;sssssssssssssssssssssssssssssssssssssss
PCLR:           ;************ Target frequency setting clear processing
        CMP     DMODE,#DMFOUT    ; Target frequency display?
        BNZ     $PCLR1
        MOV     A,SFOUT
        MOV     NSET,A           ; Target frequency setting clear
        BR      $PCLR4
PCLR1:          ;************ Carrier frequency setting clear processing
        CMP     DMODE,#DMCRRY    ; Carrier frequency display?
        BNZ     $PCLR2
        MOV     A,NCRRY
        MOV     NSET,A           ; Carrier frequency setting clear
        BR      $PCLR4
PCLR2:          ;************ Dead time setting clear processing
        CMP     DMODE,#DMDEAD    ; Dead time display?
        BNZ     $PCLR3
        MOV     A,NDEAD
        MOV     NSET,A           ; Dead time setting clear
        BR      $PCLR4
PCLR3:          ;************ Setting clear processing of rate of frequency change
        CMP     DMODE,#DMCHNG    ; Display of frequency change rate?
        BNZ     $PCLR4
        MOV     A,NCHNG
        MOV     NSET,A           ; Clear frequency change rate setting
PCLR4:
        RET
```

(13) Set value change subroutine

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss     Set value change subroutine     ss
        ;sssssssssssssssssssssssssssssssssssssss
PCHNG:          ;************ Changing set values other than carrier frequency
        CMP     DMODE,#DMCRRY
        BZ      $PCHNG2
        CMP     KCODE2,#KPLUS
        BNZ     $PCHNG1
                ;************ [+] key processing
        MOV     A,NSET
        CMP     A,NSETMX        ; Maximum set value?
        BZ      $PCHNG4
        ADD     NSET,#1         ; Increase set value
        BR      $PCHNG4
PCHNG1:         ;************ [-] key processing
        MOV     A,NSET
        CMP     A,NSETMN        ; Minimum set value?
        BZ      $PCHNG4
        SUB     NSET,#1         ; Decrease set value
        BR      $PCHNG4
PCHNG2:         ;************ Changing set value of carrier frequency
        CMP     KCODE2,#KPLUS
        BNZ     $PCHNG3
                ;************ [+] key processing
        MOV     A,NSET
        CMP     A,NSETMX        ; Maximum set value?
        BZ      $PCHNG4
        MOV     A,NSET
        INC     A
        ;@MOV   A,DMXTBL[A]
         MOV    C,A
         MOVW   HL,#DMXTBL
         MOV    A,[HL+C]
        CMP     A,NDEAD
        BC      $PCHNG4
        INC     NSET
        BR      $PCHNG4
PCHNG3:         ;************ [-] key processing
        MOV     A,NSET
        CMP     A,NSETMN        ; Minimum set value?
        BZ      $PCHNG4
        MOV     A,NSET
        DEC     A
        ;@MOV   A,FMXTBL[A]
         MOV    C,A
         MOVW   HL,#FMXTBL
         MOV    A,[HL+C]
        CMP     A,SFOUT
        BC      $PCHNG4
        DEC     NSET
PCHNG4:
        RET
```

(14) Display changeover processing

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss    Display changeover processing    ss
        ;sssssssssssssssssssssssssssssssssssssss
DCHNG:          ;************ Target frequency to carrier frequency
        CMP     DMODE,#DMFOUT    ; Display target frequency?
        BNZ     $DCHNG1
        MOV     DMODE,#DMCRRY    ; Carrier frequency display setting
        MOV     A,TM7CLK
        MOV     C,A
        MOVW    HL,#CMNTBL10
        BT      _10BIT,$DCHNG01
        MOVW    HL,#CMNTBL08
DCHNG01:
        MOV     A,[HL+C]
        MOV     NSETMX,#100      ; Upper limit setting
        MOV     NSETMN,A         ; Lower limit setting
        MOV     A,NCRRY
        MOV     NSET,A
        BR      DCHNG4
DCHNG1:         ;************ Carrier frequency to dead time
        CMP     DMODE,#DMCRRY    ; Display carrier frequency?
        BNZ     $DCHNG2
        CMP     PMODE,#PMSTOP    ; PWM operating?
        BNZ     $DCHNG21
        MOV     DMODE,#DMDEAD    ; Dead time display setting
        MOV     A,NCRRY
        ;@MOV   A,DMXTBL[A]
         MOV    C,A
         MOVW   HL,#DMXTBL
         MOV    A,[HL+C]
        MOV     NSETMX,A         ; Upper limit setting
        MOV     NSETMN,#DEADMN1
        MOV     A,NDEAD
        MOV     NSET,A
        BR      DCHNG4
DCHNG2:         ;************ Dead time to frequency change rate
        CMP     DMODE,#DMDEAD    ; Display dead time?
        BNZ     $DCHNG3
DCHNG21:
        MOV     DMODE,#DMCHNG    ; Frequency change rate display setting
        MOV     NSETMX,#3        ; Upper limit setting
        MOV     NSETMN,#0        ; Lower limit setting
        MOV     A,NCHNG
        MOV     NSET,A
        BR      $DCHNG4
DCHNG3:         ;************ Frequency change rate to target frequency
        MOV     DMODE,#DMFOUT    ; Target frequency display setting
        MOV     A,NCRRY
        ;@MOV   A,FMXTBL[A]
         MOV    C,A
         MOVW   HL,#FMXTBL
         MOV    A,[HL+C]
        MOV     NSETMX,A         ; Upper limit setting
```

```
        MOV     NSETMN,#4       ; Lower limit setting
        MOV     A,SFOUT
        MOV     NSET,A
DCHNG4:
        RET
```

(15) Key input processing

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS         Key input processing        SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
KEYIN:
        MOV     A,KCODE2
        MOV     KCODE1,A
        DBNZ    KSMPCNT,$KEYIN8
        MOV     KSMPCNT,#KSMPINI
        MOV     A,P5
        MOV     B,#2
KEYIN1:
        DBNZ    B,$KEYIN1
        CMP     A,P5
        BNZ     $KEYIN7
        XOR     A,#0FFH
        AND     A,#0F0H
        MOV     X,A
        AND     A,KIN
        BZ      $KEYIN5
        BF      A.4,$KEYIN2
        MOV     KCODE2,#KONOF
        BR      $KEYIN6
KEYIN2:
        BF      A.5,$KEYIN3
        MOV     KCODE2,#KPLUS
        BR      $KEYIN6
KEYIN3:
        BF      A.6,$KEYIN4
        MOV     KCODE2,#KMINS
        BR      $KEYIN6
KEYIN4:
        MOV     KCODE2,#KCHNG
        BR      $KEYIN6
KEYIN5:
        MOV     A,X
        OR      A,KIN
        BNZ     $KEYIN6
        MOV     KCODE2,#KNULL
KEYIN6:
        MOV     A,X
        MOV     KIN,A
        BR      $KEYIN8
KEYIN7:
        MOV     KCODE2,#KERR
KEYIN8:
        RET
```

(16) Setting mode transition processing

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS  Setting mode transition processing SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
SMCHNG:
        MOV     A,KCODE1
        CMP     A,KCODE2
        BZ      $SMCHNG4
        CMP     SMODE,#SMOUT
        BNZ     $SMCHNG2
        CMP     KCODE2,#KONOF
        BZ      $SMCHNG1
        CMP     KCODE2,#KCHNG
        BZ      $SMCHNG1
        MOV     SMODE,#SMOUT
        BR      $SMCHNG4
SMCHNG1:
        MOV     SMODE,#SMOFF
        BR      $SMCHNG4
SMCHNG2:
        BF      KCODE2.1,$SMCHNG4
        MOV     SMODE,#SMOUT
SMCHNG4:
        RET
```

(17) Inverter output setting

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS       Inverter output setting       SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
INVSET:
        BF      _MINIT,$INVSET5
        CMP     PMODE,#PMSTOP
        BNZ     $INVSET1
                ;************ Initialization for stop mode
        SET1    PMK0            ; Prohibit INTP0
        SET1    TMMK7           ; Prohibit INTTM7
        CLR1    CE7             ; TM7 count stop
        SET1    P6.4            ; Output enable signal setting (prohibit output)
        MOV     NFOUT,#FRQSTOP  ; Output frequency stop setting
        MOV     RFOUT,#FRQSTOP  ; Target frequency stop setting
        BR      !INVSET8
INVSET1:
        CMP     PMODE,#PMCHNG
        BNZ     $INVSET8
                ;************ Initialization for change mode
        CMP     NFOUT,#FRQSTOP
        BNZ     $INVSET3
                ;************ Output start processing
        MOV     NFOUT,#FOUTINI  ; Output frequency setting
        MOVW    VFP,#VFPINI     ; Vf modulation ratio pointer setting
        CALL    !FRQCNG         ; Variable buffer setting
        CALL    !WAITSET
        CALL    !OUTST          ; Output start processing
        CLR1    P6.4            ; Output enable signal setting
        BR      $INVSET8
INVSET3:        ;************ Output frequency setting change
        MOV     A,NFOUT
        CMP     A,RFOUT
        BC      $INVSET4
        DEC     NFOUT           ; Reduce output frequency
        ;@SUBW  VFP,#2          ; Change Vf modulation ratio pointer
         MOVW   AX,VFP
         SUBW   AX,#1
         MOVW   VFP,AX
        BR      $INVSET6
INVSET4:
        INC     NFOUT           ; Increase output frequency
        ;@ADDW  VFP,#2          ; Increase Vf modulation ratio pointer
         MOVW   AX,VFP
         ADDW   AX,#1
         MOVW   VFP,AX
        BR      $INVSET6
INVSET5:        ;************ Frequency change mode processing
        CMP     PMODE,#PMCHNG
        BNZ     $INVSET10
        ;@CMPW  WAITCNT,#0
         MOVW   AX,WAITCNT
         CMPW   AX,#0
        BZ      $INVSET3
```

```
        DECW    AX
        MOVW    WAITCNT,AX
        BTCLR   _PCHNG,$INVSET9
        BR      $INVSET8
INVSET6:
        CALL    !WAITSET
INVSET9:
        CALL    !FRQCNG         ; Variable buffer setting
        SET1    _CHNGST         ; Change start flag setting
INVSET8:
        RET
INVSET10:       ;************ Constant-rate output mode processing
        CMP     PMODE,#PMFOUT
        BNZ     $INVSET11
        BTCLR   _PCHNG,$INVSET9
        BR      $INVSET8
INVSET11:       ;************ Stop mode processing
        MOV     RFOUT,#FRQSTOP
        BR      $INVSET8
```

(18) PWM output start processing

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss     PWM output start processing     ss
        ;sssssssssssssssssssssssssssssssssssssss
OUTST:
        BT      _10BIT,$OUTST_10
        MOVW    AX,BVF
        MOVW    VF,AX           ; V/f modulation ratio transfer
        MOVW    AX,BSADR
        MOVW    SADR,AX         ; Step address transfer
        MOV     A,BOFFSET
        MOV     OFFSET,A        ; V/f offset revision value transfer
        MOVW    TM0WADR,#00H    ; Address calculation variable setting
        MOV1    CY,_BSVF
        MOV1    _SVF,CY         ; V/f modulation ratio flag transfer
        MOV     X,#0H
        MOV     A,BCM03
        XCH     A,X
        MOVW    BFCM3,AX
        MOVW    CM3,AX          ; Carrier frequency change
        XCH     A,X
        CLR1    CY
        RORC    A,1             ; CM03/2

        MOV     BFCM0L,A        ; Buffer register initialization
        MOV     BFCM1L,A
        MOV     BFCM2L,A
        MOV     A,BDTIME        ; Dead time change
        MOV     DTIME,A

        MOVW    AX,#0FFH
        MOVW    CM0,AX          ; U-phase switching avoidance
        MOVW    CM1,AX          ; V-phase switching avoidance
        MOVW    CM2,AX          ; W-phase switching avoidance
        CLR1    PIF0            ; INTP0 interrupt request clear
        CLR1    PMK0            ; INTP0 interrupt enable
        CLR1    TMIF7           ; INTTM7 interrupt request clear
        CLR1    TMMK7           ; INTTM7 interrupt enable
        SET1    CE7             ; TM7 operation setting
        RET

OUTST_10:
        MOVW    AX,BVF
        MOVW    VF,AX           ; V/f modulation ratio transfer
        MOVW    AX,BSADR
        MOVW    SADR,AX         ; Step address transfer
        MOVW    AX,BOFFSET
        MOVW    OFFSET,AX       ; V/f offset revision value transfer
        MOVW    TM0WADR,#00H    ; Address calculation variable setting
        MOV1    CY,_BSVF
        MOV1    _SVF,CY         ; V/f modulation flag transfer
        MOVW    AX,BCM03
        MOVW    BFCM3,AX
        MOVW    CM3,AX          ; Carrier frequency change
```

```
        MOVW    CM3,AX          ; Carrier frequency change
        ;@SHRW  AX,1            ; CM03/2
         CLR1   CY
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X

        MOVW    BFCM0,AX        ; Buffer register initialization
        MOVW    BFCM1,AX
        MOVW    BFCM2,AX
        MOV     A,BDTIME        ; Dead time change
        MOV     DTIME,A

        MOVW    AX,#03FFH
        MOVW    CM0,AX          ; U-phase switching avoidance
        MOVW    CM1,AX          ; V-phase switching avoidance
        MOVW    CM2,AX          ; W-phase switching avoidance
        CLR1    TMIF7           ; INTTM7 interrupt request clear
        CLR1    TMMK7           ; INTTM7 interrupt enable
        SET1    CE7             ; TM7 operation setting
        RET
```

(19) LED and 8-segment LED output processing

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS  LED and 8-segment LED output processing  SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
LEDOUT:
        MOV     A,P5            ;
        MOV     P5,#0           ; Digit output stop
        MOV     P4,#0           ; Pattern output stop
        CLR1    CY
        RORC    A,1
        MOV1    A.2,CY
        MOV1    CY,_LEDOUT
        AND1    CY,LEDCNT.7
        MOV1    A.3,CY          ; LED output setting
        MOV     P5,A            ; Digit output start
        BF      SEGCNT.7,$LEDOUT1
        MOV1    CY,A.1
        ROLC    A,1
        AND     A,#00000011B
        ;@MOV   A,SEGBUF[A]     ; Display buffer reference
         MOV    C,A
         MOVW   HL,#SEGBUF
         MOV    A,[HL+C]
        ;@MOV   A,LEDTBL[A]     ; Display pattern reference
         MOV    C,A
         MOVW   HL,#LEDTBL
         MOV    A,[HL+C]
        MOV     P4,A            ; Pattern output start
LEDOUT1:
        RET
```

(20) LED and 8-segment LED display setting

```
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
        ;SS  LED and 8-segment LED display setting  SS
        ;SSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSSS
LEDSET:         ;************ Output frequency display setting
        CMP     DMODE,#DMFOUT
        BNZ     $LEDSET3
        CMP     SMODE,#SMOFF
        BNZ     $LEDSET1
        CMP     PMODE,#PMCHNG
        BZ      $LEDSET30
        MOV     A,SFOUT
        BR      $LEDSET2
LEDSET30:
        MOV     A,NFOUT
        BR      $LEDSET2
LEDSET1:
        MOV     A,NSET
LEDSET2:
        CALL    !BUFSET         ; SEG LED display buffer setting
        BR      $LEDSET13
LEDSET3:        ;************ Carrier frequency display setting
        CMP     DMODE,#DMCRRY
        BNZ     $LEDSET6
        CMP     SMODE,#SMOFF
        BNZ     $LEDSET4
        MOV     A,NCRRY
        BR      $LEDSET5
LEDSET4:
        MOV     A,NSET
LEDSET5:
        ROL     A,1
        AND     A,#11111110B
        ;@MOVW  AX,CRRYTBL[A]
         MOV    C,A
         MOVW   HL,#CRRYTBL
         MOV    A,[HL+C]
         MOV    X,A
         INC    C
         MOV    A,[HL+C]
        MOV     C,#100
        DIVUW   C
        MOV     A,X
        CALL    !BUFSET         ; SEG LED display buffer setting
        CMP     SEGBUF+1,#CHRSPC ; Less than 1.0?
        BZ      $LEDSET50
        ADD     SEGBUF+1,#10H   ; Add decimal point
        BR      $LEDSET13
LEDSET50:
        MOV     SEGBUF+1,#CHRZ  ; Set "0."
        BR      $LEDSET13
LEDSET6:        ;************ Dead time display setting
        CMP     DMODE,#DMDEAD
        BNZ     $LEDSET9
        CMP     SMODE,#SMOFF    ; Setting mode off?
```

```
        BNZ     $LEDSET7
        MOV     A,NDEAD
        BR      $LEDSET8
LEDSET7:
        MOV     A,NSET
LEDSET8:
        CALL    !BUFSET         ; SEG LED display buffer setting
        MOV     SEGBUF,#CHRD    ; Set "d "
        BR      $LEDSET13
LEDSET9:        ;************ Change rate display setting
        CMP     SMODE,#SMOFF
        BNZ     $LEDSET10
        MOV     A,NCHNG
        BR      $LEDSET11
LEDSET10:
        MOV     A,NSET
LEDSET11:
        ;@MOV   A,CHDSPTBL[A]
         MOV    C,A
         MOVW   HL,#CHDSPTBL
         MOV    A,[HL+C]
        CALL    !BUFSET         ; SEG LED display buffer setting
        MOV     SEGBUF,#CHRO    ; Set "o "
        CMP     SEGBUF+1,#CHRSPC
        BZ      $LEDSET60
        ADD     SEGBUF+1,#10H   ; Add decimal point
        BR      $LEDSET13
LEDSET60:
        MOV     SEGBUF+1,#CHRZ
LEDSET13:       ;************ LED flash counter setting
        CMP     PMODE,#PMSTOP
        BNZ     $LEDSET17
        CLR1    _LEDOUT
        BR      $LEDSET14
LEDSET17:
        CMP     PMODE,#PMCHNG
        BNZ     $LEDSET18
        DEC     LEDCNT
        CMP     LEDCNT,#80H-LEDINI
        BNZ     $LEDSET19

LEDSET18:
        MOV     LEDCNT,#80H+LEDINI
LEDSET19:
        MOV1    CY,LEDCNT.7
        MOV1    _LEDOUT,CY
LEDSET14:       ;************ 8-segment LED flash counter setting
        CMP     SMODE,#SMOFF
        BZ      $LEDSET16
        DEC     SEGCNT
        CMP     SEGCNT,#80H-SEGINI
        BNZ     $LEDSET15
        MOV     SEGCNT,#80H+SEGINI
        BR      $LEDSET15
LEDSET16:
        MOV     SEGCNT,#80H+SEGINI
```

```
LEDSET15:
        RET
```

(21) 8-segment LED output buffer setting

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss 8-segment LED output buffer setting ss
        ;sssssssssssssssssssssssssssssssssssssss
BUFSET:         ;************ Initialization, third digit setting
        MOV     SEGBUF,#0               ; Set "0 "
        MOV     SEGBUF+1,#0             ; Set "0 "
BUFSET1:        ;************ First-digit setting
        CMP     A,#100
        BC      $BUFSET2
        INC     SEGBUF
        SUB     A,#100
        BR      $BUFSET1
BUFSET2:        ;************ Second-digit setting
        CMP     A,#10
        BC      $BUFSET3
        INC     SEGBUF+1
        SUB     A,#10
        BR      $BUFSET2
BUFSET3:        ;************ Leading zero deletion
        CMP     SEGBUF,#0
        BNZ     $BUFSET4
        MOV     SEGBUF,#CHRSPC
        CMP     SEGBUF+1,#0
        BNZ     $BUFSET4
        MOV     SEGBUF+1,#CHRSPC
BUFSET4:        ;************ First-digit setting
        MOV     SEGBUF+2,A
        RET
```

(22) Frequency setting change processing

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss Frequency setting change processing ss
        ;sssssssssssssssssssssssssssssssssssssss
FRQCNG:         ;********** Change pattern setting (8-bit timer in use)
        BF      _10BIT,$FRQCNG_
        BR      FRQCNG_X
FRQCNG_:
                ;************ DTIME (dead time) setting
        MOV     A,NDEAD
        MOV     X,#8
        MULU    X
        MOV     A,X
        MOV     BDTIME,A
                ;************ BCM03 (carrier frequency) setting
        MOV     A,NCRRY
        ADD     A,A
        ;@MOVW  AX,CRRYTBL[A]
         MOV    C,A
         MOVW   HL,#CRRYTBL      ;
FRQCNG1:
         MOV    A,[HL+C]         ;
         MOV    X,A              ;
         INC    C                ;
         MOV    A,[HL+C]         ;
        ;@ADDW  AX,AX
         CLR1   CY
         XCH    A,X
         ROLC   A,1
         XCH    A,X
         ROLC   A,1
        MOVW    WARU2,AX
        MOV     A,TM7CLK
        ROL     A,1
        ROL     A,1
        AND     A,#11111100B
        MOV     C,A
        MOVW    HL,#TMCLKTBL
        MOV     A,[HL+C]
        MOV     X,A
        INC     C
        MOV     A,[HL+C]
        MOVW    WARU1,AX
        INC     C
        MOV     A,[HL+C]
        MOV     X,A
        INC     C
        MOV     A,[HL+C]
        MOVW    WARU1+2,AX
        CALL    !DIVUX
        MOV     A,WARU1
        MOV     BCM03,A
                ;************ BSADR (step address) setting
        MOV     A,NCRRY
        ADD     A,A
```

```
        ;@MOVW   AX,CRRYTBL[A]
         MOV     C,A
         MOVW    HL,#CRRYTBL      ;
FRQCNG10:
         MOV     A,[HL+C]         ;
         MOV     X,A              ;
         INC     C                ;
         MOV     A,[HL+C]         ;
        MOVW     WARU2,AX
        MOV      A,NFOUT
        MOV      X,#0
        XCH      A,X
        MOVW     WARU1,#00H
        MOVW     WARU1+2,AX
        CALL     !DIVUX
        MOV      A,WARU1
        MOV      X,A
        MOV      A,TM7CNT
        MULU     X
        MOVW     BC,AX
        MOV      A,WARU1+1
        MOV      X,A
        MOV      A,TM7CNT
        MULU     X
        XCH      A,X
        ADD      B,A
        MOVW     AX,BC
        MOVW     BSADR,AX
                 ;************ BVF (modulation ratio buffer) setting
        MOVW     AX,BCM03
        MOVW     MKAKE1,AX
        MOVW     AX,VFP
        MOVW     HL,AX
        ;@MOVW   HL,AX
        ;@MOVW   AX,VFTBL1[HL]
         MOVW    AX,VFTBLNO
         XCH     A,X
         ADD     L,A
         XCH     A,X              ;
         ADDC    H,A              ;
         MOV     A,[HL]           ;
        BT       _VFON,$FRQCNG15
        MOV      A,#80H
FRQCNG15:
        CLR1     _BSVF
        CMP      A,#80H           ; V/f modulation ratio < 0?
        BC       $FRQCNG20        ; THEN [Next]
        SET1     _BSVF            ; ELSE [_BSVF set]
FRQCNG20:
        MOV      X,A
        MOV      A,BCM03
        MULU     X
        XCH      A,X
        ROLC     A,1
        XCH      A,X
        ROLC     A,1
```

```
        XCH     A,X
        ROLC    A,1
        AND     A,#00000001B
        MOVW    BVF,AX
                ;************ BOFFSET (V/f offset revision value) setting
        MOV     A,BCM03
        CLR1    CY
        RORC    A,1             ; CM03/2
        MOV     E,A
        MOVW    AX,BVF
        ;@SHRW  AX,1             ; VF/2
         CLR1   CY
         RORC   A,1
         XCH    A,X
         RORC   A,1
        CMP     A,E
        BNC     $FRQCNG30
        XCH     A,E
FRQCNG30:
        SUB     A,E     ; Offset revision value = |VF/2 - CM03/2|
        MOV     BOFFSET,A
        DEC     BCM03
        DEC     BDTIME
        RET

FRQCNG_X:       ;********** Change pattern setting (10-bit timer in use)
                ;************ DTIME (dead time) setting
        MOV     A,NDEAD
        MOV     X,#8
        MULU    X
        MOV     A,X
        MOV     BDTIME,A
                ;************ BCM03 (carrier frequency) setting
        MOV     A,NCRRY
        ADD     A,A
        ;@MOVW  AX,CRRYTBL[A]
         MOV    C,A
         MOVW   HL,#CRRYTBL
FRQC1_X:
         MOV    A,[HL+C]        ;
         MOV    X,A             ;
         INC    C               ;
         MOV    A,[HL+C]        ;
        ;@ADDW  AX,AX
         CLR1   CY
         XCH    A,X
         ROLC   A,1
         XCH    A,X
         ROLC   A,1
        MOVW    WARU2,AX
        MOV     A,TM7CLK
        ROL     A,1
        ROL     A,1
        AND     A,#11111100B
        MOV     C,A
        MOVW    HL,#TMCLKTBL
```

```
        MOV     A,[HL+C]
        MOV     X,A
        INC     C
        MOV     A,[HL+C]
        MOVW    WARU1,AX
        INC     C
        MOV     A,[HL+C]
        MOV     X,A
        INC     C
        MOV     A,[HL+C]
        MOVW    WARU1+2,AX
        CALL    !DIVUX
        MOV     A,WARU1
        MOV     BCM03,A
                ;************ BSADR (step address) setting
        MOV     A,NCRRY
        ADD     A,A
        ;@MOVW  AX,CRRYTBL[A]
         MOV    C,A
         MOVW   HL,#CRRYTBL      ;
FRQCNG10:
         MOV    A,[HL+C]         ;
         MOV    X,A              ;
         INC    C                ;
         MOV    A,[HL+C]         ;
        MOVW    WARU2,AX
        MOV     A,NFOUT
        MOV     X,#0
        XCH     A,X
        MOVW    WARU1,#00H
        MOVW    WARU1+2,AX
        CALL    !DIVUX
        MOV     A,WARU1
        MOV     X,A
        MOV     A,TM7CNT
        MULU    X
        MOVW    BC,AX
        MOV     A,WARU1+1
        MOV     X,A
        MOV     A,TM7CNT
        MULU    X
        XCH     A,X
        ADD     B,A
        MOVW    AX,BC
        MOVW    BSADR,AX
                ;************ BVF (modulation ratio buffer) setting
        MOVW    AX,BCM03
        MOVW    MKAKE1,AX
        MOVW    AX,VFP
        MOVW    HL,AX
        ;@MOVW  HL,AX
        ;@MOVW  AX,VFTBL1[HL]
         MOVW   AX,VFTBLNO
         XCH    A,X
         ADD    L,A
         XCH    A,X              ;
```

```
         ADDC    H,A             ;
         MOV     A,[HL]          ;
        BT      _VFON,$FRQC15_X
        MOV     A,#80H
FRQC15_X:
        CLR1    _BSVF
        CMP     A,#80H          ; V/f modulation ratio < 0?
        BC      $FRQC20_X       ; THEN [Next]
        SET1    _BSVF           ; ELSE [_BSVF set]
FRQC20_X:
        XCH     A,X
        MOV     A,#0
        MOVW    MKAKE2,AX
        CALL    !MULUW
        MOV     A,MKOTAE
        ROLC    A,1
        MOV     A,MKOTAE+1
        ROLC    A,1
        XCH     A,X
        MOV     A,MKOTAE+2
        ROLC    A,1
        MOVW    BVF,AX
                ;************ BOFFSET (V/f offset revision value) setting
        MOVW    AX,BCM03
        ;@SHRW  AX,1             ; CM03/2
         CLR1   CY
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
        MOVW    DE,AX
        MOVW    AX,BVF
        ;@SHRW  AX,1             ; VF/2
         CLR1   CY
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
        ;@CMPW  AX,DE
         CMP    A,D
         BZ     $FRQC40_X
         BNC    $FRQC30_X
FRQC29_X:
        XCHW    AX,DE
FRQC30_X:
        ;@SUBW  AX,DE            ; Offset revision value = |VF/2 - CM03/2|
         XCH    A,X
         SUB    A,E
         XCH    A,X
         SUBC   A,D
        MOVW    BOFFSET,AX
        ;@DECW  BCM03
         MOVW   AX,BCM03
         DECW   AX
         MOVW   BCM03,AX
        DEC     BDTIME
```

```
        RET
FRQC40_X:
        XCH     A,X
        CMP     A,E
        XCH     A,X
        BNC     $FRQC30_X
        BR      FRQC29_X
```

(23) Binary division (32 ÷ 16)

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss      Binary division (32 ÷ 16)      ss
        ;sssssssssssssssssssssssssssssssssssssss

DIVUX:
        MOVW    AMARI,#00H      ;
        MOV     B,#32
DIVUX1:
        CLR1    CY
        MOV     A,WARU1         ;
        ROLC    A,1
        MOV     WARU1,A
        MOV     A,WARU1+1       ;
        ROLC    A,1
        MOV     WARU1+1,A
        MOV     A,WARU1+2       ;
        ROLC    A,1
        MOV     WARU1+2,A
        MOV     A,WARU1+3       ;
        ROLC    A,1
        MOV     WARU1+3,A
        MOV     A,AMARI         ;
        ROLC    A,1
        MOV     AMARI,A
        MOV     A,AMARI+1       ;
        ROLC    A,1
        MOV     AMARI+1,A

        MOVW    AX,AMARI
        XCH     A,X
        SUB     A,WARU2
        XCH     A,X
        SUBC    A,WARU2+1
        BC      $DIVUX2

        MOVW    AMARI,AX
        SET1    WARU1.0         ;
DIVUX2:
        DBNZ    B,$DIVUX1
        RET
```

(24) Binary multiplication (16 × 16)

```
        ;sssssssssssssssssssssssssssssssssssssss
        ;ss   Binary multiplication (16 × 16)   ss
        ;sssssssssssssssssssssssssssssssssssssss

MULUW:
        MOV     A,MKAKE1
        MOV     X,A
        MOV     A,MKAKE2
        MULU    X
        MOVW    MKOTAE,AX

        MOV     A,MKAKE1+1
        MOV     X,A
        MOV     A,MKAKE2+1
        MULU    X
        MOVW    MKOTAE+2,AX

        MOV     A,MKAKE1
        MOV     X,A
        MOV     A,MKAKE2+1
        MULU    X
        XCH     A,X
        ADD     A,MKOTAE+1
        MOV     MKOTAE+1,A
        XCH     A,X
        ADDC    A,MKOTAE+2
        MOV     MKOTAE+2,A
        ADDC    MKOTAE+3,#0

        MOV     A,MKAKE1+1
        MOV     X,A
        MOV     A,MKAKE2
        MULU    X
        XCH     A,X
        ADD     A,MKOTAE+1
        MOV     MKOTAE+1,A
        XCH     A,X
        ADDC    A,MKOTAE+2
        MOV     MKOTAE+2,A
        ADDC    MKOTAE+3,#0
        RET
```

(25) Output frequency change rate setting

```
        ;sssssssssssssssssssssssssssssssssssssssss
        ;ss  Output frequency change rate setting  ss
        ;sssssssssssssssssssssssssssssssssssssssss
WAITSET:
        MOV     A,NCHNG
        ROL     A,1
        AND     A,#11111110B
        ;@MOVW  AX,CHNGTBL[A]
         MOV    C,A
         MOVW   HL,#CHNGTBL
         MOV    A,[HL+C]
         MOV    X,A
         INC    C
         MOV    A,[HL+C]
        MOVW    WAITCNT,AX      ; Wait counter setting
        RET

        END
```

6.2 Interrupt Processing

```
$       PROCESSOR(F0924)
$INCLUDE(INC092X.INC)                   ; Constant definition
EXTRN   SINTBL, SINTBL1                 ; Table
EXTRN   BVF,    VF,     BSADR,  SADR    ; saddr variable
EXTRN   BCM03,  BOFFSET,OFFSET          ; saddr variable
EXTRN   IKAKE1, IKAKE2, IKOTAE          ; saddr variable
EXTRN   RFOUT                           ; saddr variable
EXTBIT  _CHNGST,_BSVF,  _SVF,_10BIT     ; Flags
PUBLIC  LADR,   INTP0                   ; Interrupts

CODE    CSEG
; IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII
; II       INTP0 vectored interrupt      II
; IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII

INTP0:
        SEL     RB2             ; Register bank setting
INTP0_1:
        MOV     A,P0            ; Stop signal input (first time)
        AND     A,#00000001B
        XCH     A,X
        MOV     B,#1
INTP0_2:
        DBNZ    B,$INTP0_2
        MOV     A,P0            ; Stop signal input (second time)
        AND     A,#00000001B
        CMP     A,X
        BNZ     $INTP0_1        ; Match?

        BT      A.0,$INTP0_3    ; Error signal active?
        MOV     RFOUT,#0FFH     ;
        CLR1    CE7             ; Stop setting
        SET1    PMK0            ; INTP0 DI
INTP0_3:
        RET1

;IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII
;II      INTTM7 vectored interrupt      II
;IIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIIII

LADR:           ;************ Output enable setting
         SEL    RB1
LADR0:          ;************ Test pin output processing
         SET1   P6.6
         ;;BT   _10BIT,$LADR1_X
          BF    _10BIT,$LADR1
          BR    LADR1_X
; *---------------------------------------------
; *     8-bit timer in use
; *---------------------------------------------

LADR1:          ;************ Reference address calculation
        MOVW    AX,HL
        XCH     A,X
```

```
        ADD     A,SADR
        XCH     A,X
        ADDC    A,SADR+1
        MOVW    HL,AX
LUADR:          ;************ U-phase timing setting
        MOVW    AX,VF
        MOV     A,H
        MOVW    DE,#SINTBL      ; Sine wave table reference
        ADD     A,E
        XCH     A,E
        MOV     A,#00
        ADDC    A,D
        XCH     A,D
        MOV     A,[DE]
        MOV     E,A
        MULU    X               ; Multiplication by modulation ratio
        CLR1    CY
        BF      (VF+1).0,$LUADR0
        ADD     A,E
LUADR0:
        XCH     AX
        ROLC    A,1
        AND     A,#00000001B
        XCH     A,X
        BF      _SVF,$LUADR1    ; V/f modulation ratio < 1?
        SUB     A,OFFSET        ; ELSE [subtract offset value]
        XCH     A,X
        SUBC    A,#0
        BNC     $LUSKP
        MOVW    AX,#00H
        BR      $LUSKP
LUADR1:
        ADD     A,OFFSET        ; THEN [add offset value]
        XCH     A,X
        ADDC    A,#0
LUSKP:
        BF      A.0,$LUSKP_0
        MOV     X,#0FFH
LUSKP_0:
        XCH     A,X
        MOV     BFCM0L,A        ; Timing setting
LVADR:          ;************ V-phase timing setting
        MOVW    AX,VF
        MOV     A,H
        ADD     A,#ADDADR1
        MOVW    DE,#SINTBL      ; Sine wave table reference
        ADD     A,E
        XCH     A,E
        MOV     A,#00
        ADDC    A,D
        XCH     A,D
        MOV     A,[DE]
        MOV     E,A
        MULU    X               ; Multiplication by modulation ratio
        CLR1    CY
        BF      (VF+1).0,$LVADR0
```

```
        ADD     A,E
LUADR0:
        XCH     A,X
        ROLC    A,1
        AND     A,#00000001B
        XCH     A,X
        BF      _SVF,$LUADR1    ; V/f modulation ratio < 1?
        SUB     A,OFFSET        ; ELSE [subtract offset value]
        XCH     A,X
        SUBC    A,#0
        BNC     $LUSKP
        MOVW    AX,#00H
        BR      $LUSKP
LUADR1:
        ADD     A,OFFSET        ; THEN [add offset value]
        XCH     A,X
        ADDC    A,#0
LUSKP:
        BF      A.0,$LUSKP_0
        MOV     X,#0FFH
LUSKP_0:
        XCH     A,X
        MOV     BFCM0L,A        ; Timing setting
LVADR:          ;************ V-phase timing setting
        MOVW    AX,VF
        MOV     A,H
        ADD     A,#ADDADR1
        MOVW    DE,#SINTBL      ; Sine wave table reference
        ADD     A,E
        XCH     A,E
        MOV     A,#00
        ADDC    A,D
        XCH     A,D
        MOV     A,[DE]
        MOV     E,A
        MULU    X               ; Multiplication by modulation ratio
        CLR1    CY
        BF      (VF+1).0,$LVADR0
        ADD     A,E
LVADR0:
        XCH     A,X
        ROLC    A,1
        AND     A,#00000001B
        XCH     A,X
        BF      _SVF,$LVADR1    ; V/f modulation ratio < 1?
        SUB     A,OFFSET        ; ELSE [subtract offset value]
        XCH     A,X
        SUBC    A,#0
        BNC     $LVSKP
        MOVW    AX,#00H
        BR      $LVSKP
LVADR1:
        ADD     A,OFFSET        ; THEN [add offset value]
        XCH     A,X
        ADDC    A,#0
LVSKP:
```

```
        BF      A.0,$LVSKP_0
        MOV     X,#0FFH
LWSKP_0:
        XCH     A,X
        MOV     BFCM2L,A        ; Timing setting
LEND:
        BF      _CHNGST,$LADR3
LADR2:
        CLR1    _CHNGST         ; Change flag clear
        MOV     X,#0
        MOV     A,BCM03
        XCH     A,X
        MOVW    BFCM3,AX        ; Carrier frequency transfer
        MOVW    AX,BVF          ;
        MOVW    VF,AX           ; V/f modulation ratio transfer
        MOVW    AX,BSADR        ;
        MOVW    SADR,AX         ; Step address transfer
        MOV     A,BOFFSET       ;
        MOV     OFFSET,A        ; V/f offset revision value transfer
        MOV1    CY,_BSVF        ;
        MOV1    _SVF,CY         ; V/f modulation ratio < 1 (flag transfer)
LADR3:          ;************ Test pin output processing
        CLR1    P6.6
        RETI

; *-----------------------------------------------
; *     10-bit timer in use
; *-----------------------------------------------

LADR1_X:                ;************ Reference address calculation
        MOVW    AX,VF
        MOVW    IKAKE1,AX
        MOVW    AX,HL
        ;;ADDW  AX,SADR
         XCH    A,X
         ADD    A,SADR
         XCH    A,X
         ADDC   A,SADR+1
        MOVW    HL,AX
        XCH     A,X
        ROL     A,1
        XCH     A,X
        ROLC    A,1
        XCH     A,X
        MOV     A,#00H
        ADDC    A,#00H
        ;;ADDW  AX,AX
         CLR1   CY
         XCH    A,X
         ROLC   A,1
         XCH    A,X
         ROLC   A,1
         ROLC   A,1
         XCH    A,X
         ROLC   A,1
         MOVW   BC,AX
```

```
LUADR_X:                ;************ U-phase timing setting
        ;;@MOVW AX,SINTBL[DE]   ; Sine wave table reference
         MOVW   DE,#SINTBL1     ;
         XCH    A,X
         ADD    E,A
         XCH    A,X
         ADDC   D,A
         MOV    A,[DE]
         MOV    X,A
         INCW   DE
         MOV    A,[DE]
        ;;VFxSINTBL[]           ; Multiplication by modulation ratio
         MOVW   IKAKE2,AX
         CALL   !SMULUW
         MOV    A,IKOTAE+1
         MOV    X,A
         MOV    A,IKOTAE+2
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         AND    A,#00000111B
        BF      _SVF,$LUADR1_X  ; V/f modulation ratio < 1?
        ;;SUBW  AX,OFFSET       ; ELSE [subtract offset value]
         XCH    A,X
         SUB    A,OFFSET
         XCH    A,X
         SUBC   A,OFFSET+1
        BNC     $LUSKP_X
        MOVW    AX,#0000H
        BR      $LUSKP_X
LUADR1_X:
        ;;ADDW  AX,OFFSET       ; THEN [add offset value]
         XCH    A,X
         ADD    A,OFFSET
         XCH    A,X
         ADDC   A,OFFSET+1
LUSKP_X:
        BF      A.2,$LUSKP_X1
        MOVW    AX,#03FFH
LUSKP_X1:
        MOVW    BFCM0,AX        ; Timing setting
LVADR_X:        ;************ V-phase timing setting
;;      MOVW    AX,VF
;;      MOVW    IKAKE1,AX
        MOVW    AX,BC
        ADDW    AX,#ADDADR1X
        AND     A,#00000011B
        ;;@MOVW AX,SINTBL[DE]   ; Sine wave table reference
         MOVW   DE,#SINTBL1
         XCH    A,X
         ADD    E,A
```

```
         XCH    A,X
         ADDC   D,A
         MOV    A,[DE]
         MOV    X,A
         INCW   DE
         MOV    A,[DE]
        ;;VFxSINTBL[]           ; Multiplication by modulation ratio
         MOVW   IKAKE2,AX
         CALL   !SMULUW
         MOV    A,IKOTAE+1
         MOV    X,A
         MOV    A,IKOTAE+2
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         AND    A,#00000111B
        BF      _SVF,$LVADR1_X  ; V/f modulation ratio < 1?
        ;;SUBW  AX,OFFSET       ; ELSE [subtract offset value]
         XCH    A,X
         SUB    A,OFFSET
         XCH    A,X
         SUBC   A,OFFSET+1
        BNC     $LVSKP_X
        MOVW    AX,#0000H
        BR      $LVSKP_X
LVADR1_X:
        ;;ADDW  AX,OFFSET       ; THEN [add offset value]
         XCH    A,X
         ADD    A,OFFSET
         XCH    A,X
         ADDC   A,OFFSET+1
LVSKP_X:
        BF      A.2,$LVSKP_X1
        MOVW    AX,#03FFH
LVSKP_X1:
        MOVW    BFCM1,AX        ; Timing setting
LWADR_X:        ;************ W-phase timing setting
;;      MOVW    AX,VF
;;      MOVW    IKAKE1,AX
        MOVW    AX,BC
        ADDW    AX,#ADDADR2X
        AND     A,#00000011B
        ;@MOVW  AX,SINTBL[DE]   ; Sine wave table reference
         MOVW   DE,#SINTBL1
         XCH    A,X
         ADD    E,A
         XCH    A,X
         ADDC   D,A
         MOV    A,[DE]
         MOV    X,A
         INCW   DE
```

```
         MOV    A,[DE]
        ;;VFxSINTBL[]           ; Multiplication by modulation ratio
         MOVW   IKAKE2,AX
         CALL   !SMULUW
         MOV    A,IKOTAE+1
         MOV    X,V
         MOV    A,IKOTAE+2
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         RORC   A,1
         XCH    A,X
         AND    A,#00000111B
        BF      _SVF,$LWADR1_X  ; V/f modulation ratio < 1?
        ;;SUBW  AX,OFFSET       ; ELSE [subtract offset value]
         XCH    A,X
         SUB    A,OFFSET
         XCH    A,X
         SUBC   A,OFFSET+1
        BNC     $LWSKP_X
        MOVW    AX,#0000H
        BR      $LWSKP_X
LWADR1_X:
        ;;ADDW  AX,OFFSET       ; THEN [add offset value]
         XCH    A,X
         ADD    A,OFFSET
         XCH    A,X
         ADDC   A,OFFSET+1
LWSKP_X:
        BF      A.2,$LWSKP_X1
        MOVW    AX,#03FFH
LWSKP_X1:
        MOVW    BFCM2,AX        ; Timing setting
LEND_X:
        BF      _CHNGST,$LADR3_X
LADR2_X:
        CLR1    _CHNGST         ; Change flag clear
        MOVW    AX,BCM03
        MOVW    BFCM3,AX        ; Carrier frequency transfer
        MOVW    AX,BVF          ;
        MOVW    VF,AX           ; V/f modulation ratio transfer
        MOVW    AX,BSADR        ;
        MOVW    SADR,AX         ; Step address transfer
        MOVW    AX,BOFFSET      ;
        MOVW    OFFSET,AX       ; V/f offset revision value transfer
        MOV1    CY,_BSVF        ;
        MOV1    _SVF,CY         ; V/f modulation ratio < 1 (flag transfer)
LADR3_X:        ;************ Test pin output processing
        CLR1    P6.6
        RETI
```

```
; *-------------------------------------------------------
; *     16 bit x 16 bit  Multiplication subroutine
; *-------------------------------------------------------

SMULUW:
        MOV     A,IKAKE1
        MOV     X,A
        MOV     A,IKAKE2
        MULU    X
        MOVW    IKOTAE,AX

        MOV     A,IKAKE1+1
        MOV     X,A
        MOV     A,IKAKE2+1
        MULU    X
        MOVW    IKOTAE+2,AX

        MOV     A,IKAKE1
        MOV     X,A
        MOV     A,IKAKE2+1
        MULU    X
        XCH     A,X
        ADD     A,IKOTAE+1
        MOV     IKOTAE+1,A
        XCH     A,X
        ADDC    A,IKOTAE+2
        MOV     IKOTAE+2,A
        ADDC    IKOTAE+3,#0

        MOV     A,IKAKE1+1
        MOV     X,A
        MOV     A,IKAKE2
        MULU    X
        XCH     A,X
        ADD     A,IKOTAE+1
        MOV     IKOTAE+1,A
        XCH     A,X
        ADDC    A,IKOTAE+2
        MOV     IKOTAE+2,A
        ADDC    IKOTAE+3,#0

        RET
        END
```

6.3 Table Data

```
PUBLIC  SINTBL, SINTBL1,VFTBL            ; Table
PUBLIC  VFTBL1, VFTBL2, VFTBL3, VFTBL4   ; Table
PUBLIC  VFTBL5, VFTBL6, VFTBL7, VFTBL8   ; Table
PUBLIC  CRRYTBL,FMXTBL, DMXTBL           ; Table
PUBLIC  CHNGTBL,LEDTBL, CHDSPTBL         ; Table
PUBLIC  TMCLKTBL,CMNTBL10,CMNTBL08       ; Table
```

(1) Sine wave table (256*1 bytes)/007FH

```
TABLE   CSEG
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT      Sine wave table           (256*1 bytes) / 007FH      TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;       Table data = sin(X)*007FH + 007FH                              ;
SINTBL:
DB      07FH,    082H,    085H,    088H,    08BH,    08FH,    092H,    095H     ;
DB      098H,    09BH,    09EH,    0A1H,    0A4H,    0A7H,    0AAH,    0ADH     ;
DB      0B0H,    0B2H,    0B5H,    0B8H,    0BBH,    0BEH,    0C0H,    0C3H     ;
DB      0C6H,    0C8H,    0CBH,    0CDH,    0D0H,    0D2H,    0D4H,    0D7H     ;
DB      0D9H,    0DBH,    0DDH,    0DFH,    0E1H,    0E3H,    0E5H,    0E7H     ;
DB      0E9H,    0EAH,    0ECH,    0EDH,    0EFH,    0F0H,    0F2H,    0F3H     ;
DB      0F4H,    0F5H,    0F7H,    0F8H,    0F9H,    0F9H,    0FAH,    0FBH     ;
DB      0FCH,    0FCH,    0FDH,    0FDH,    0FDH,    0FEH,    0FEH,    0FEH     ;
DB      0FEH,    0FEH,    0FEH,    0FEH,    0FDH,    0FDH,    0FDH,    0FCH     ;
DB      0FCH,    0FBH,    0FAH,    0F9H,    0F9H,    0F8H,    0F7H,    0F6H     ;
DB      0F4H,    0F3H,    0F2H,    0F0H,    0EFH,    0EEH,    0ECH,    0EAH     ;
DB      0E9H,    0E7H,    0E5H,    0E3H,    0E1H,    0DFH,    0DDH,    0DBH     ;
DB      0D9H,    0D7H,    0D4H,    0D2H,    0D0H,    0CDH,    0CBH,    0C8H     ;
DB      0C6H,    0C3H,    0C0H,    0BEH,    0BBH,    0B8H,    0B5H,    0B3H     ;
DB      0B0H,    0ADH,    0AAH,    0A7H,    0A4H,    0A1H,    09EH,    09BH     ;
DB      098H,    095H,    092H,    08FH,    08CH,    088H,    085H,    082H     ;
DB      07FH,    07CH,    079H,    076H,    073H,    070H,    06CH,    069H     ;
DB      066H,    063H,    060H,    05DH,    05AH,    057H,    054H,    051H     ;
DB      04EH,    04CH,    049H,    046H,    043H,    040H,    03EH,    03BH     ;
DB      039H,    036H,    033H,    031H,    02EH,    02CH,    02AH,    027H     ;
DB      025H,    023H,    021H,    01FH,    01DH,    01BH,    019H,    017H     ;
DB      015H,    014H,    012H,    011H,    00FH,    00EH,    00CH,    00BH     ;
DB      00AH,    009H,    007H,    006H,    005H,    005H,    004H,    003H     ;
DB      002H,    002H,    001H,    001H,    001H,    000H,    000H,    000H     ;
DB      000H,    000H,    000H,    000H,    001H,    001H,    001H,    002H     ;
DB      002H,    003H,    004H,    005H,    005H,    006H,    007H,    008H     ;
DB      00AH,    00BH,    00CH,    00EH,    00FH,    010H,    012H,    014H     ;
DB      015H,    017H,    019H,    01BH,    01DH,    01FH,    021H,    023H     ;
DB      025H,    027H,    02AH,    02CH,    02EH,    031H,    033H,    036H     ;
DB      038H,    03BH,    03EH,    040H,    043H,    046H,    049H,    04BH     ;
DB      04EH,    051H,    054H,    057H,    05AH,    05DH,    060H,    063H     ;
DB      066H,    069H,    06CH,    06FH,    072H,    076H,    079H,    07CH     ;
```

(2) Sine wave table (512*2 bytes)/01FFH

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT        Sine wave table       (512*2 bytes) / 01FFH        TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;       Table data = sin(X)*01FFH + 01FFH                                ;
SINTBL1:
DW      01FFH,   0205H,   020CH,   0212H,   0218H,   021EH,   0225H,   022BH    ;
DW      0231H,   0237H,   023EH,   0244H,   024AH,   0250H,   0256H,   025DH    ;
DW      0263H,   0269H,   026FH,   0275H,   027BH,   0281H,   0287H,   028DH    ;
DW      0293H,   0299H,   029FH,   02A5H,   02ABH,   02B1H,   02B7H,   02BDH    ;
DW      02C3H,   02C8H,   02CEH,   02D4H,   02D9H,   02DFH,   02E5H,   02EAH    ;
DW      02F0H,   02F5H,   02FBH,   0300H,   0306H,   030BH,   0310H,   0316H    ;
DW      031BH,   0320H,   0325H,   032AH,   032FH,   0334H,   0339H,   033EH    ;
DW      0343H,   0348H,   034DH,   0351H,   0356H,   035BH,   035FH,   0364H    ;
DW      0368H,   036DH,   0371H,   0375H,   037AH,   037EH,   0382H,   0386H    ;
DW      038AH,   038EH,   0392H,   0396H,   0399H,   039DH,   03A1H,   03A4H    ;
DW      03A8H,   03ABH,   03AFH,   03B2H,   03B5H,   03B8H,   03BCH,   03BFH    ;
DW      03C2H,   03C5H,   03C7H,   03CAH,   03CDH,   03D0H,   03D2H,   03D5H    ;
DW      03D7H,   03D9H,   03DCH,   03DEH,   03E0H,   03E2H,   03E4H,   03E6H    ;
DW      03E8H,   03EAH,   03EBH,   03EDH,   03EFH,   03F0H,   03F2H,   03F3H    ;
DW      03F4H,   03F5H,   03F6H,   03F7H,   03F8H,   03F9H,   03FAH,   03FBH    ;
DW      03FCH,   03FCH,   03FDH,   03FDH,   03FDH,   03FEH,   03FEH,   03FEH    ;
DW      03FEH,   03FEH,   03FEH,   03FEH,   03FDH,   03FDH,   03FDH,   03FCH    ;
DW      03FCH,   03FBH,   03FAH,   03F9H,   03F8H,   03F8H,   03F7H,   03F5H    ;
DW      03F4H,   03F3H,   03F2H,   03F0H,   03EFH,   03EDH,   03ECH,   03EAH    ;
DW      03E8H,   03E6H,   03E4H,   03E2H,   03E0H,   03DEH,   03DCH,   03DAH    ;
DW      03D7H,   03D5H,   03D2H,   03D0H,   03CDH,   03CAH,   03C8H,   03C5H    ;
DW      03C2H,   03BFH,   03BCH,   03B9H,   03B5H,   03B2H,   03AFH,   03ABH    ;
DW      03A8H,   03A4H,   03A1H,   039DH,   039AH,   0396H,   0392H,   038EH    ;
DW      038AH,   0386H,   0382H,   037EH,   037AH,   0376H,   0371H,   036DH    ;
DW      0368H,   0364H,   0360H,   035BH,   0356H,   0352H,   034DH,   0348H    ;
DW      0343H,   033EH,   033AH,   0335H,   0330H,   032BH,   0325H,   0320H    ;
DW      031BH,   0316H,   0311H,   030BH,   0306H,   0301H,   02FBH,   02F6H    ;
DW      02F0H,   02EBH,   02E5H,   02DFH,   02DAH,   02D4H,   02CEH,   02C9H    ;
DW      02C3H,   02BDH,   02B7H,   02B1H,   02ABH,   02A5H,   02A0H,   029AH    ;
DW      0294H,   028EH,   0288H,   0281H,   027BH,   0275H,   026FH,   0269H    ;
DW      0263H,   025DH,   0257H,   0250H,   024AH,   0244H,   023EH,   0238H    ;
DW      0231H,   022BH,   0225H,   021FH,   0218H,   0212H,   020CH,   0206H    ;
DW      01FFH,   01F9H,   01F3H,   01ECH,   01E6H,   01E0H,   01DAH,   01D3H    ;
DW      01CDH,   01C7H,   01C1H,   01BBH,   01B4H,   01AEH,   01A8H,   01A2H    ;
DW      019CH,   0195H,   018FH,   0189H,   0183H,   017DH,   0177H,   0171H    ;
DW      016BH,   0165H,   015FH,   0159H,   0153H,   014DH,   0147H,   0142H    ;
DW      013CH,   0136H,   0130H,   012AH,   0125H,   011FH,   011AH,   0114H    ;
DW      010EH,   0109H,   0103H,   00FEH,   00F9H,   00F3H,   00EEH,   00E9H    ;
DW      00E3H,   00DEH,   00D9H,   00D4H,   00CFH,   00CAH,   00C5H,   00C0H    ;
DW      00BBH,   00B6H,   00B1H,   00ADH,   00A8H,   00A3H,   009FH,   009AH    ;
DW      0096H,   0092H,   008DH,   0089H,   0085H,   0080H,   007CH,   0078H    ;
DW      0074H,   0070H,   006CH,   0069H,   0065H,   0061H,   005DH,   005AH    ;
DW      0056H,   0053H,   004FH,   004CH,   0049H,   0046H,   0043H,   0040H    ;
DW      003DH,   003AH,   0037H,   0034H,   0031H,   002FH,   002CH,   0029H    ;
DW      0027H,   0025H,   0022H,   0020H,   001EH,   001CH,   001AH,   0018H    ;
DW      0016H,   0014H,   0013H,   0011H,   000FH,   000EH,   000DH,   000BH    ;
DW      000AH,   0009H,   0008H,   0007H,   0006H,   0005H,   0004H,   0003H    ;
DW      0003H,   0002H,   0001H,   0001H,   0001H,   0000H,   0000H,   0000H    ;
DW      0000H,   0000H,   0000H,   0000H,   0001H,   0001H,   0001H,   0002H    ;
```

```
DW      0002H,   0003H,   0004H,   0005H,   0005H,   0006H,   0007H,   0009H    ;
DW      000AH,   000BH,   000CH,   000EH,   000FH,   0011H,   0012H,   0014H    ;
DW      0016H,   0018H,   001AH,   001CH,   001EH,   0020H,   0022H,   0024H    ;
DW      0027H,   0029H,   002CH,   002EH,   0031H,   0034H,   0036H,   0039H    ;
DW      003CH,   003FH,   0042H,   0045H,   0048H,   004CH,   004FH,   0052H    ;
DW      0056H,   0059H,   005DH,   0061H,   0064H,   0068H,   006CH,   0070H    ;
DW      0074H,   0078H,   007CH,   0080H,   0084H,   0088H,   008DH,   0091H    ;
DW      0095H,   009AH,   009EH,   00A3H,   00A7H,   00ACH,   00B1H,   00B6H    ;
DW      00BAH,   00BFH,   00C4H,   00C9H,   00CEH,   00D3H,   00D8H,   00DDH    ;
DW      00E3H,   00E8H,   00EDH,   00F2H,   00F8H,   00FDH,   0103H,   0108H    ;
DW      010EH,   0113H,   0119H,   011EH,   0124H,   012AH,   012FH,   0135H    ;
DW      013BH,   0141H,   0147H,   014CH,   0152H,   0158H,   015EH,   0164H    ;
DW      016AH,   0170H,   0176H,   017CH,   0182H,   0188H,   018FH,   0195H    ;
DW      019BH,   01A1H,   01A7H,   01ADH,   01B3H,   01BAH,   01C0H,   01C6H    ;
DW      01CCH,   01D3H,   01D9H,   01DFH,   01E5H,   01ECH,   01F2H,   01F8H    ;
```

(3) Vf modulation ratio table No. 1

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 1   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.4  60 Hz:  1.0  110 Hz:  1.6
        ;  Table data = (modulation ratio)*100H
VFTBL1: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          02AH,02CH,02DH,02FH,030H,032H ;   0 Hz
DB      033H,035H,036H,038H,039H,03BH,03CH,03EH,03FH,041H ;  10 Hz
DB      043H,044H,046H,047H,049H,04AH,04CH,04DH,04FH,050H ;  20 Hz
DB      052H,053H,055H,057H,058H,05AH,05BH,05DH,05EH,060H ;  30 Hz
DB      061H,063H,064H,066H,067H,069H,06AH,06CH,06EH,06FH ;  40 Hz
DB      071H,072H,074H,075H,077H,078H,07AH,07BH,07DH,07EH ;  50 Hz
DB      080H,082H,083H,085H,086H,088H,089H,08BH,08CH,08EH ;  60 Hz
DB      08FH,091H,092H,094H,096H,097H,099H,09AH,09CH,09DH ;  70 Hz
DB      09FH,0A1H,0A2H,0A3H,0A5H,0A6H,0A8H,0A9H,0ABH,0ADH ;  80 Hz
DB      0AEH,0B0H,0B1H,0B3H,0B4H,0B6H,0B7H,0B9H,0BAH,0BCH ;  90 Hz
DB      0BDH,0BFH,0C1H,0C2H,0C4H,0C5H,0C7H,0C8H,0CAH,0CBH ; 100 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 110 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 120 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 130 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 140 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 150 Hz
DB      0CDH                                              ; 160 Hz
```

(4) Vf modulation ratio table No. 2

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 2   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.2  60 Hz:  1.0  110 Hz:  1.6
        ;  Table data = (modulation ratio)*100H
VFTBL2: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          00DH,00FH,011H,013H,016H,018H ;   0 Hz
DB      01AH,01CH,01EH,020H,022H,024H,026H,028H,02AH,02CH ;  10 Hz
DB      02EH,030H,032H,034H,036H,038H,03AH,03CH,03EH,041H ;  20 Hz
DB      043H,045H,047H,049H,04BH,04DH,04FH,051H,053H,055H ;  30 Hz
DB      057H,059H,05BH,05DH,05FH,061H,063H,065H,067H,069H ;  40 Hz
DB      06CH,06EH,070H,072H,074H,076H,078H,07AH,07CH,07EH ;  50 Hz
```

```
DB      080H,082H,083H,085H,086H,088H,089H,08BH,08CH,08EH ;  60 Hz
DB      0B8H,0B9H,0B9H,0BAH,0BAH,0BBH,0BBH,0BCH,0BCH,0BDH ;  70 Hz
DB      0BDH,0BEH,0BEH,0BFH,0BFH,0C0H,0C1H,0C1H,0C2H,0C2H ;  80 Hz
DB      0C3H,0C3H,0C4H,0C4H,0C5H,0C5H,0C6H,0C6H,0C7H,0C7H ;  90 Hz
DB      0C8H,0C8H,0C9H,0C9H,0CAH,0CAH,0CBH,0CBH,0CCH,0CCH ; 100 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 110 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 120 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 130 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 140 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 150 Hz
DB      0CDH                                               ; 160 Hz
```

(5) Vf modulation ratio table No. 3

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 3   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.4  60 Hz:  1.4  110 Hz:  1.6
        ;  Table data = (modulation ratio)*100H
VFTBL3: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          024H,026H,029H,02CH,02EH,031H ;   0 Hz
DB      033H,036H,038H,03BH,03DH,040H,043H,045H,048H,04AH ;  10 Hz
DB      04DH,04FH,052H,054H,057H,05AH,05CH,05FH,061H,064H ;  20 Hz
DB      066H,069H,06CH,06EH,071H,073H,076H,078H,07BH,07DH ;  30 Hz
DB      080H,083H,085H,088H,08AH,08DH,08FH,092H,094H,097H ;  40 Hz
DB      09AH,09CH,09FH,0A1H,0A4H,0A6H,0A9H,0ACH,0AEH,0B1H ;  50 Hz
DB      0B3H,0B4H,0B4H,0B5H,0B5H,0B6H,0B6H,0B7H,0B7H,0B8H ;  60 Hz
DB      0B8H,0B9H,0B9H,0BAH,0BAH,0BBH,0BBH,0BCH,0BCH,0BDH ;  70 Hz
DB      0BDH,0BEH,0BEH,0BFH,0BFH,0C0H,0C1H,0C1H,0C2H,0C2H ;  80 Hz
DB      0C3H,0C3H,0C4H,0C4H,0C5H,0C5H,0C6H,0C6H,0C7H,0C7H ;  90 Hz
DB      0C8H,0C8H,0C9H,0C9H,0CAH,0CAH,0CBH,0CBH,0CCH,0CCH ; 100 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 110 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 120 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 130 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 140 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 150 Hz
DB      0CDH                                               ; 160 Hz
```

(6) Vf modulation ratio table No. 4

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 4   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.2  60 Hz:  1.4  110 Hz:  1.6
        ;  Table data = (modulation ratio)*100H
VFTBL4: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          007H,00AH,00DH,010H,013H,017H ;   0 Hz
DB      01AH,01DH,020H,023H,026H,029H,02CH,02FH,032H,035H ;  10 Hz
DB      038H,03BH,03EH,042H,045H,048H,04BH,04EH,051H,054H ;  20 Hz
DB      057H,05AH,05DH,060H,063H,066H,069H,06DH,070H,073H ;  30 Hz
DB      076H,079H,07CH,07FH,082H,085H,088H,08BH,08EH,091H ;  40 Hz
DB      094H,098H,09BH,09EH,0A1H,0A4H,0A7H,0AAH,0ADH,0B0H ;  50 Hz
DB      0B3H,0B4H,0B4H,0B5H,0B5H,0B6H,0B6H,0B7H,0B7H,0B8H ;  60 Hz
DB      0B8H,0B9H,0B9H,0BAH,0BAH,0BBH,0BBH,0BCH,0BCH,0BDH ;  70 Hz
DB      0BDH,0BEH,0BEH,0BFH,0BFH,0C0H,0C1H,0C1H,0C2H,0C2H ;  80 Hz
DB      0C3H,0C3H,0C4H,0C4H,0C5H,0C5H,0C6H,0C6H,0C7H,0C7H ;  90 Hz
```

```
DB      0C8H,0C8H,0C9H,0C9H,0CAH,0CAH,0CBH,0CBH,0CCH,0CCH ; 100 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 110 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 120 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 130 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 140 Hz
DB      0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH,0CDH ; 150 Hz
DB      0CDH                                               ; 160 Hz
```

(7) Vf modulation ratio table No. 5

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 5   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.4  60 Hz:  1.0  80 Hz:  1.2
        ;  Table data = (modulation ratio)*100H
VFTBL5: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          02AH,02CH,02DH,02FH,030H,032H ;   0 Hz
DB      033H,035H,036H,038H,039H,03BH,03CH,03EH,03FH,041H ;  10 Hz
DB      043H,044H,046H,047H,049H,04AH,04CH,04DH,04FH,050H ;  20 Hz
DB      052H,053H,055H,057H,058H,05AH,05BH,05DH,05EH,060H ;  30 Hz
DB      061H,063H,064H,066H,067H,069H,06AH,06CH,06EH,06FH ;  40 Hz
DB      071H,072H,074H,075H,077H,078H,07AH,07BH,07DH,07EH ;  50 Hz
DB      080H,081H,083H,084H,085H,086H,088H,089H,08AH,08CH ;  60 Hz
DB      08DH,08EH,08FH,091H,092H,093H,094H,096H,097H,098H ;  70 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  80 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  90 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 100 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 110 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 120 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 130 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 140 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 150 Hz
DB      09AH                                               ; 160 Hz
```

(8) Vf modulation ratio table No. 6

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 6   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.2  60 Hz:  1.0  80 Hz  :1.2
        ;  Table data = (modulation ratio)*100H
VFTBL6: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          00DH,00FH,011H,013H,016H,018H ;   0 Hz
DB      01AH,01CH,01EH,020H,022H,024H,026H,028H,02AH,02CH ;  10 Hz
DB      02EH,030H,032H,034H,036H,038H,03AH,03CH,03EH,041H ;  20 Hz
DB      043H,045H,047H,049H,04BH,04DH,04FH,051H,053H,055H ;  30 Hz
DB      057H,059H,05BH,05DH,05FH,061H,063H,065H,067H,069H ;  40 Hz
DB      06CH,06EH,070H,072H,074H,076H,078H,07AH,07CH,07EH ;  50 Hz
DB      080H,081H,083H,084H,085H,086H,088H,089H,08AH,08CH ;  60 Hz
DB      08DH,08EH,08FH,091H,092H,093H,094H,096H,097H,098H ;  70 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  80 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  90 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 100 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 110 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 120 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 130 Hz
```

```
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 140 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 150 Hz
DB      09AH                                               ; 160 Hz
```

(9) Vf modulation ratio table No. 7

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 7   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.2  60 Hz:  1.2  80 Hz:  1.2
        ;  Table data = (modulation ratio)*100H
VFTBL7: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          027H,029H,02BH,02DH,02FH,031H ;   0 Hz
DB      033H,035H,037H,039H,03BH,03DH,03FH,042H,044H,046H ;  10 Hz
DB      048H,04AH,04CH,04EH,050H,052H,054H,056H,058H,05AH ;  20 Hz
DB      05CH,05EH,060H,062H,064H,066H,068H,06AH,06DH,06FH ;  30 Hz
DB      071H,073H,075H,077H,079H,07BH,07DH,07FH,081H,083H ;  40 Hz
DB      085H,087H,089H,08BH,08DH,08FH,091H,093H,096H,098H ;  50 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  60 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  70 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  80 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  90 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 100 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 110 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 120 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 130 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 140 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 150 Hz
DB      09AH                                               ; 160 Hz
```

(10) Vf modulation ratio table No. 8

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf modulation ratio table No. 8   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  10 Hz:  0.2  60 Hz:  1.2  80 Hz:  1.2
        ;  Table data = (modulation ratio)*100H
VFTBL8: ;+0   +1   +2   +3   +4   +5   +6   +7   +8   +9    [Hz]
DB                          00AH,00DH,00FH,012H,014H,017H ;   0 Hz
DB      01AH,01CH,01FH,021H,024H,026H,029H,02CH,02EH,031H ;  10 Hz
DB      033H,036H,038H,03BH,03DH,040H,043H,045H,048H,04AH ;  20 Hz
DB      04DH,04FH,052H,054H,057H,05AH,05CH,05FH,061H,064H ;  30 Hz
DB      066H,069H,06CH,06EH,071H,073H,076H,078H,07BH,07DH ;  40 Hz
DB      080H,083H,085H,088H,08AH,08DH,08FH,092H,094H,097H ;  50 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  60 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  70 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  80 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ;  90 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 100 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 110 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 120 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 130 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 140 Hz
DB      09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH,09AH ; 150 Hz
DB      09AH                                               ; 160 Hz
```

(11) Vf table storage address table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT   Vf table storage address table   TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
VFTBL:
DW      VFTBL1, VFTBL2, VFTBL3, VFTBL4
DW      VFTBL5, VFTBL6, VFTBL7, VFTBL8
```

(12) Carrier frequency table (10*2 bytes)

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT  Carrier frequency table (10*2 bytes)  TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  Table data = (carrier frequency [Hz])
CRRYTBL:
DW          0,  200,  400,  600,  800, 1000, 1200, 1400, 1600, 1800
DW       2000, 2200, 2400, 2600, 2800, 3000, 3200, 3400, 3600, 3800
DW       4000, 4200, 4400, 4600, 4800, 5000, 5200, 5400, 5600, 5800
DW       6000, 6200, 6400, 6600, 6800, 7000, 7200, 7400, 7600, 7800
DW       8000, 8200, 8400, 8600, 8800, 9000, 9200, 9400, 9600, 9800
DW      10000,10200,10400,10600,10800,11000,11200,11400,11600,11800
DW      12000,12200,12400,12600,12800,13000,13200,13400,13600,13800
DW      14000,14200,14400,14600,14800,15000,15200,15400,15600,15800
DW      16000,16200,16400,16600,16800,17000,17200,17400,17600,17800
DW      18000,18200,18400,18600,18800,19000,19200,19400,19600,19800
DW      20000
```

(13) Maximum frequency limit table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT    Maximum frequency limit table    TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;  Table data = (output frequency number)
FMXTBL: ;+0.2 +0.4 +0.6 +0.8 +1.0 +1.2 +1.4 +1.6 +1.8 +2.0
DB      0, 25,  50,  75, 100, 120, 140, 160, 160, 160, 160   ;  0[kHz]
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ;  2
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ;  4
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ;  6
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ;  8
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 10
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 12
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 14
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 16
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 18
DB        160, 160, 160, 160, 160, 160, 160, 160, 160, 160   ; 20
```

(14) Maximum dead time limit table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT    Maximum dead time limit table    TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ; Table data = (dead time number)
DMXTBL: ;+0.2 +0.4 +0.6 +0.8 +1.0 +1.2 +1.4 +1.6 +1.8 +2.0
DB      0, 32,  32,  32,  32,  32,  32,  32,  32,  32,  32   ;  0[kHz]
DB         32,  32,  32,  32,  32,  32,  32,  32,  32,  31   ;  2
DB         29,  28,  27,  26,  25,  24,  23,  22,  21,  20   ;  4
DB         20,  19,  18,  18,  17,  17,  16,  16,  16,  15   ;  6
DB         15,  14,  14,  14,  13,  13,  13,  13,  12,  12   ;  8
DB         12,  12,  11,  11,  11,  11,  10,  10,  10,  10   ; 10
DB         10,  10,   9,   9,   9,   9,   9,   9,   9,   8   ; 12
DB          8,   8,   8,   8,   8,   8,   8,   9,   7,   7   ; 14
DB          7,   7,   7,   7,   7,   7,   7,   7,   7,   6   ; 16
DB          6,   6,   6,   6,   6,   6,   6,   6,   6,   6   ; 18
```

(15) TM7 operating clock table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT      TM7 operating clock table      TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
TMCLKTBL:
DW       1200H, 007AH          ; fclk
DW       0900H, 003DH          ; fclk/2
DW       8480H, 001EH          ; fclk/4
DW       4240H, 000FH          ; fclk/8
DW      0A120H, 0007H          ; fclk/16
DW      0D090H, 0003H          ; fclk/32
DW      0D090H, 0003H          ; fclk/32
DW      0D090H, 0003H          ; fclk/32
```

(16) Minimum carrier frequency limit table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT  Minimum carrier frequency limit table  TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
CMNTBL10: ;  4 kHz  2 kHz  1 kHz  600 Hz  400 Hz  200 Hz  200 Hz  200 Hz
DB              20,    10,     5,     3,      2,      1,      1,      1

CMNTBL08: ;  16 kHz  8 kHz  4 kHz  2 kHz   1 kHz  600 Hz  600 Hz  600 Hz
DB              80,    40,    20,    10,      5,      3,      3,      3
```

(17) Change rate table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT          Change rate table          TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
CHDSPTBL:       ;************ Display table
DB          5,   10,   15,   20
CHNGTBL:        ;************ Counter table
DW        400,  200,  133,  100
```

(18) Display pattern table

```
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
        ;TT        Display pattern table        TT
        ;TTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTTT
LEDTBL: ; 0    1    2    3    4    5    6    7    8    9
DB       03FH,006H,05BH,04FH,066H,06DH,07DH,027H,07FH,06FH
        ; d    o    P    _
DB       05EH,05CH,073H,000H,000H,000H
        ; 0.   1.   2.   3.   4.   5.   6.   7.   8.   9.
DB       0BFH,086H,0DBH,0CFH,0E6H,0EDH,0FDH,0A7H,0FFH,0EFH
        END
```

6.4 Constant Definitions

```
; *********************************************
;             Constant definitions
; *********************************************

FRQSTOP EQU      0FFH     ; Output stop setting
FOUTINI EQU      004H     ; Initial value of output frequency
DEADMN1 EQU      1        ; Initial value of dead time
VFPINI  EQU      0        ; Initial value of Vf modulation ratio pointer
ADDADR1 EQU      85       ; Inter-phase step address 120° (256/3)
ADDADR2 EQU      170      ; Inter-phase step address 240° ((256/3) x 2)
ADDADR1X EQU     170*2    ; Inter-phase step address 120° (512/3)
ADDADR2X EQU     340*2    ; Inter-phase step address 240° ((512/3) x 2)
KONINI  EQU      100      ; Initial value of hold-down counter
KONRES  EQU      19       ; Re-set value of hold-down counter
KSMPINI EQU      2        ; Key input sampling interval
PSMPINI EQU      2        ; Stop signal sampling interval
SEGINI  EQU      100      ; 8-segment LED flash cycle
LEDINI  EQU      100      ; LED flash cycle
PMSTOP  EQU      0        ; Main mode:  Signal output stop
PMFOUT  EQU      1        ; Main mode:  Constant-frequency output
PMCHNG  EQU      2        ; Main mode:  Output frequency change
SMOUT   EQU      0        ; Key setting mode:  PWM output setting
SMOFF   EQU      1        ; Key setting mode:  Off
KNULL   EQU      0        ; Key code:  Null
KCHNG   EQU      1        ; Key code:  [Changeover]
KMINS   EQU      2        ; Key code:  [-]
KPLUS   EQU      3        ; Key code:  [+]
KONOF   EQU      4        ; Key code:  [ON/OFF]
KERR    EQU      10H      ; Key code:  Inconsistency
DMFOUT  EQU      10H      ; 8-segment LED display mode:  Output frequency
DMCRRY  EQU      11H      ; 8-segment LED display mode:  Carrier frequency
DMDEAD  EQU      12H      ; 8-segment LED display mode:  Dead time
DMCHNG  EQU      03H      ; 8-segment LED display mode:  Frequency change rate
CHRD    EQU      0AH      ; "d " pattern code
CHRO    EQU      0BH      ; "o " pattern code
CHRP    EQU      0CH      ; "P " pattern code
CHRSPC  EQU      0DH      ; "  " pattern code
CHRZ    EQU      10H      ; "0." pattern code

TM0WADR EQU      0FEF6H   ; INTP0 table reference address work register
```

APPENDIX REVISION HISTORY

The revision history of this manual is listed below. The applicable chapter column indicates the chapters in the corresponding edition.

Edition	Revisions from Previous Edition	Revised Section
2nd edition	The following products have been deleted: μPD780924, μPD780964 Subseries The following products have been deleted: μPD780921, μPD780922, μPD780923, μPD780924, μPD78F0924, μPD780961, μPD780962, μPD780963, μPD780964, μPD78F0964 The following products has been added: μPD780983 The representative product has been changed from the μPD780924 to the μPD780988.	Throughout
	The memory map in Figure 2-2 is changed to that of the μPD780988. The circuit diagram in 2.3 is changed to that of the μPD780988.	CHAPTER 2 HARDWARE CONFIGURATION
3rd edition	The following product has been added: μPD780982 The status of the following products has been changed from “under development” to “development completed”: μPD780983, μPD780984	Throughout
4th edition	The following product name has been modified: μPD78F0988 → μPD78F0988A	Throughout
	Figure 3-8 TM7 Operation Timing has been modified.	CHAPTER 3 CONTROL
	The interrupt processing time has been modified accordingly under the following conditions: • TM7 is used as an 8-bit timer. • TM7 is used as a 10-bit timer.	CHAPTER 4 NOTES ON TIME REQUIRED FOR TIMING SET INTERRUPT PROCESSING

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