NEC

MOS INTEGRATED CIRCUIT

μPD784218, 784218Y

16-/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD784218 is a member of the μPD784218 Subseries of the 78K/IV Series. In addition to a high-speed and high-performance CPU, the μPD784218 incorporates a variety of peripheral hardware such as ROM, RAM, I/O ports, 8-bit resolution A/D and D/A converters, timers, serial interfaces, real-time output ports, and an interrupt function.

The μPD784218Y**Note** is the μPD784218 Subseries with a multi-master supporting I^2C bus interface added.

Flash memory versions, the μPD78F4218 and 78F4218Y, which can operate in the same voltage range as the mask ROM versions, and various development tools are also available.

Note Under development

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784218, 784218Y Subseries User's Manual Hardware: U12970E
78K/IV Series User's Manual Instructions: U10905E

FEATURES

- On-chip ROM correction function
- Inherits peripheral functions of μPD78078Y Subseries
- Minimum instruction execution time
  160 ns
  (@ f_{XX} = 12.5 MHz operation with main system clock)
  61 μs
  (@ f_{XT} = 32.768 kHz operation with subsystem clock)
- Internal high-capacity memory
  · ROM: 256 KB
  · RAM: 12,800 bytes
- I/O ports: 86
- Timer/counters: 16-bit timer/event counter × 1 unit
  8-bit timer/event counter × 6 units
- Serial interfaces: 3 channels
  UART/IOE (3-wire serial I/O): 2 channels
  CSI (3-wire serial I/O, multi-master supporting I^2C bus**Note**): 1 channel
- Standby function
  HALT/STOP/IDLE mode
  In power-saving mode: HALT/IDLE mode (with subsystem clock)
- Clock division function
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Clock output function
  Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
- Buzzer output function
  Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
- A/D converter: 8-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- Supply voltage: V_{DD} = 2.2 to 5.5 V

Note μPD784218Y only

Unless otherwise specified, references in this document to the μPD784218 refer to the μPD784218 and the μPD784218Y.

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The mark ★ shows major revised points.

APPLICATIONS

Cellular phones, personal handy phone system (PHS), cordless telephones, CD-ROM, AV equipment

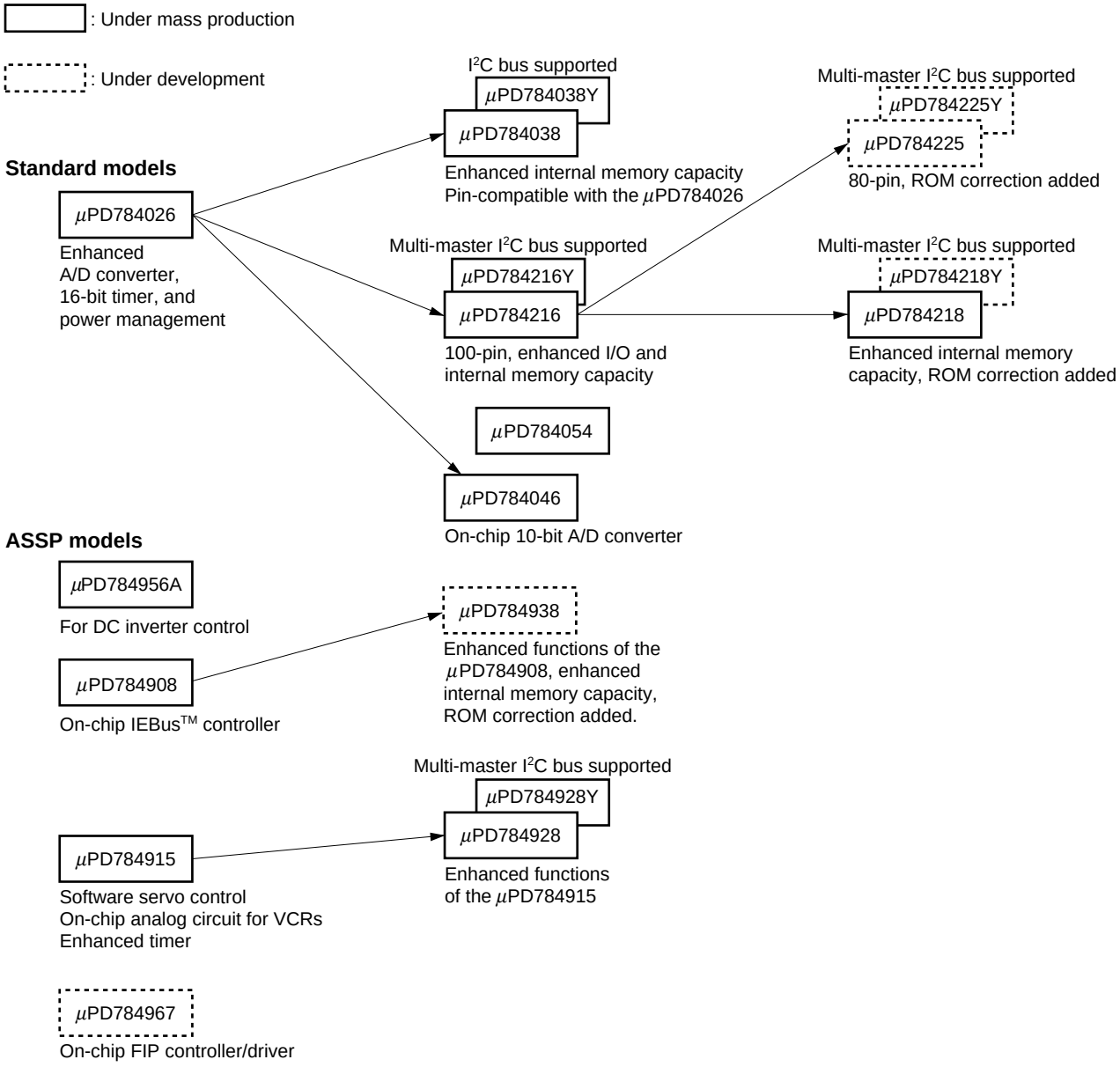
ORDERING INFORMATION

Part Number	Package	Internal ROM (Bytes)	Internal RAM (Bytes)
μPD784218GC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	256 K	12,800
μPD784218GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)	256 K	12,800
μPD784218YGC-×××-8EU**Note**	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	256 K	12,800
μPD784218YGF-×××-3BA**Note**	100-pin plastic QFP (14 × 20 mm)	256 K	12,800

Note Under development

Remark ××× indicates ROM code suffix.

★ 78K/IV SERIES LINEUP



OVERVIEW OF FUNCTIONS (1/2)

Item \ Part Number		μPD784218, μPD784218Y[Note 1]		
Number of basic instructions (mnemonics)		113		
General-purpose registers		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)		
Minimum instruction execution time		• 160 ns/320 ns/640 ns/1,280 ns/2,560 ns (@ f_{XX} = 12.5 MHz operation with main system clock) • 61 μs (@ f_{XT} = 32.768 kHz operation with subsystem clock)		
Internal memory	ROM	256 KB		
	RAM	12,800 bytes		
Memory space		1 MB with program and data spaces combined		
I/O ports	Total	86		
	CMOS input	8		
	CMOS I/O	72		
	N-ch open-drain I/O	6		
Pins with ancillary functions[Note 2]	Pins with pull-up resistor	70		
	LED direct drive outputs	22		
	Middle-voltage pins	6		
Real-time output port		4 bits × 2, or 8 bits × 1		
Timer/counters		Timer/event counter: (16-bit)	Timer counter × 1 Capture/compare register × 2	Pulse output • PPG output • Square wave output • One-shot pulse output
		Timer/event counter 1: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 2: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 5: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 6: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 7: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 8: (8-bit)	Timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
Serial interfaces		• UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O, multi-master supporting I^2C bus[Note 3]): 1 channel		
A/D converter		8-bit resolution × 8 channels		
D/A converter		8-bit resolution × 2 channels		

Notes 1. Under development

2. The pins with ancillary functions are included in the I/O pins.

3. μPD784218Y only

OVERVIEW OF FUNCTIONS (2/2)

Item \ Part Number		μPD784218, μPD784218Y[Note]
Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
Watch timer		1 channel
Watchdog timer		1 channel
Standby		• HALT/STOP/IDLE modes • In low-power consumption mode (with subsystem clock): HALT/IDLE mode
Interrupts	Hardware sources	29 (internal: 20, external: 9)
	Software sources	BRK instruction, BRKCS instruction, operand error
	Non-maskable	Internal: 1, external: 1
	Maskable	Internal: 19, external: 8
		• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
Supply voltage		V_{DD} = 2.2 to 5.5 V
Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)

Note Under development

CONTENTS

★ 1. DIFFERENCES AMONG MODELS IN μPD784218, 784218Y SUBSERIES

The μPD784218Y is the μPD784218 with I^2C bus control added.

The μPD78F4218 and 78F4218Y are provided with a 256 KB flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

Table 1-1. Differences Among Models in μPD784218, 784218Y Subseries

Part Number / Item	μPD784218, μPD784218Y	μPD78F4218, μPD78F4218Y
Internal ROM	256 KB (mask ROM)	256 KB (Flash memory)
Internal RAM	12,800 bytes	
Internal memory size switching register (IMS)	None	Provided[Note]
Supply voltage	V_{DD} = 2.2 to 5.5 V	V_{DD} = 2.7 to 5.5 V
Electrical specifications	Refer to the data sheet for each device.	
Recommended soldering conditions		
TEST pin	Provided	None
V_{PP} pin	None	Provided

Note The internal flash memory capacity and internal RAM capacity can be changed using the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (not engineering samples) of the mask ROM version.

2. DIFFERENCES BETWEEN μPD784218 AND μPD784216

Table 2-1 shows the differences between the μPD784218 and μPD784216.

Table 2-1. Differences between μPD784218 and μPD784216

Part Number / Item	μPD784218	μPD784216
Internal ROM	256 KB	128 KB
Internal RAM	12,800 bytes	8,192 bytes
ROM correction	Provided	None
External access status function	Provided	None

3. MAJOR DIFFERENCES FROM μPD78078, 78079Y SUBSERIES

Item \ Series Name		μPD784218, 784218Y Subseries	μPD78078, 78078Y Subseries
CPU		16-bit CPU	8-bit CPU
Minimum instruction execution time	With main system clock	160 ns (@ 12.5 MHz operation)	400 ns (@ 5.0 MHz operation)
	With subsystem clock	61 μs (@ 32.768 kHz operation)	122 μs (@ 32.768 kHz operation)
Memory space		1 MB	64 KB
I/O ports	Total	86	88
	CMOS input	8	2
	CMOS I/O	72	78
	N-ch open-drain I/O	6	8
Pins with ancillary functions[Note 1]	Pins with pull-up resistor	70	86
	LED direct drive outputs	22	16
	Middle-voltage pins	6	8
Timer/counters		• 16-bit timer/event counter × 1 unit • 8-bit timer/event counter × 6 units	• 16-bit timer/event counter × 1 unit • 8-bit timer/event counter × 4 units
Serial interfaces		• UART/IOE (3-wire serial I/O) × 2 channels • CSI (3-wire serial I/O, multi-master supporting I^2C bus[Note 2]) × 1 channel	• UART/IOE (3-wire serial I/O) × 1 channel • CSI (3-wire serial I/O, 2-wire serial I/O, I^2C bus[Note 3]) × 1 channel • CSI (3-wire serial I/O, 3-wire serial I/O with automatic transmit/receive function) × 1 channel
Interrupts	NMI pin	Provided	None
	Macro service	Provided	None
	Context switching	Provided	None
	Programmable priority	4 levels	None
Standby function		HALT/STOP/IDLE modes In low-power consumption mode: HALT/IDLE modes	HALT/STOP modes
ROM correction		Provided	None
External access status function		Provided	None
Package		• 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)	• 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm) (μPD78P078 and 78P078Y only)

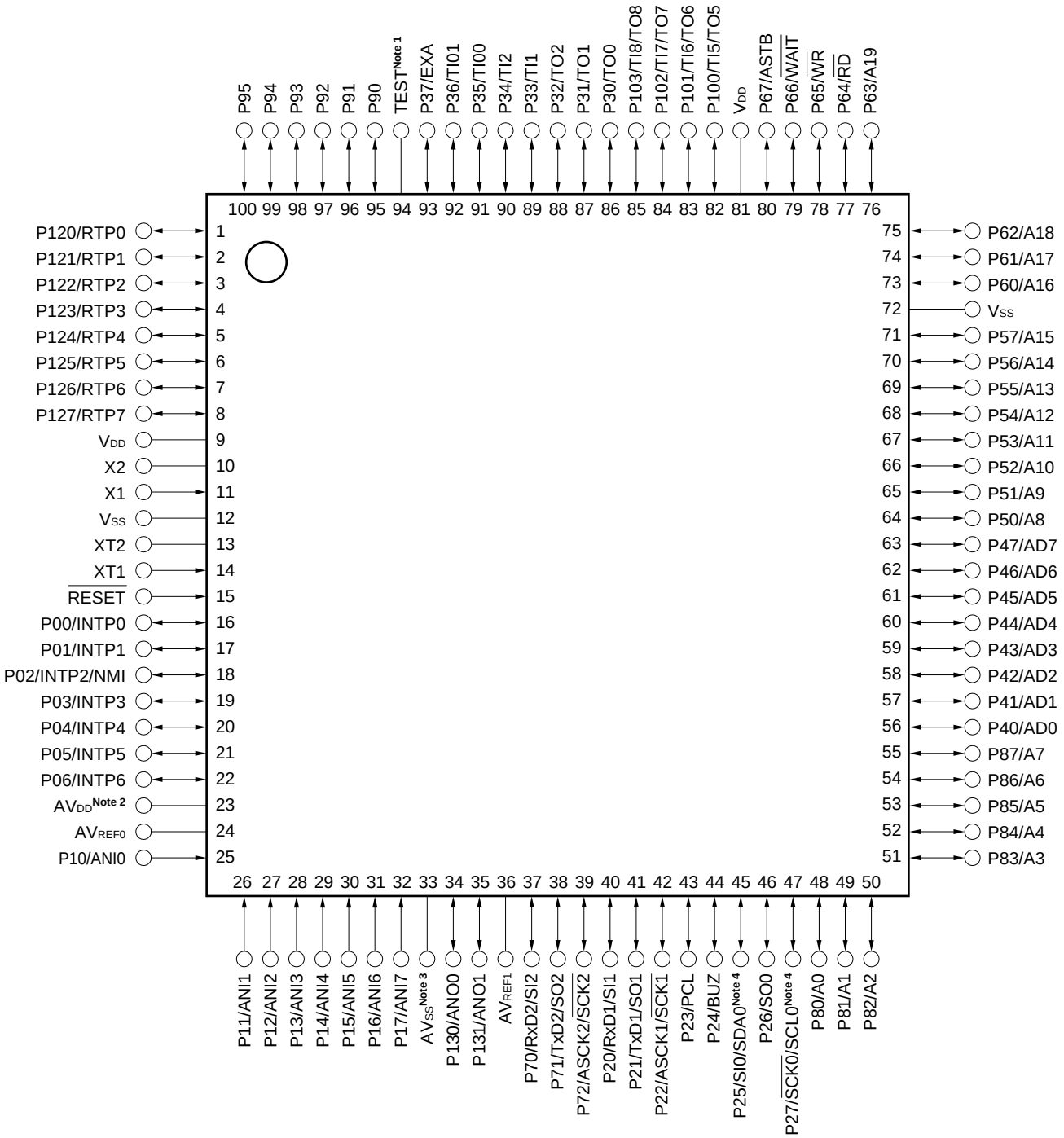
Notes 1. The pins with ancillary functions are included in the I/O pins.

2. μPD784218Y Subseries only

3. μPD78078Y Subseries only

4. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**
  μPD784218GC-×××-8EU, 784218YGC-×××-8EU[Note 5]



Notes 1. Connect the TEST pin directly to VSS or pull down. For the pull-down connection, use of a resistor whose resistance is between 470 Ω and 10 kΩ is recommended.

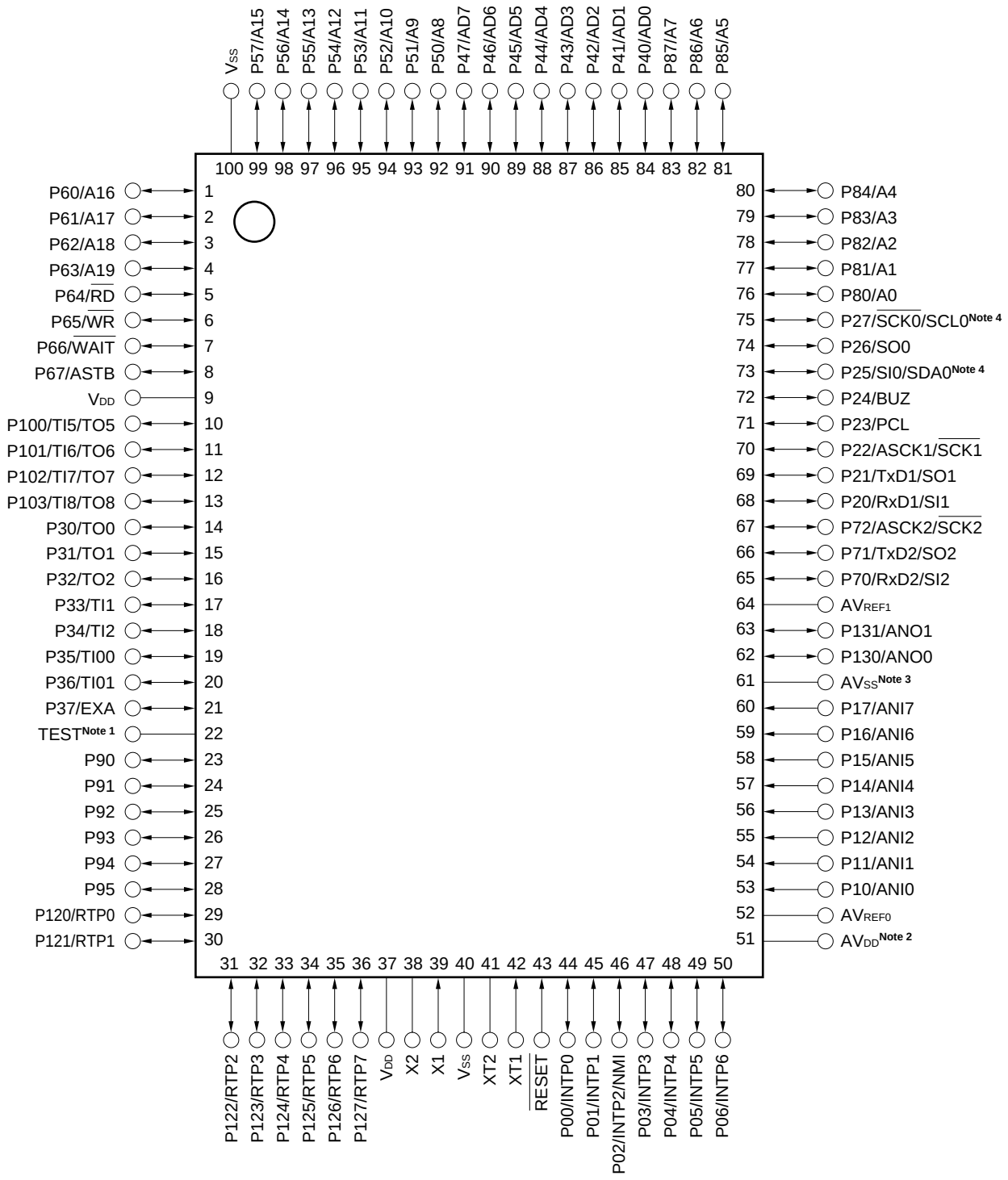
2. Connect the AVDD pin to VDD.

3. Connect the AVSS pin to VSS.

★ **4.** The SCL0 and SDA0 pins are incorporated only in the μPD784218Y.

5. Under development

- **100-pin plastic QFP (14 × 20 mm)**
  μPD784218GF-×××-3BA, 784218YGF-×××-3BA[Note 5]



Notes 1. Connect the TEST pin directly to VSS or pull down. For the pull-down connection, use of a resistor whose resistance is between 470 Ω and 10 kΩ is recommended.

2. Connect the AVDD pin to VDD.

3. Connect the AVSS pin to VSS.

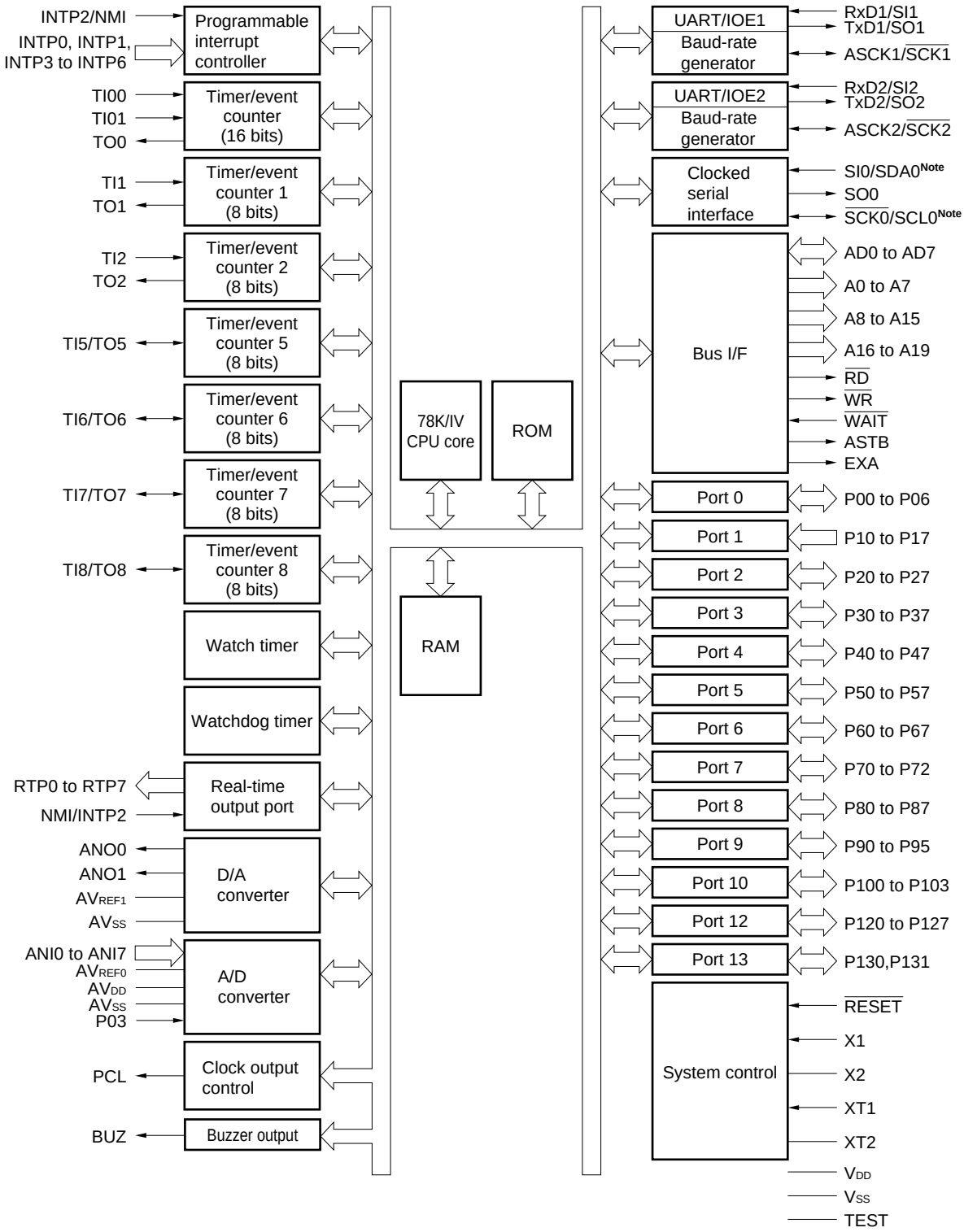
★ **4.** The SCL0 and SDA0 pins are incorporated only in the μPD784218Y.

5. Under development

A0 to A19:	Address Bus	P100 to P103:	Port 10
AD0 to AD7:	Address/Data Bus	P120 to P127:	Port 12
ANI0 to ANI7:	Analog Input	P130, P131:	Port 13
ANO0, ANO1:	Analog Output	PCL:	Programmable Clock
ASCK1, ASCK2	Asynchronous Serial Clock	$\overline{RD}$:	Read Strobe
ASTB:	Address Strobe	$\overline{RESET}$:	Reset
AV_{DD}:	Analog Power Supply	RTP0 to RTP7:	Real-time Output Port
AV_{REF0}, AV_{REF1}:	Analog Reference Voltage	RxD1, RxD2:	Receive Data
AV_{SS}:	Analog Ground	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
BUZ:	Buzzer Clock	SCL0**Note**:	Serial Clock
EXA:	External Access Status Output	SDA0**Note**:	Serial Data
INTP0 to INTP6:	Interrupt from Peripherals	SI0 to SI2:	Serial Input
NMI:	Non-maskable Interrupt	SO0 to SO2:	Serial Output
P00 to P06:	Port 0	TEST:	Test
P10 to P17:	Port 1	TI00, TI01,	
P20 to P27:	Port 2	TI1, TI2, TI5 to TI8:	Timer Input
P30 to P37:	Port 3	TO0 to TO2, TO5 to TO8:	Timer Output
P40 to P47:	Port 4	TxD1, TxD2:	Transmit Data
P50 to P57:	Port 5	V_{DD}:	Power Supply
P60 to P67:	Port 6	V_{SS}:	Ground
P70 to P72:	Port 7	$\overline{WAIT}$:	Wait
P80 to P87:	Port 8	$\overline{WR}$:	Write Strobe
P90 to P95:	Port 9	X1, X2:	Crystal (Main System Clock)
		XT1, XT2:	Crystal (Subsystem Clock)

Note The SCL0 and SDA0 pins are incorporated only in the μPD784218Y.

★ 5. BLOCK DIAGRAM



Note SDA0 and SCL0 are incorporated only in the μPD784218Y and support the I^2C bus interface.

Remark The internal ROM capacity varies depending on the product.

6. PIN FUNCTIONS

6.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 7-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P01		INTP1	
P02		INTP2/NMI	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P06		INTP6	
P10 to P17	Input	ANI0 to ANI7	Port 1 (P1): • 8-bit input-only port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0**Note**	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0**Note**	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software. • LEDs can be driven directly.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software. • LEDs can be driven directly.

Note SDA0 and SCL0 are incorporated only in the μPD784218Y.

6.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software.
P61		A17	
P62		A18	
P63		A19	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P80 to P87	I/O	A0 to A7	Port 8 (P8): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software. • The interrupt control flag (KRIF) is set to 1 when the falling edge is detected at a pin of this port.
P90 to P95	I/O	—	Port 9 (P9): • N-ch open-drain middle-voltage I/O port • 6-bit I/O port • Input/output can be specified in 1-bit units. • LEDs can be driven directly.
P100	I/O	TI5/TO5	Port 10 (P10): • 4-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P101		TI6/TO6	
P102		TI7/TO7	
P103		TI8/TO8	
P120 to P127	I/O	RTP0 to RTP7	Port 12 (P12): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, use of an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Input/output can be specified in 1-bit units.

6.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer counter
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer counter 1
TI2		P34	External count clock input to 8-bit timer counter 2
TI5		P100/TO5	External count clock input to 8-bit timer counter 5
TI6		P101/TO6	External count clock input to 8-bit timer counter 6
TI7		P102/TO7	External count clock input to 8-bit timer counter 7
TI8		P103/TO8	External count clock input to 8-bit timer counter 8
TO0	Output	P30	16-bit timer output (also used as 14-bit PWM output)
TO1		P31	8-bit timer output (also used as 8-bit PWM output)
TO2		P32	
TO5		P100/TI5	
TO6		P101/TI6	
TO7		P102/TI7	
TO8		P103/TI8	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Input	P22/$\overline{\text{SCK1}}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0	Serial data input (3-wire serial clock I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0**Note**	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{\text{SCK0}}$		P27	Serial clock input/output (3-wire serial I/O0)
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0**Note**		P27/$\overline{\text{SCK0}}$	Serial data input/output (I^2C bus)

Note Incorporated only in the μPD784218Y.

6.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
INTP6		P06	
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0 to RTP7	Output	P120 to P127	Real-time output port that outputs data in synchronization with trigger
AD0 to AD7	I/O	P40 to P47	Lower address/data bus for expanding memory externally
A0 to A7	Output	P80 to P87	Lower address bus for expanding memory externally
A8 to A15		P50 to P57	Middle address bus for expanding memory externally
A16 to A19		P60 to P63	Higher address bus for expanding memory externally
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 and port 8 to access external memory
EXA	Output	P37	Status signal output during external memory access
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	Crystal connection for main system clock oscillation
X2	—		
XT1	Input	—	Crystal connection for subsystem clock oscillation
XT2	—		
ANI0 to ANI7	Input	P10 to P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF0}	—	—	To apply reference voltage for A/D converter
AV_{REF1}			To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connect to V_{DD}.
AV_{SS}			GND for A/D converter and D/A converter. Connect to V_{SS}.
V_{DD}			Positive power supply
V_{SS}			GND
TEST			Connect directly to V_{SS} or pull down (this pin is for the IC test). For the pull-down connection, use of a resistor whose resistance is between 470 Ω and 10 kΩ is recommended.

6.3 Pin I/O Circuits and Recommended Connections of Unused Pins

The input/output circuit type of each pin and recommended connections of unused pins are shown in Table 6-1.

For the input/output circuit configuration of each type, refer to Figure 6-1.

★ **Table 6-1. Type of Pin Input/Output Circuits and Recommended Connections of Unused Pins (1/2)**

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-N	I/O	Input: Independently connect to V_{SS} via a resistor Output: Leave open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3 to P06/INTP6			
P10/ANI0 to P17/ANI7	9	Input	Connect to V_{SS} or V_{DD}
P20/RxD1/SI1	10-K	I/O	Input: Independently connect to V_{SS} via a resistor Output: Leave open
P21/TxD1/SO1	10-L		
P22/ASCK1/$\overline{SCK1}$	10-K		
P23/PCL	10-L		
P24/BUZ			
P25/SDA0**Note**/SI0	10-K		
P26/SO0	10-L		
P27/SCL0**Note**/$\overline{SCK0}$	10-K		
P30/TO0 to P32/TO2	12-E		
P33/TI1, P34/TI2	8-N		
P35/TI00, P36/TI01	10-M		
P37/EXA	12-E		
P40/AD0 to P47/AD7	5-A		
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-N		
P71/TxD2/SO2	10-M		
P72/ASCK2/$\overline{SCK2}$	8-N		
P80/A0 to P87/A7	12-E		
P90 to P95	13-D		
P100/TI5/TO5	8-N		
P101/TI6/TO6			
P102/TI7/TO7			
P103/TI8/TO8			
P120/RTP0 to P127/RTP7	12-E		

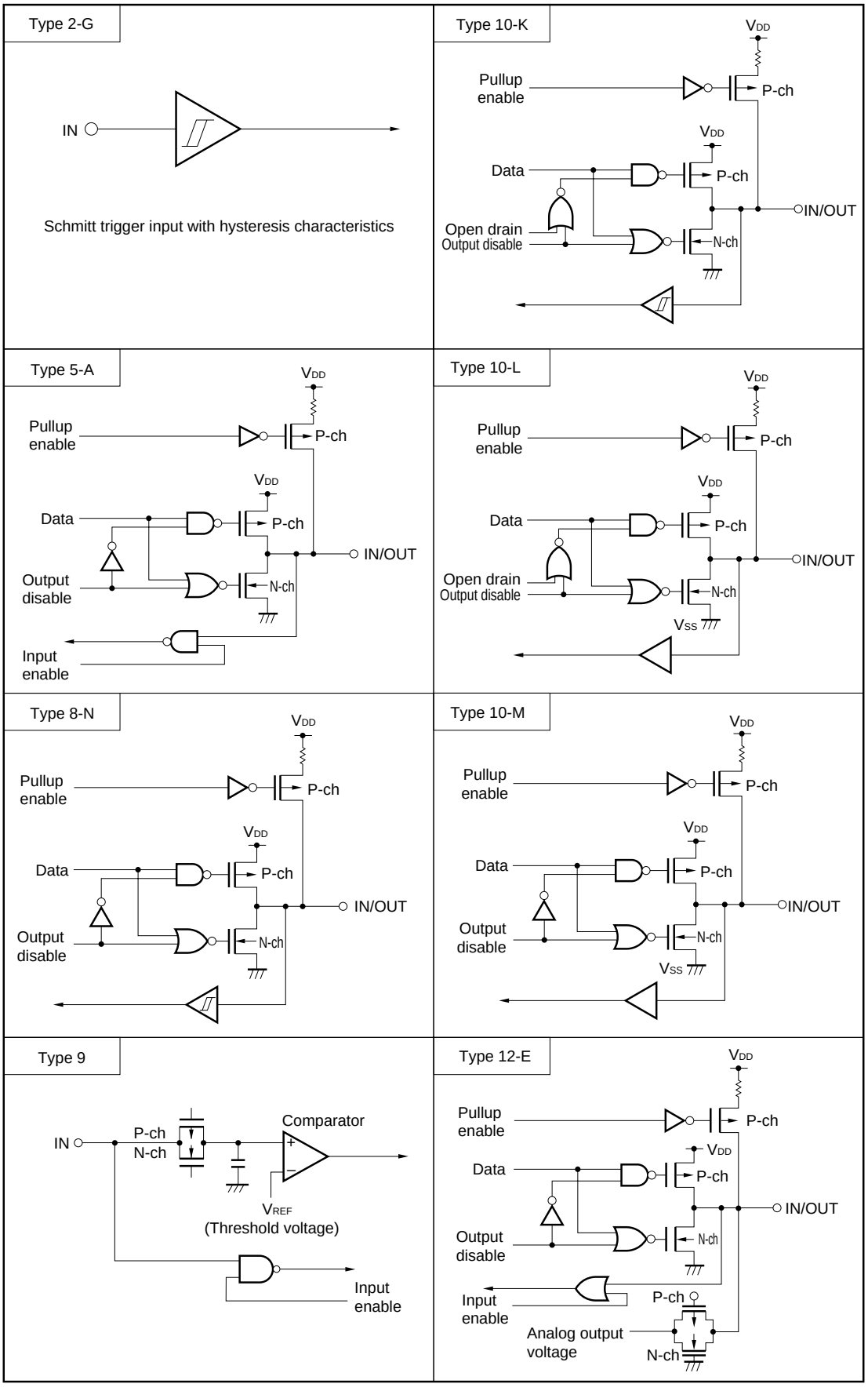
Note SDA0 and SCL0 are incorporated only in the μPD784218Y.

Table 6-1. Types of Pin Input/Output Circuits and Recommended Connections of Unused Pins (2/2)

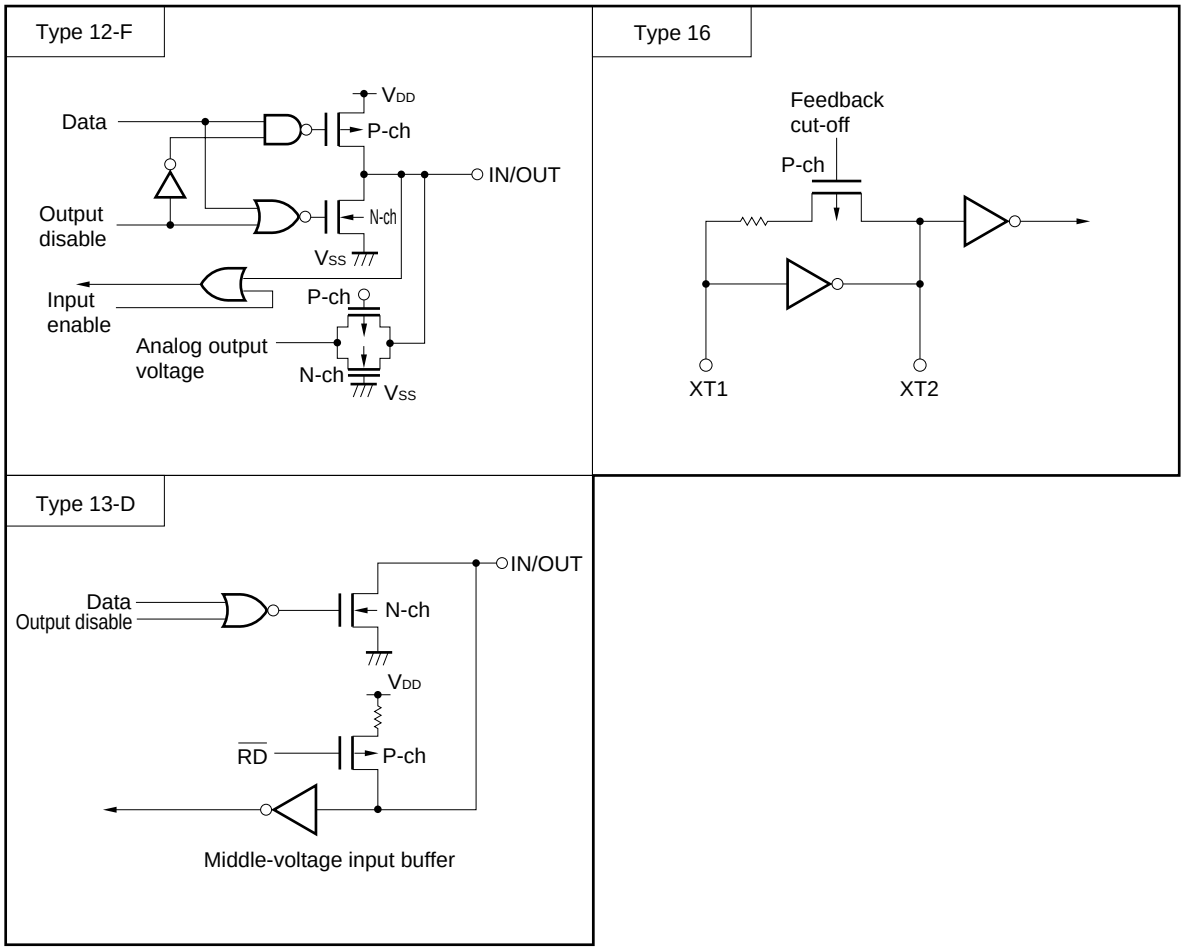
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P130/ANO0, P131/ANO1	12-F	I/O	Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
$\overline{RESET}$	2-G	Input	—
XT1	16		Connect to V_{SS}
XT2		—	Leave open
AV_{REF0}	—		Connect to V_{SS}
AV_{REF1}			Connect to V_{DD}
AV_{DD}			
AV_{SS}			Connect to V_{SS}
TEST			Connect directly to V_{SS} or pull down. For the pull-down connection, use of a resistor whose resistance is between 470 Ω and 10 kΩ is recommended.

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

★ **Figure 6-1. Types of Pin I/O Circuits (1/2)**



★ **Figure 6-1. Types of Pin I/O Circuits (2/2)**



7. CPU ARCHITECTURE

★ 7.1 Memory Space

A memory space of 1 MB can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be specified by the LOCATION instruction. The LOCATION instruction must always be executed after reset cancellation, and must not be used more than once.

(1) When LOCATION 0H instruction is executed

- **Internal memory**

  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784218, μPD784218Y	0CD00H to 0FFFFH	00000H to 0CCFFH 10000H to 3FFFFH

Caution The following areas that overlap the internal data area of the internal ROM cannot be used when the LOCATION 0 instruction is executed.

Part Number	Unusable Area
μPD784218, μPD784218Y	0CD00H to 0FFFFH (13,056 bytes)

- **External memory**

  The external memory is accessed in external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

- **Internal memory**

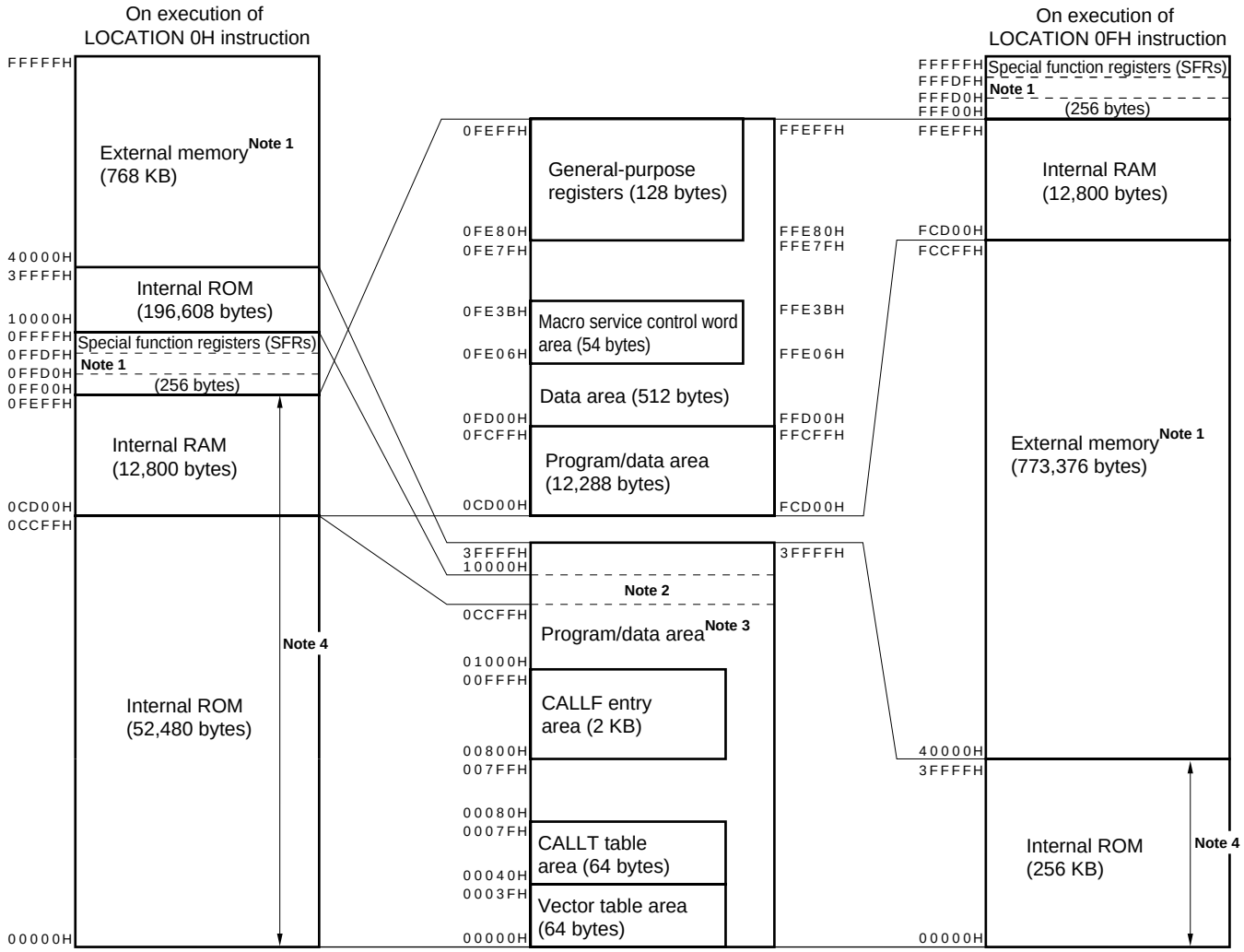
  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784218, μPD784218Y	FCD00H to FFFFFH	00000H to 3FFFFH

- **External memory**

  The external memory is accessed in external memory expansion mode.

Figure 7-1. Memory Map of μPD784218, 784218Y



Notes 1. Accessed in external memory expansion mode.

2. This 13,056-byte area can be used as internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0H instruction: 249,088 bytes, on execution of LOCATION 0FH instruction: 262,144 bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

7.2 CPU Registers

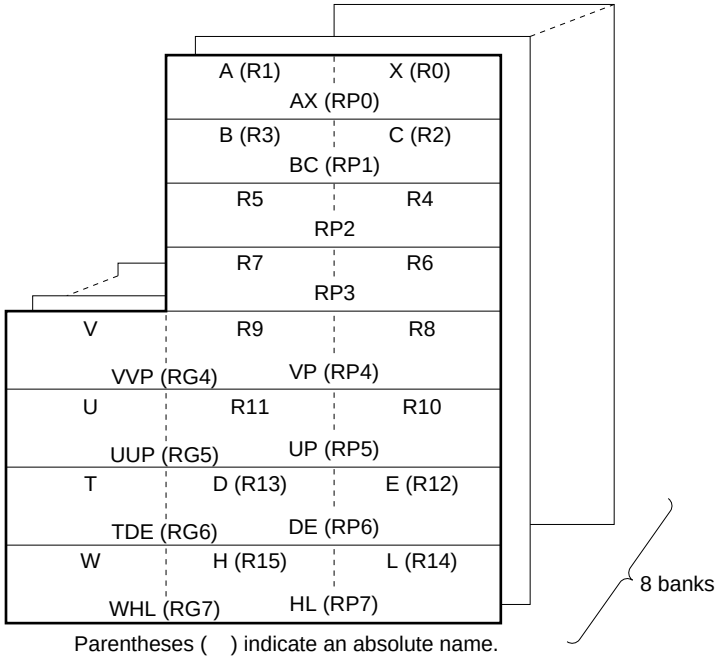
7.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit registers can be also used in pairs as a 16-bit register. Of the 16-bit registers, four can be used in combination with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of these register sets are available and can be selected by using software or the context switching function.

The general-purpose registers except the V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 7-2. General-Purpose Register Format



Parentheses ( ) indicate an absolute name.

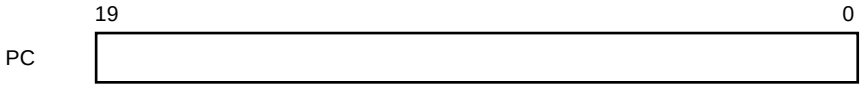
Caution Registers R4, R5, R6, R7, RP2, and RP3 can be used as the X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only for recycling the program of the 78K/III Series.

7.2.2 Control registers

(1) Program counter (PC)

The program counter is a 20-bit register whose contents are automatically updated when the program is executed.

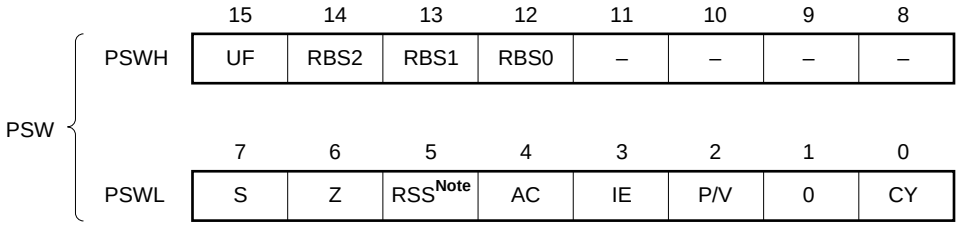
Figure 7-3. Program Counter (PC) Format



(2) Program status word (PSW)

This register holds the statuses of the CPU. Its contents are automatically updated when the program is executed.

Figure 7-4. Program Status Word (PSW) Format

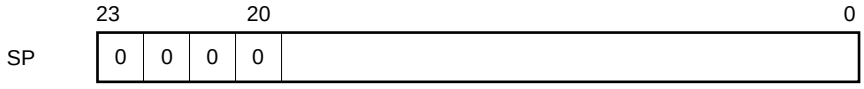


Note This flag is provided to maintain compatibility with the 78K/III Series. Be sure to clear this flag to 0, except when the software for the 78K/III Series is used.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the higher 4 bits of this pointer.

Figure 7-5. Stack Pointer (SP) Format



7.2.3 Special function registers (SFRs)

The special function registers, such as the mode registers and control registers of the internal peripheral hardware, are registers to which special functions are allocated. These registers are mapped to the 256-byte space of addresses 0FF00H through 0FFFFH[Note].

Note On execution of the LOCATION 0H instruction. FFF00H through FFFFFH on execution of the LOCATION 0FH instruction.

Caution Do not access an address in this area to which no SFR is allocated. If such an address is accessed by mistake, the μPD784218 may enter a deadlock state. This deadlock state can be cleared only by inputting the $\overline{\text{RESET}}$ signal.

Table 7-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Symbol ..... Symbol indicating an SFR. This symbol is reserved for NEC's assembler (RA78K4). It can be used as sfr variable by the #pragma sfr command with the C compiler (CC78K4).

- R/W ..... Indicates whether the SFR is read-only, write-only, or read/write.
  R/W: Read/write
  R: Read-only
  W: Write-only

- Bit units for manipulation .. Bit units in which the value of the SFR can be manipulated.
  SFRs that can be manipulated in 16-bit units can be described as the operand sfrp of an instruction. To specify the address of this SFR, describe an even address.
  SFRs that can be manipulated in 1-bit units can be described as the operand of a bit manipulation instruction.

- After reset ..... Indicates the status of the register when the $\overline{\text{RESET}}$ signal has been input.

Table 7-1. Special Function Register (SFR) List (1/4)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FF00H	Port 0	P0	R/W	√	√	—	00H[Note 2]
0FF01H	Port 1	P1	R	√	√	—	
0FF02H	Port 2	P2	R/W	√	√	—	
0FF03H	Port 3	P3		√	√	—	
0FF04H	Port 4	P4		√	√	—	
0FF05H	Port 5	P5		√	√	—	
0FF06H	Port 6	P6		√	√	—	
0FF07H	Port 7	P7		√	√	—	
0FF08H	Port 8	P8		√	√	—	
0FF09H	Port 9	P9		√	√	—	
0FF0AH	Port 10	P10		√	√	—	
0FF0CH	Port 12	P12		√	√	—	
0FF0DH	Port 13	P13		√	√	—	
0FF10H	16-bit timer counter	TM0	R	—	—	√	0000H
0FF11H							
0FF12H	Capture/compare register 00 (16-bit timer/event counter)	CR00	R/W	—	—	√	
0FF13H							
0FF14H	Capture/compare register 01 (16-bit timer/event counter)	CR01		—	—	√	
0FF15H							
0FF16H	Capture/compare control register 0	CRC0		√	√	—	00H
0FF18H	16-bit timer mode control register	TMC0		√	√	—	
0FF1AH	16-bit timer output control register	TOC0		√	√	—	
0FF1CH	Prescaler mode register 0	PRM0		√	√	—	
0FF20H	Port mode 0 register	PM0		√	√	—	FFH
0FF22H	Port mode 2 register	PM2		√	√	—	
0FF23H	Port mode 3 register	PM3		√	√	—	
0FF24H	Port mode 4 register	PM4		√	√	—	
0FF25H	Port mode 5 register	PM5		√	√	—	
0FF26H	Port mode 6 register	PM6		√	√	—	
0FF27H	Port mode 7 register	PM7		√	√	—	
0FF28H	Port mode 8 register	PM8		√	√	—	
0FF29H	Port mode 9 register	PM9		√	√	—	
0FF2AH	Port mode 10 register	PM10		√	√	—	
0FF2CH	Port mode 12 register	PM12		√	√	—	
0FF2DH	Port mode 13 register	PM13		√	√	—	

Notes 1. When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. Because each port is initialized to input mode after reset, “00H” is not actually read. The output latch is initialized to “0”.

Table 7-1. Special Function Register (SFR) List (2/4)

Address[Note]	Special Function Register (SFR) Name	Symbol		R/W	Bit Units for Manipulation			After Reset
					1 bit	8 bits	16 bits	
0FF30H	Pull-up resistor option register 0	PU0		R/W	√	√	—	00H
0FF32H	Pull-up resistor option register 2	PU2			√	√	—	
0FF33H	Pull-up resistor option register 3	PU3			√	√	—	
0FF37H	Pull-up resistor option register 7	PU7			√	√	—	
0FF38H	Pull-up resistor option register 8	PU8			√	√	—	
0FF3AH	Pull-up resistor option register 10	PU10			√	√	—	
0FF3CH	Pull-up resistor option register 12	PU12			√	√	—	
0FF40H	Clock output control register	CKS			√	√	—	
0FF42H	Port function control register	PF2			√	√	—	
0FF4EH	Pull-up resistor option register	PUO			√	√	—	
0FF50H	8-bit timer counter 1	TM1	TM1W	R	—	√	√	0000H
0FF51H	8-bit timer counter 2	TM2			—	√		
0FF52H	Compare register 10 (8-bit timer/event counter 1)	CR10	CR1W	R/W	—	√	√	
0FF53H	Compare register 20 (8-bit timer/event counter 2)	CR20			—	√		
0FF54H	8-bit timer mode control register 1	TMC1	TMC1W		√	√	√	
0FF55H	8-bit timer mode control register 2	TMC2			√	√		
0FF56H	Prescaler mode register 1	PRM1	PRM1W		√	√	√	
0FF57H	Prescaler mode register 2	PRM2			√	√		
0FF60H	8-bit timer counter 5	TM5	TM5W	R	—	√	√	
0FF61H	8-bit timer counter 6	TM6			—	√		
0FF62H	8-bit timer counter 7	TM7	TM7W		—	√	√	
0FF63H	8-bit timer counter 8	TM8			—	√		
0FF64H	Compare register 50 (8-bit timer/event counter 5)	CR50	CR5W	R/W	—	√	√	
0FF65H	Compare register 60 (8-bit timer/event counter 6)	CR60			—	√		
0FF66H	Compare register 70 (8-bit timer/event counter 7)	CR70	CR7W		—	√	√	
0FF67H	Compare register 80 (8-bit timer/event counter 8)	CR80			—	√		
0FF68H	8-bit timer mode control register 5	TMC5	TMC5W		√	√	√	
0FF69H	8-bit timer mode control register 6	TMC6			√	√		
0FF6AH	8-bit timer mode control register 7	TMC7	TMC7W		√	√	√	
0FF6BH	8-bit timer mode control register 8	TMC8			√	√		
0FF6CH	Prescaler mode register 5	PRM5	PRM5W		√	√	√	
0FF6DH	Prescaler mode register 6	PRM6			√	√		
0FF6EH	Prescaler mode register 7	PRM7	PRM7W		√	√	√	
0FF6FH	Prescaler mode register 8	PRM8			√	√		
0FF70H	Asynchronous serial interface mode register 1	ASIM1			√	√	—	00H
0FF71H	Asynchronous serial interface mode register 2	ASIM2			√	√	—	
0FF72H	Asynchronous serial interface status register 1	ASIS1		R	√	√	—	
0FF73H	Asynchronous serial interface status register 2	ASIS2			√	√	—	

Note When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

Table 7-1. Special Function Register (SFR) List (3/4)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FF74H	Transmit shift register 1	TXS1	W	—	√	—	FFH
	Receive buffer register 1	RXB1	R	—	√	—	
0FF75H	Transmit shift register 2	TXS2	W	—	√	—	
	Receive buffer register 2	RXB2	R	—	√	—	
0FF76H	Baud rate generator control register 1	BRGC1	R/W	√	√	—	00H
0FF77H	Baud rate generator control register 2	BRGC2		√	√	—	
0FF7AH	Oscillation mode select register	CC		√	√	—	
0FF80H	A/D converter mode register	ADM		√	√	—	
0FF81H	A/D converter input select register	ADIS		√	√	—	
0FF83H	A/D conversion result register	ADCR	R	—	√	—	Undefined
0FF84H	D/A conversion value setting register 0	DACS0	R/W	√	√	—	00H
0FF85H	D/A conversion value setting register 1	DACS1		√	√	—	
0FF86H	D/A converter mode register 0	DAM0		√	√	—	
0FF87H	D/A converter mode register 1	DAM1		√	√	—	
0FF88H	ROM correction control register	CORC		√	√	—	
0FF89H	ROM correction address pointer H	CORAH		—	√	—	
0FF8AH	ROM correction address pointer L	CORAL		—	—	√	0000H
0FF8BH							
0FF8CH	External bus type select register	EBTS		√	√	—	00H
0FF8DH	External access status enable register	EXAE		√	√	—	
0FF90H	Serial operation mode register 0	CSIM0		√	√	—	
0FF91H	Serial operation mode register 1	CSIM1		√	√	—	
0FF92H	Serial operation mode register 2	CSIM2		√	√	—	
0FF94H	Serial I/O shift register 0	SIO0		—	√	—	
0FF95H	Serial I/O shift register 1	SIO1		—	√	—	
0FF96H	Serial I/O shift register 2	SIO2		—	√	—	
0FF98H	Real-time output buffer register L	RTBL		—	√	—	
0FF99H	Real-time output buffer register H	RTBH		—	√	—	
0FF9AH	Real-time output port mode register	RTPM		√	√	—	
0FF9BH	Real-time output port control register	RTPC		√	√	—	
0FF9CH	Watch timer mode control register	WTM		√	√	—	
0FFA0H	External interrupt rising edge enable register	EGP0		√	√	—	
0FFA2H	External interrupt falling edge enable register	EGN0		√	√	—	
0FFA8H	In-service priority register	ISPR	R	√	√	—	
0FFA9H	Interrupt select control register	SNMI	R/W	√	√	—	
0FFAAH	Interrupt mode control register	IMC		√	√	—	80H
0FFACH	Interrupt mask flag register 0L	MK0L | MK0		√	√	√	FFFFH
0FFADH	Interrupt mask flag register 0H	MK0H		√	√		
0FFAEH	Interrupt mask flag register 1L	MK1L | MK1		√	√	√	
0FFAFH	Interrupt mask flag register 1H	MK1H		√	√		
0FFB0H	I^2C bus control register[Note 2]	IICC0		√	√	—	00H
0FFB2H	Prescaler mode register for serial clock	SRPM0		√	√	—	

Notes 1. When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. μPD784218Y only

Table 7-1. Special Function Register (SFR) List (4/4)

Address[Note 1]	Special Function Register (SFR) Name	Symbol	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FFB4H	Slave address register	SVA0	R/W	√	√	—	00H
0FFB6H	I^2C bus status register[Note 2]	IICS0	R	√	√	—	
0FFB8H	Serial shift register	IIC0	R/W	√	√	—	
0FFC0H	Standby control register	STBC		—	√	—	30H
0FFC2H	Watchdog timer mode register	WDM		—	√	—	00H
0FFC4H	Memory expansion mode register	MM		√	√	—	20H
0FFC7H	Programmable wait control register 1	PWC1		√	√	—	AAH
0FFCEH	Clock status register	PCS	R	√	√	—	32H
0FFCFH	Oscillation stabilization time specification register	OSTS	R/W	√	√	—	00H
0FFD0H to 0FFDFH	External SFR area	—		√	√	—	—
0FFE0H	Interrupt control register (INTWDTM)	WDTIC		√	√	—	43H
0FFE1H	Interrupt control register (INTP0)	PIC0		√	√	—	
0FFE2H	Interrupt control register (INTP1)	PIC1		√	√	—	
0FFE3H	Interrupt control register (INTP2)	PIC2		√	√	—	
0FFE4H	Interrupt control register (INTP3)	PIC3		√	√	—	
0FFE5H	Interrupt control register (INTP4)	PIC4		√	√	—	
0FFE6H	Interrupt control register (INTP5)	PIC5		√	√	—	
0FFE7H	Interrupt control register (INTP6)	PIC6		√	√	—	
0FFE8H	Interrupt control register (INTIIC0/INTCSI0)	CSIIC0		√	√	—	
0FFE9H	Interrupt control register (INTSER1)	SERIC1		√	√	—	
0FFEAH	Interrupt control register (INTSR1/INTCSI1)	SRIC1		√	√	—	
0FFEBH	Interrupt control register (INTST1)	STIC1		√	√	—	
0FFECH	Interrupt control register (INTSER2)	SERIC2		√	√	—	
0FFEDH	Interrupt control register (INTSR2/INTCSI2)	SRIC2		√	√	—	
0FFEEH	Interrupt control register (INTST2)	STIC2		√	√	—	
0FFEFH	Interrupt control register (INTTM3)	TMIC3		√	√	—	
0FFF0H	Interrupt control register (INTTM00)	TMIC00		√	√	—	
0FFF1H	Interrupt control register (INTTM01)	TMIC01		√	√	—	
0FFF2H	Interrupt control register (INTTM1)	TMIC1		√	√	—	
0FFF3H	Interrupt control register (INTTM2)	TMIC2		√	√	—	
0FFF4H	Interrupt control register (INTAD)	ADIC		√	√	—	
0FFF5H	Interrupt control register (INTTM5)	TMIC5		√	√	—	
0FFF6H	Interrupt control register (INTTM6)	TMIC6		√	√	—	
0FFF7H	Interrupt control register (INTTM7)	TMIC7		√	√	—	
0FFF8H	Interrupt control register (INTTM8)	TMIC8		√	√	—	
0FFF9H	Interrupt control register (INTWT)	WTIC		√	√	—	
0FFFAH	Interrupt control register (INTKR)	KRIC		√	√	—	

Notes 1. When the LOCATION 0H instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

2. μPD784218Y only

8. PERIPHERAL HARDWARE FUNCTION FEATURES

8.1 Ports

The ports shown in Figure 8-1 are provided to make various control operations possible. Table 8-1 shows the function of each port. Ports 0, 2 through 8, 10, and 12 can be connected to internal pull-up resistors by software when inputting.

Figure 8-1. Port Configuration

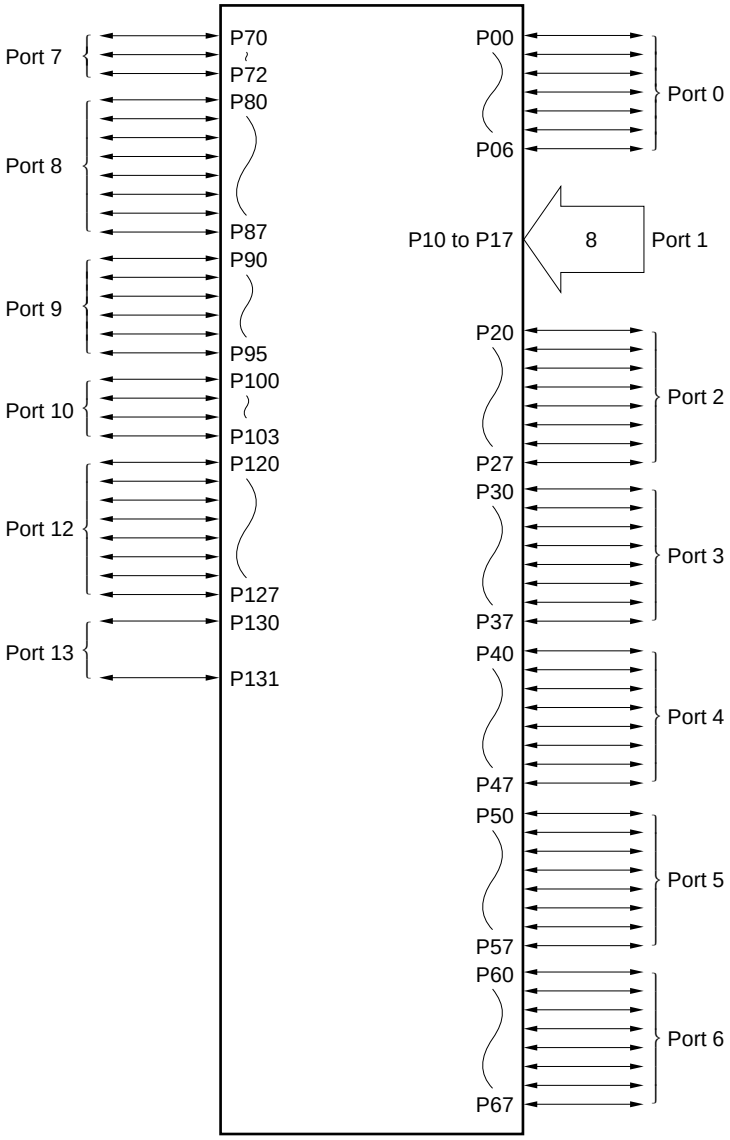


Table 8-1. Port Functions

Port Name	Pin Name	Function	Specification of Pull-up Resistor Connection by Software
Port 0	P00 to P06	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 1	P10 to P17	• Input port	—
Port 2	P20 to P27	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 3	P30 to P37	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 4	P40 to P47	• Can be set in input or output mode in 1-bit units • Can directly drive LEDs	Can be specified in 1-port units
Port 5	P50 to P57	• Can be set in input or output mode in 1-bit units • Can directly drive LEDs	Can be specified in 1-port units
Port 6	P60 to P67	• Can be set in input or output mode in 1-bit units	Can be specified in 1-port units
Port 7	P70 to P72	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 8	P80 to P87	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 9	P90 to P95	• N-ch open-drain I/O port • Can be set in input or output mode in 1-bit units • Can directly drive LEDs	—
Port 10	P100 to P103	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 12	P120 to P127	• Can be set in input or output mode in 1-bit units	Can be specified in 1-bit units
Port 13	P130, P131	• Can be set in input or output mode in 1-bit units	—

8.2 Clock Generator

An on-chip clock generator necessary for operation is provided. This clock generator has a frequency divider. If high-speed operation is not necessary, the internal operating frequency can be lowered by the frequency divider to reduce the current consumption.

★ **Figure 8-2. Clock Generator Block Diagram**

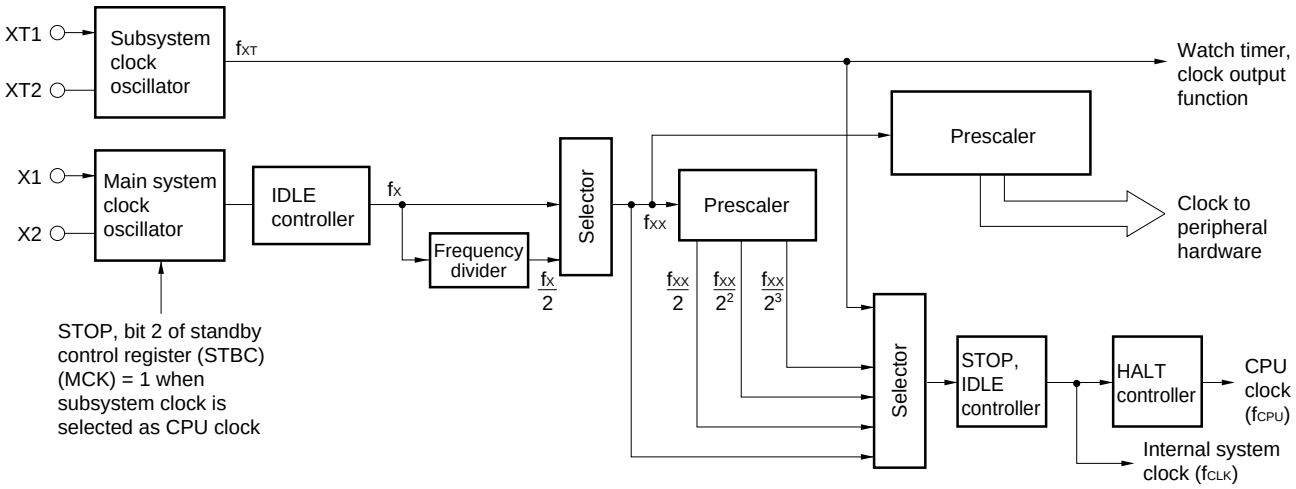
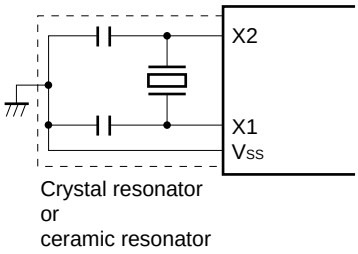


Figure 8-3. Example of Using Main System Clock Oscillator

(1) Crystal/ceramic oscillation



(2) External clock

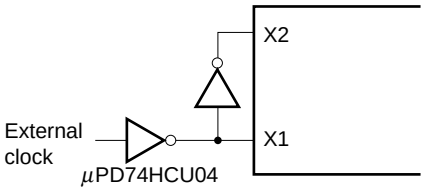
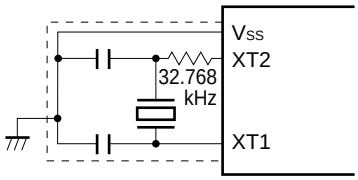
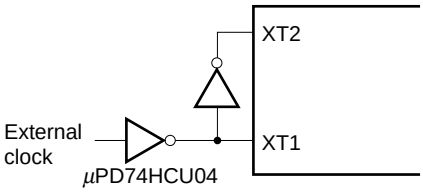


Figure 8-4. Example of Using Subsystem Clock Oscillator

(1) Crystal oscillation



(2) External clock



Caution When using the main system clock and subsystem clock oscillator, wire as following in the area enclosed by the broken lines in Figures 8-3 and 8-4 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}. Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

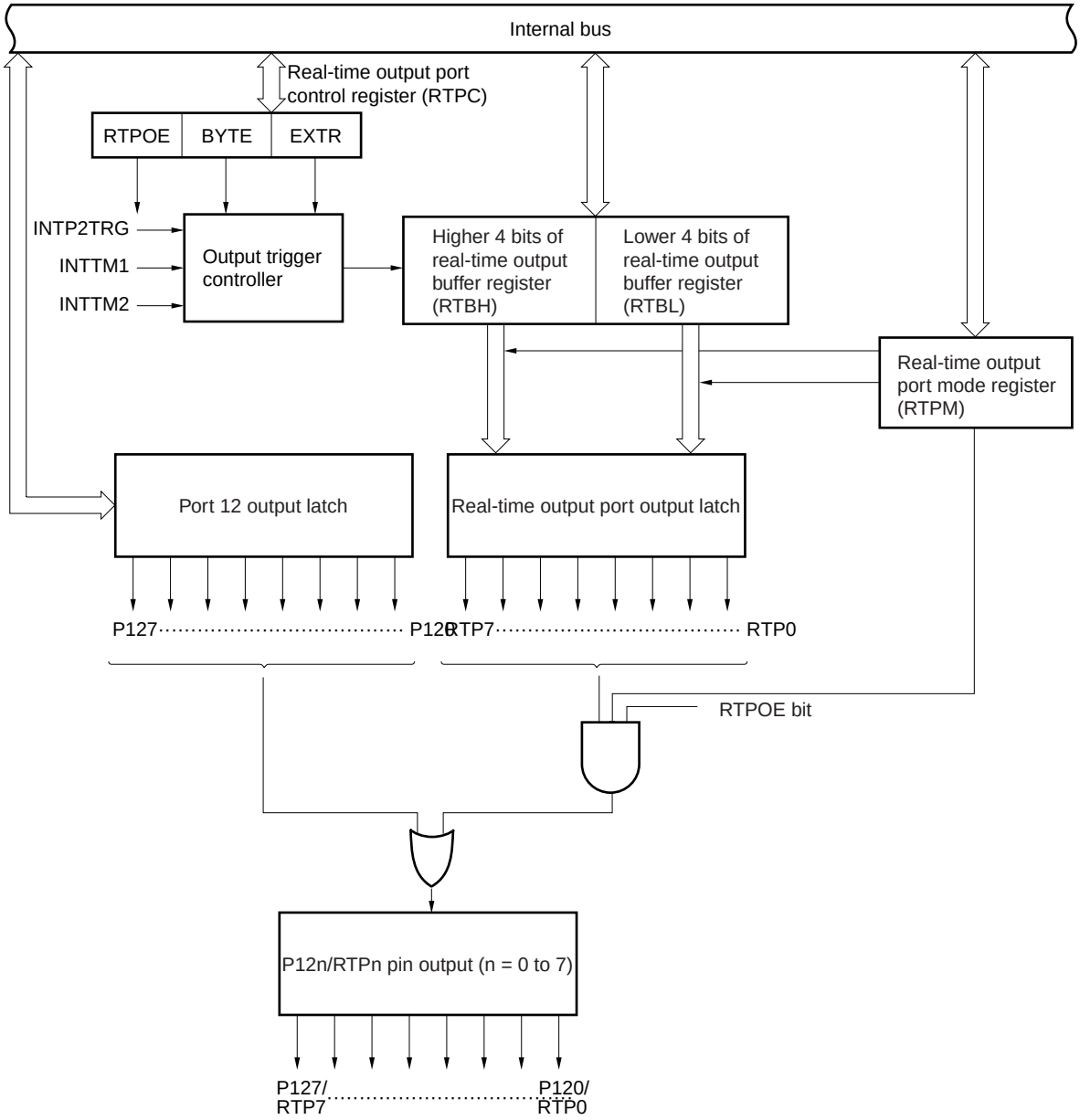
Note that the subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption.

8.3 Real-Time Output Port

The real-time output function is to transfer data preset in the real-time output buffer register to the output latch as soon as the timer interrupt or external interrupt has occurred in order to output the data to an external device. The pins that output the data to the external device constitute a port called a real-time output port.

Because the real-time output port can output signals without jitter, it is ideal for controlling stepper motors, etc.

Figure 8-5. Block Diagram of Real-Time Output Port



8.4 Timer/Event Counter

One unit of 16-bit timer/event counters and six units of 8-bit timer/event counters are provided.

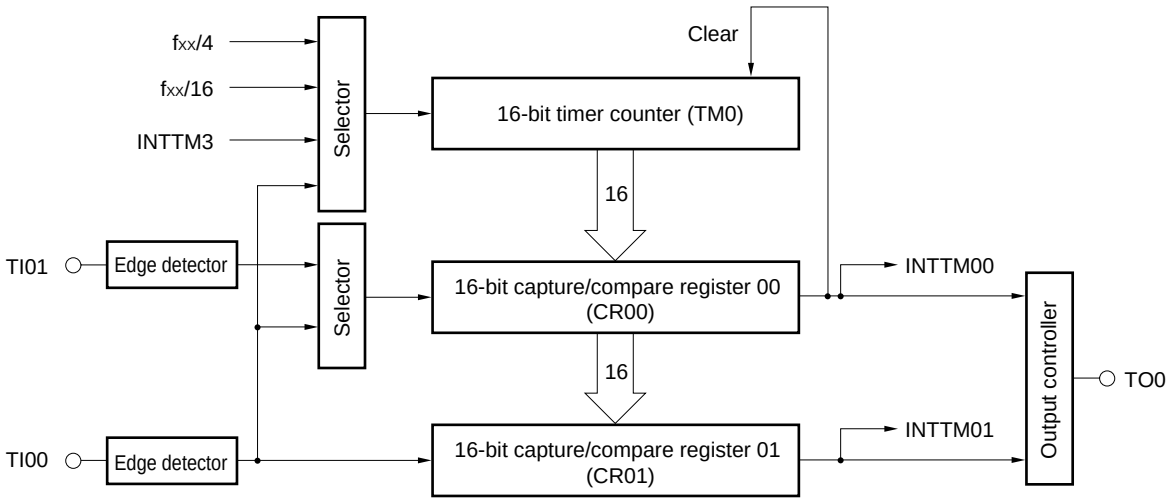
Because a total of eight interrupt requests are supported, these timer/event counters can be used as eight units of timers/counters.

Table 8-2. Operations of Timer/Event Counters

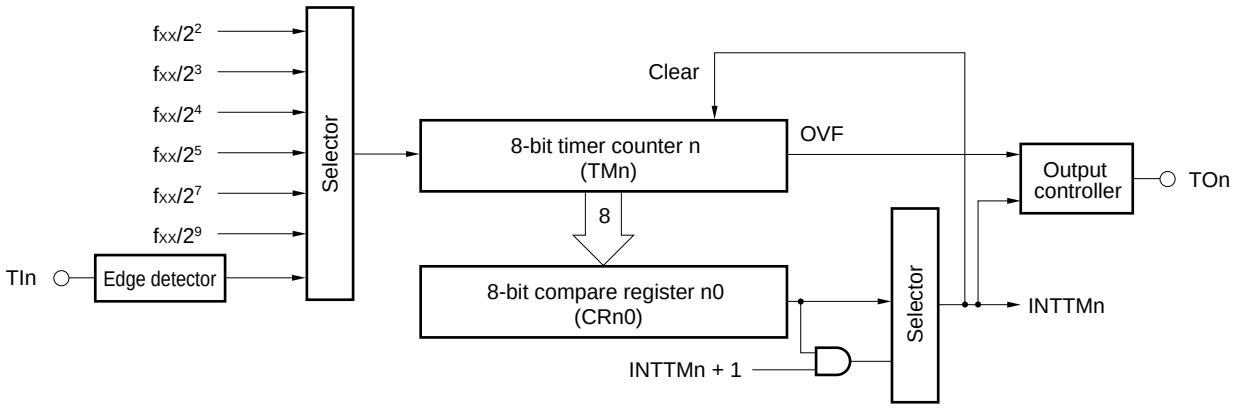
Item \ Name		16-Bit Timer/Event Counter	8-Bit Timer/Event Counter 1	8-Bit Timer/Event Counter 2	8-Bit Timer/Event Counter 5	8-Bit Timer/Event Counter 6	8-Bit Timer/Event Counter 7	8-Bit Timer/Event Counter 8
Count width	8 bits	—	√	√	√	√	√	√
	16 bits	√	√		√		√	
Operation mode	Interval timer	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
	External event counter	√	√	√	√	√	√	√
Function	Timer output	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch	1 ch
	PPG output	√	—	—	—	—	—	—
	PWM output	—	√	√	√	√	√	√
	Square wave output	√	√	√	√	√	√	√
	One-shot pulse output	√	—	—	—	—	—	—
	Pulse width measurement	2 inputs	—	—	—	—	—	—
	Number of interrupt requests	2	1	1	1	1	1	1

Figure 8-6. Block Diagram of Timer/Event Counters

16-bit timer/event counter



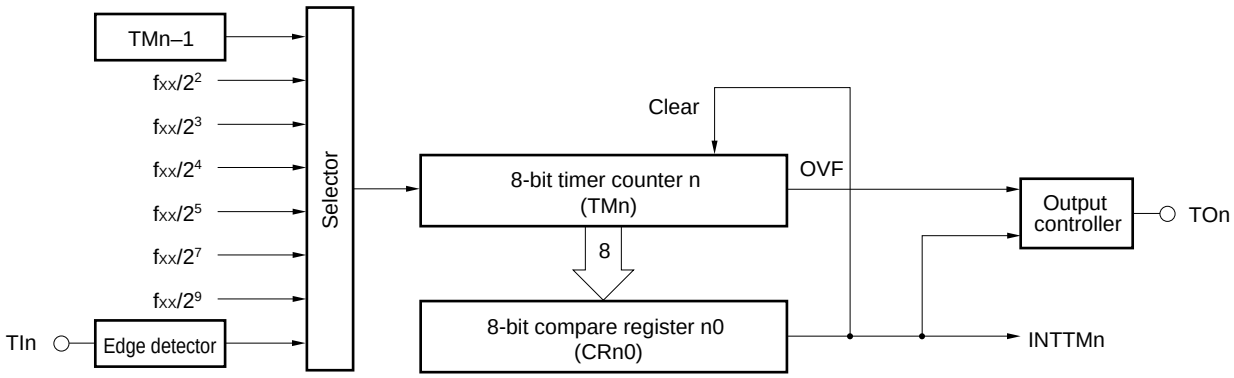
8-bit timer/event counter 1, 5, 7



Remarks 1. n = 1, 5, 7

2. OVF: Overflow flag

8-bit timer/event counter 2, 6, 8



Remarks 1. n = 2, 6, 8

2. OVF: Overflow flag

8.5 A/D Converter

An A/D converter converts an analog input variable into a digital signal. This microcontroller is provided with an A/D converter with a resolution of 8 bits and 8 channels (ANI0 through ANI7).

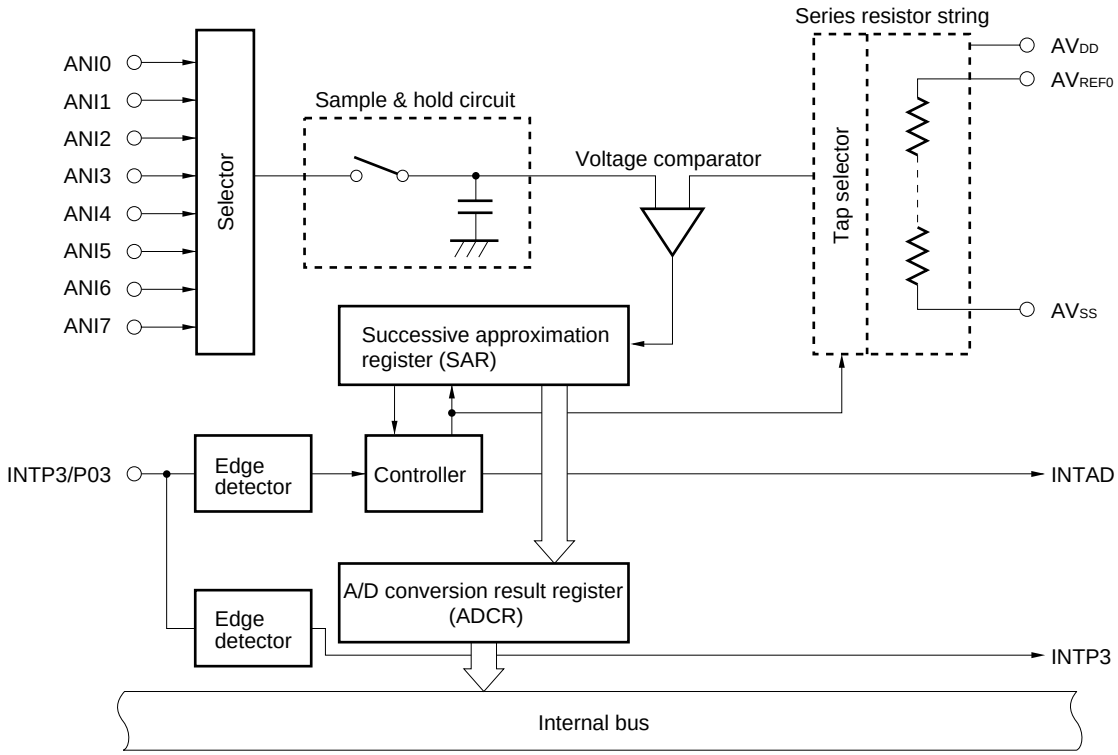
This A/D converter is of successive approximation type and the result of conversion is stored in the 8-bit A/D conversion result register (ADCR).

The A/D converter can be started in the following two ways:

- Hardware start
  Conversion is started by trigger input (P03).
- Software start
  Conversion is started by setting the A/D converter mode register (ADM).

One analog input channel is selected from ANI0 through ANI7 for A/D conversion. When A/D conversion is started by means of hardware start, conversion is stopped after it has been completed. When conversion is started by means of software start, A/D conversion is repeatedly executed, and each time conversion has been completed, an interrupt request (INTAD) is generated.

Figure 8-7. A/D Converter Block Diagram



8.6 D/A Converter

A D/A converter converts an input digital signal into an analog voltage. This microcontroller is provided with a voltage output type D/A converter with a resolution of 8 bits and two channels.

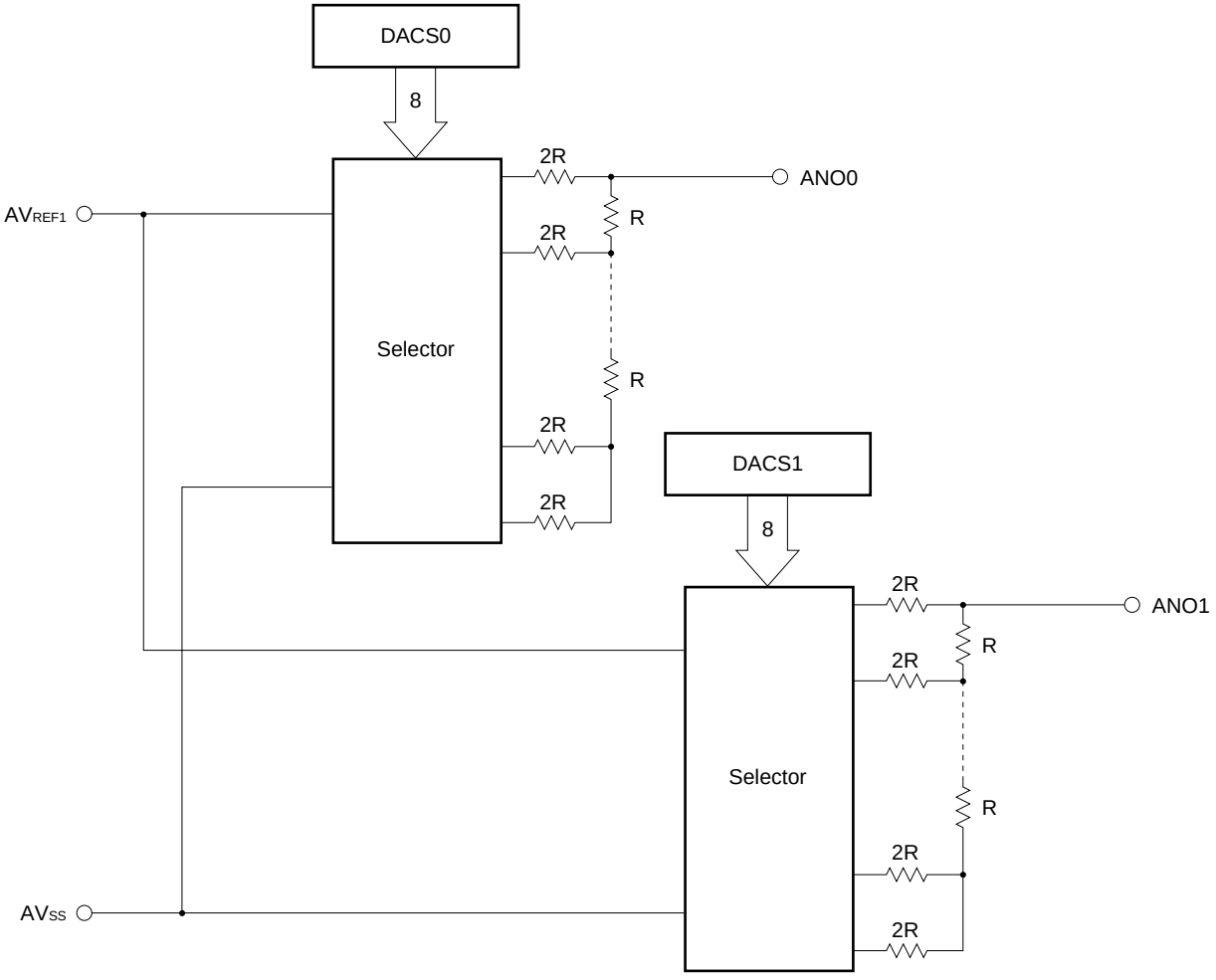
The conversion method is of R-2R resistor ladder type.

D/A conversion is started by setting DACE0 of D/A converter mode register 0 (DAM0) and DACE1 of D/A converter mode register 1 (DAM1).

The D/A converter operates in the following two modes:

- Normal mode
  The converter outputs an analog voltage immediately after it has completed D/A conversion.
- Real-time output mode
  The converter outputs an analog voltage in synchronization with an output trigger after it has completed D/A conversion.

Figure 8-8. D/A Converter Block Diagram



8.7 Serial Interfaces

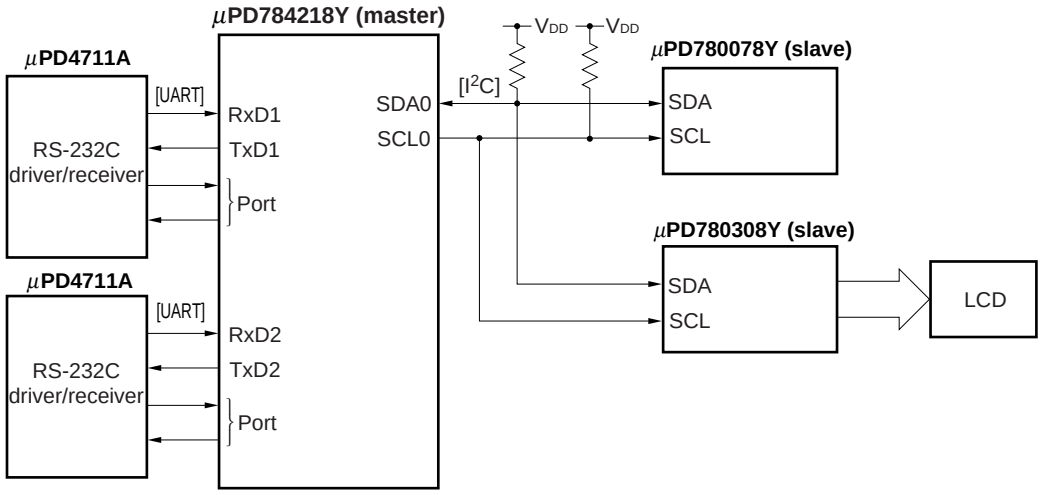
Three independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 1
  - 3-wire serial I/O (IOE)
  - I^2C bus interface (I^2C) (μPD784218Y Subseries only)

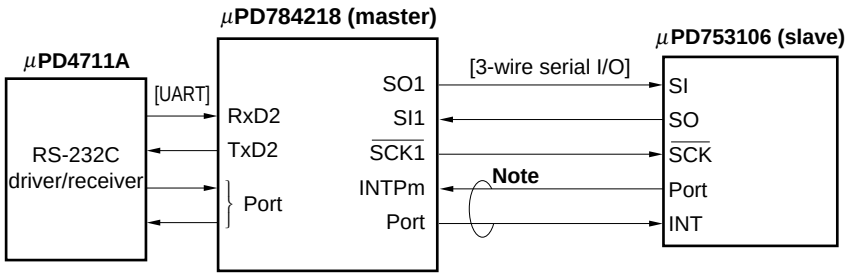
Therefore, communication with an external system and local communication within the system can be simultaneously executed (refer to **Figure 8-9**).

Figure 8-9. Example of Serial Interface

(a) UART + I^2C



(b) UART + 3-wire serial I/O



Note Handshake line

8.7.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two channels of serial interfaces for which an asynchronous serial interface mode and 3-wire serial I/O mode can be selected are provided.

(1) Asynchronous serial interface mode

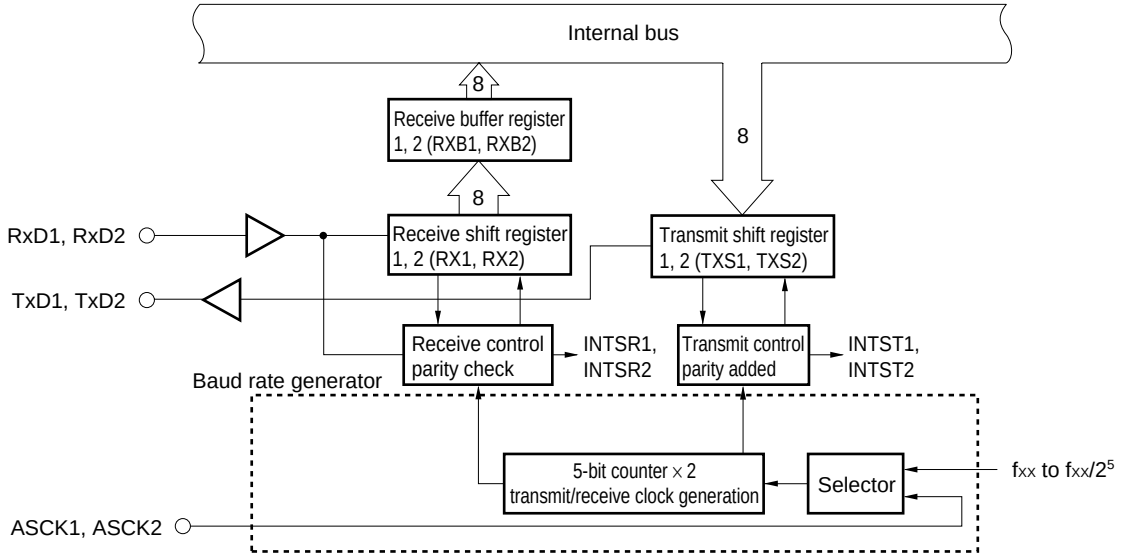
In this mode, data of 1 byte following the start bit is transmitted or received.

Because an on-chip baud rate generator is provided, a wide range of baud rates can be set.

Moreover, the clock input to the ASCK pin can be divided to define a baud rate.

When the baud rate generator is used, a baud rate conforming to the MIDI standard (31.25 kbps) can also be obtained.

★ **Figure 8-10. Block Diagram When in Asynchronous Serial Interface Mode**

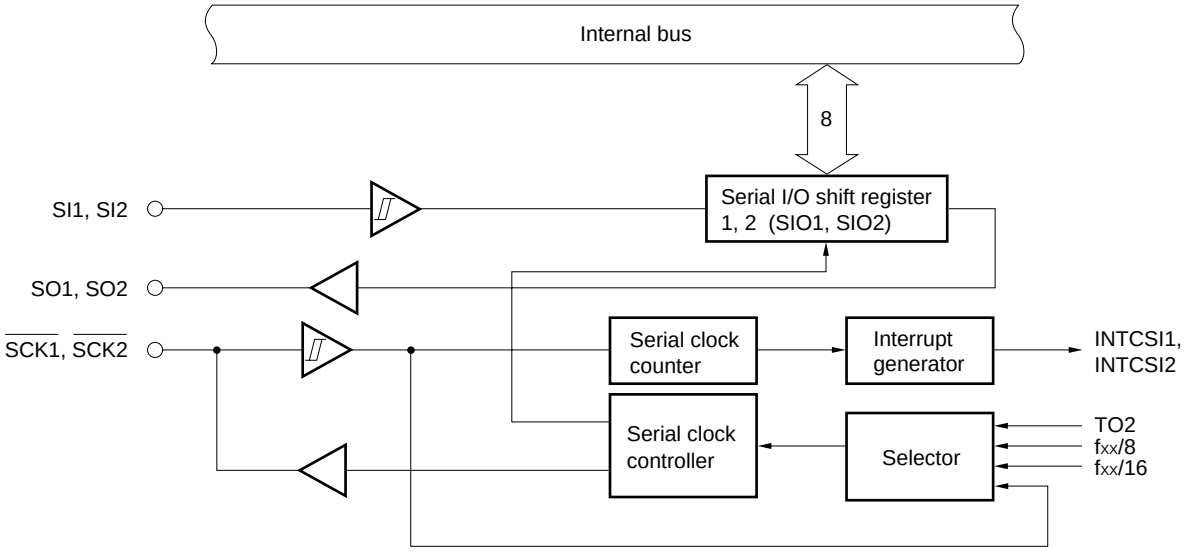


(2) 3-wire serial I/O mode

In this mode, the master device starts transfer by making the serial clock active and transfers 1-byte data in synchronization with this clock.

This mode is used to communicate with a device having the conventional clocked serial interface. Basically, communication is established by using three lines: serial clocks ($\overline{SCK1}$ and $\overline{SCK2}$), serial data inputs (SI1 and SI2), and serial data outputs (SO1 and SO2). To connect two or more devices, a handshake line is necessary.

★ **Figure 8-11. Block Diagram When in 3-Wire Serial I/O Mode**



8.7.2 Clocked serial interface (CSI)

In this mode, the master device starts transfer by making the serial clock active and transfers 1-byte data in synchronization with this clock.

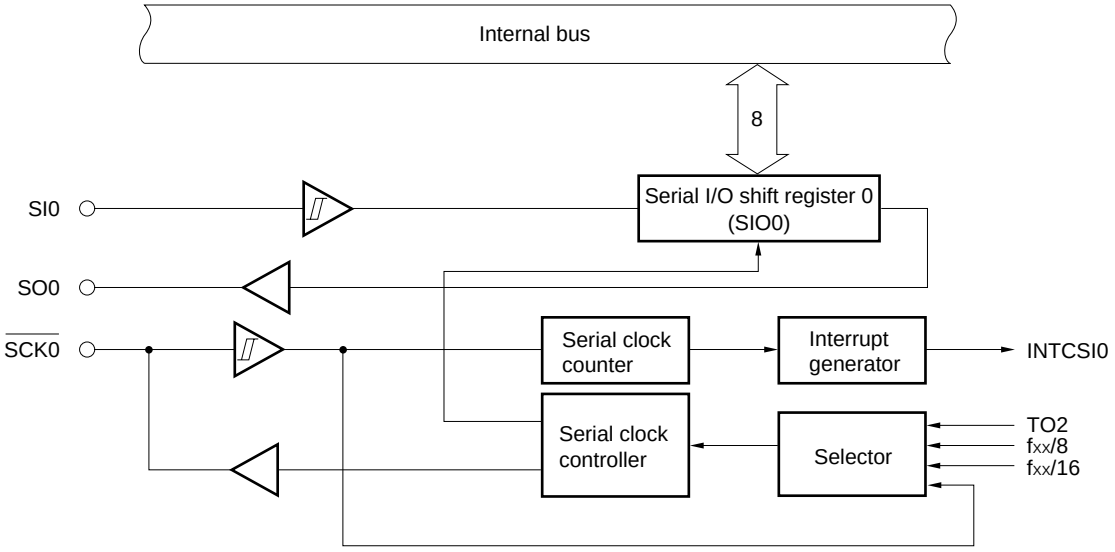
(1) 3-wire serial I/O mode

This mode is to communicate with devices having the conventional clocked serial interface.

Basically, communication is established in this mode with three lines: one serial clock ($\overline{SCK0}$) and two serial data (SI0 and SO0) lines.

Generally, a handshake line is necessary to check the reception status.

★ **Figure 8-12. Block Diagram When in 3-Wire Serial I/O Mode**



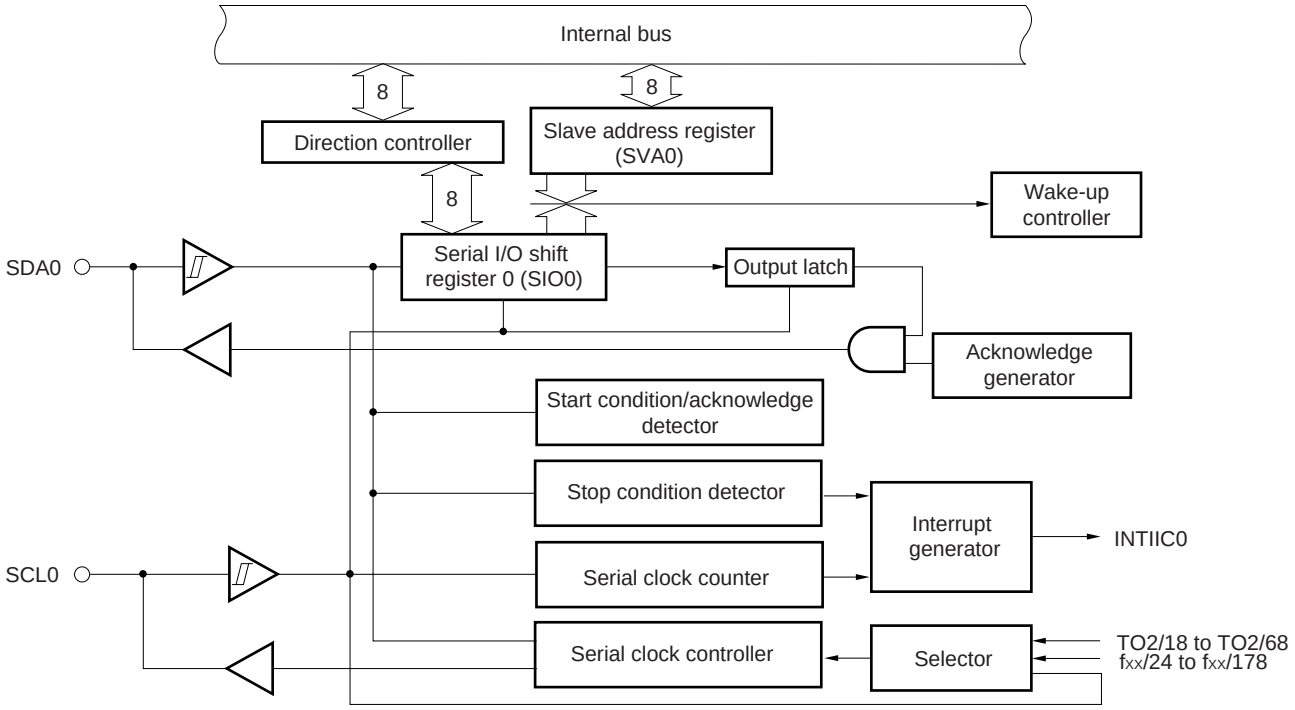
(2) I^2C bus (Inter IC) bus mode (multi-master supporting)

This mode is for communication with devices conforming to the I^2C bus format.

This mode is for transferring 8-bit data between two or more devices by using two lines: a serial clock (SCL0) and a serial data bus (SDA0).

During transfer, a "start condition", "data", and "stop condition" can be output onto the serial data bus. During reception, this data is automatically detected by hardware.

Figure 8-13. Block Diagram of I²C Bus Mode

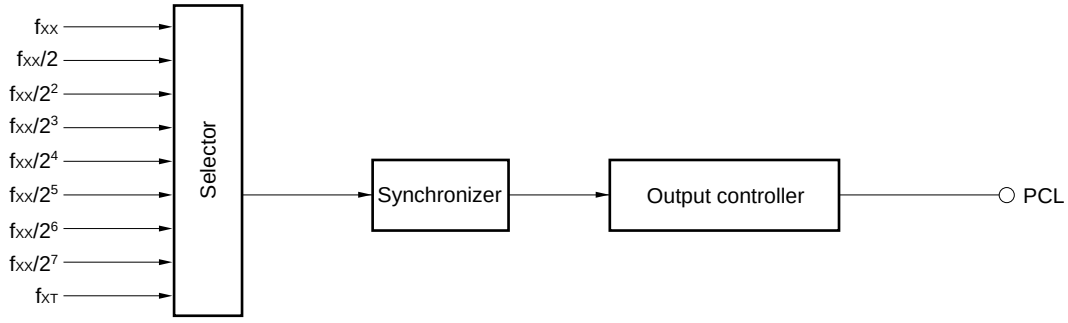


8.8 Clock Output Function

Clocks of the following frequencies can be output as clock output.

- 97.7 kHz/195 kHz/391 kHz/781 kHz/1.56 MHz/3.13 MHz/6.25 MHz/12.5 MHz (@ 12.5 MHz operation with main system clock)
- 32.768 kHz (@ 32.768 kHz operation with subsystem clock)

Figure 8-14. Block Diagram of Clock Output Function

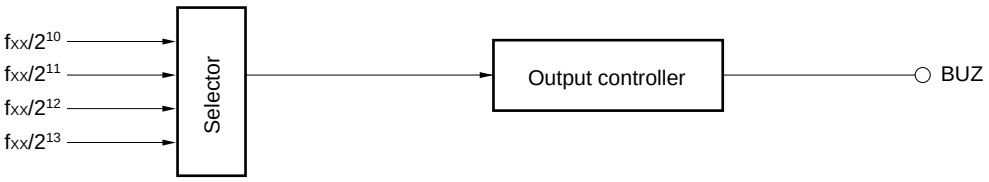


8.9 Buzzer Output Function

Clocks of the following frequencies can be output as buzzer output.

• 1.5 kHz/3.1 kHz/6.1 kHz/12.2 kHz (@ 12.5 MHz operation with main system clock)

Figure 8-15. Block Diagram of Buzzer Output Function



8.10 Edge Detection Function

The interrupt input pins (INTP0, INTP1, NMI/INTP2, INTP3 through INTP6) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at an edge of the input signal, they have a function to detect an edge. Moreover, a noise reduction function is also provided to prevent erroneous detection due to noise.

Pin Name	Detectable Edge	Noise Reduction
NMI	Either or both of rising and falling edges	By analog delay
INTP0 to INTP6		

8.11 Watch Timer

The watch timer has the following functions:

• Watch timer
• Interval timer

The watch timer and interval timer functions can be used at the same time.

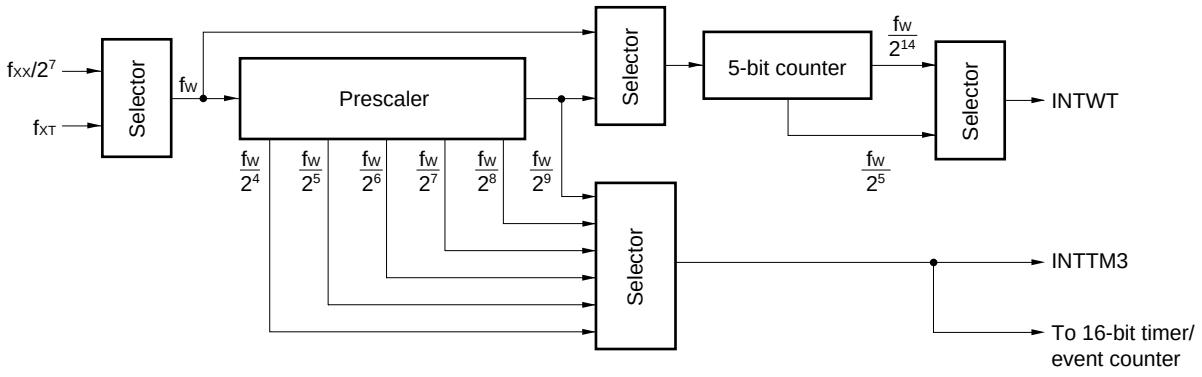
(1) Watch timer

The watch timer sets the WTIF flag of the interrupt control register (WTIC) at time intervals of 0.5 seconds using the 32.768 kHz subsystem clock.

(2) Interval timer

The interval timer generates an interrupt request (INTTM3) at preset time intervals.

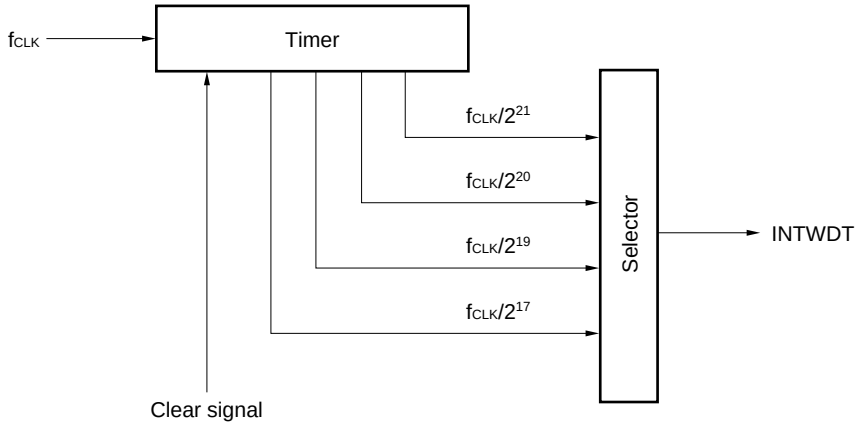
Figure 8-16. Watch Timer Block Diagram



8.12 Watchdog Timer

A watchdog timer is provided to detect a CPU runaway. This watchdog timer generates a non-maskable or maskable interrupt unless it is cleared by software within a specified interval time. Once enabled to operate, the watchdog timer cannot be stopped by software. Whether the interrupt by the watchdog timer or the interrupt input from the NMI pin takes precedence can be specified.

Figure 8-17. Watchdog Timer Block Diagram



Remark f_{CLK}: Internal system clock (f_{XX} to $f_{XX}/8$)

9. INTERRUPT FUNCTION

The three types of servicing in response to an interrupt request shown in Table 9-1 can be selected by program.

Table 9-1. Servicing of Interrupt Request

Servicing Mode	Servicing Means	Servicing	Contents of PC and PSW
Vectored interrupt	Software	Branches and executes servicing routine (servicing is arbitrary)	Saves to and restores from stack
Context switching		Automatically switches register bank, branches and executes servicing routine (servicing is arbitrary)	Saves to or restores from fixed area in register bank
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed)	Retained

9.1 Interrupt Sources

Table 9-2 shows the interrupt sources available. As shown, interrupts are generated by 29 sources, execution of the BRK instruction, BRKCS instruction, or an operand error.

The priority of interrupt servicing can be set to four levels, so that nesting can be controlled during interrupt servicing, and so that which of the two or more interrupts that simultaneously occur should be serviced first can be decided. When the macro service function is used, however, nesting always proceeds (i.e., is not held pending).

The default priority is the priority (fixed) of the service that is performed if two or more interrupt requests, having the same priority, are simultaneously generated (refer to **Table 9-2**).

Table 9-2. Interrupt Sources (1/2)

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Instruction execution	—	—
		BRKCS instruction	Instruction execution		
		Operand error	If result of exclusive OR between operands byte and $\overline{\text{byte}}$ is not FFH when MOV STBC, #byte instruction, MOV WDM, #byte instruction, or LOCATION instruction is executed		
Non-maskable	—	NMI	Pin input edge detection	External	—
		INTWDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTWDTM	Overflow of watchdog timer	Internal	√
	1	INTP0	Pin input edge detection	External	
	2	INTP1			
	3	INTP2			
	4	INTP3			
	5	INTP4			
	6	INTP5			
	7	INTP6			
	8	INTIIC0	End of I^2C bus transfer by CSI0	Internal	
		INTCSI0	End of 3-wire transfer by CSI0		
	9	INTSER1	Occurrence of UART reception error in ASI1		

Table 9-2. Interrupt Sources (2/2)

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Maskable	10	INTSR1	End of UART reception by ASI1	Internal	√
		INTCSI1	End of 3-wire transfer by CSI1		
	11	INTST1	End of UART transmission by ASI1		
	12	INTSER2	Occurrence of UART reception error in ASI2		
	13	INTSR2	End of UART reception by ASI2		
		INTCSI2	End of 3-wire transfer by CSI2		
	14	INTST2	End of UART transmission by ASI2		
	15	INTTM3	Reference time interval signal from watch timer		
	16	INTTM00	Signal indicating coincidence between 16-bit timer counter and capture/compare register (CR00)		
	17	INTTM01	Signal indicating coincidence between 16-bit timer counter and capture/compare register (CR01)		
	18	INTTM1	Occurrence of coincidence signal of 8-bit timer/event counter 1		
	19	INTTM2	Occurrence of coincidence signal of 8-bit timer/event counter 2		
	20	INTAD	End of conversion by A/D converter		
	21	INTTM5	Occurrence of coincidence signal of 8-bit timer/event counter 5		
	22	INTTM6	Occurrence of coincidence signal of 8-bit timer/event counter 6		
	23	INTTM7	Occurrence of coincidence signal of 8-bit timer/event counter 7		
	24	INTTM8	Occurrence of coincidence signal of 8-bit timer/event counter 8		
	25	INTWT	Overflow of watch timer		
	26 (lowest)	INTKR	Detection of falling edge of port 8	External	

Remarks 1. ASI: Asynchronous Serial Interface
CSI: Clocked Serial Interface

★ **2.** Two watchdog timer interrupt sources, non-maskable interrupt (INTWDT) and maskable interrupt (INTWDTM), are available and only one of those can be selected.

9.2 Vectored Interrupt

Execution branches to a servicing routine by using the memory contents of a vector table address corresponding to the interrupt source as the address of the branch destination.

So that the CPU performs interrupt servicing, the following operations are performed:

- On branching: Saves the status of the CPU (contents of PC and PSW) to stack
- On returning: Restores the status of the CPU (contents of PC and PSW) from stack

To return to the main routine from an interrupt service routine, the RETI instruction is used.

The branch destination address is in a range of 0 to FFFFH.

Table 9-3. Vector Table Address

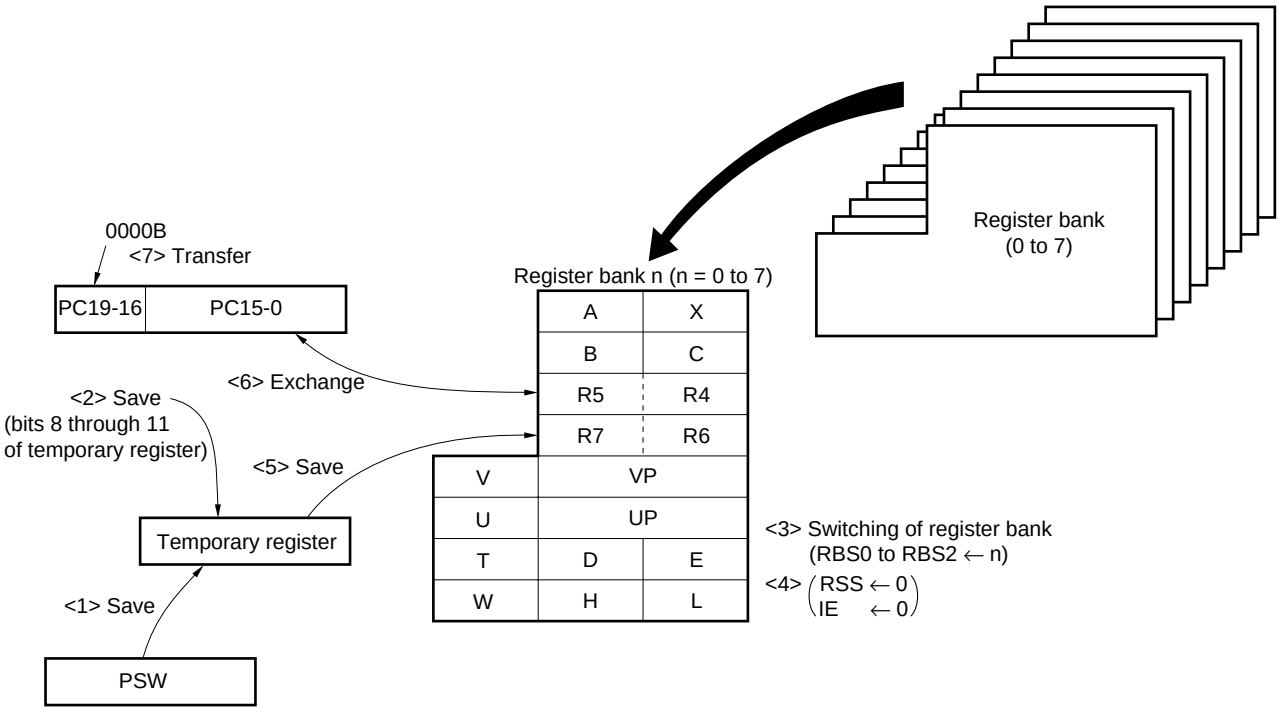
Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK instruction	003EH	INTST1	001CH
TRAP0 (operand error)	003CH	INTSER2	001EH
NMI	0002H	INSR2	0020H
INTWDT (non-maskable)	0004H	INTCSI2	
INTWDTM (maskable)	0006H	INTST2	0022H
INTP0	0008H	INTTM3	0024H
INTP1	000AH	INTTM00	0026H
INTP2	000CH	INTTM01	0028H
INTP3	000EH	INTTM1	002AH
INTP4	0010H	INTTM2	002CH
INTP5	0012H	INTAD	002EH
INTP6	0014H	INTTM5	0030H
INTIIC0	0016H	INTTM6	0032H
INTCSI0		INTTM7	0034H
INTSER0	0018H	INTTM8	0036H
INTSR1	001AH	INTWT	0038H
INTCSI1		INTKR	003AH

9.3 Context Switching

When an interrupt request is generated or when the BRKCS instruction is executed, a predetermined register bank is selected by hardware. Context switching is a function that branches execution to a vector address stored in advance in the register bank, and stacks the current contents of the program counter (PC) and program status word (PSW) to the register bank.

The branch address is in a range of 0 to FFFFH.

Figure 9-1. Context Switching Operation When Interrupt Request Is Generated

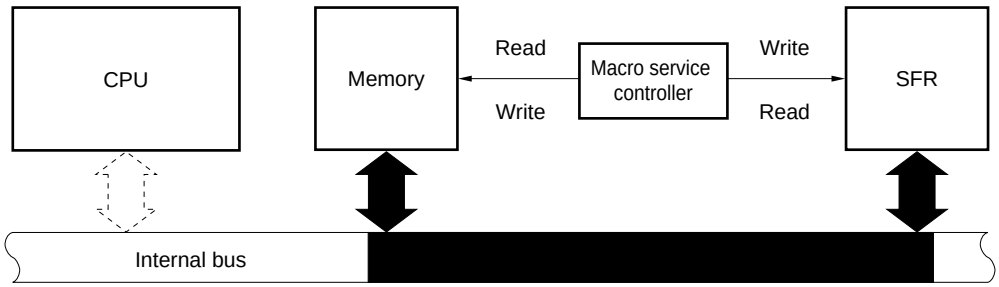


9.4 Macro Service

This function is to transfer data between memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR in the same transfer cycle and directly transfers data without loading it.

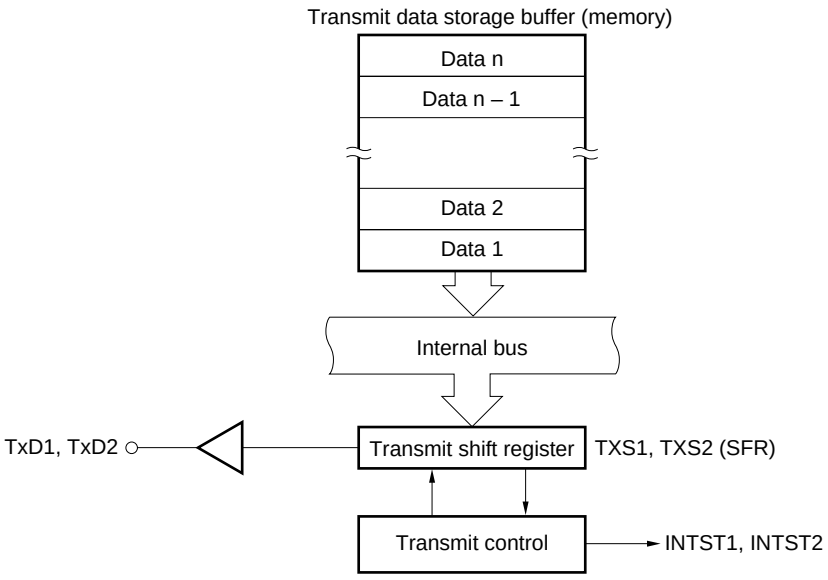
Because this function does not save or restore the status of the CPU, or load data, data can be transferred at high speeds.

Figure 9-2. Macro Service



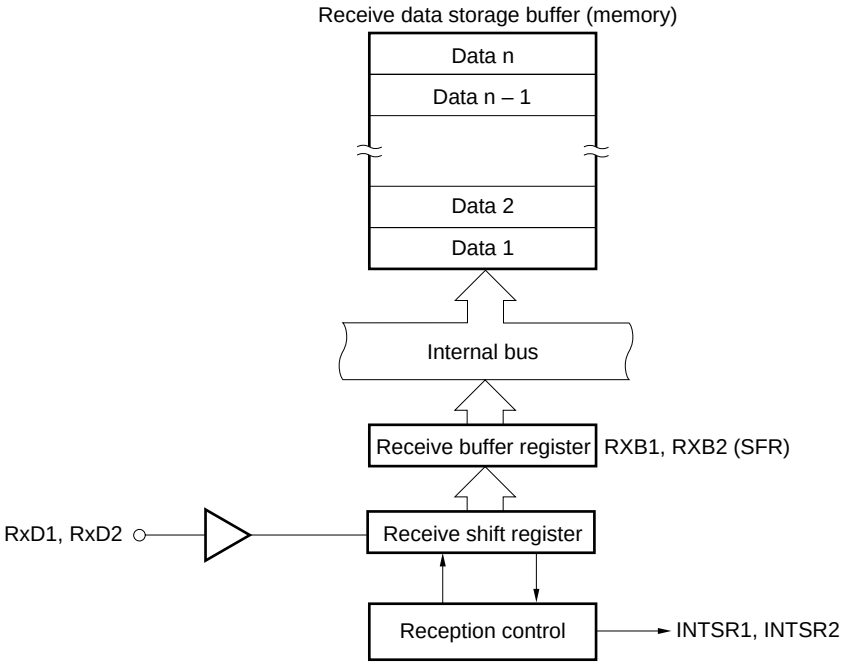
9.5 Application Example of Macro Service

(1) Serial interface transmission



Each time macro service requests INTST1 and INTST2 are generated, the next transmit data is transferred from memory to TXS1 and TXS2. When data n (last byte) has been transferred to TXS1 and TXS2 (when the transmit data storage buffer has become empty), vectored interrupt requests INTST1 and INTST2 are generated.

(2) Serial interface reception



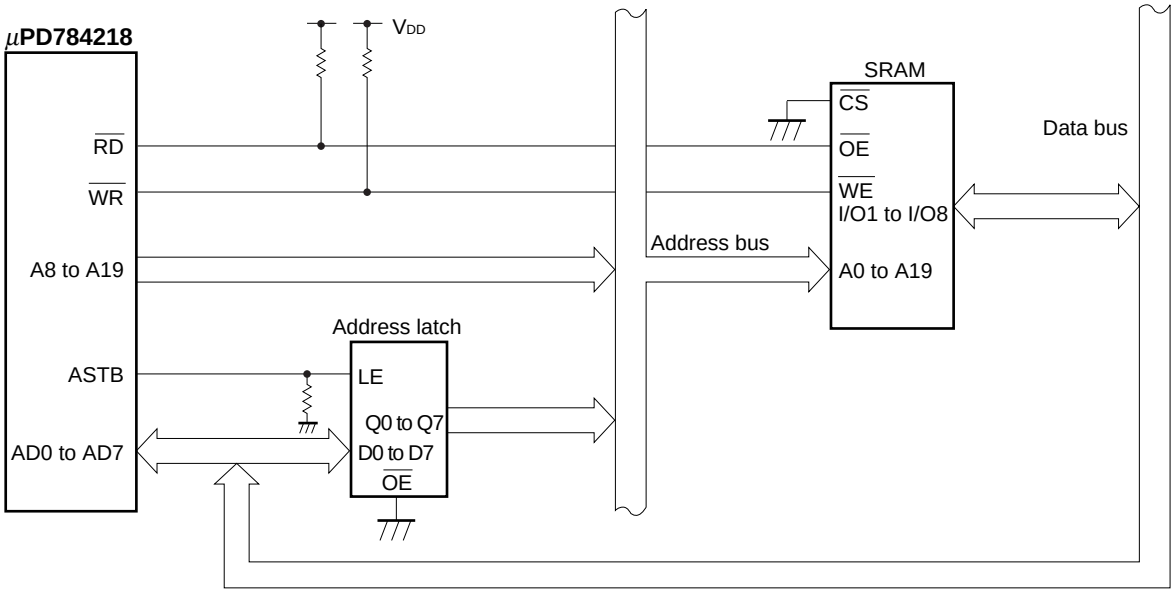
Each time macro service requests INTSR1 and INTSR2 are generated, the receive data is transferred from RXB1 and RXB2 to memory. When data n (last byte) has been transferred to memory (when the receive data storage buffer has become full), vectored interrupt requests INTSR1 and INTSR2 are generated.

10. LOCAL BUS INTERFACE

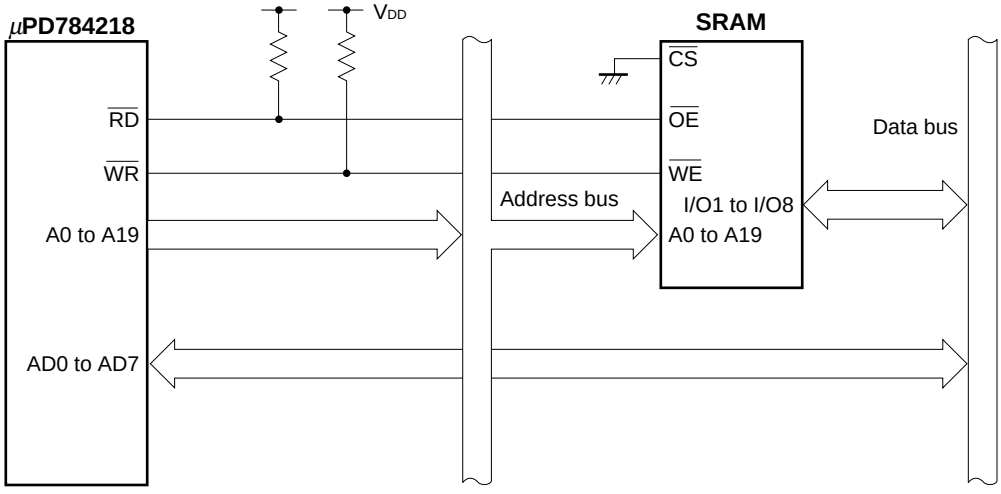
The local bus interface can connect an external memory or I/O (memory mapped I/O) and support a memory space of 1 MB (refer to **Figure 10-1**).

Figure 10-1. Example of Local Bus Interface

(a) Multiplexed bus mode



(b) Separate bus mode



10.1 Memory Expansion

External program memory and data memory can be connected in two stages: 256 KB and 1 MB.

To connect the external memory, ports 4 through 6 and port 8 are used.

The external memory can be connected in the following two modes:

- Multiplexed bus mode: The external memory is connected by using a time-division address/data bus. The number of ports used when the external memory is connected can be reduced in this mode.
- Separate bus mode: The external memory is connected by using an address bus and data bus independent of each other. Because an external latch circuit is not necessary, this mode is useful for reducing the number of components and mounting area on the printed wiring board.

10.2 Programmable Wait

Wait state(s) can be inserted to the memory space (00000H through FFFFFH) while the $\overline{RD}$ and $\overline{WR}$ signals are active.

In addition, there is an address wait function that extends the active period of the ASTB signal to gain the address decode time.

10.3 External Access Status Function

An active-low external access status signal is output from the P37/EXA pin. This signal informs other devices that are connected with external buses of the external access status, prohibits other devices from outputting data to an external bus, and enables receive operations.

The external access status signal is output during external accessing.

11. STANDBY FUNCTION

This function is to reduce the power consumption of the chip, and can be used in the following modes:

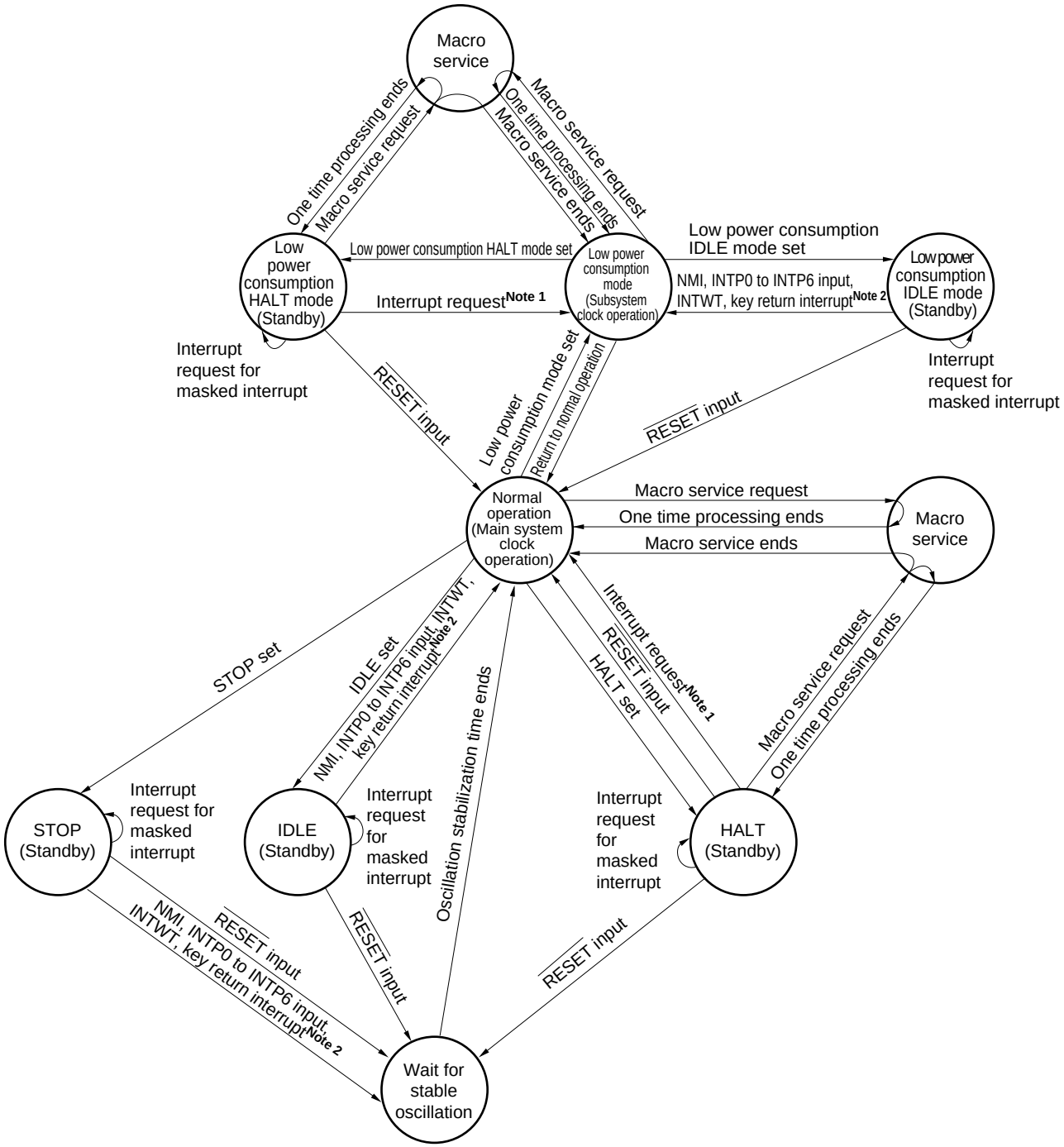
- HALT mode: Stops supply of the operating clock to the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power consumption.
- IDLE mode: Stops the entire system with the oscillator continuing operation. The power consumption in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode: Stops the main system clock and thereby stops all the internal operations of the chip. Consequently, the power consumption is minimized with only leakage current flowing.
- Low power consumption mode: The main system clock is stopped with the subsystem clock used as the system clock. The CPU can operate on the subsystem clock to reduce the current consumption.
- Low power consumption HALT mode: This is a standby function in the low power consumption mode and stops the operation clock of the CPU, to reduce the power consumption of the entire system.
- Low power consumption IDLE mode: This is a standby function in the low power consumption mode and stops the entire system except the oscillator, to reduce the power consumption of the entire system.

These modes are programmable.

The macro service can be started from the HALT mode or low power consumption HALT mode. After macro service processing is executed, the system returns to the HALT mode again.

The transition of the standby status is shown in Figure 11-1.

★ **Figure 11-1. Standby Function State Transition**



Notes 1. Only unmasked interrupt requests

2. Only unmasked INTP0 to INTP6, INTWT, key return interrupt (P80 to P87)

Remark NMI is valid only for an external input.

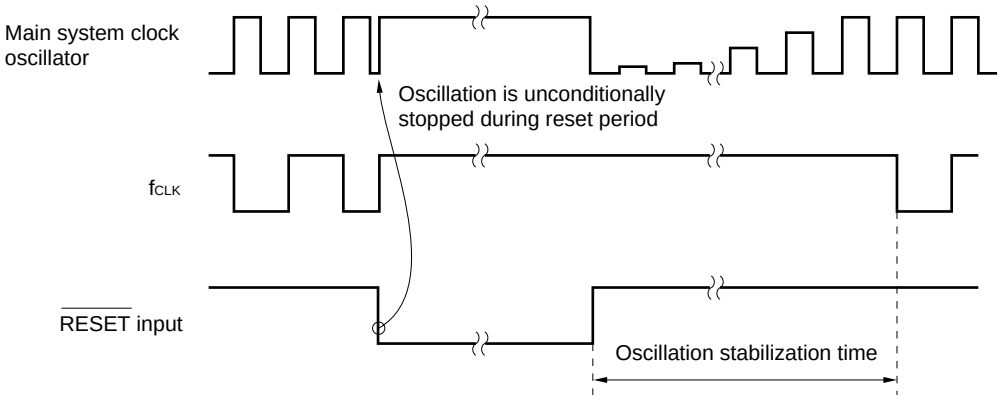
The watchdog timer cannot be used for the release of standby (HALT mode/STOP mode/IDLE mode).

12. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized (reset). During the reset period, oscillation of the main system clock is unconditionally stopped. Consequently, the current consumption of the entire system can be reduced.

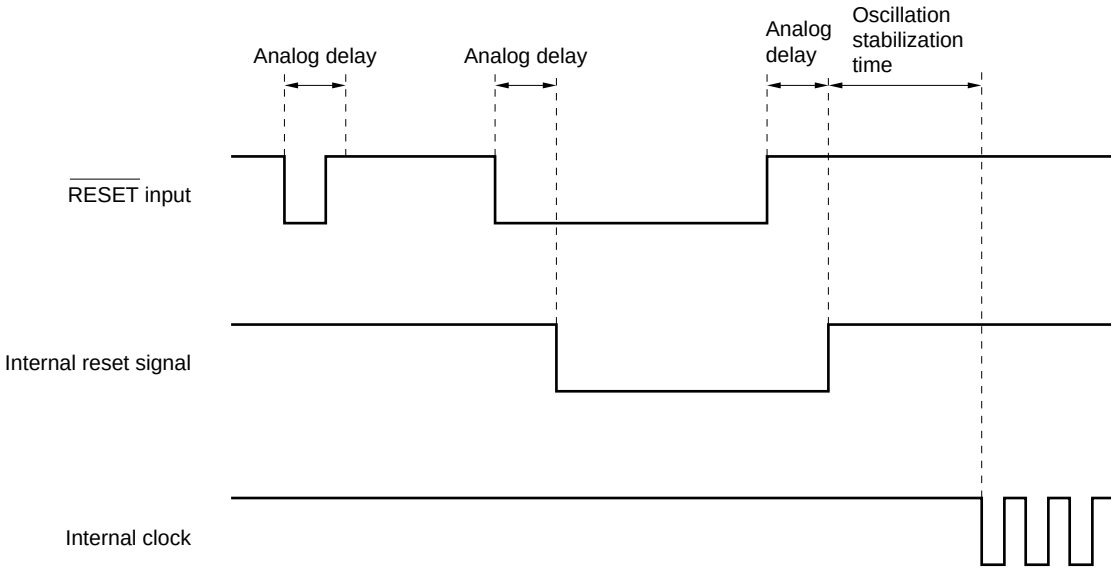
When the $\overline{\text{RESET}}$ signal goes high, the reset status is cleared, the oscillation stabilization time (84.0 ms at 12.5 MHz operation) elapses, the contents of the reset vector table are set to the program counter (PC), execution branches to an address set to the PC, and program execution is started from that branch address. Therefore, the program can be reset and started from any address.

Figure 12-1. Oscillation of Main System Clock During Reset Period



The $\overline{\text{RESET}}$ input pin has an analog delay noise eliminator to prevent malfunctioning due to noise.

Figure 12-2. Acknowledgement of Reset Signal



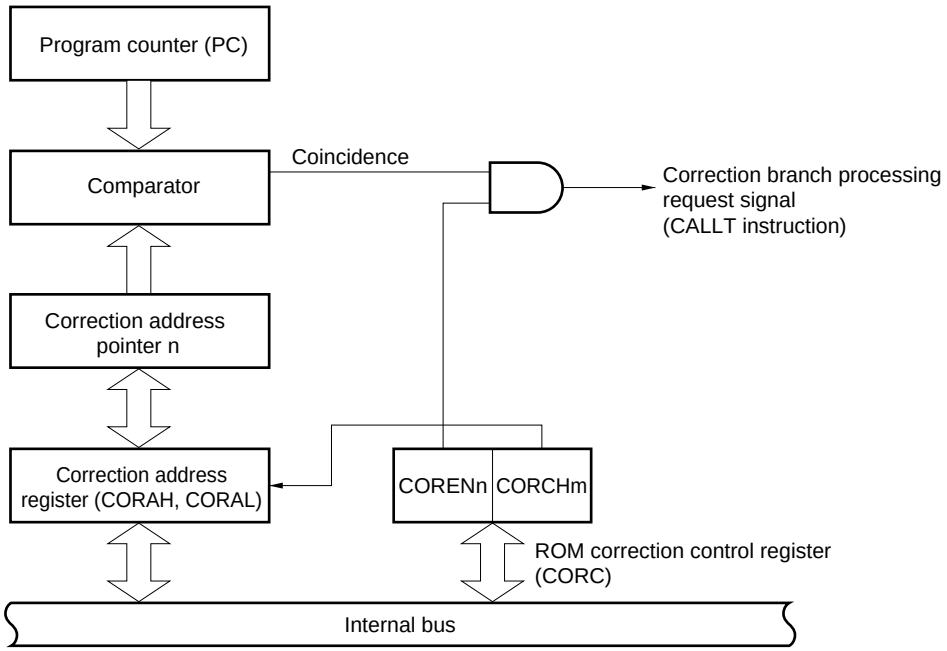
13. ROM CORRECTION

ROM correction is a function for avoiding execution of a part of a program in the internal ROM that needs to be corrected by executing the corrected program, which is stored in the internal RAM.

By using this function, instruction bugs found in the internal ROM can be avoided and the program flow can be changed.

Up to four combinations between source internal ROM (program) and target RAM sections are available for the ROM correction.

Figure 13-1. ROM Correction Block Diagram



Remark n = 0 to 3, m = 0, 1

14. INSTRUCTION SET

(1) 8-bit instructions (The instructions in parentheses are combinations realized by describing A as r)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC

Table 14-1. Instruction List by 8-Bit Addressing

First Operand \ Second Operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Notes 1,6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes 1. The operands of ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as those of ADD.

2. Either the second operand is not used, or the second operand is not an operand address.

3. The operands of ROL, RORC, ROLC, SHR, and SHL are the same as those of ROR.

4. The operands of XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC are the same as those of MOVM.

5. The operands of XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC are the same as those of MOVBK.

6. The code length of some instructions having saddr2 as saddr in this combination is short.

(2) 16-bit instructions (The instructions in parentheses are combinations realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 14-2. Instruction List by 16-Bit Addressing

First Operand \ Second Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Notes 1, 3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. The operands of SUBW and CMPW are the same as those of ADDW.

2. Either the second operand is not used, or the second operand is not an operand address.

3. The code length of some instructions having saddrp2 as saddrp in this combination is short.

4. The operands of MULUW and DIVUX are the same as those of MULW.

(3) 24-bit instructions (The instructions in parentheses are combinations realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 14-3. Instruction List by 24-Bit Addressing

First Operand \ Second Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 14-4. Instruction List by Bit Manipulation Instruction Addressing

First Operand \ Second Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr. bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used, or the second operand is not an operand address.

(5) Call and return/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 14-5. Instruction List by Call and Return/Branch Instruction Addressing

Operand of Instruction Address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note The operands of BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as those of BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

15. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

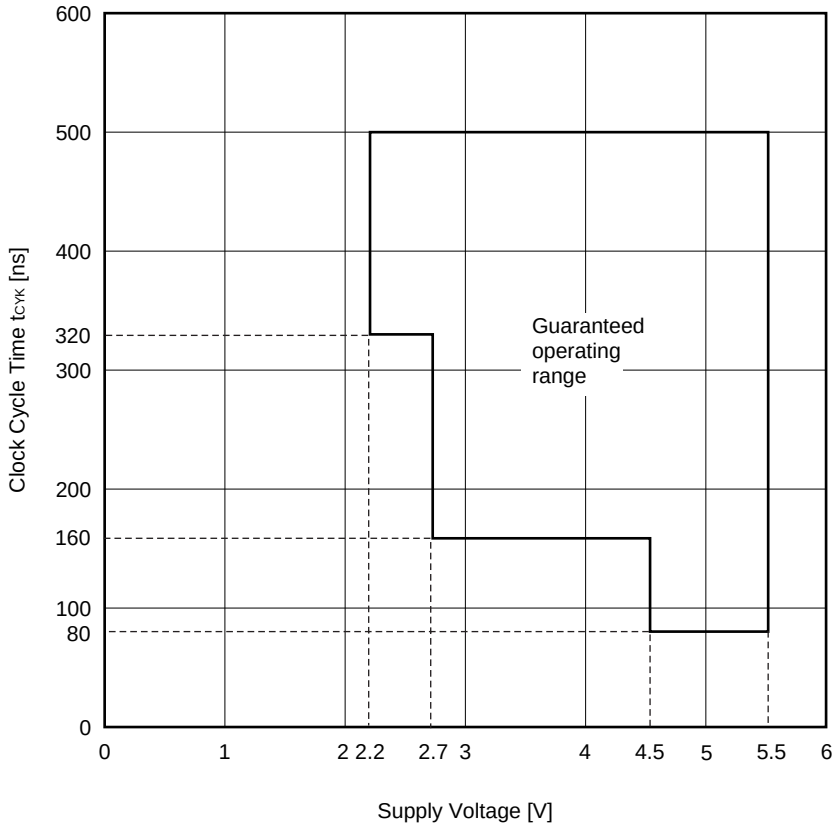
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to V_{SS} + 0.3	V
	AV_{REF0}	A/D converter reference voltage input		–0.3 to V_{DD} + 0.3	V
	AV_{REF1}	D/A converter reference voltage input		–0.3 to V_{DD} + 0.3	V
Input voltage	V_{I1}	Other than P90 to P95		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P90 to P95	N-ch open drain	–0.3 to +12	V
Analog input voltage	V_{AN}	Analog input pin		AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin		15	mA
		Total of P2, P4 to P8		75	mA
		Total of P0, P3, P9, P10, P12, P13		75	mA
Output current, high	I_{OH}	Per pin		–10	mA
		Total of P2, P4 to P8		–50	mA
		Total of P0, P3, P9, P10, P12, P13		–50	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Operating Conditions

- Operating ambient temperature (T_A): –40 to +85°C
- Power supply voltage and clock cycle time: see **Figure 15-1**

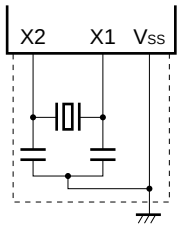
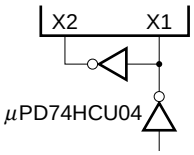
Figure 15-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.	Other than Port 9			15	pF
			Port 9			20	pF
Output capacitance	C_O		Other than Port 9			15	pF
			Port 9			20	pF
I/O capacitance	C_{IO}		Other than Port 9			15	pF
			Port 9			20	pF

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
			2.2 V ≤ V_{DD} < 2.7 V	2		3	
External clock		X1 input frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		25	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		12.5	
			2.2 V ≤ V_{DD} < 2.7 V	2		6.25	
		X1 input high-/low-level width (t_{WXH}, t_{WXL})		15		250	ns
		X1 input rise/fall time (t_{XR}, t_{XF})	4.5 V ≤ V_{DD} ≤ 5.5 V	0		5	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		10	
			2.2 V ≤ V_{DD} < 2.7 V	0		20	

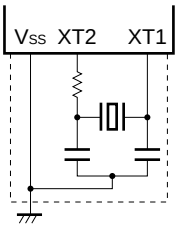
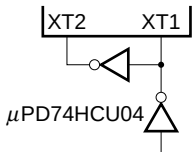
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

★ **Remark** For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			2.2 V ≤ V_{DD} < 4.5 V			10	
External clock		XT1 input frequency (f_{XT})		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Note Time required to stabilize oscillation after the power supply voltage (V_{DD}) is applied.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

★ **Remark** For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	**Note 1**		0		0.3V_{DD}	V
	V_{IL2}	Total for P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P90 to P95 (N-ch open drain)		0		0.3V_{DD}	V
	V_{IL4}	Total for P10 to P17, P130, P131		0		0.3V_{DD}	V
	V_{IL5}	Total for X1, X2, XT1, XT2		0		0.2V_{DD}	V
	V_{IL6}	P25, P27		0		0.3V_{DD}	V
Input voltage, high	V_{IH1}	**Note 1**		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Total for P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P90 to P95 (N-ch open drain)		0.7V_{DD}		12	V
	V_{IH4}	Total for P10 to P17, P130, P131		0.7V_{DD}		V_{DD}	V
	V_{IH5}	Total for X1, X2, XT1, XT2		0.8V_{DD}		V_{DD}	V
	V_{IH6}	P25, P27		0.7V_{DD}		V_{DD}	V
Output voltage, low	V_{OL1}	For pins other than P40 to P47, P50 to P57, P90 to P95 I_{OL} = 1.6 mA**Note 2**	V_{DD} = 4.5 to 5.5 V			0.4	V
		Total for P40 to P47, P50 to P57 I_{OL} = 8 mA**Note 2**	V_{DD} = 4.5 to 5.5 V			1.0	V
★		P90 to P95 I_{OL} = 15 mA**Note 2**	V_{DD} = 4.5 to 5.5 V		0.8	2.0	V
	V_{OL2}	I_{OL} = 400 μA**Note 2**				0.5	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA**Note 2**	V_{DD} = 4.5 to 5.5 V	V_{DD} – 1.0			V
		I_{OL} = –100 μA**Note 2**		V_{DD} – 0.5			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Except X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–3	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				3	μA

Notes 1. P21, P23, P24, P26, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P71, P80 to P87, P120 to P127

2. Per pin

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	Operation mode	f_{XX} = 12.5 MHz		20	40	mA
			f_{XX} = 6 MHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		8	17	mA
			f_{XX} = 3 MHz, 2.2 V ≤ V_{DD} < 2.7 V		4	8	mA
	I_{DD2}	HALT mode	f_{XX} = 12.5 MHz		8	20	mA
			f_{XX} = 6 MHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		3	8	mA
			f_{XX} = 3 MHz, 2.2 V ≤ V_{DD} < 2.7 V		1.3	3.5	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.5 MHz		1	2.5	mA
			f_{XX} = 6 MHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		0.5	1.3	mA
			f_{XX} = 3 MHz, 2.2 V ≤ V_{DD} < 2.7 V		0.3	0.9	mA
	I_{DD4}	Operation mode**Note**	f_{XX} = 32 kHz		100	200	μA
			f_{XX} = 32 kHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		55	110	μA
			f_{XX} = 32 kHz, 2.2 V ≤ V_{DD} < 2.7 V		50	100	μA
	I_{DD5}	HALT mode**Note**	f_{XX} = 32 kHz		80	160	μA
			f_{XX} = 32 kHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		40	80	μA
			f_{XX} = 32 kHz, 2.2 V ≤ V_{DD} < 2.7 V		35	70	μA
	I_{DD6}	IDLE mode**Note**	f_{XX} = 32 kHz		75	150	μA
			f_{XX} = 32 kHz, 2.7 V ≤ V_{DD} ≤ 3.3 V		35	70	μA
			f_{XX} = 32 kHz, 2.2 V ≤ V_{DD} < 2.7 V		30	60	μA
Data retention voltage	V_{DDDR}	HALT, IDLE modes		2.2		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DD} = 2.2 V		2	10	μA
			V_{DD} = 4.5 to 5.5 V		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Note When main system clock is stopped

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYK}	4.5 V ≤ V_{DD} ≤ 5.5 V	80			ns
		2.7 V ≤ V_{DD} < 4.5 V	160			ns
		2.2 V ≤ V_{DD} < 2.7 V	320			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5 + a) T – 11			ns
		V_{DD} = 3.0 V	(0.5 + a) T – 15			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T – 19			ns
		V_{DD} = 3.0 V	0.5T – 24			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5 + a) T – 17			ns
		V_{DD} = 3.0 V	(0.5 + a) T – 40			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T – 14			ns
		V_{DD} = 3.0 V	0.5T – 14			ns
Delay time from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V	(1 + a) T – 24			ns
		V_{DD} = 3.0 V	(1 + a) T – 24			ns
Address float time (from $\overline{RD}$↓)	t_{FRA}		0			ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V			(2.5 + a + n) T – 37	ns
		V_{DD} = 3.0 V			(2.5 + a + n) T – 52	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V			(2 + n) T – 35	ns
		V_{DD} = 3.0 V			(2 + n) T – 50	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V			(1.5 + n) T – 40	ns
		V_{DD} = 3.0 V			(1.5 + n) T – 50	ns
Delay time from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T – 9			ns
		V_{DD} = 3.0 V	0.5T – 9			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V	0.5T – 2			ns
		V_{DD} = 3.0 V	0.5T – 12			ns
Delay time from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V	0.5T – 9			ns
		V_{DD} = 3.0 V	0.5T – 9			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5 + n) T – 25			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 30			ns
Delay time from address to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V	(1 + a) T – 24			ns
		V_{DD} = 3.0 V	(1 + a) T – 24			ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T – 14			ns
		V_{DD} = 3.0 V	0.5T – 14			ns
Delay time from ASTB↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V			0.5T + 15	ns
		V_{DD} = 3.0 V			0.5T + 20	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise 0
n: Number of waits (n ≥ 0)

AC Characteristics

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time $\overline{WR}\downarrow$	t_{DWOD}			10	62	ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{DSTW}	V_{DD} = 5.0 V	0.5T – 9			ns
		V_{DD} = 3.0 V	0.5T – 9			ns
Data setup time (to $\overline{WR}\uparrow$)	t_{SODWR}	V_{DD} = 5.0 V	(1.5 + n) T – 20			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 25			ns
Data hold time (from $\overline{WR}\uparrow$)	t_{HWOD}	V_{DD} = 5.0 V	0.5T – 14			ns
		V_{DD} = 3.0 V	0.5T – 14			ns
ASTB↑ delay time (from $\overline{WR}\uparrow$)	t_{DWST}	V_{DD} = 5.0 V	0.5T – 9			ns
		V_{DD} = 3.0 V	0.5T – 9			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5 + n) T – 25			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 30			ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise 0
n: Number of waits ($n \geq 0$)

AC Characteristics

(2) External wait timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input time from address to $\overline{WAIT}$↓	t_{DAWT}	V_{DD} = 5.0 V			(2 + a) T – 40	ns
		V_{DD} = 3.0 V			(2 + a) T – 60	ns
Input time from ASTB↓ to $\overline{WAIT}$↓	t_{DSTWT}	V_{DD} = 5.0 V			1.5T – 40	ns
		V_{DD} = 3.0 V			1.5T – 60	ns
Hold time from ASTB↓ to $\overline{WAIT}$	t_{HSTWT}	V_{DD} = 5.0 V	(0.5 + n) T + 5			ns
		V_{DD} = 3.0 V	(0.5 + n) T + 10			ns
Delay time from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V			(1.5 + n) T – 40	ns
		V_{DD} = 3.0 V			(1.5 + n) T – 60	ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{DRWTL}	V_{DD} = 5.0 V			T – 40	ns
		V_{DD} = 3.0 V			T – 60	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{HRWT}	V_{DD} = 5.0 V	nT + 5			ns
		V_{DD} = 3.0 V	nT + 10			ns
Delay time from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V			(1 + n) T – 40	ns
		V_{DD} = 3.0 V			(1 + n) T – 60	ns
Input time from $\overline{WAIT}$↑ to data	t_{DWTID}	V_{DD} = 5.0 V			0.5T – 5	ns
		V_{DD} = 3.0 V			0.5T – 10	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{DWWTL}	V_{DD} = 5.0 V			T – 40	ns
		V_{DD} = 3.0 V			T – 60	ns
Hold time from $\overline{WR}$↓ to $\overline{WAIT}$	t_{HWWT}	V_{DD} = 5.0 V	nT + 5			ns
		V_{DD} = 3.0 V	nT + 10			ns
Delay time from $\overline{WR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	V_{DD} = 5.0 V			(1 + n) T – 40	ns
		V_{DD} = 3.0 V			(1 + n) T – 60	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise 0
n: Number of waits (n ≥ 0)

Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	2.7 V ≤ V_{DD} ≤ 5.5 V	800			ns
			3,200			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V	350			ns
			1,500			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO1}				30	ns

(b) 3-wire serial I/O mode ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	800			ns
			3,200			ns
$\overline{SCK}$ high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ V_{DD} ≤ 5.5 V	400			ns
			1,600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO2}				30	ns

(c) UART mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V	417			ns
		2.7 V ≤ V_{DD} < 4.5 V	833			ns
			1,667			ns
ASCK high-/low-level width	t_{KH3}, t_{KL3}	4.5 V ≤ V_{DD} ≤ 5.5 V	208			ns
		2.7 V ≤ V_{DD} < 4.5 V	416			ns
			833			ns

(d) I^2C bus mode (μPD784218Y only)

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
Low-level width of SCL0 clock		t_{LOW}	4.7	—	1.3	—	μs
High-level width of SCL0 clock		t_{HIGH}	4.0	—	0.6	—	μs
Setup time of start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	When using I^2C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
Rise time of SDA0 and SCL0 signals		t_R	—	1,000	20 + 0.1Cb[Note 5]	300	ns
Fall time of SDA0 and SCL0 signals		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Setup time of stop condition		$t_{SU:STO}$	4.0	—	0.6	—	μs
Pulse width of spike restricted by input filter		t_{SP}	—	—	0	50	ns
Load capacitance of each bus line		Cb	—	400	—	400	pF

Notes 1. For the start condition, the first clock pulse is generated after the hold time.

2. To fill the undefined area of the SCL0 falling edge, it is necessary for the device to provide an internal SDA0 signal (on $V_{IHmin.}$) with at least 300 ns of hold time.

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be satisfied.

4. The high-speed mode I^2C bus can be used in a standard mode I^2C bus system. In this case, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the data bit to the SDA0 line before the SCL0 line is released
  ($t_{Rmax.} + t_{SU:DAT} = 1{,}250$ ns by standard mode I^2C bus specification)

5. Cb: total capacitance per one bus line (unit: pF)

Other Operations (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
INTP input high-/low-level width	t_{WITL} t_{WITH}	INTP0 to INTP6	10			μs
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSL} t_{WRSH}		10			μs

Clock Output Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PCL cycle time	t_{CYCL}	V_{DD} = 4.5 to 5.5 V, nT	80		31,250	ns
PCL high-/low-level width	t_{CLL} t_{CLH}	V_{DD} = 4.5 to 5.5 V, 0.5T – 10	30		15,615	ns
PCL rise/fall time	t_{CLR} t_{CLF}	4.5 V ≤ V_{DD} ≤ 5.5 V			5	ns
		2.7 V ≤ V_{DD} < 4.5 V			10	ns
		2.2 V ≤ V_{DD} < 2.7 V			20	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

n: Divided frequency ratio set by software in the CPU

- When using the main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- When using the subsystem clock: n = 1

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			±1.2	%
		2.2 V ≤ AV_{REF0} < 2.7 V (only when AV_{REF0} = AV_{DD})			±1.6	%
Conversion time	t_{CONV}		14		144	μs
Sampling time	t_{SAMP}		24/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.2		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AVREF0}			29.4		kΩ

Note Excludes quantization error (±1/2 LSB).

Remark f_{XX}: Main system clock frequency

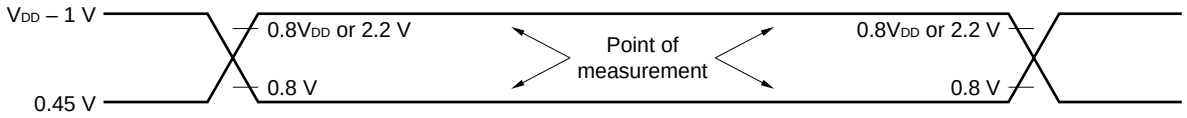
D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error		R = 2 MΩ, 2.2 V < AV_{REF1} ≤ 5.5 V				±1.2	%
		R = 4 MΩ, 2.2 V < AV_{REF1} ≤ 5.5 V				±0.8	%
		R = 10 MΩ, 2.2 V < AV_{REF1} ≤ 5.5 V				±0.6	%
Settling time		Load conditions: C = 30 pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.2 V ≤ AV_{REF1} < 2.7 V			20	μs
★ Output resistance	R_O	DACS0, 1 = 55 H			5.3		kΩ
Reference voltage	AV_{REF1}			2.2		V_{DD}	V
AV_{REF1} current	AI_{REF1}	For only 1 channel				2.5	mA

Data Retention Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

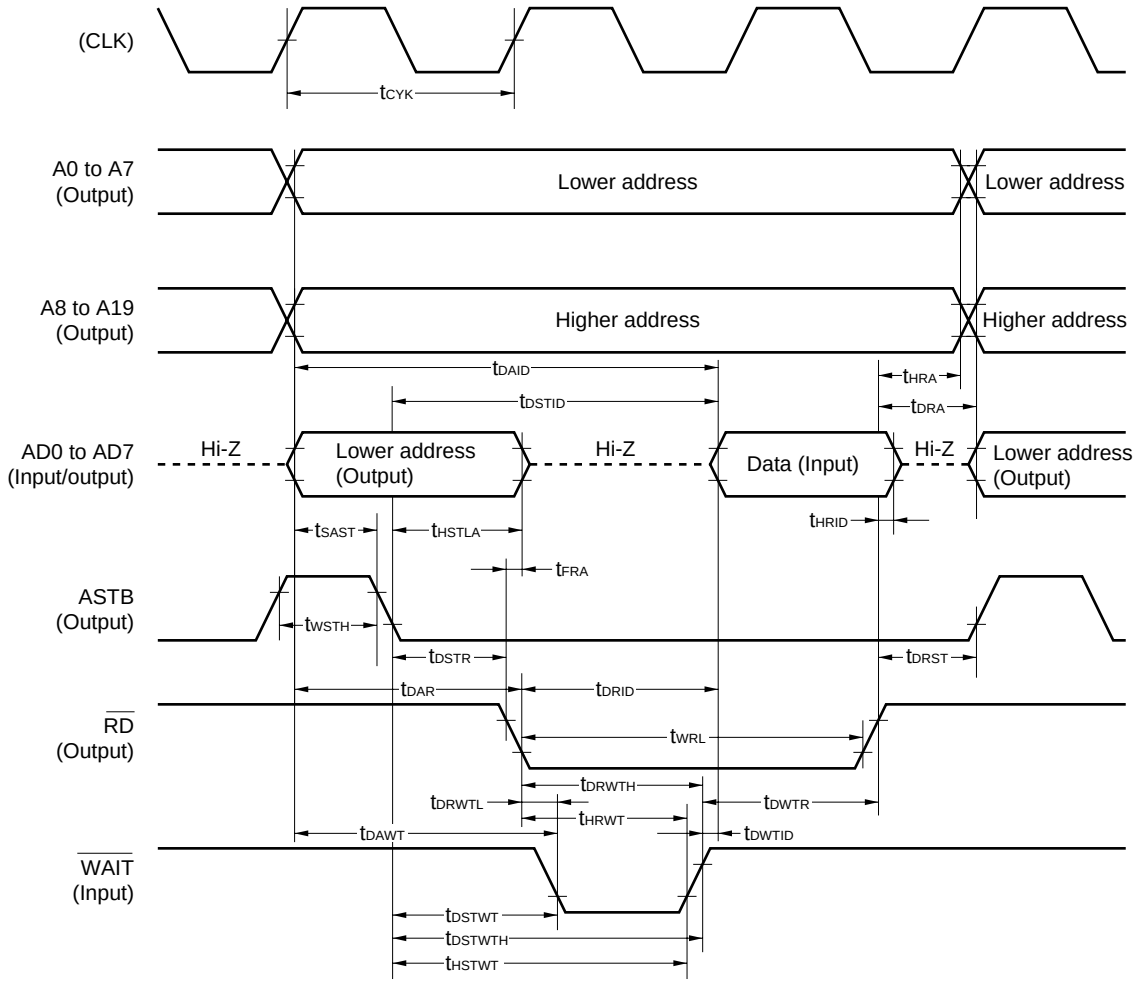
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.2		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = +4.5 to 5.5 V		10	50	μA
		V_{DDDR} = +2.5 V		2	10	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Input voltage, low	V_{IL}	$\overline{\text{RESET}}$, P00/INTP0 to P06/INTP6	0		$0.1V_{DDDR}$	V
Input voltage, high	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

AC Timing Measurement Points



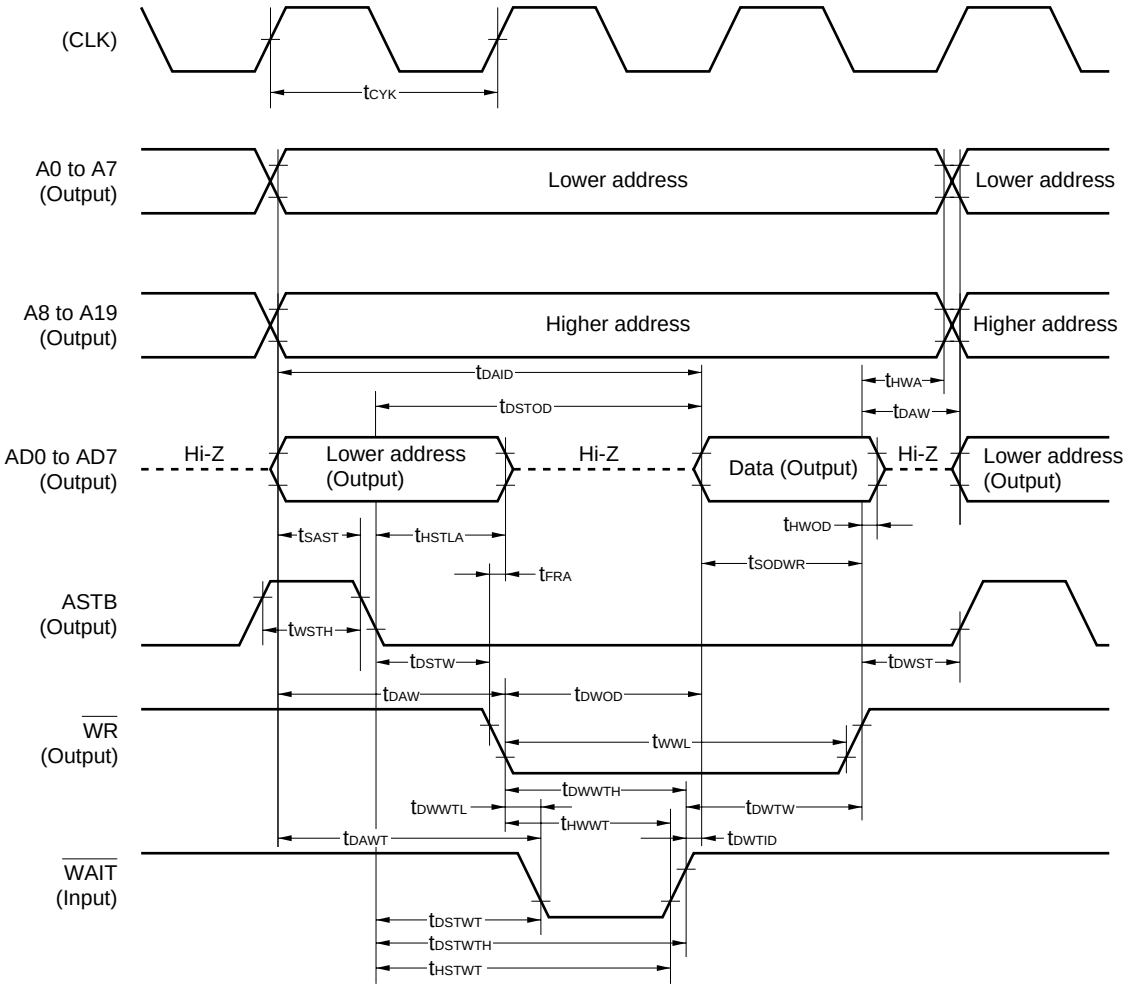
Timing Waveforms

(1) Read operation



Remark Signals are output from A0 to A7 while ports 80 to 87 are not being used.

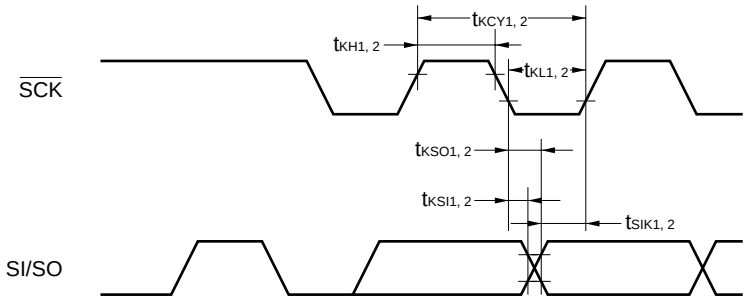
(2) Write operation



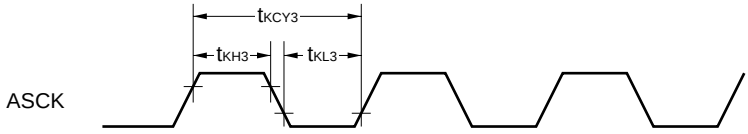
Remark Signals are output from A0 to A7 while ports 80 to 87 are not being used.

Serial Operation

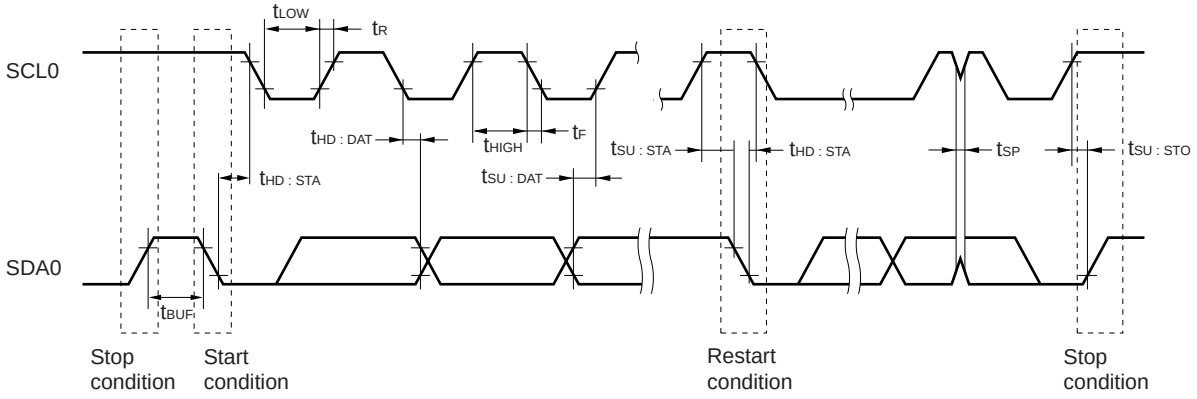
(1) 3-wire serial I/O mode



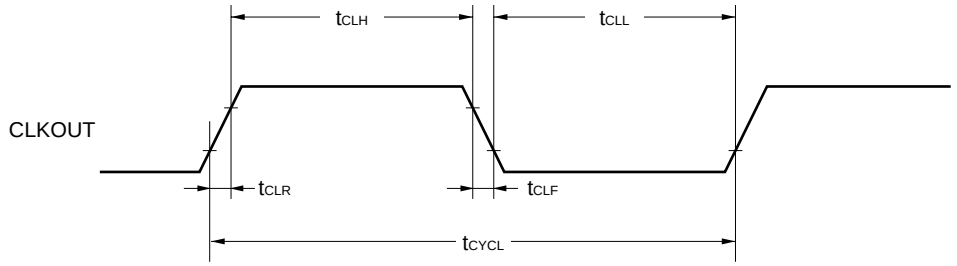
(2) UART mode



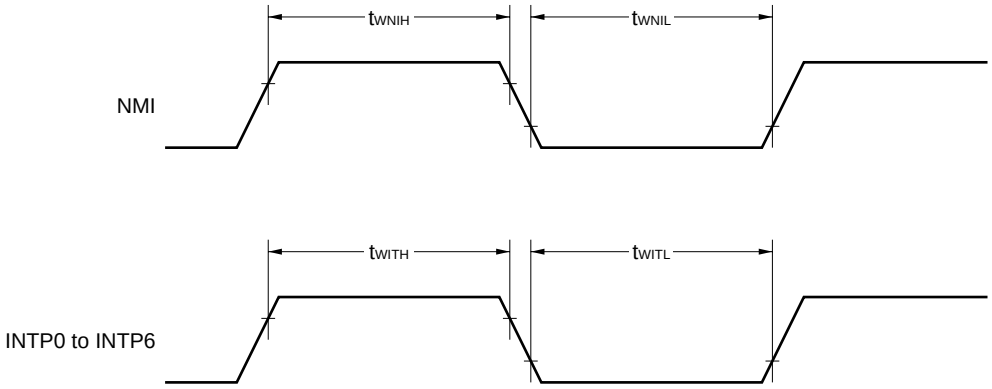
(3) I²C bus mode (μPD784218Y Subseries only)



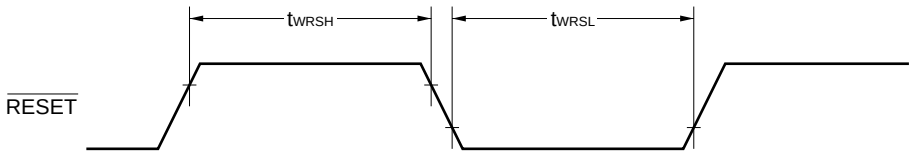
Clock Output Timing



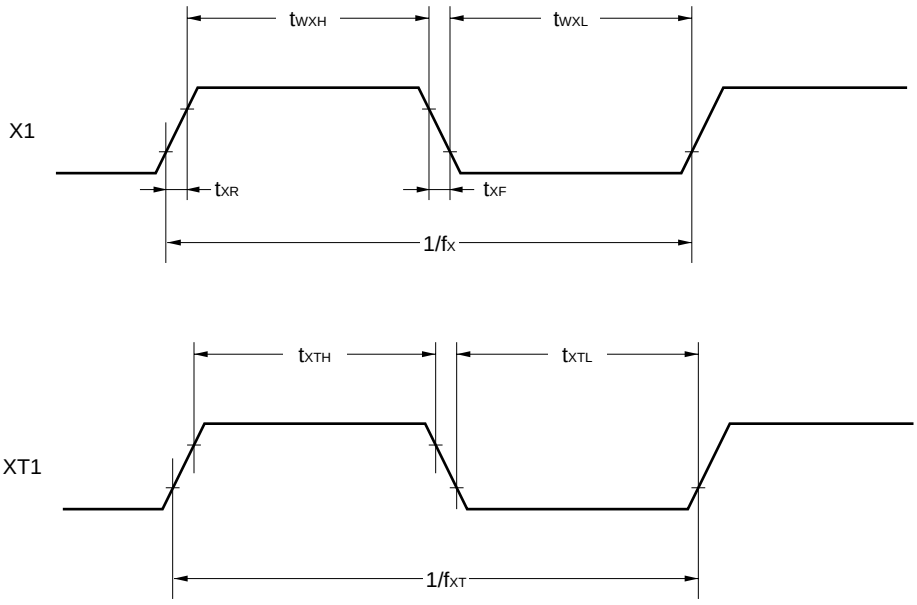
Interrupt Input Timing



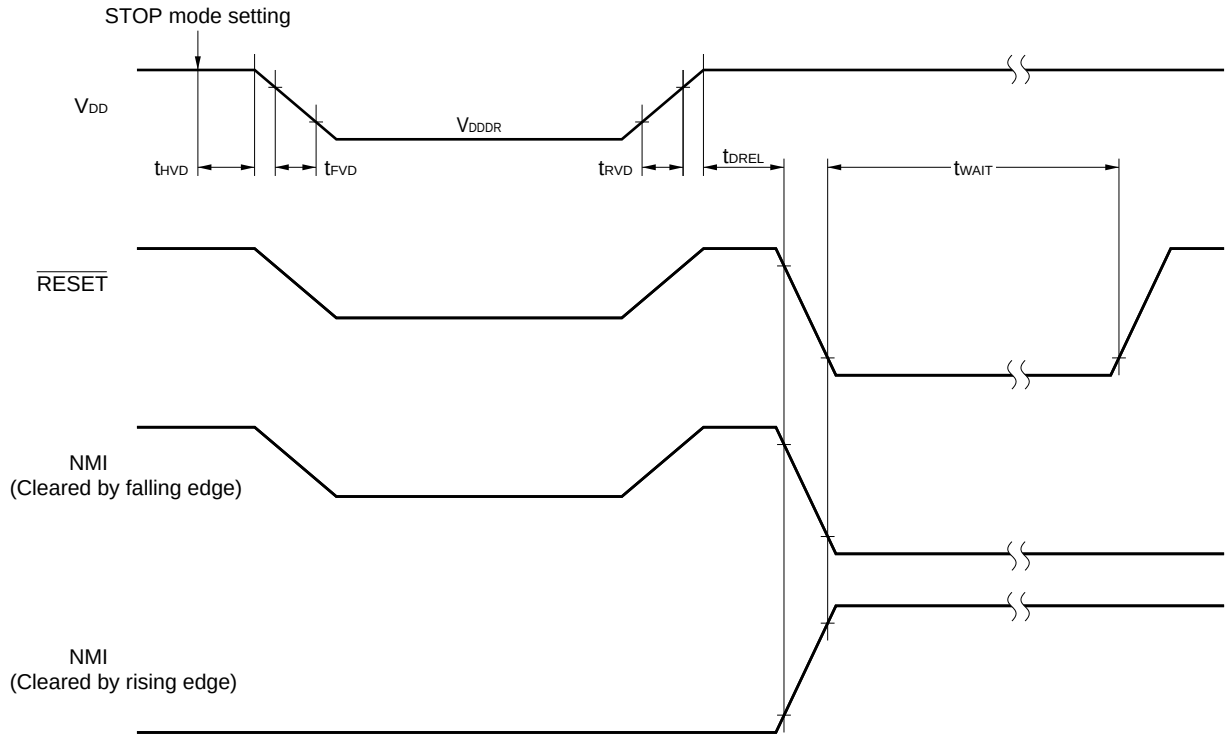
Reset Input Timing



Clock Timing

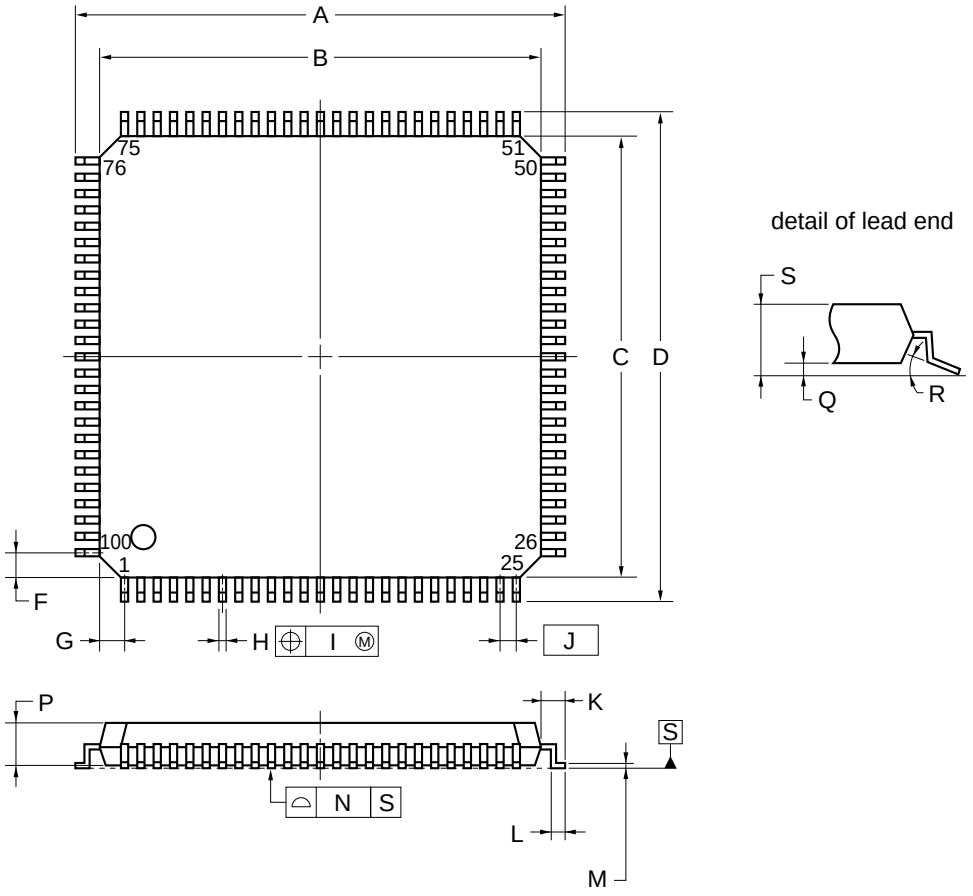


Data Retention Characteristics



★ 16. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

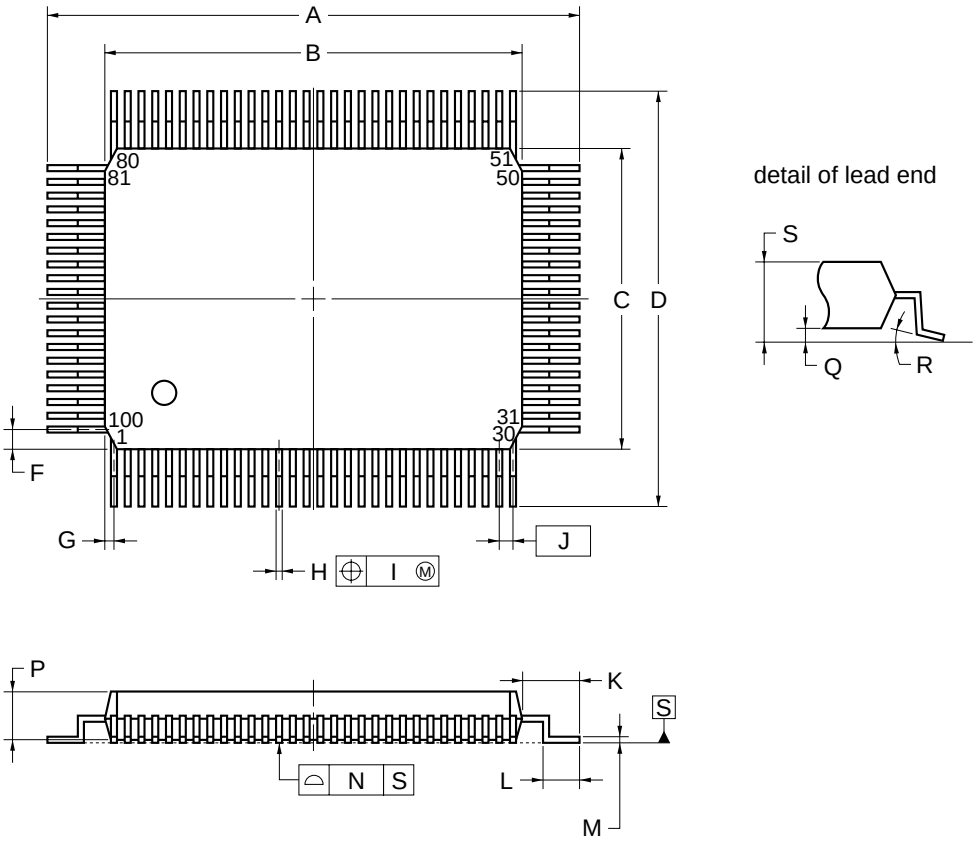
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU-1

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

100-PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

★ 17. RECOMMENDED SOLDERING CONDITIONS

The μPD784218 should be soldered and mounted under the following recommended conditions. For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Caution Soldering conditions for the μPD784218YGC-×××-8EU and μPD784218YGF-×××-3BA are undetermined because these products are under development.

Table 17-1. Soldering Conditions for Surface Mount Type

(1) μPD784218GC-×××-8EU: 100-pin plastic LQFP (Fine pitch) (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP-15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD784218GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784218. Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784218	Device file common to μPD784218, 784218Y Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash Memory Writing Tools

Flashpro II (Part No.: FL-PR2), Flashpro III (Part No.: FL-PR3, PG-FP3)	Dedicated flash programmer for microcontroller incorporating flash memory
FA-100GF	Adapter for writing 100-pin plastic QFP (GF-3BA type) flash memory.
FA-100GC	Adapter for writing 100-pin plastic LQFP (GC-8EU type) flash memory.

(3) Debugging Tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and cable when notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
IE-784225-NS-EM1	Emulation board to emulate μPD784218, 784218Y Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784218	Device file common to μPD784218, 784218Y Subseries

- **When IE-784000-R in-circuit emulator is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Interface adapter when using PC that incorporates PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784225-NS-EM1 IE-784218-R-EM1	Emulation board to emulate μPD784218, 784218Y Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX3	Emulation probe conversion board necessary when using IE-784225-NS-EM1 on IE-784000-R. Not necessary when IE-784216-R-EM1 is used.
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784218	Device file common to μPD784218, 784218Y Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on Using Development Tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784218.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784218.
- The FL-PR2, FL-PR3, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- The TGC-100SDW is a product made by TOKYO ELETECH CORPORATION.
- For further information, contact Daimaru Kogyo, Ltd.
  Tokyo Electronic Division (TEL: +81-3-3820-7112)
  Osaka Electronic Division (TEL: +81-6-6244-6672)
- For third-party development tools, see the **78K/IV Series Selection Guide (U13355E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√Note	√
CC78K4	√Note	√
ID78K4-NS	√	–
ID78K4	√	√
SM78K4	√	–
RX78K/IV	√Note	√
MX78K4	√Note	√

Note DOS-based software

APPENDIX B RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD784218, 784218Y Data Sheet	U12304J	This document
μPD78F4218, 78F4218Y Preliminary Product Information	U12440J	U12440E
μPD784218, 784218Y Subseries User's Manual Hardware	U12970J	U12970E
78K/IV Series User's Manual Instructions	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note Software Fundamentals	U10095J	U10095E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Language	U11162J	U11162E
	Operation	U11334J	U11334E
RA78K Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Language	U11571J	U11571E
	Operation	U11572J	U11572E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784218-R-EM1		U12155J	U12155E
IE-784225-NS-EM1		U13742J	U13742E
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger PC Based	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Based	Reference	U11960J	U11960E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamentals	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–
78K/IV Series OS MK78K4	Fundamentals	U11779J	–

Other Related Documents

Document Name	Document No.	
	Japanese	English
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Microcontroller-Related Products by Third Parties	U11416J	–

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Eindhoven, The Netherlands
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Fax: 040-2444580

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Fax: 01-30-67 58 99

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Tel: 91-504-2787
Fax: 91-504-2860

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Fax: 08-63 80 388

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  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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