NEC

MOS INTEGRATED CIRCUITS

μPD78F4938A

16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F4938A is a product in the μPD784938A Subseries in the 78K/IV Series.

The μPD78F4938A has flash memory in place of the internal ROM of the μPD784938A. The flash memory incorporated enables program writing or erasing with the microcontroller mounted on the target board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784938A Subseries User's Manual Hardware: U13570E
78K/IV Series User's Manual Instructions: U10905E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 256 KB
- Internal RAM: 10496 bytes
- Serial interface: 4 channels
  - UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator)
  - CSI (3-wire serial I/O): 2 channels
- On-chip IEBus™ controller
- Supply voltage: V_{DD} = 4.0 to 5.5 V (@12.58 MHz operation)
  V_{DD} = 3.0 to 5.5 V (@6.29 MHz operation)

APPLICATION

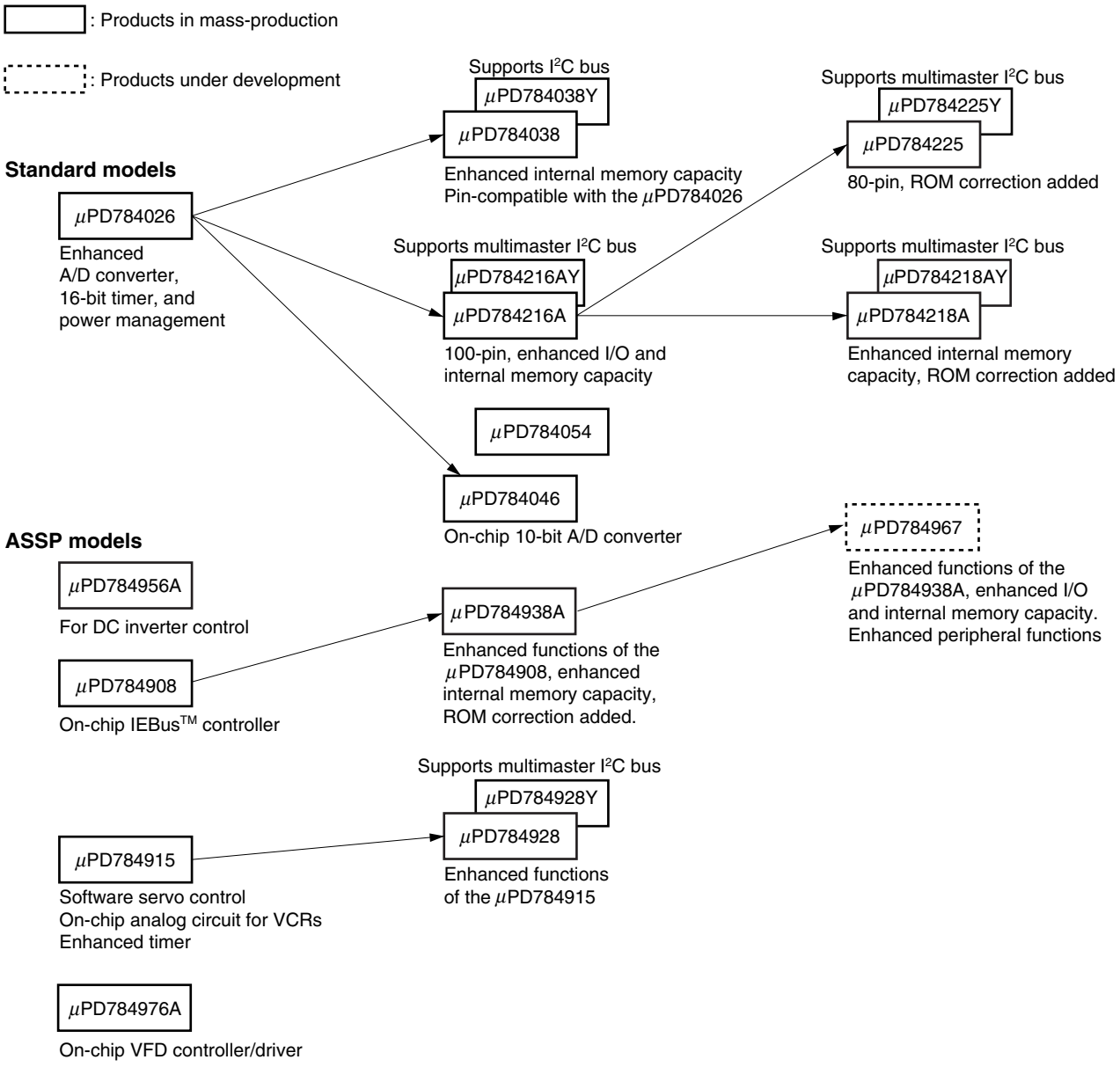
Car audio, etc.

ORDERING INFORMATION

Part Number	Package	Internal ROM	Internal RAM
μPD78F4938AGF-3BA	100-pin plastic QFP (14 × 20)	256 KB	10496 bytes

Document No. U14118EJ1V0DS00
Date Published March 2001 N CP(K)
Printed in Japan

78K/IV SERIES LINEUP



Remark Although VFD (Vacuum Florescent Display is generally used, in some documents, the display is described as FIP™ (Florescent Inidicator Panel). VFD and FIP are functionally equivalent.

OVERVIEW OF FUNCTIONS

(1/2)

Item \ Part Number		μPD78F4938A		
Number of basic instructions (mnemonics)		113		
General-purpose registers		8 bits × 32 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory map)		
Minimum instruction execution time		320 ns/636 ns/1.27 μs/2.54 μs (@6.29 MHz operation) 160 ns/320 ns/636 ns/1.27 μs (@12.58 MHz operation)		
Internal memory	ROM	256 KB		
	RAM	10496 bytes		
Memory space		1 MB with program and data spaces combined		
I/O port	Total	80 pins		
	Input	8 pins		
	I/O	72 pins		
Pins with ancillary function[Note]	LED direct drive output	24 pins		
	Transistor direct drive	8 pins		
	N-ch open drain drive	4 pins		
Real-time output port		4 bits × 2, or 8 bits × 1		
IEBus controller		Internal (simple version)		
Timer/counter		Timer/event counter 0: (16 bits)	Timer counter × 1 Capture register × 1 Compare register × 2	Pulse output possible • Toggle output • PWM/PPG output • One-shot pulse output
		Timer/event counter 1: (16 bits)	Timer counter × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Real-time output port
		Timer/event counter 2: (16 bits)	Timer counter × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Pulse output possible • Toggle output • PWM/PPG output
		Timer 3 (16 bits):	Timer counter × 1 Compare register × 1	
Watch timer		Generates interrupt request at 0.5-second intervals (On-chip watch clock oscillator) Main clock (12.58 MHz) or watch clock (32.7 kHz) selectable as input clock		
Clock output		Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (also usable as 1-bit output port)		
PWM output		12-bit resolution × 2 channels		
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O): 2 channels		
A/D converter		8-bit resolution × 8 channels		
Watchdog timer		1 channel		
ROM correction function		Internal (4 points of correction addresses can be set.)		
External expansion function		Provided (up to 1 MB)		

Note Pins with ancillary functions are included in the I/O pins.

(2/2)

Item \ Part Number		μPD78F4938A
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	27 (internal: 20, external: 7 (sampling clock variable input: 1))
	Software source	BRK instruction, BRKCS instruction, operand error
	Non-maskable	Internal: 1, external: 1
	Maskable	Internal: 19, external: 6
		Four programmable priority levels Three types of processing formats: Vectored interrupt/macro service/context switching
Supply voltage		• V_{DD} = 4.0 to 5.5 V (@12.58 MHz operation) • V_{DD} = 3.0 to 5.5 V (@6.29 MHz operation)
Package		100-pin plastic QFP (14 × 20)

CONTENTS

1. DIFFERENCES AMONG PRODUCTS IN μPD784938A SUBSERIES

The only difference between the μPD784935A, 784936A, 784937A, and 784938A is the internal memory capacity.

The μPD78F4938A has a 256 KB flash memory in the place of the mask ROM of the above products. Table 1-1 shows the differences between these products.

Table 1-1. Differences Among Products in μPD784938A Subseries

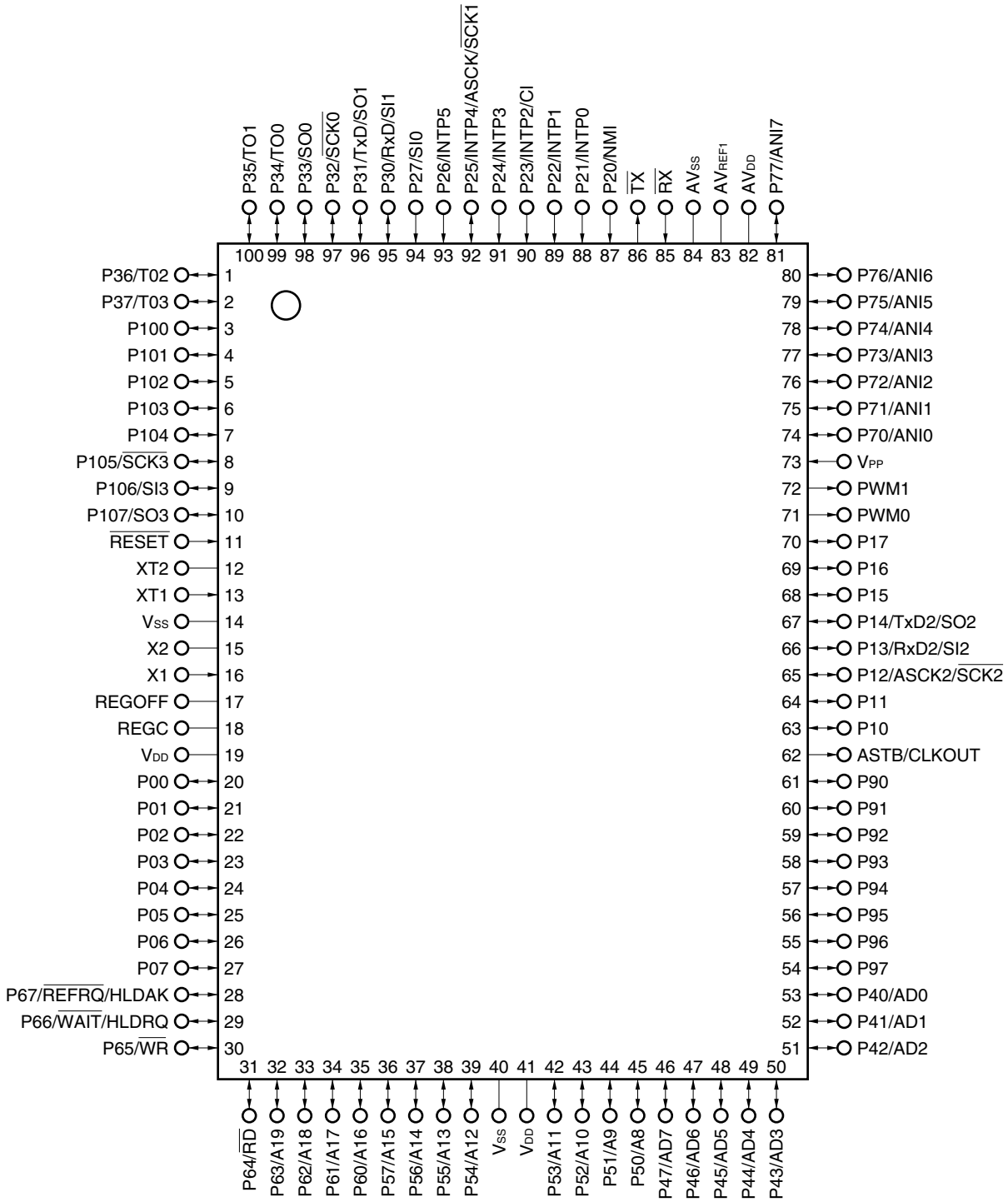
Item \ Part Number	μPD784935A	μPD784936A	μPD784937A	μPD784938A	μPD78F4938A
Internal ROM	96 KB	128 KB	192 KB	256 KB	
	Mask ROM				Flash memory
Internal RAM	5120 bytes	6656 bytes	8192 bytes	10496 bytes	
Regulator	Provided				None
Electrical specifications	Refer to the data sheet of each product.				
Internal memory size switching register[Note]	None				Provided
IC pin	Provided				None
V_{PP} pin	None				Provided

Note The internal flash memory capacity and internal RAM capacity can be changed by using the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic QFP (14 × 20)**
  μPD78F4938AGF-3BA



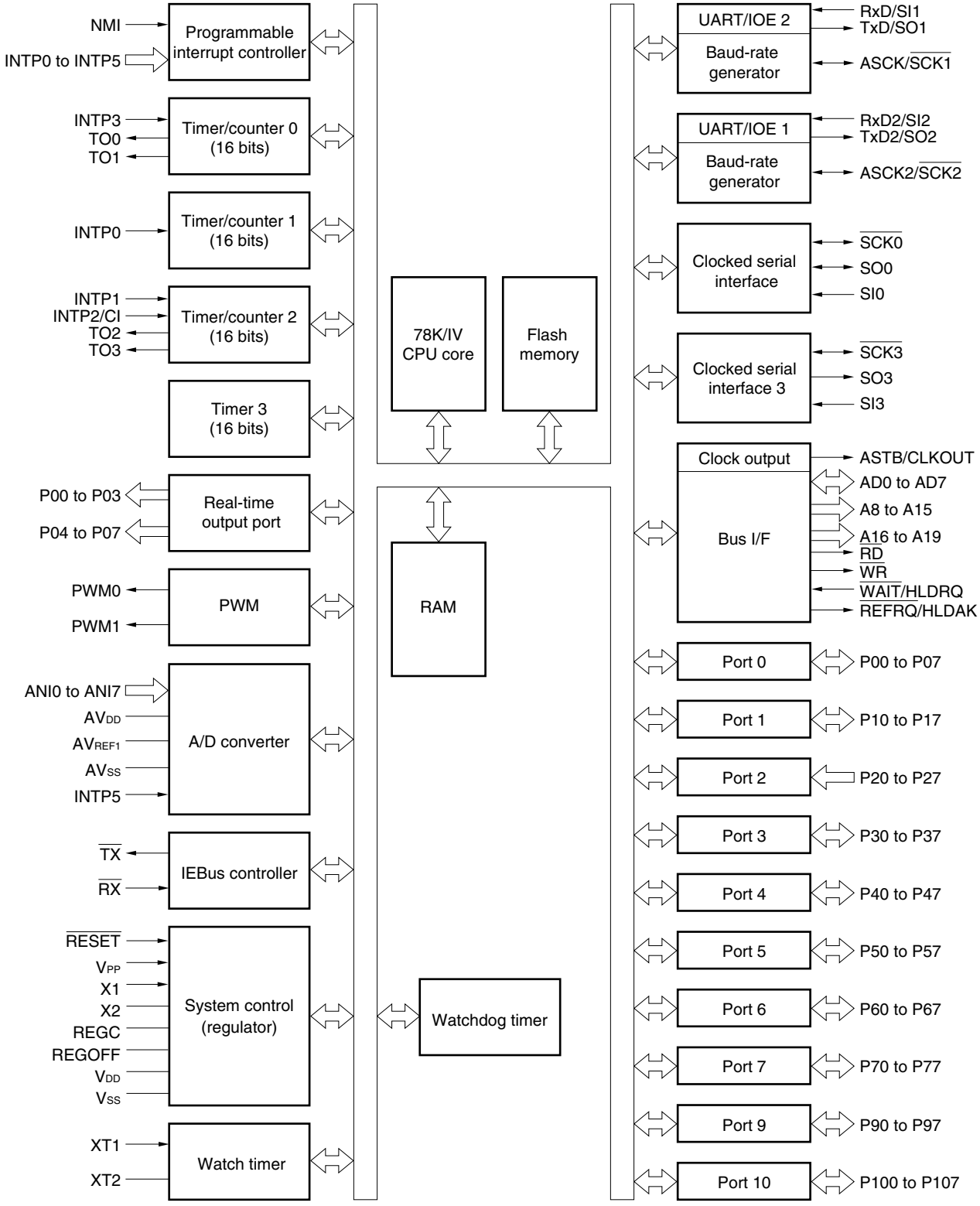
Cautions 1. In normal operation mode, connect V_{PP} pin directly to the V_{SS} pin, or pull it down.
In a system where the internal flash memory is rewritten while mounted on board, pull the V_{PP} pin down.
When pulling down, connection via a 470 Ω or higher and 10 kΩ or lower resistor is recommended.

2. Connect the AV_{DD} pin directly to V_{DD}.

3. Connect the AV_{SS} pin directly to V_{SS}.

A8 to A19:	Address bus
AD0 to AD7:	Address/data bus
ANI0 to ANI7:	Analog input
ASCK, ASCK2:	Asynchronous serial clock
ASTB:	Address strobe
AV_{DD}:	Analog power supply
AV_{REF1}:	Reference voltage
AV_{SS}:	Analog ground
CI:	Clock input
CLKOUT:	Clock output
HLDAK:	Hold acknowledge
HLDRQ:	Hold request
INTP0 to INTP5:	Interrupt from peripherals
NMI:	Non-maskable interrupt
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P90 to P97:	Port 9
P100 to P107:	Port 10
PWM0, PWM1:	Pulse width modulation output
$\overline{RD}$:	Read strobe
$\overline{REFRQ}$:	Refresh request
REGC:	Regulator capacitance
REGOFF:	Regulator off
$\overline{RESET}$:	Reset
$\overline{RX}$:	IEBus receive data
RxD, RxD2:	Receive data
$\overline{SCK0}$ to $\overline{SCK3}$:	Serial clock
SI0 to SI3:	Serial input
SO0 to SO3:	Serial output
TO0 to TO3:	Timer output
$\overline{TX}$:	IEBus transmit data
TxD, TxD2:	Transmit data
V_{DD}:	Power supply
V_{PP}:	Programming power supply
V_{SS}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write strobe
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (watch)

3. BLOCK DIAGRAM



4. PIN FUNCTIONS

4.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00 to P07	I/O	—	Port 0 (P0): • 8-bit I/O port. • Can be used as real-time output port (4 bits × 2). • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive transistor.
P10	I/O	—	Port 1 (P1): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P11		—	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15 to 17		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input port. • P20 cannot be used as general-purpose port pin (non-maskable interrupt). However, input level can be checked by interrupt routine. • An on-chip pull-up resistor can be specified for P22 to P27 by means of software in 6-bit units. • P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin operates as $\overline{\text{SCK1}}$ I/O pin if so specified by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • P32 and P33 can be specified for N-ch open-drain connection.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34 to P37		TO0 to TO3	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P60 to P63	I/O	A16 to A19	Port 6 (P6): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode.
P64		$\overline{\text{RD}}$	
P65		$\overline{\text{WR}}$	
P66		$\overline{\text{WAIT}}$/HLDRQ	
P67		$\overline{\text{REFRQ}}$/HLDAK	

4.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P70 to P77	I/O	ANI0 to ANI7	Port 7 (P7): • 8-bit I/O port. • Input/output can be specified in 1-bit units.
P90 to P97	I/O	—	Port 9 (P9): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode.
P100 to P104	I/O	—	Port 10 (P10): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • P105 and P107 can be specified for N-ch open-drain connection.
P105		$\overline{\text{SCK3}}$	
P106		SI3	
P107		SO3	

4.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
TO0 to TO3	Output	P34 to P37	Timer output	
CI	Input	P23/INTP2	Count clock input to timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{SCK1}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{SCK2}$	Baud rate clock input (UART2)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SI3		P106	Serial data input (3-wire serial I/O3)	
SO0	Output	P33	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
SO3		P107	Serial data output (3-wire serial I/O3)	
$\overline{SCK0}$	I/O	P32	Serial clock input/output (3-wire serial I/O0)	
$\overline{SCK1}$		P25/INTP4/ASCK	Serial clock input/output (3-wire serial I/O1)	
$\overline{SCK2}$		P12/ASCK2	Serial clock input/output (3-wire serial I/O2)	
$\overline{SCK3}$		P105	Serial clock input/output (3-wire serial I/O3)	
NMI	Input	P20	External interrupt requests	—
INTP0		P21		• Count clock input to timer/counter 1 • Capture trigger signal of CR11 or CR12
INTP1		P22		• Count clock input to timer/counter 2 • Capture trigger signal of CR22
INTP2		P23/CI		• Count clock input to timer/counter 2 • Capture trigger signal of CR21
INTP3		P24		• Count clock input to timer/counter 0 • Capture trigger signal of CR02
INTP4		P25/ASCK/$\overline{SCK1}$		—
INTP5		P26		Conversion start trigger input of A/D converter
AD0 to AD7	I/O	P40 to P47	Time-division address/data bus (external memory connection)	
A8 to A15	Output	P50 to P57	Higher address bus (external memory connection)	
A16 to A19	Output	P60 to P63	Higher address for address extension (external memory connection)	
$\overline{RD}$	Output	P64	Read strobe to external memory	
$\overline{WR}$	Output	P65	Write strobe to external memory	
$\overline{WAIT}$	Input	P66/HLDRQ	Wait insertion	
$\overline{REFRQ}$	Output	P67/HLDAK	Refresh pulse output to external pseudo-static memory	
HLDRQ	Input	P66/$\overline{WAIT}$	Bus hold request input	
HLDAK	Output	P67/$\overline{REFRQ}$	Bus hold acknowledge output	
ASTB	Output	CLKOUT	Latch timing output of time-division address (A0 to A7) (when external memory is accessed)	

4.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	—	PWM output 0
PWM1	Output	—	PWM output 1
$\overline{RX}$	Input	—	Data input (IEBus)
$\overline{TX}$	Output	—	Data output (IEBus)
REGC	—	—	Connecting capacitor for regulation output stabilization/power supply when regulator is stopped
REGOFF	—	—	Regulator operation specification signal
$\overline{RESET}$	Input	—	Chip reset
X1	Input	—	Connecting crystal resonator for system clock oscillation (clock can be also input to X1.)
X2	—		
XT1	Input	—	Watch clock connection
XT2	—	—	
ANI0 to ANI7	Input	P70 to P77	Analog voltage input for A/D converter
AV_{REF1}	—	—	Application of reference voltage for A/D converter
AV_{DD}			Positive power supply for A/D converter
AV_{SS}			GND for A/D converter
V_{DD}			Positive power supply
V_{SS}			GND
V_{PP}	Input		Sets flash memory programming mode. For high voltage application when program is written or verified. In normal operation mode, connect V_{PP} pin directly to the V_{SS} pin, or pull it down. In a system where the internal flash memory is rewritten while mounted on board, pull the V_{PP} pin down. When pulling down, connection via a 470 Ω or higher and 10 kΩ or lower resistor is recommended.

4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 4-1.

For the I/O circuit configuration of each type, refer to **Figure 4-1**.

Table 4-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-A	I/O	Input: Connect to V_{DD}.
P10, P11			Output: Leave open.
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15 to P17			
P20/NMI	2	Input	Connect to V_{DD} or V_{SS}.
P21/INTP0			
P22/INTP1	2-A		Connect to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	I/O	Input: Connect to V_{DD}.
			Output: Leave open.
P26/INTP5	2-A	Input	Connect to V_{DD}.
P27/SI0			
P30/RxD/SI1	5-A	I/O	Input: Connect to V_{DD}.
P31/TxD/SO1			Output: Leave open.
P32/$\overline{SCK0}$	10-A		
P33/SO0			
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0 to P77/ANI7	20	I/O	Input: Connect to V_{DD} or V_{SS}.
P90 to P97	5-A		Output: Leave open.
P100 to P104			
P105/$\overline{SCK3}$	10-A		
P106/SI3	8-A		
P107/SO3	10-A		
ASTB/CLKOUT	4	Output	Leave open.
$\overline{RESET}$	2	Input	—
V_{PP}	1		Connect directly to V_{SS}.
XT2	—	—	Leave open.
XT1	—	Input	Connect directly to V_{SS}.

Table 4-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

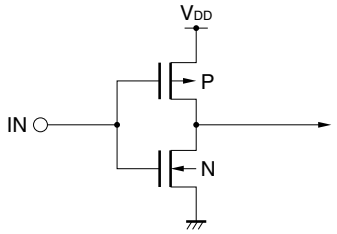
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
REGOFF	1	—	Connect directly to V_{DD}.
REGC	—	—	Connect to V_{DD}.
PWM0, PWM1	3	Output	Leave open.
$\overline{RX}$	1	Input	Connect to V_{DD} or V_{SS}.
$\overline{TX}$	3	Output	Leave open.
AV_{REF1}	—	—	Connect to V_{SS}.
AV_{SS}			
AV_{DD}			Connect to V_{DD}.

Caution Connect an I/O pin to V_{DD} via a resistor of several 10 kΩ if the I/O mode of the pin is unstable (especially if the voltage on the reset pin is higher than the low-level input voltage on power application or if the mode is changed between input and output by software).

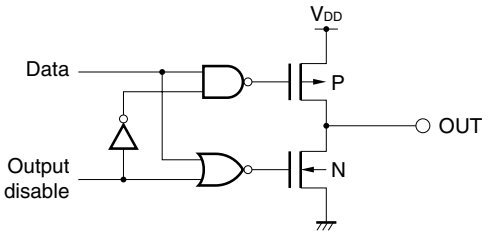
Remark The circuit type numbers are common for the 78K Series and are not always sequential for one product (some circuits are not provided).

Figure 4-1. Pin I/O Circuits (1/2)

Type 1

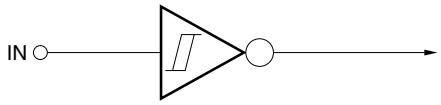


Type 4



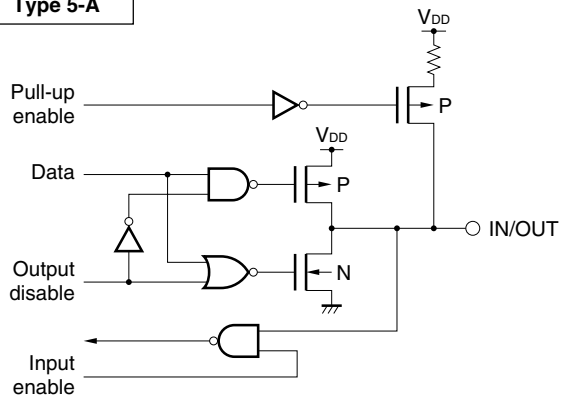
Push-pull output that can go into a high-impedance state (both P-ch and N-ch are off).

Type 2

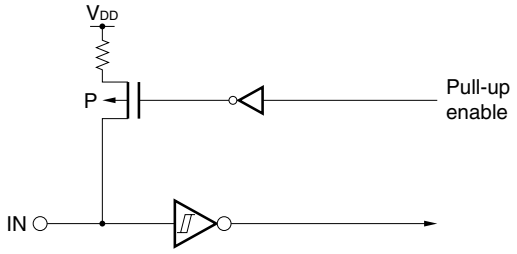


Schmitt-triggered input with hysteresis characteristics

Type 5-A

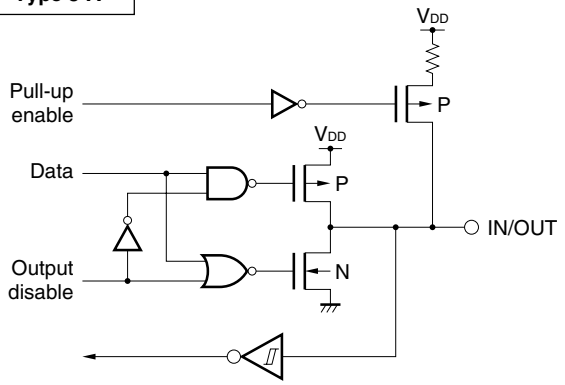


Type 2-A

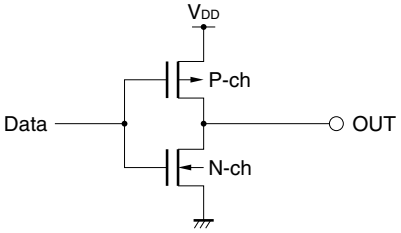


Schmitt-triggered input with hysteresis characteristics

Type 8-A



Type 3



Type 10-A

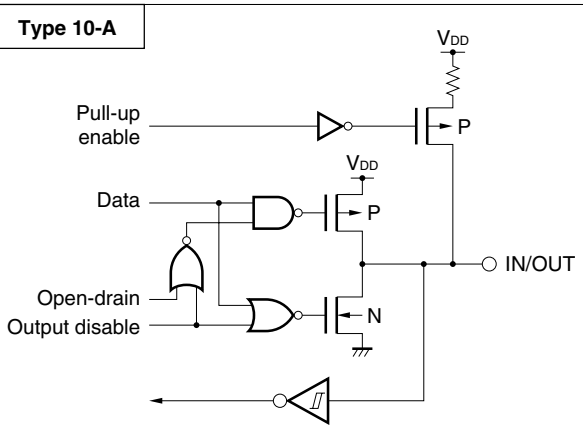
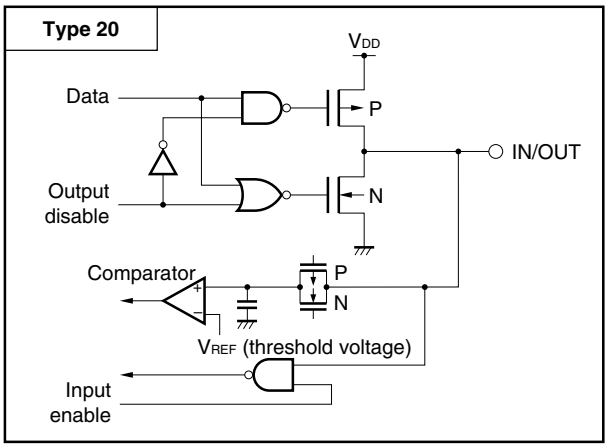


Figure 4-1. Pin I/O Circuits (2/2)



5. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register to prevent a certain part of the internal memory from being used by software. By setting the IMS, it is possible to establish a memory map that is the same as that of mask ROM version with a different internal memory (ROM, RAM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to FFH.

Figure 5-1. Internal Memory Size Switching Register (IMS) Format

Address 0FFFCH After reset FFH W

Symbol	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Internal ROM Capacity Selection
0	0	256 KB
0	1	96 KB
1	0	128 KB
1	1	192 KB

RAM1	RAM0	Internal RAM Capacity Selection
0	0	10496 bytes
0	1	5120 bytes
1	0	6656 bytes
1	1	8192 bytes

Caution IMS is not available for mask ROM versions (μPD784935A, 784936A, 784937A, and 784938A).

The IMS settings to create the same memory map as mask ROM versions are shown in Table 5-1.

Table 5-1. Internal Memory Size Switching Register (IMS) Settings

Relevant Mask ROM Version	IMS Setting
μPD784935A	DDH
μPD784936A	EEH
μPD784937A	FFH
μPD784938A	CCH

Note Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, if the external devices do not acknowledge the port state immediately after reset, handling such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor is required.

6. PROGRAMMING FLASH MEMORY

Flash memory can be written while mounted on the target system (on-board writing). Connect the dedicated flash programmer (Flashpro III (part No.: FL-PR3, PG-FP3)) to the host machine and target system for programming. Moreover, writing to flash memory can also be performed using a flash memory writing adapter connected to Flashpro III.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting Communication Mode

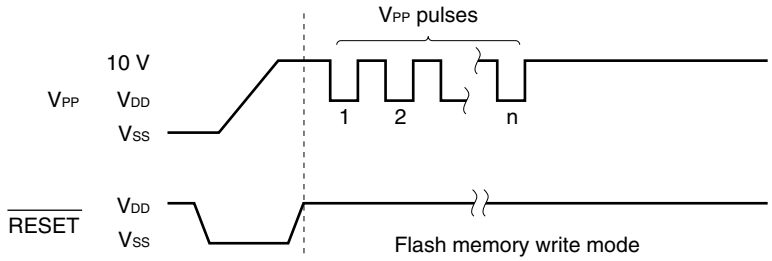
The Flashpro III is used to write data into a flash memory by serial communications. Select the communication mode for writing from Table 6-1. Figure 6-1 shows the format used to select the communication mode. Each communication mode is selected with the number of V_{PP} pulses shown in Table 6-1.

Table 6-1. Communication Mode

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	3	$\overline{SCK3}$/P105 SI3/P106 SO3/P107	1
		$\overline{SCK0}$/P32 SI0/P27 SO0/P33	0
		$\overline{SCK3}$/P105 SI3/P106 SO3/P107 P104 (for handshake)	3
UART	1	RxD/P30 TxD/P31	8

Caution Always select the communication mode using the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Communication Mode Selection Format



6.2 Flash Memory Programming Functions

By transmitting and receiving various commands and data by the selected communication mode, operations such as writing to the flash memory are performed. Table 6-2 shows the major functions.

Table 6-2. Flash Memory Programming Functions

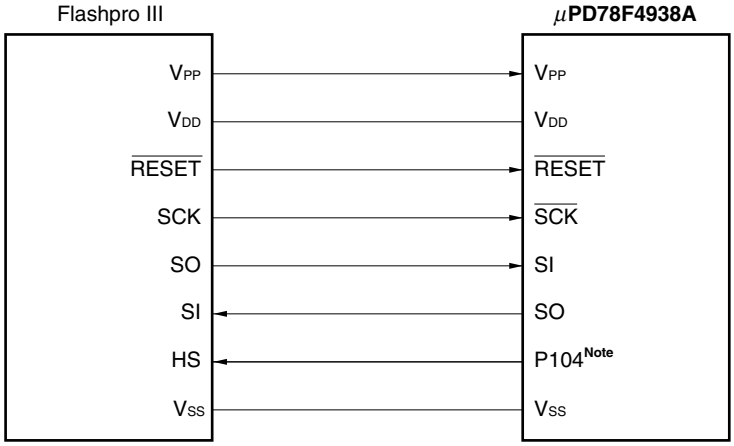
Function	Description
Area erase	Erase the contents of the specified memory area where one memory block is 16 KB.
Area blank check	Checks the erase state of the specified area.
Data write	Writes to the flash memory based on the start write address and the number of data written (number of bytes).
Area verify	Compares the data input with the contents of the specified memory area.

Verification for the flash memory entails supplying the data to be verified from an external source via a serial interface, and then outputting the existence of unmatched data to the external source after referencing the areas or all of the data. Consequently, the flash memory is not equipped with a read function, and it is not possible for third parties to read the contents of the flash memory with the use of the verification function.

6.3 Connecting Flashpro III

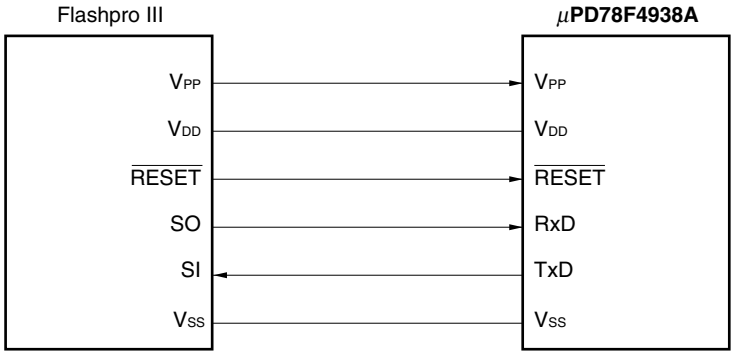
The connection between the Flashpro III and the μPD78F4938A differs depending on the communication mode (3-wire serial I/O or UART). Figures 6-2 and 6-3 are the connection diagrams in each case.

Figure 6-2. Flashpro III Connection in 3-Wire Serial I/O Mode



Note Only in the handshake communication

Figure 6-3. Flashpro III Connection in UART Mode



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	AV_{DD}		–0.3 to V_{DD} + 0.3	V
	AV_{SS}		–0.3 to V_{SS} + 0.3	V
	AV_{REF1}	A/D converter reference voltage input	–0.3 to V_{DD} + 0.3	V
Input voltage	V_{I2}		–0.3 to +10.5	V
Analog input voltage	V_{IAN}	Analog input voltage	AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin	10	mA
		Total for all pins of ports 0, 3, 6, 10 and P54 to P57	50	mA
		Total for all pins of ports 1, 4, 7, 9, P50 to P53, PWM0, PWM1, and $\overline{TX}$ pins	50	mA
Output current, high	I_{OH}	Per pin	–6	mA
		Total for all pins of ports 0, 3, 6, 10,and P54 to P57	–30	mA
		Total for all pins of ports 1, 4, 7, 9, P50 to P53, PWM0, PWM1, and $\overline{TX}$ pins	–30	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–40 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

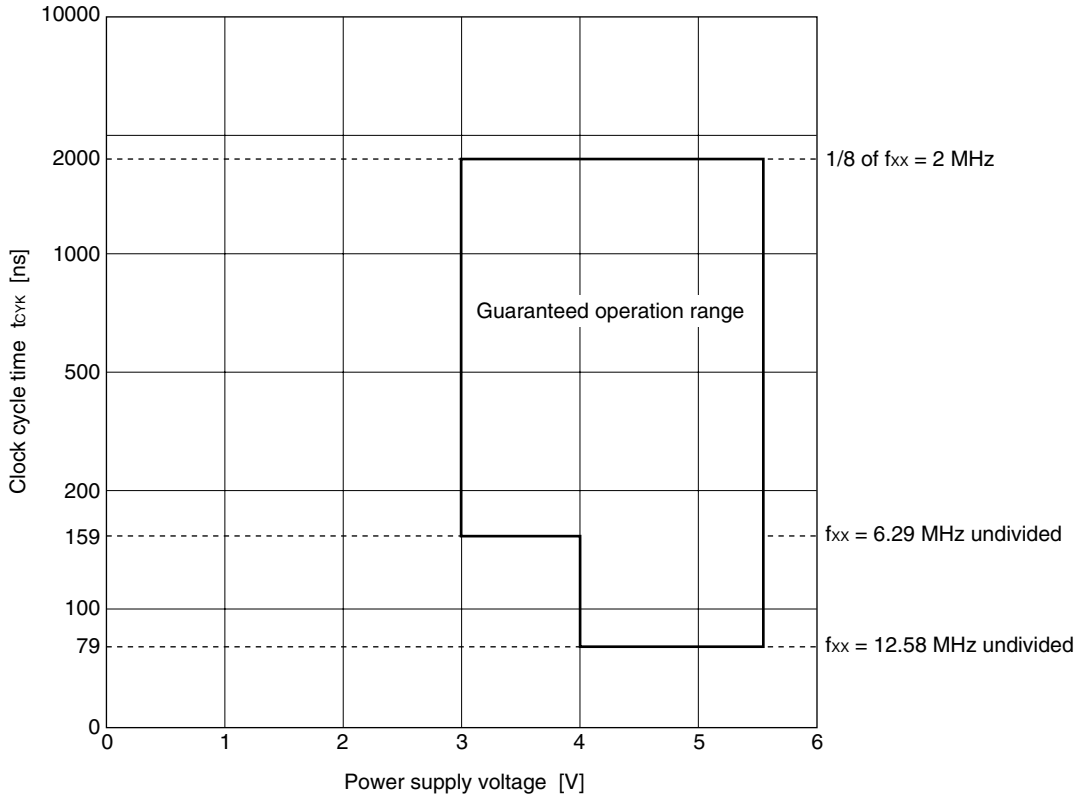
Operating Conditions

- Clock frequency

Clock Frequency	Supply Voltage
4 MHz ≤ f_{XX} ≤ 12.58 MHz	4.0 ≤ V_{DD} ≤ 5.5 V
4 MHz ≤ f_{XX} ≤ 6.29 MHz	3.0 ≤ V_{DD} ≤ 5.5 V

- Operating ambient temperature (T_A): –40 to +85°C
- Power supply voltage and clock cycle time: Refer to **Figure 7-1**
- Selection of internal regulator operation (REGOFF pin: low-level input)

Figure 7-1. Power Supply Voltage and Clock Cycle Time



Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

Main Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Oscillator frequency	f_{XX}	Ceramic resonator or recommended resonator	4.0 ≤ V_{DD} ≤ 5.5 V	4.0	12.58	MHz
			3.0 ≤ V_{DD} ≤ 5.5 V	4.0	6.29	MHz

Caution When using the main clock oscillator, wire as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remarks 1. Connect a 12.582912 MHz or 6.291456 MHz oscillator to operate the internal clock timer with the main clock.

2. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{XT}	Ceramic resonator or crystal resonator	32	32.768	35	kHz
Oscillation stabilization time	f_{sxt}	4.5 ≤ V_{DD} ≤ 5.5 V		1.2	2	s
					10	s
Oscillation hold voltage	V_{DDXT}		3.0		5.5	V
Watch timer operating voltage	V_{DDW}		3.0		5.5	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low[Note]	V_{IL1}	P10, P11, P13 to P17, P30, P31, P34 to P37, P70 to P77, P90 to P97, P100 to P104, X1, X2, XT1, XT2		–0.3		$0.3V_{DD}$	V
	V_{IL2}	P12, P20 to P27, P32, P33, P105 to P107 $\overline{RESET}$		–0.3		$0.2V_{DD}$	V
	V_{IL3}	P00 to P07, P40 to P47,	4.5 ≤ V_{DD} ≤ 5.5 V	–0.3		0.8	V
	V_{IL4}	P50 to P57, P60 to P67		–0.3		$0.2V_{DD}$	V
Input voltage, high	V_{IH1}	P10, P11, P13 to P17, P30, P31, P34 to P37, P70 to P77, P90 to P97, P100 to P104, X1, X2, XT1, XT2		$0.7V_{DD}$		V_{DD}+0.3	V
	V_{IH2}	P12, P20 to P27, P32, P33, P105 to P107 $\overline{RESET}$		$0.8V_{DD}$		V_{DD}+0.3	V
	V_{IH3}	P00 to P07, P40 to P47,	4.5 ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}+0.3	V
	V_{IH4}	P50 to P57, P60 to P67		$0.7V_{DD}$		$0.3V_{DD}$	V
Output voltage, low	V_{OL1}	I_{OL} = 20 μA				0.1	V
		I_{OL} = 100 μA				0.2	V
		I_{OL} = 2 mA				0.4	V
	V_{OL2}	I_{OL} = 8 mA, P10 to P17, P40 to P47, P50 to P57	4.5 ≤ V_{DD} ≤ 5.5 V			1.0	V
Output voltage, high	V_{OH1}	I_{OH} = –20 μA		V_{DD}–0.1			V
		I_{OL} = –100 μA		V_{DD}–0.2			V
		I_{OL} = –2 mA		V_{DD}–1.0			V
	V_{OH2}	I_{OL} = –5 mA, P10 to P17, P40 to P47, P50 to P57	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD}–2.4			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	For pins other than X1, X2, XT1, and XT2			10	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	For pins other than X1, X2, XT1, and XT2			10	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–10	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				10	μA

Note These values are valid when the pull-up resistor is off.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1}	Operating mode	f_{XX} = 12.58 MHz, 4.0 V ≤ V_{DD} ≤ 5.5 V		19	38	mA
			f_{XX} = 6.29 MHz, 3.0 V ≤ V_{DD} ≤ 5.5 V		10	20	mA
	I_{DD2}	HALT mode	f_{XX} = 12.58 MHz, when peripheral clock stops[Note], 4.0 V ≤ V_{DD} ≤ 5.5 V		3	6	mA
			f_{XX} = 6.29 MHz, when peripheral clock stops[Note], 3.0 V ≤ V_{DD} ≤ 5.5 V		1.8	3.6	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.58 MHz, 4.0 ≤ V_{DD} ≤ 5.5 V		2	4	mA
			f_{XX} = 6.29 MHz, 3.0 V ≤ V_{DD} ≤ 5.5 V		1	2	mA
Data hold voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data hold current	I_{DDDR}	STOP mode	V_{DD} = 2.5 V, subsystem clock stops		4	20	μA
			V_{DD} = 5.5 V, subsystem clock stops		20	100	μA
Pull-up resistor	R_L	V_{IN} = 0 V		15	40	80	kΩ

Note When the main system clock: f_{CLK} = f_{XX}/8 is selected (set by the standby control register (STBC)) and the watch timer is operating.

Remark These values are valid when the internal regulator is on (REGOFF pin = low-level input).

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYK}	4.0 ≤ V_{DD} ≤ 5.5 V	79			ns
		V_{DD} = 3.0 V	159			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5+a) T–11			ns
		V_{DD} = 3.0 V	(0.5+a) T–15			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T–19			ns
		V_{DD} = 3.0 V	0.5T–24			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5+a) T–17			ns
		V_{DD} = 3.0 V	(0.5+a) T–40			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay time from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V	(1+a) T–5			ns
		V_{DD} = 3.0 V	(1+a) T–10			ns
Address float time (from $\overline{RD}$↓)	t_{FAR}				0	ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V			(2.5+a+n) T–37	ns
		V_{DD} = 3.0 V			(2.5+a+n) T–52	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V			(2+n) T–35	ns
		V_{DD} = 3.0 V			(2+n) T–50	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V			(1.5+n) T–40	ns
		V_{DD} = 3.0 V			(1.5+n) T–50	ns
Delay time from ASTB ↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V	0.5T–2			ns
		V_{DD} = 3.0 V	0.5T–12			ns
Delay time from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5+n) T–25			ns
		V_{DD} = 3.0 V	(1.5+n) T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay time from address to $\overline{WR}\downarrow$	t_{DAW}	V_{DD} = 5.0 V	(1+a) T–5			ns
		V_{DD} = 3.0 V	(1+a) T–10			ns
Address hold time (from $\overline{WR}\uparrow$)	t_{HWA}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay time from ASTB ↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V			0.5T+15	ns
		V_{DD} = 3.0 V			0.5T+20	ns
Data output time from $\overline{WR}\downarrow$	t_{DWOD}				15	ns
Delay time from ASTB ↓ to $\overline{WR}\downarrow$	t_{DSTW}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Data setup time (to $\overline{WR}\uparrow$)	t_{SODWR}	V_{DD} = 5.0 V	(1.5+n) T–20			ns
		V_{DD} = 3.0 V	(1.5+n) T–25			ns
Data hold time (from $\overline{WR}\uparrow$)	t_{HWOD}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay time from $\overline{WR}$ ↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5+n) T–25			ns
		V_{DD} = 3.0 V	(1.5+n) T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(2) External wait timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{WAIT}$↓ input time from address	t_{DAWT}	V_{DD} = 5.0 V			(2+a) T–40	ns
		V_{DD} = 3.0 V			(2+a) T–60	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	V_{DD} = 5.0 V			1.5T–40	ns
		V_{DD} = 3.0 V			1.5T–60	ns
$\overline{WAIT}$ hold time from ASTB ↓	t_{HSTWTH}	V_{DD} = 5.0 V	(0.5+n) T+5			ns
		V_{DD} = 3.0 V	(0.5+n) T+10			ns
Delay time from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V			(1.5+a) T–40	ns
		V_{DD} = 3.0 V			(1.5+a) T–60	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	V_{DD} = 5.0 V			T–40	ns
		V_{DD} = 3.0 V			T–60	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓	t_{HRWT}	V_{DD} = 5.0 V	nT+5			ns
		V_{DD} = 3.0 V	nT+10			ns
Delay time from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V			(1+n) T–40	ns
		V_{DD} = 3.0 V			(1+n) T–60	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = 5.0 V			0.5T–5	ns
		V_{DD} = 3.0 V			0.5T–10	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	V_{DD} = 5.0 V			T–40	ns
		V_{DD} = 3.0 V			T–60	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	V_{DD} = 5.0 V	nT+5			ns
		V_{DD} = 3.0 V	nT+10			ns
Delay time from $\overline{WR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	V_{DD} = 5.0 V			(1+n) T–40	ns
		V_{DD} = 3.0 V			(1+n) T–60	ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(3) Bus hold/refresh timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay time from HLDRQ↑ to float	t_{FHQC}	V_{DD} = 5.0 V			(2+4+a+n) T+50	ns
		V_{DD} = 3.0 V			(2+4+a+n) T+50	ns
Delay time from HLDRQ↑ to HLDAK↑	$t_{DHQHHAH}$	V_{DD} = 5.0 V			(3+4+a+n) T+30	ns
		V_{DD} = 3.0 V			(3+4+a+n) T+40	ns
Delay time from float to HLDAK↑	t_{DCFHA}	V_{DD} = 5.0 V			T+30	ns
		V_{DD} = 3.0 V			T+30	ns
Delay time from HLDRQ↓ to HLDAK↓	$t_{DHQLHAL}$	V_{DD} = 5.0 V			2T+40	ns
		V_{DD} = 3.0 V			2T+60	ns
Delay time from HLDAK↓ to active	t_{DHAC}	V_{DD} = 5.0 V	T–20			ns
		V_{DD} = 3.0 V	T–30			ns
Random read/write cycle time	t_{RC}	V_{DD} = 5.0 V	3T			ns
		V_{DD} = 3.0 V	3T			ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = 5.0 V	1.5T–25			ns
		V_{DD} = 3.0 V	1.5T–30			ns
Delay time from ASTB↓ to $\overline{REFRQ}$	t_{DSTRFQ}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Delay time from RD↑ to $\overline{REFRQ}$	t_{DRRFQ}	V_{DD} = 5.0 V	1.5T–9			ns
		V_{DD} = 3.0 V	1.5T–9			ns
Delay time from WR↑ to $\overline{REFRQ}$	t_{DWRFQ}	V_{DD} = 5.0 V	1.5T–9			ns
		V_{DD} = 3.0 V	1.5T–9			ns
Delay time from $\overline{REFRQ}$↑ to ASTB	t_{DRFQST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = 5.0 V	1.5T–25			ns
		V_{DD} = 3.0 V	1.5T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock)

2. a: 1 during address wait; otherwise 0

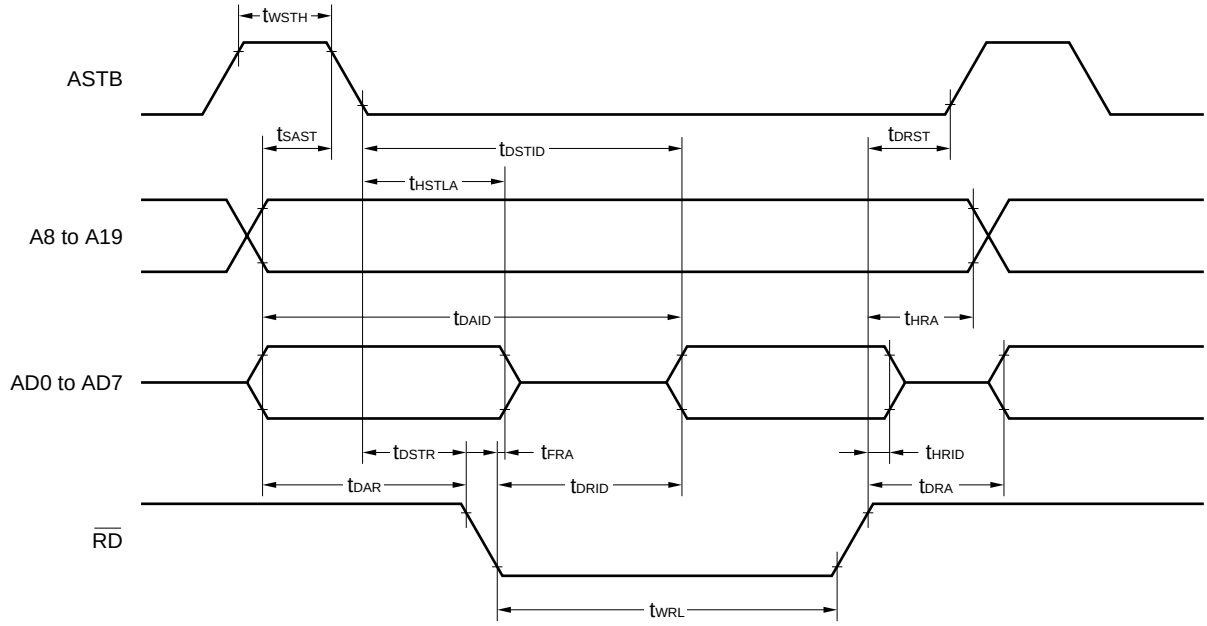
3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

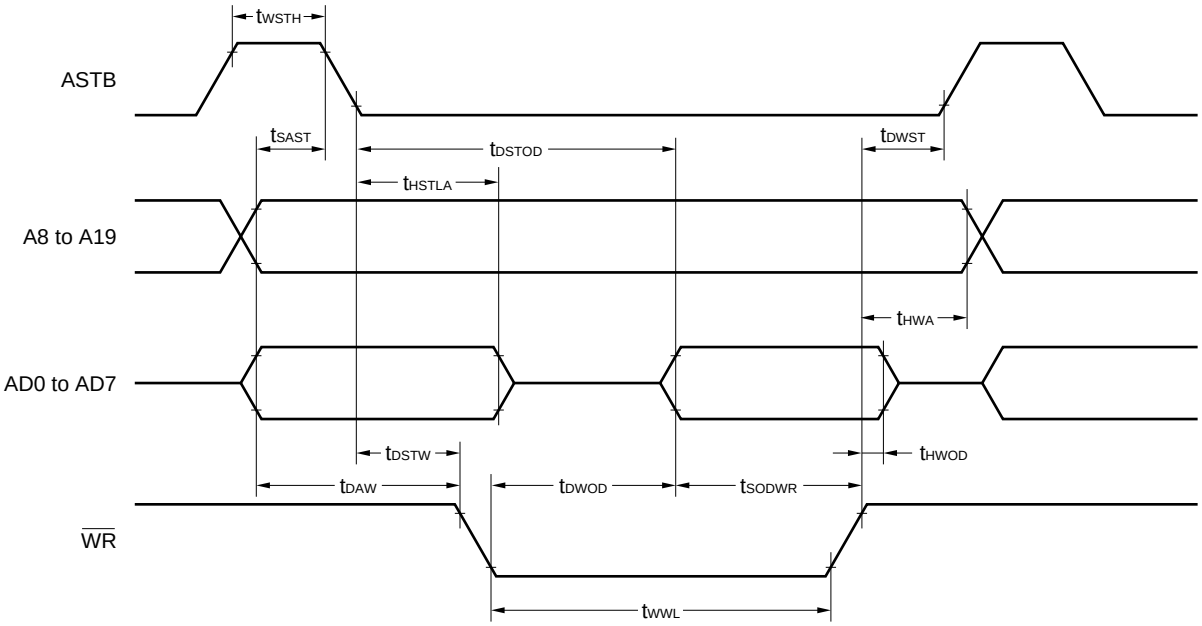
5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

Timing Waveform

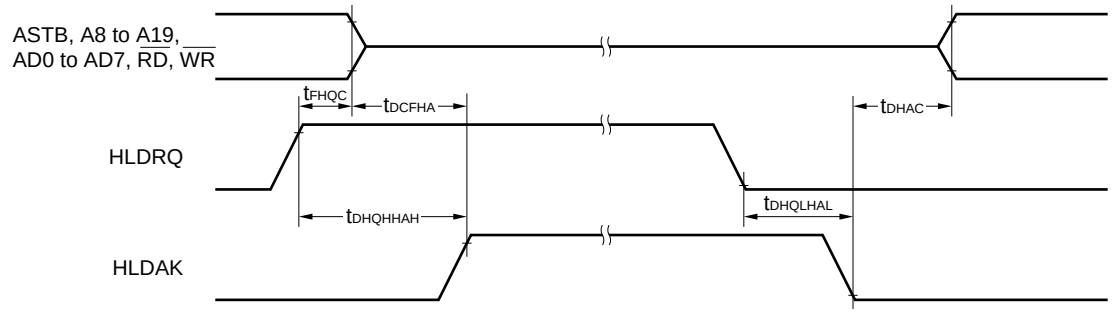
(1) Read operation



(2) Write operation

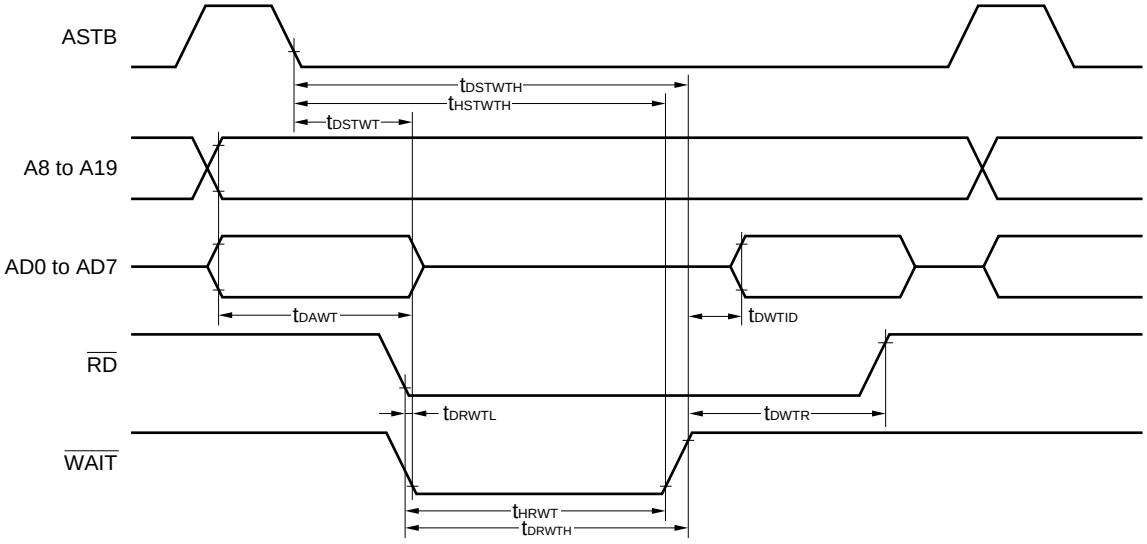


Hold Timing

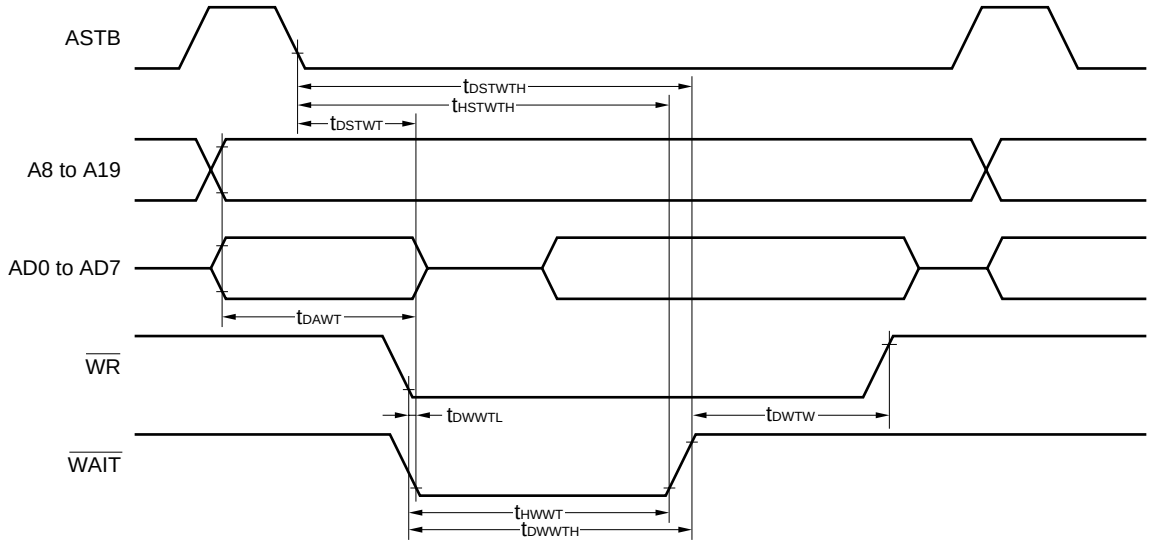


External Wait Signal Input Timing

(1) Read operation

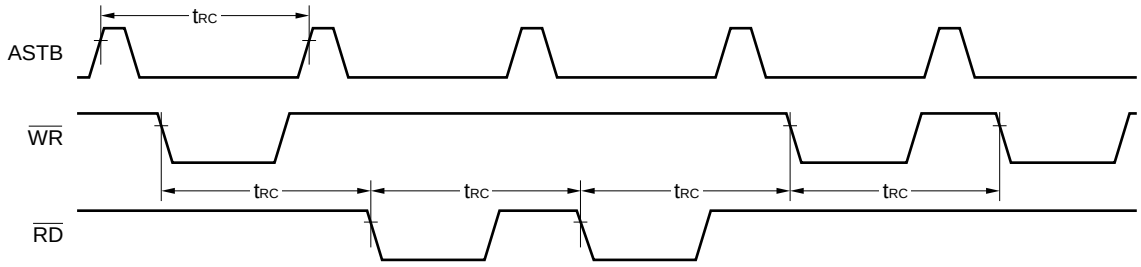


(2) Write operation

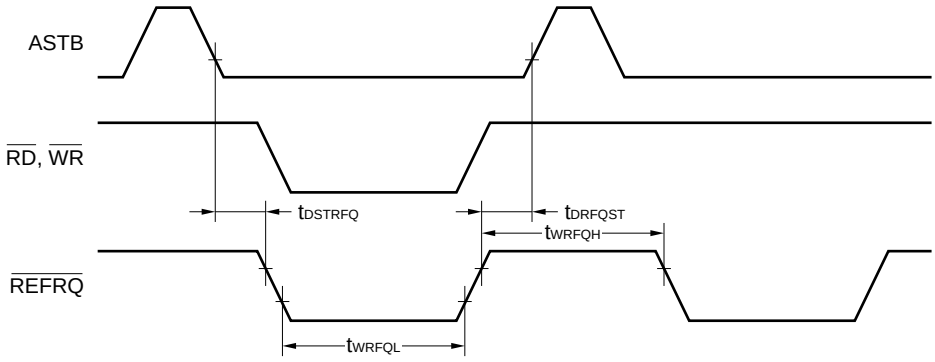


Refresh Timing Waveform

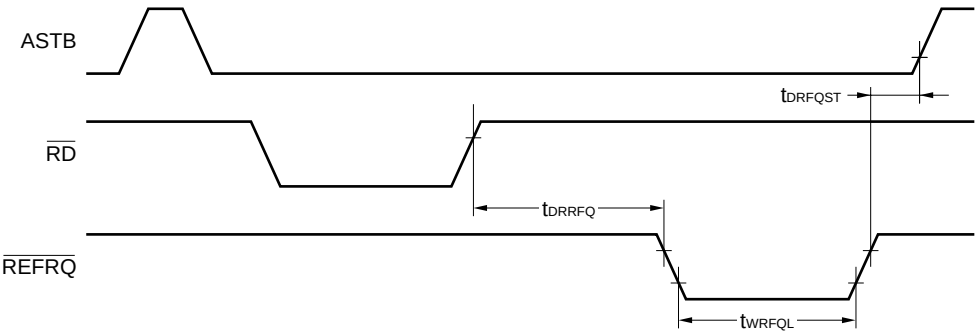
(1) Random read/write cycle



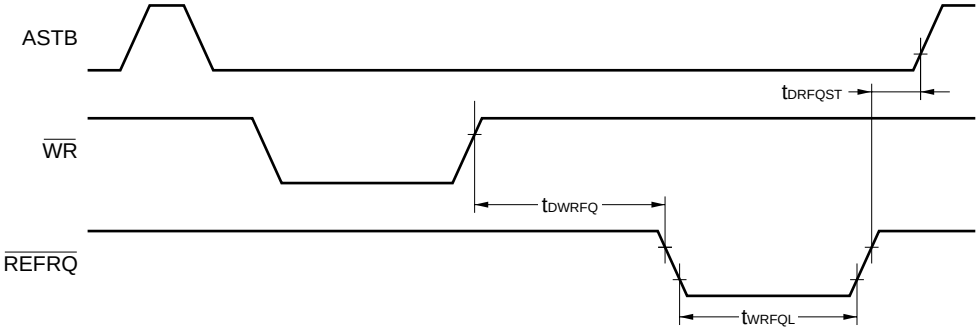
(2) When refresh memory is accessed for a read and write at the same time



(3) Refresh after a read



(4) Refresh after a write



Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) CSI0, CSI3 3-wire serial I/O mode ($\overline{SCK0}$, $\overline{SCK3}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}, t_{CYSK3}	SO0 and SO3 are CMOS outputs	$f_{CLK} = f_{XX}$	8/f_{XX}		ns
			Except $f_{CLK} = f_{XX}$	4/f_{CLK}		ns
$\overline{SCK}$ low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}, t_{WSKL3}	SO0 and SO3 are CMOS outputs	$f_{CLK} = f_{XX}$	4/f_{XX} – 40		ns
			Except $f_{CLK} = f_{XX}$	2/f_{CLK} – 40		ns
$\overline{SCK}$ high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}, t_{WSKH3}	SO0 and SO3 are CMOS outputs	$f_{CLK} = f_{XX}$	4/f_{XX} – 40		ns
			Except $f_{CLK} = f_{XX}$	2/f_{CLK} – 40		ns
SI0, SI3 setup time (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}, t_{SSSK3}			80		ns
SI0, SI3 hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}, t_{HSSK3}			1/f_{CLK} + 80		ns
Delay time from $\overline{SCK0}$, $\overline{SCK3}$↓ to output	t_{DBSK0}, t_{DBSK3}	CMOS output		0	1/f_{CLK} + 150	ns
		N-ch open-drain output (R_L = 1 kΩ)		0	1/f_{CLK} + 400	ns
SO0, SO3 output hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK0}, t_{HSBSK3}	When data is transferred		0.5t_{CYSK0} – 40, 0.5t_{CYSK3} – 40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. f_{XX}: External oscillator frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

3. f_{CLK}: System clock oscillation frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

(b) CSI0, CSI3 3-wire serial I/O mode ($\overline{SCK0}$, $\overline{SCK3}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}, t_{CYSK3}	SO0 and SO3 are CMOS outputs	Except $f_{CLK} = f_{XX}$/8	8/f_{XX}		ns
			$f_{CLK} = f_{XX}$/8	16/f_{XX}		ns
$\overline{SCK}$ low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}, t_{WSKL3}	SO0 and SO3 are CMOS outputs	Except $f_{CLK} = f_{XX}$/8	4/f_{XX} – 40		ns
			$f_{CLK} = f_{XX}$/8	8/f_{XX} – 40		ns
$\overline{SCK}$ high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}, t_{WSKH3}	SO0 and SO3 are CMOS outputs	Except $f_{CLK} = f_{XX}$/8	4/f_{XX} – 40		ns
			$f_{CLK} = f_{XX}$/8	8/f_{XX} – 40		ns
SI0, SI3 setup time (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}, t_{SSSK3}			80		ns
SI0, SI3 hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}, t_{HSSK3}			80		ns
Delay time from $\overline{SCK0}$, $\overline{SCK3}$↓ to output	t_{DBSK0}, t_{DBSK3}	CMOS output		0	150	ns
		N-ch open-drain output (R_L = 1 kΩ)		0	400	ns
SO0, SO3 output hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK0}, t_{HSBSK3}	When data is transferred		0.5t_{CYSK0} – 40, 0.5t_{CYSK3} – 40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. f_{XX}: External oscillator frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

3. f_{CLK}: System clock oscillation frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(c) UART0, UART3 (Asynchronous serial interface mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0, ASCK2 cycle time	t_{CYASK}	4.0 ≤ V_{DD} ≤ 5.5 V	160			ns
			320			ns
ASCK0, ASCK2 low-level width	t_{WASKL}	4.0 ≤ V_{DD} ≤ 5.5 V	65			ns
			120			ns
ASCK0, ASCK2 high-level width	t_{WASKH}	4.0 ≤ V_{DD} ≤ 5.5 V	65			ns
			120			ns

Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(d) IOE1, IOE2 3-wire serial I/O mode ($\overline{SCK1}$, $\overline{SCK2}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	4.0 ≤ V_{DD} ≤ 5.5 V	640		ns
	t_{CYSK2}		1280		ns
$\overline{SCK}$ low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1},	4.0 ≤ V_{DD} ≤ 5.5 V	280		ns
	t_{WSKL2}		600		ns
$\overline{SCK}$ high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1},	4.0 ≤ V_{DD} ≤ 5.5 V	280		ns
	t_{WSKH2}		600		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}, t_{SSSK2}		40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}, t_{HSSK2}		40		ns
Delay time from $\overline{SCK1}$, $\overline{SCK2}$↓ to output	t_{DSOSK1}, t_{DSOSK2}		0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK1}, t_{HSOSK2}	When data is transferred	$0.5t_{CYSK1}$ – 40, $0.5t_{CYSK2}$ – 40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. T: Selected serial clock cycle. The minimum value is 8/fxx.

(e) IOE1, IOE2 3-wire serial I/O mode ($\overline{SCK1}$, $\overline{SCK2}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1} t_{CYSK2}		T		ns
$\overline{SCK}$ low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}, t_{WSKL2}		0.5T – 40		ns
$\overline{SCK}$ high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}, t_{WSKH2}		0.5T – 40		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}, t_{SSSK2}		40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}, t_{HSSK2}		40		ns
Delay time from $\overline{SCK1}$, $\overline{SCK2}$↓ to output	t_{DSOSK1}, t_{DSOSK2}		0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK1}, t_{HSOSK2}	When data is transferred	$0.5t_{CYSK1}$ – 40, $0.5t_{CYSK2}$ – 40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. T: Selected serial clock cycle. The minimum value is 8/fxx.

Other Operations (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
INTP0 high-/low-level width	t_{WIT0L} t_{WIT0H}		$4t_{CYSMP}$			s
INTP1 to INTP3, CI high-/low-level width	t_{WIT1L} t_{WIT1H}		$4t_{CYCPU}$			s
INTP4, INTP5 high-/low-level width	t_{WIT2L} t_{WIT2H}		10			μs
$\overline{\text{RESET}}$ high-/low-level width[Note]	t_{WRSL} t_{WRSH}		10			μs

Note When the power is turned on or when STOP mode is released by reset, secure the oscillation stabilization wait time while the $\overline{\text{RESET}}$ is at a low-level width.
When the power is applied, be sure to activate V_{DD} in the $\overline{\text{RESET}}$ = low-level state.

Remark t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU clock set by software in the CPU

Clock Output Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle time	t_{CYCL}	nT	79		32000	ns
CLKOUT low-level width	t_{CLL}	$4.5 \le V_{DD} \le 5.5$ V	0.5T – 10			ns
			0.5T – 20			ns
CLKOUT high-level width	t_{CLH}	$4.5 \le V_{DD} \le 5.5$ V	0.5T – 10			ns
			0.5T – 20			ns
CLKOUT rise time	t_{CLR}	$4.5 \le V_{DD} \le 5.5$ V			10	ns
		$3.0 \le V_{DD} \le 4.5$ V			20	ns
CLKOUT fall time	t_{CLF}	$4.5 \le V_{DD} \le 5.5$ V			10	ns
		$3.0 \le V_{DD} \le 4.5$ V			20	ns

Remark n: Division ratio of clock output frequency, T: $t_{CYK} = 1/f_{CLK}$ (system clock cycle time)

IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_s	Mode 1		6.29		MHz

Remark Although the system clock frequency in the IEBus specifications is 6.0 MHz, in the μPD784938A, operation at 6.29 MHz is also guaranteed. Note, however, that operation at 6.0 MHz and 6.29 MHz cannot be used together.

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

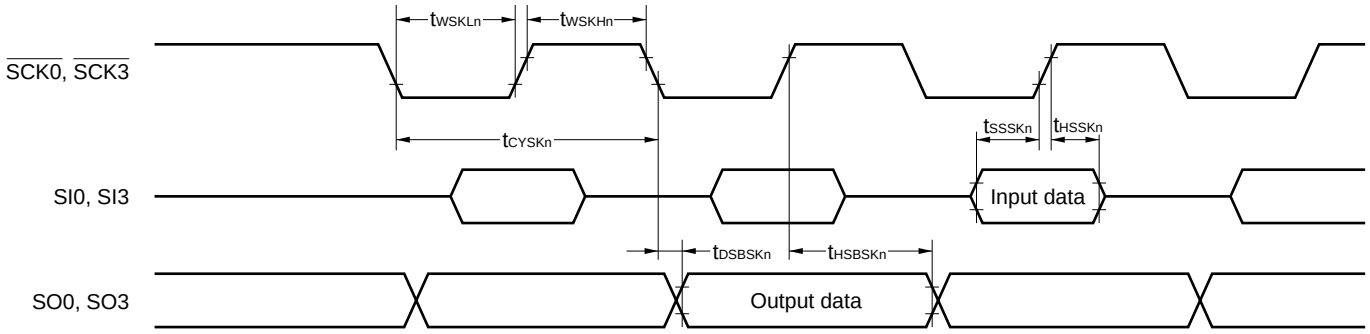
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Overall error[Note 1]		IEAD = 00H	6.29 MHz ≤ f_{XX} ≤ 12.58 MHz and other than FR = 1			±0.6	%FSR[Note 2]
			6.29 MHz ≤ f_{XX} ≤ 12.58 MHz and FR = 1			±1.5	%FSR[Note 2]
		IEAD = 01H	4.5 ≤ V_{DD} ≤ 5.5 V		±1	±2.2	%FSR[Note 2]
			3.0 ≤ V_{DD} < 5.5 V		±1.4	±2.6	%FSR[Note 2]
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	FR = 1: 120t_{CYK}		9.5		480	μs
		FR = 0: 240t_{CYK}		19.1		960	μs
Sampling time	t_{SAMP}	FR = 1: 18t_{CYK}		1.4		72	μs
		FR = 0: 36t_{CYK}		2.9		144	μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF1}	V
Analog input impedance	R_{AN}				1000		MΩ
Reference voltage	AV_{REF1}			3.0		AV_{DD}	V
AV_{REF1} resistor	R_{AVREF1}			3.0	10		kΩ
AV_{REF1} current	AI_{REF1}				0.5	1.5	mA
AV_{DD} current	AI_{DD1}				2.0	5.0	mA
	AI_{DD2}					20	mA

Notes 1. Excludes quantization error (±1/2 LSB).

2. It is indicated as a ratio (%FSR) to the full-scale value.

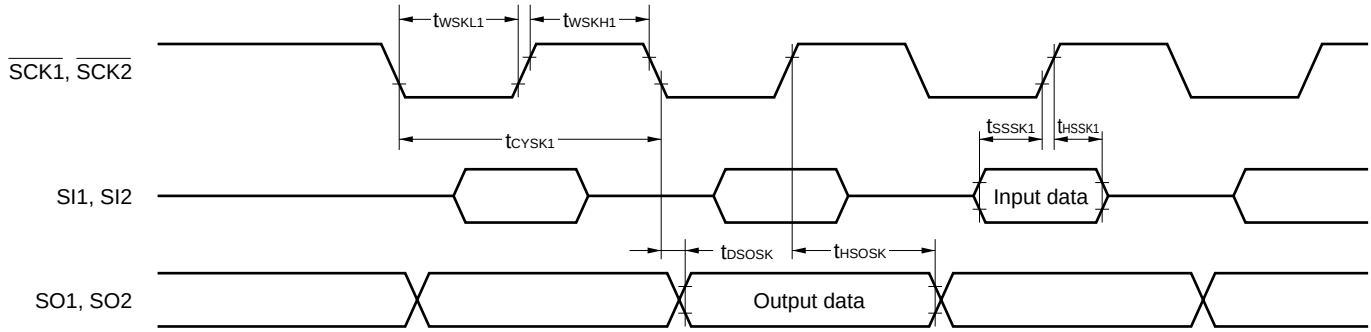
Caution The analog input pins of the μPD78F4938A function alternately as the port 7 pins (I/O port pins). However when using the A/D converter, it is necessary to set all the pins of port 7 to input mode in order to prevent data from being inverted by the output port operation, thus degrading the A/D conversion accuracy. At this time, pins cannot be used as output ports even though they are not used as A/D analog input port.

Serial Operation (CSI, CSI3)

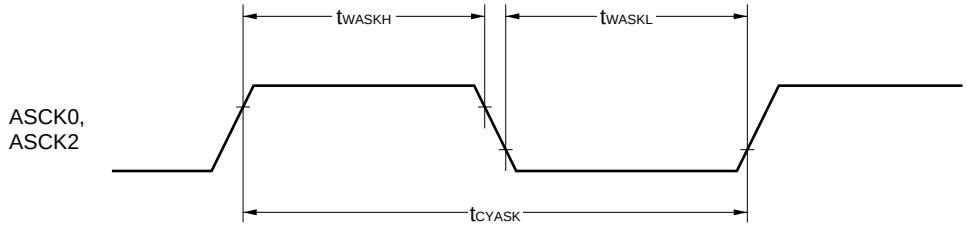


n = 0, 3

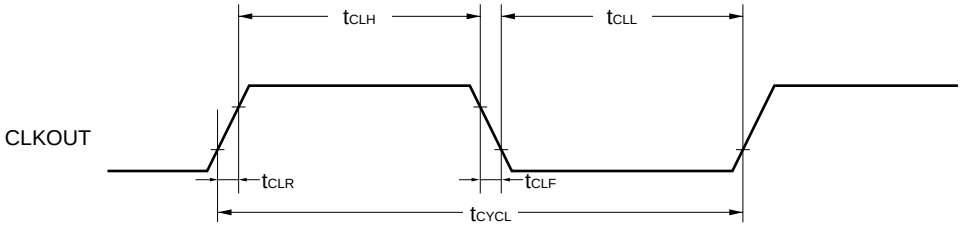
Serial Operation (IOE1, IOE2)



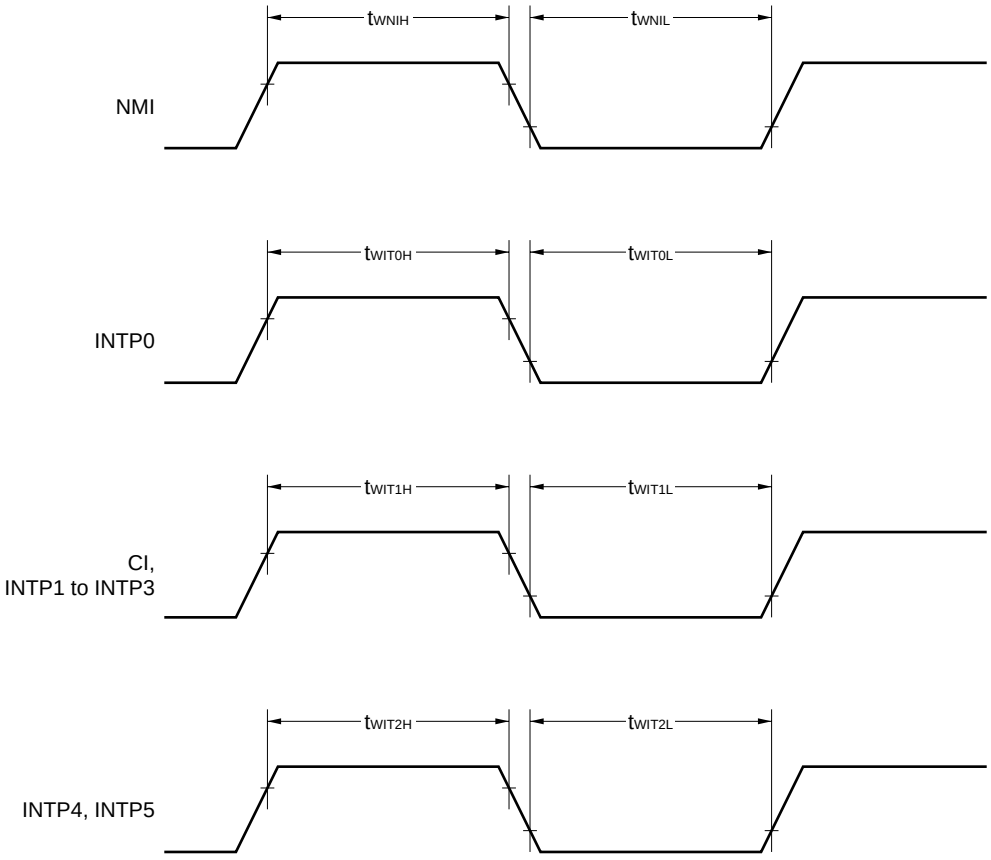
Serial Operation (UART0, UART2)



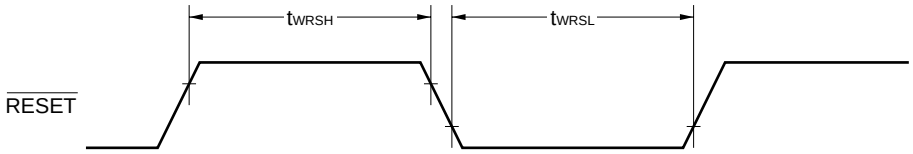
Clock Output Timing



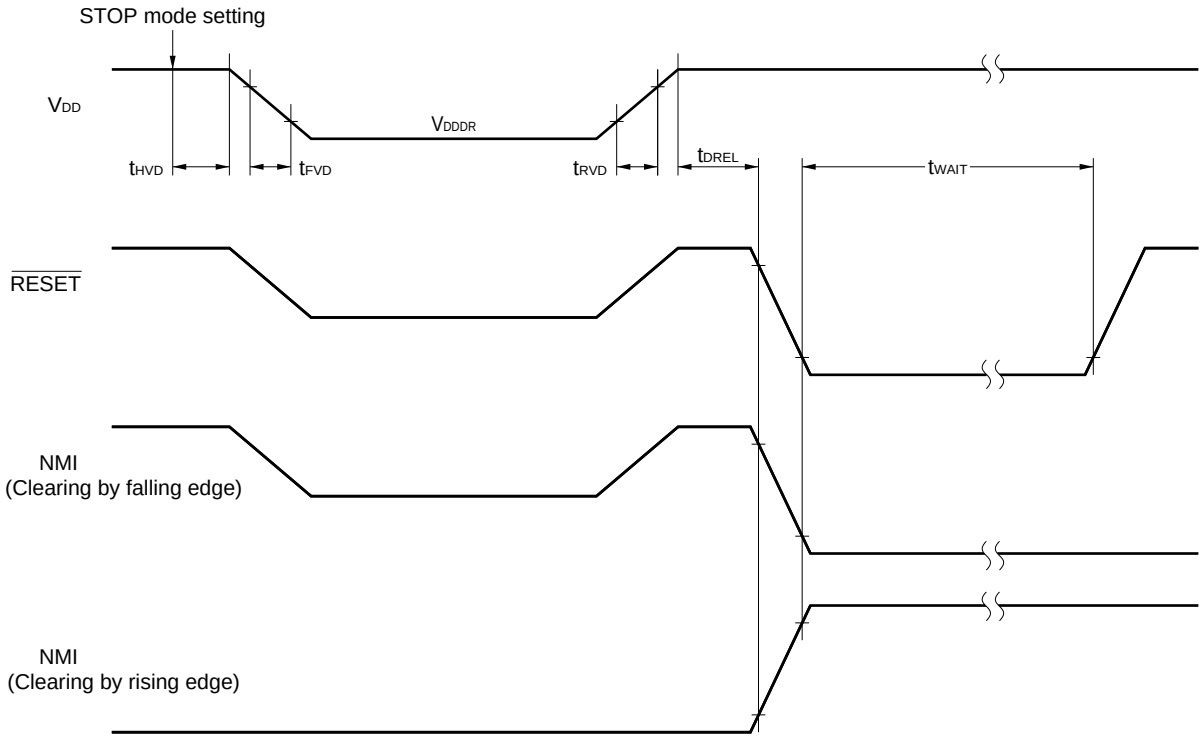
Interrupt Request Input Timing



Reset Input Timing

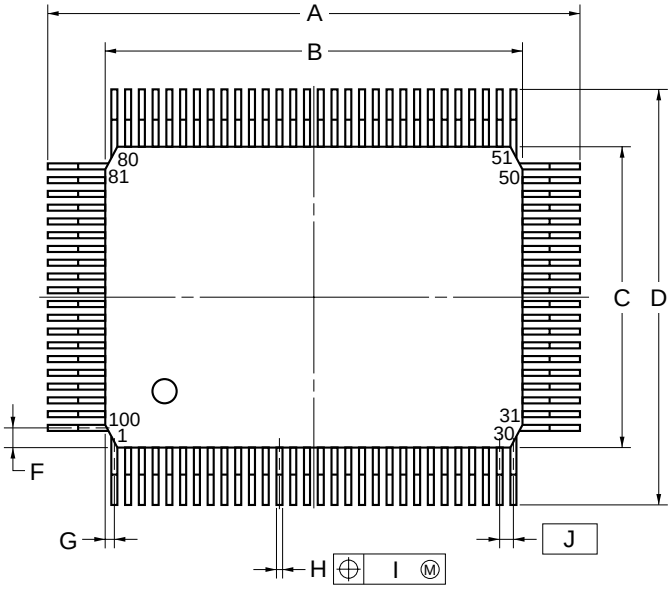


Data Retention Characteristics

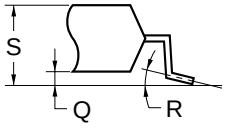


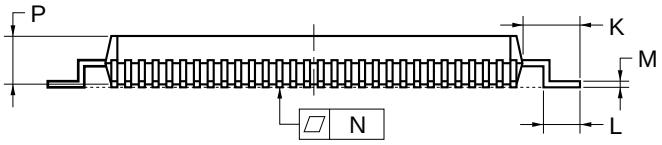
8. PACKAGE DRAWING

100PIN PLASTIC QFP (14x20)



detail of lead end





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F4938A should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 9-1. Surface Mounting Type Soldering Conditions

μPD78F4938AGF-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	VP15-207-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 20 hours)	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4938A.
Also refer to **(5) Cautions on using development tools**.

(1) Language processing software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash memory writing tools

Flashpro III (PG-FP3)	Flash programmer for microcontroller with on-chip flash memory
FA-100GF	Flash memory writing adapter for 100-pin plastic QFP (GF-3BA type). Wiring must be performed according to the product used.

(3) Debugging tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine
IE-70000-CD-IF-C	PC card and cable used when PC-9800 series notebook type PC is used as host machine
IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT™ or compatible is used as host machine
IE-784937-NS-EM1	Emulation board to emulate μPD784938A Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries

- **When IE-784000-R in-circuit emulator is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-B IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine
IE-70000-98N-IF	Interface adapter and cable used when PC-9800 series notebook type PC is used as host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT or compatible is used as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784937-NS-EM1	Emulation board to emulate μPD784938A Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX2	Emulation probe conversion board necessary when using IE-784937-NS-EM1 on IE-784000-R. Not necessary when using IE-784937-R-EM1
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on using development tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784937.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 or DF784937.
- The Flashpro III, FA-100GF, and NP-100GF are products made by Naito Densei Machida Mfg. Co, Ltd (TEL +81-44-822-3813).
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√ Note	√
CC78K4	√ Note	√
ID78K4-NS	√	—
ID78K4	√	√
SM78K4	√	—
RX78K/IV	√ Note	√
MX78K4	√ Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- **Documents related to devices**

Document Name	Document No.
μPD784935A, 784936A, 784937A, 784938A Data Sheet	Under preparation
μPD78F4938A Data Sheet	This document
μPD784938 Subseries User's Manual Hardware	U13987E
78K/IV Series User's Manual Instructions	U10905E
78K/IV Series Application Note Software Basics	U10095E

- **Documents related to development tools (user's manuals)**

Document Name		Document No.
RA78K4 Assembler Package	Language	U11162E
	Operation	U11334E
	Structured Assembler Preprocessor	U11743E
CC78K4 C Compiler	Language	U11571E
	Operation	U11572E
PG-FP3 Flash Memory Programmer		U13502E
IE-78K4-NS		U13556E
IE-784000-R		U12903E
IE-784937-R-EM1		To be prepared
IE-784937-NS-EM1		To be prepared
EP-78064		EEU-1469
SM78K4 System Simulator Windows Based	Reference	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
ID78K4 Integrated Debugger Windows Based	Reference	U10440E
ID78K4-NS Integrated Debugger Windows Based	Reference	U12796E
Project Manager Ver. 3.12 or Later Windows Based		U14610E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

- **Documents related to embedded software (user's manuals)**

Document Name		Document No.
78K/IV Series Real-Time OS	Fundamental	U10603E
	Installation	U10604E

- **Other documents**

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	U10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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