



## UT12N10

Preliminary

Power MOSFET

### 12 Amps, 100 Volts N-CHANNEL POWER MOSFET

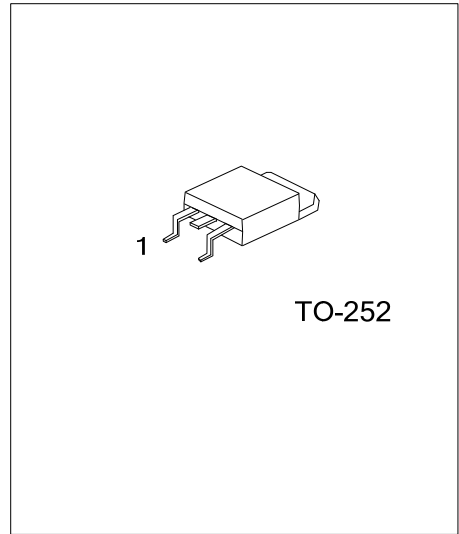
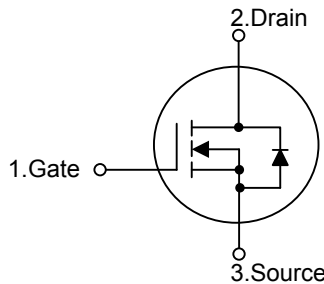
#### DESCRIPTION

The UTC **UT12N10** is an N-channel mode Power FET using UTC's advanced technology to provide customers with minimum on-state resistance by extremely high dense cell design. Moreover, it's good at handling high power and current.

#### FEATURES

- \* 100V, 12A,  $R_{DS(ON)} = 180m\Omega @ V_{GS} = 10V$ .
- \* Be good at handling high power and current.
- \* Very high dense cell design for super low  $R_{DS(ON)}$ .
- \* Lead free product is acquired.

#### SYMBOL



#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT12N10L-TN3-R	UT12N10G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>UT12N10L-TN3-R</p>	<p>(1) Packing Type (1) R: Tape Reel</p> <p>(2) Package Type (2) TN3: TO-252</p> <p>(3) Lead Free (3) G: Halogen Free, L: Lead Free</p>
-----------------------	---

■ ABSOLUTE MAXIMUM RATINGS ( $T_C=25^{\circ}\text{C}$ , unless otherwise noted)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DSS}$	100	V
Gate-Source Voltage		$V_{GSS}$	$\pm 20$	V
Drain Current	Continuous	$I_D$	12	A
	Pulsed (Note 1)	$I_{DM}$	44	A
Power Dissipation		$P_D$	43	W/ $^{\circ}\text{C}$
Junction Temperature		$T_J$	+150	$^{\circ}\text{C}$
Storage Temperature		$T_{STG}$	-55~+150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Note:1 Repetitive Rating: Pulse width limited by maximum junction temperature

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient (Note 2)	$\theta_{JA}$	50	$^{\circ}\text{C}/\text{W}$
Junction to Case	$\theta_{JC}$	3.5	$^{\circ}\text{C}/\text{W}$

Note:  $\theta_{JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$\theta_{JC}$  is guaranteed by design while  $\theta_{JA}$  is determined by the user's board design.

Note:2 When mounted on a 1 in<sup>2</sup> pad of 2 oz copper

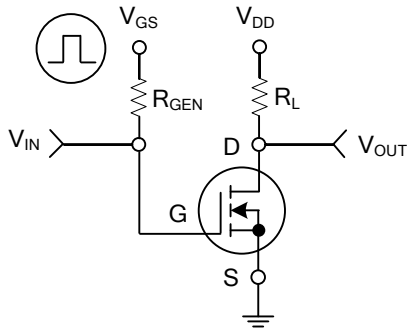
■ ELECTRICAL CHARACTERISTICS (T<sub>c</sub>=25°C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	100			V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V			1	μA
Gate- Source Leakage Current	Forward	V <sub>GS</sub> =+20V, V <sub>DS</sub> =0V			+100	nA
	Reverse	V <sub>GS</sub> =-20V, V <sub>DS</sub> =0V			-100	nA
<b>ON CHARACTERISTICS (Note 1)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2		4	V
Static Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =6A		150	180	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =6A		5		S
<b>DYNAMIC PARAMETERS (Note 2)</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1.0MHz		430		pF
Output Capacitance	C <sub>OSS</sub>			90		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			20		pF
<b>SWITCHING PARAMETERS (Note 2)</b>						
Total Gate Charge	Q <sub>G</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =80V, I <sub>D</sub> =12A		8	16	nC
Gate to Source Charge	Q <sub>GS</sub>			1.5		nC
Gate to Drain Charge	Q <sub>GD</sub>			2		nC
Turn-ON Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =80V, I <sub>D</sub> =12A, V <sub>GS</sub> =10V, R <sub>G</sub> =9.1Ω		12	24	ns
Rise Time	t <sub>R</sub>			7	14	ns
Turn-OFF Delay Time	t <sub>D(OFF)</sub>			18	35	ns
Fall-Time	t <sub>F</sub>			3	6	ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Maximum Body-Diode Continuous Current	I <sub>S</sub>				12	A
Drain-Source Diode Forward Voltage (Note 1)	V <sub>SD</sub>	I <sub>S</sub> =12A, V <sub>GS</sub> =0V			1.2	V

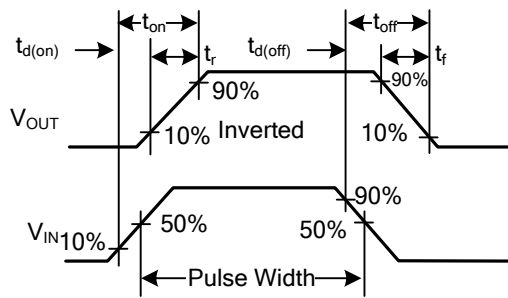
Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Guaranteed by design, not subject to production testing.

■ TEST CIRCUITS AND WAVEFORMS



Switching Test Circuit



Switching Waveforms

UTC assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all UTC products described or contained herein. UTC products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice.