



UT134E

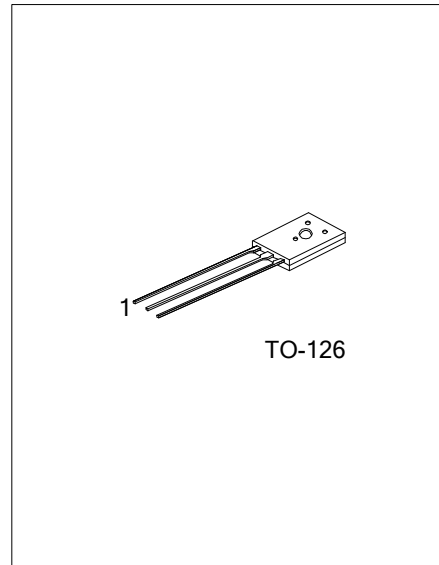
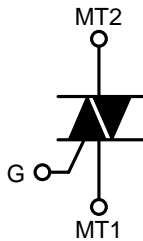
TRIAC

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DESCRIPTION

Glass passivated, sensitive gate triac in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL

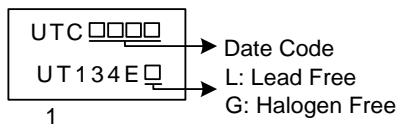


ORDERING INFORMATION

Order Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT134EL-x-T60-K	UT134EG-x-T60-K	TO-126	MT1	MT2	GATE	Bulk

<p>UT134EG-x-T60-K</p> <ul style="list-style-type: none"> (1) Packing Type (2) Package Type (3) Peak Voltage (4) Green Package 	<ul style="list-style-type: none"> (1) K: Bulk (2) T60: TO-126 (3) 5: 500V, 6: 600V, 8: 800V (4) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages	UT134E-5	V_{DRM}	500	V
	UT134E-6		600	
	UT134E-8		800	
RMS on-state current full sine wave; $T_{mb} \leq 107^{\circ}\text{C}$		$I_{T(RMS)}$	4	A
Non-repetitive peak on-state current (Full sine wave; $T_J = 25^{\circ}\text{C}$ prior to surge)	$t = 20\text{ms}$	I_{TSM}	25	A
	$t = 16.7\text{ms}$		27	
I^2t for fusing	$t = 10\text{ms}$	I^2t	3.1	A^2s
Repetitive rate of rise of on-state current after triggering $I_{TM} = 6\text{A}; I_G = 0.2\text{A}; dI_G/dt = 0.2\text{A}/\mu\text{s}$	T2+ G+	di_T/dt	50	$\text{A}/\mu\text{s}$
	T2+ G-		50	$\text{A}/\mu\text{s}$
	T2- G-		50	$\text{A}/\mu\text{s}$
	T2- G+		10	$\text{A}/\mu\text{s}$
Peak gate voltage		V_{GM}	5	V
Peak gate current		I_{GM}	2	A
Peak gate power		P_{GM}	5	W
Average gate power (over any 20 ms period)		$P_{G(AV)}$	0.5	W
Junction Temperature		T_J	125	$^{\circ}\text{C}$
Operating Temperature		T_{OPR}	-20 ~ +85	$^{\circ}\text{C}$
Storage Temperature		T_{STG}	-40 ~ +150	$^{\circ}\text{C}$

- Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The device is guaranteed to meet performance specification within $0^{\circ}\text{C} \sim 70^{\circ}\text{C}$ operating temperature range and assured by design from $-20^{\circ}\text{C} \sim 85^{\circ}\text{C}$.
3. Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed $3\text{A}/\mu\text{s}$.

■ THERMAL RESISTANCES

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to Ambient (In free air)		θ_{JA}		100		$^{\circ}\text{C}/\text{W}$
Thermal resistance Junction to mounting base	Full cycle	θ_{JC}			3.0	$^{\circ}\text{C}/\text{W}$
	Half cycle				3.7	$^{\circ}\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ($T_J=25^{\circ}\text{C}$, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Gate trigger current	I_{GT}	$V_D = 12\text{V}; I_T = 0.1\text{A}$	T2+G+		2.5	10	mA
			T2+G-		4.0	10	mA
			T2-G-		5.0	10	mA
			T2-G+		11	25	mA
Latching current	I_L	$V_D = 12\text{V}; I_{GT} = 0.1\text{A}$	T2+G+		3.0	15	mA
			T2+G-		10	20	mA
			T2-G-		2.5	15	mA
			T2-G+		4.0	20	mA
Holding current	I_H	$V_D = 12\text{V}; I_{GT} = 0.1\text{A}$		2.2	15	mA	
On-state voltage	V_T	$I_T = 5\text{A}$		1.4	1.7	V	
Gate trigger voltage	V_{GT}	$V_D = 12\text{V}; I_T = 0.1\text{A}$		0.7	1.5	V	
		$V_D = 400\text{V}; I_T = 0.1\text{A}; T_J = 125^{\circ}\text{C}$	0.25	0.4		V	
Off-state leakage current	I_D	$V_D = V_{DRM(max)}; T_J = 125^{\circ}\text{C}$		0.1	0.5	mA	

■ **DYNAMIC CHARACTERISTICS** ($T_J=25^{\circ}\text{C}$, unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of Off-state voltage	dV_D/dt	$V_{DM} = 67\% V_{DRM(max)}$; $T_J=125^{\circ}\text{C}$; exponential waveform; gate open circuit		50		V/ μs
Gate controlled turn-on time	t_{GT}	$I_{TM} = 6\text{A}$; $V_D=V_{DRM(max)}$; $I_G=0.1\text{A}$; $dI_G/dt=5\text{A}/\mu\text{s}$		2		μs

■ TYPICAL CHARACTERISTICS

Fig 1. Maximum On-State Dissipation, P_{tot} Versus Rms On-state Current, $I_{T(RMS)}$ where α =conduction angle.

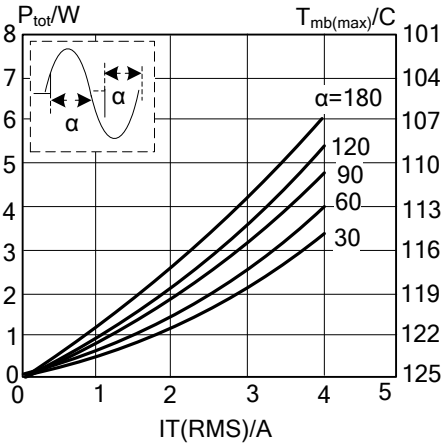


Fig 2. Maximum Permissible Non-repetitive Peak On-state Current, I_{TSM} , Versus Pulse Width t_p For Sinusoidal Currents, $t_p \leq 20ms$

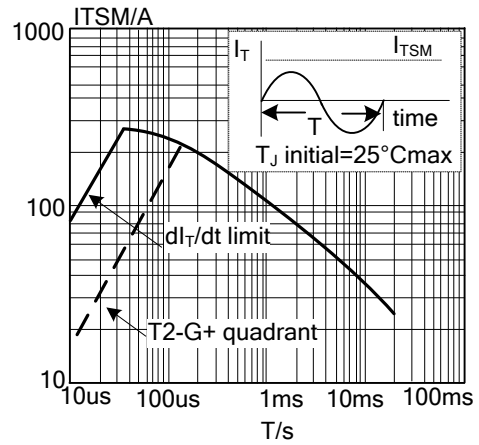


Fig 3. Maximum Permissible Non-repetitive Peak On-state Current, I_{TSM} , Versus Number Of Cycles, For Sinusoidal Currents, $f=50Hz$.

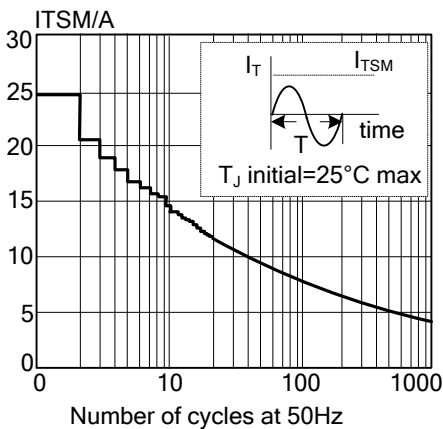


Fig 4. Maximum Permissible Rms Current, $I_{T(RMS)}$ Versus Mounting Base Temperature, T_{mb}

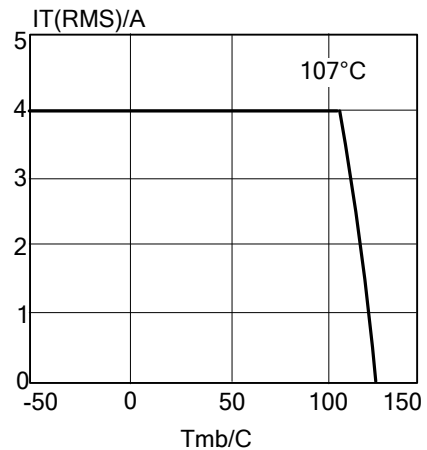


Fig 5. Maximum Permissible Repetitive Rms On-State Current, $I_{T(RMS)}$, Versus Surge Duration, For Sinusoidal Currents, $f=50HZ$, $T_{mb} \leq 107^\circ C$

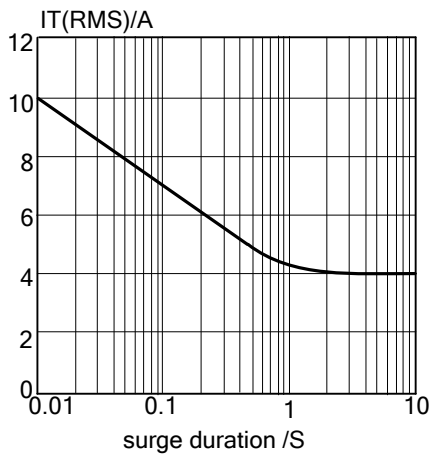
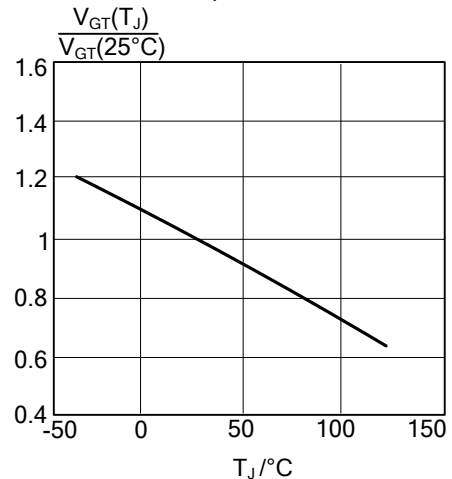


Fig 6. Normalised Gate Trigger Voltage, $V_{GT}(T_J)/V_{GT}(25^\circ C)$, Versus Junction Temperature, T_J



■ TYPICAL CHARACTERISTICS (Cont.)

Fig 7. Normalised Gate Trigger Current, $I_{GT}(T_J)/I_{GT}(25^\circ\text{C})$, Versus Junction Temperature, T_J

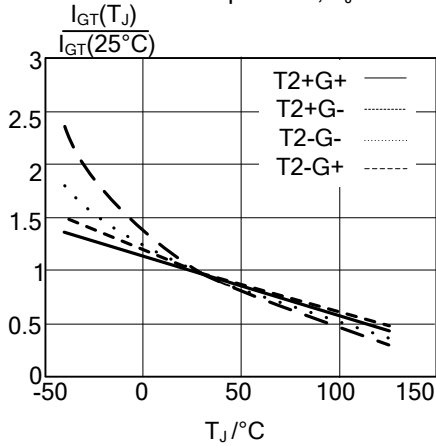


Fig 8. Normalised Latching Current, $I_L(T_J)/I_L(25^\circ\text{C})$ Versus Junction Temperature, T_J

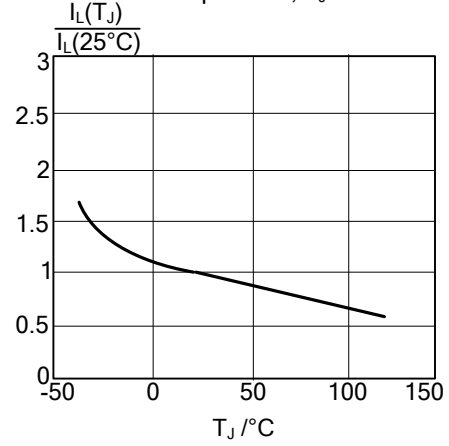


Fig 9. Normalised Holding Current, $I_H(T_J)/I_H(25^\circ\text{C})$, versus junction temperature, T_J

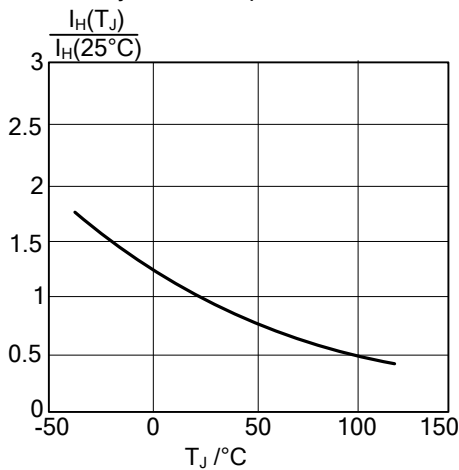


Fig 10. Typical And Maximum On-state Characteristic

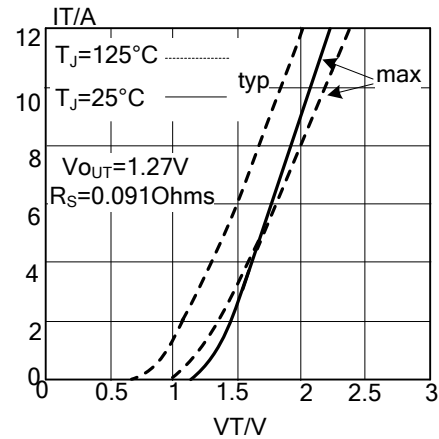


Fig 11. Transient Thermal Impedance Z_{thj-mb} , Versus Pulse Width tp

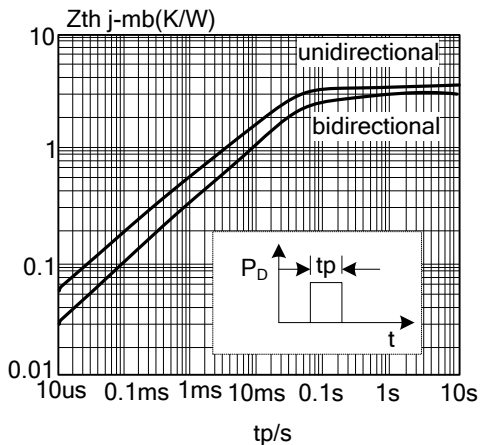
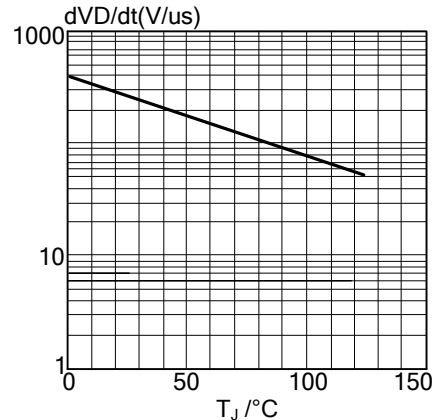


Fig 12. Typical Critical Rate Of Rise Of Off-state Voltage, dV_D/dt Versus Junction Temperature, T_J



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