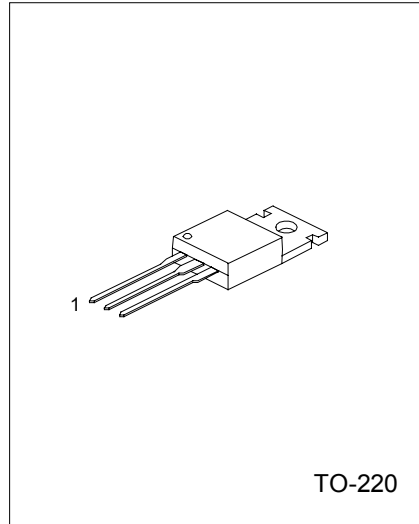
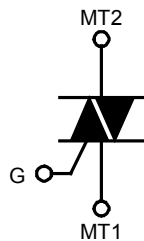


TRIACS

DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive Peak Off-State Voltage UT137E-5 UT137E-6 UT137E-8	V _{DRM}	500* 600* 800	V
RMS On-state Current Full sine wave; T _{mb} ≤ 102°C	I _{T(RMS)}	8	A
Non-Repetitive Peak On-State Current Full sine wave; T _j = 25°C prior to surge t = 20ms t = 16.7ms	I _{TSM}	65 71	A
I ² t For Fusing (t = 10ms)	I ² t	21	A ² s
Repetitive Rate of Rise of On-state Current after Triggering I _{TM} = 12A; I _G = 0.2A, dI _G /dt = 0.2A/μs T2+ G+ T2+ G- T2- G- T2- G+	dI _T /dt	50 50 50 10	A/μs
Peak Gate Voltage	V _{GM}	5	V
Peak Gate Current	I _{GM}	2	A
Peak Gate Power	P _{GM}	5	W
Average Gate Power (Over any 20ms period)	P _{G(AV)}	0.5	W
Operating Junction Temperature	T _j	125	°C
Storage Temperature	T _{stg}	-40~150	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6A/μs.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance Junction to Mounting Base Full cycle Half cycle	Rth j-mb			2.0 2.4	K/W
Thermal Resistance Junction to Ambient In free air	Rth j-a		60		K/W

STATIC CHARACTERISTICS (T_j=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	I _{GT}	V _D =12V, I _T =0.1A T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching Current	I _L	V _D =12V, I _{GT} =0.1A T2+ G+ T2+ G- T2- G- T2- G+		3.0 14 3.0 4.0	25 35 25 35	mA
Holding Current	I _H	V _D =12V, I _{GT} =0.1A		2.5	20	mA
On-State Voltage	V _T	I _T =10A		1.3	1.65	V
Gate Trigger Voltage	V _{GT}	V _D =12V, I _T =0.1A V _D =400V, I _T =0.1A, T _j =125°C	0.25	0.7 0.4	1.5	V
Off-state Leakage Current	I _D	V _D =V _{DRM(max)} , T _j =125°C		0.1	0.5	mA

DYNAMIC CHARACTERISTICS (T_j=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate of Rise of off-state Voltage	dV _D /dt	V _{DM} =67% V _{DRM(max)} , T _j =125°C Exponential waveform, Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t _{gt}	I _{TM} =12A, V _D =V _{DRM(max)} , I _G =0.1A dI _G /dt=5A/μs		2		μs

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation. P_{tot} vs RMS On-state Current, $I_T(RMS)$, Where α = conduction Angle.

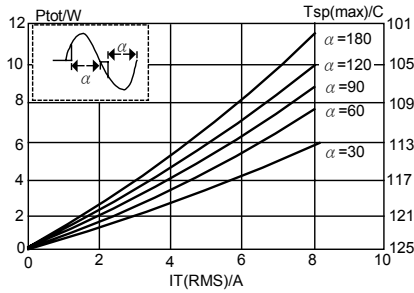


Figure 4. Maximum Permissible RMS Current $I_T(RMS)$ vs mounting base Temperature T_{mb}

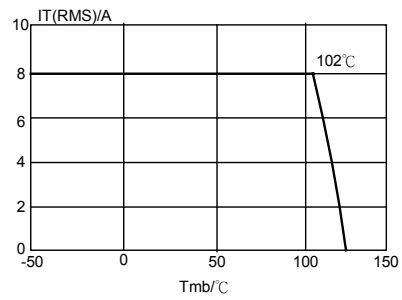


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current I_{TSM} , vs Pulse Width t_p , for Sinusoidal Currents, $t_p \leq 20ms$

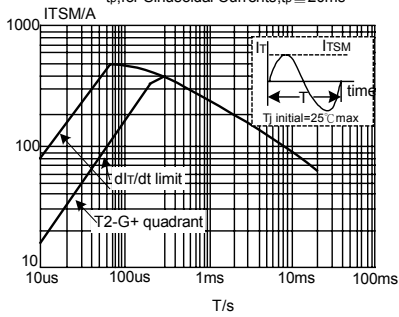


Figure 5. Maximum Permissible Repetitive RMS on-state Current $I_T(RMS)$, vs Surge Duration, for Sinusoidal Currents, $f=50Hz$; $T_{mb} \leq 102^\circ C$

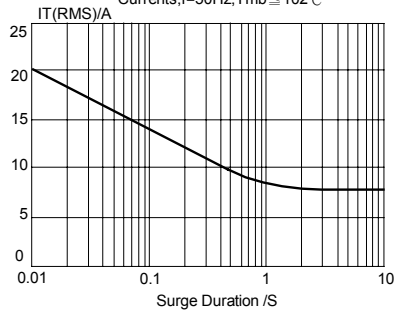


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current I_{TSM} , vs Number of Cycles, for Sinusoidal Currents, $f=50Hz$

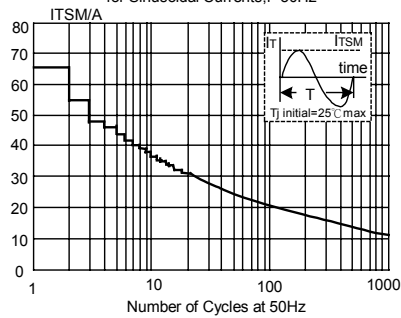


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_j) / V_{GT}(25^\circ C)$, vs Junction Temperature T_j

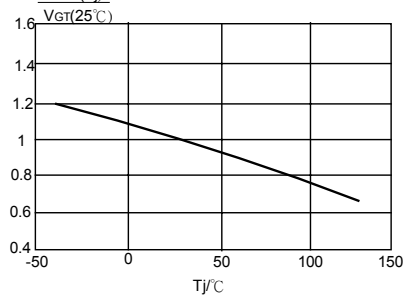


Figure 7. Normalised Gate Trigger Current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, vs Junction Temperature T_j

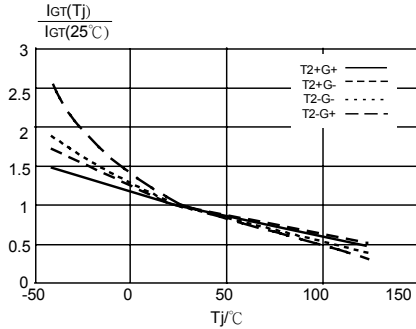


Figure 8. Normalised Latching Current $I_L(T_j)/I_L(25^\circ\text{C})$, vs Junction Temperature T_j

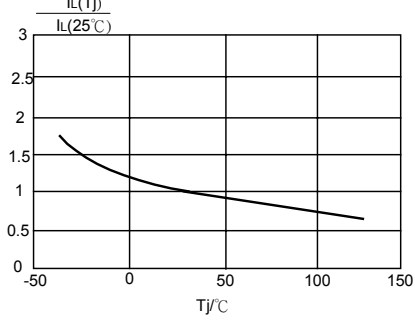


Figure 9. Normalised Holding Current $I_H(T_j)/I_H(25^\circ\text{C})$, vs Junction Temperature T_j

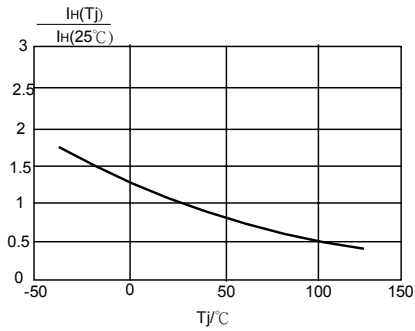


Figure 10. Typical and Maximum On-state Characteristic

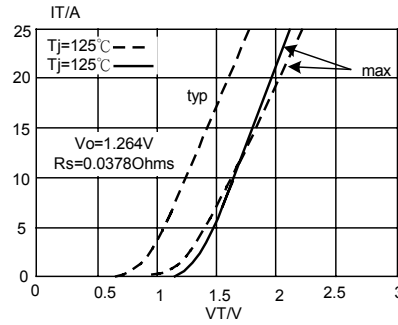


Figure 11. Transient Thermal Impedance $Z_{th\ j-mb}$, vs Pulse Width t_p

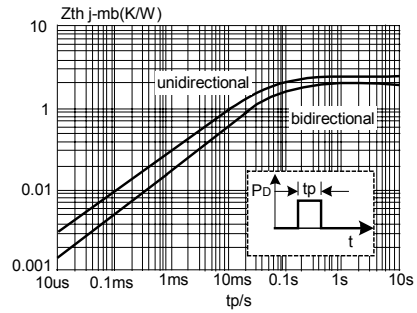
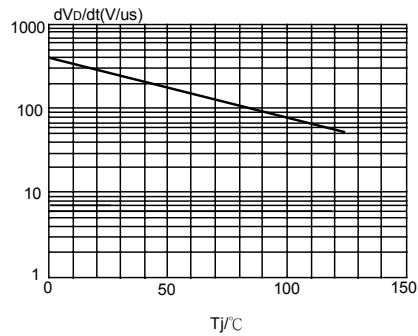


Figure 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j



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