



UT138E

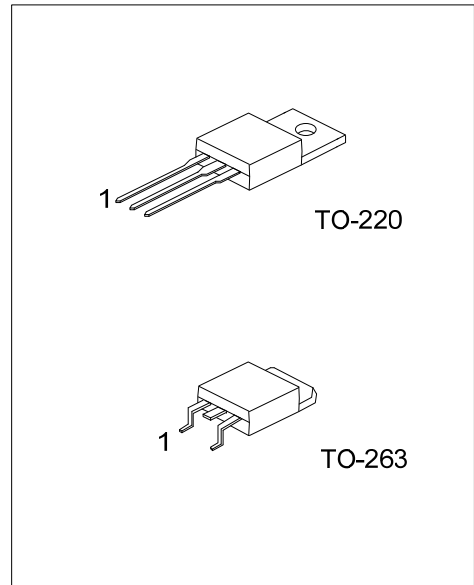
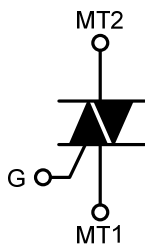
TRIAC

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■ DESCRIPTION

Glass passivated , sensitive gate triac in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

■ SYMBOL

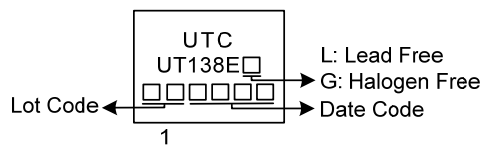


■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
UT138EL-x-TA3-T	UT138EG-x-TA3-T	TO-220	MT1	MT2	G	Tube
UT138EL-x-TQ2-T	UT138EG-x-TQ2-T	TO-263	MT1	MT2	G	Tube
UT138EL-x-TQ2-R	UT138EG-x-TQ2-R	TO-263	MT1	MT2	G	Tape Reel

<p>UT138EG-x-TA3-T</p> <p>(1)Packing Type (2)Package Type (3)Voltage (4)Green Package</p>	<p>(1) T: Tube, R: Tape Reel (2) TA3: TO-220, TQ2: TO-263 (3) 5: 500V, 6: 600V, 8: 800V (4) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATING (T_J=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive Peak Off State Voltag	UT138E-5	500	V
	UT138E-6	600	V
	UT138E-8	800	V
RMS On-state Current (Full sine wave, T _{MB} ≤99°C)	I _{T(RMS)}	12	A
Non-Repetitive Peak. On-State Current (Full sine wave, T _J =25°C prior to surge)	t=20mS	95	A
	t=16.7mS	105	A
I ² t For Fusing (t=10ms)	I ² t	45	A ² s
Repetitive Rate of Rise of On-state Current After Triggering (I _{TM} =20A, I _G =0.2A, dI _G /dt=0.2A/μs)	T2+ G+	50	A/μs
	T2+ G-	50	A/μs
	T2- G-	50	A/μs
	T2- G+	10	A/μs
Peak Gate Voltage	V _{GM}	5	V
Peak Gate Current	I _{GM}	2	A
Peak Gate Power	P _{GM}	5	W
Average Gate Power (Over any 20ms period)	P _{G(AV)}	0.5	W
Operating Junction Temperature	T _J	125	°C
Storage Temperature	T _{STG}	-40~150	°C

Notes: Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

■ THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to Ambient In free air	θ _{JA}		60		K/W
Thermal Resistance, Junction to Mounting Base	Full cycle			1.5	K/W
	Half cycle			2.0	

■ STATIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	I _{GT}	V _D =12V, I _T =0.1A	T2+ G+	2.5	10	mA
			T2+ G-	4.0	10	
			T2- G-	5.0	10	
			T2- G+	11	25	
Latching Current	I _L	V _D =12V, I _{GT} =0.1A	T2+ G+	3.2	30	mA
			T2+ G-	16	40	
			T2- G-	4.0	30	
			T2- G+	5.5	40	
Holding Current	I _H	V _D =12V, I _{GT} =0.1A		4.0	30	mA
On-State Voltage	V _T	I _T =15A		1.4	1.65	V
Gate Trigger Voltage	V _{GT}	V _D =12V, I _T =0.1A		0.7	1.5	V
		V _D =400V, I _T =0.1A, T _J =125°C	0.25	0.4		V
Off-state Leakage Current	I _D	V _D =V _{DRM(max)} , T _J =125°C		0.1	0.5	mA

■ DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate Of Rise Of Off-State Voltage	dV _D /dt	V _{DM} =67% V _{DRM(max)} , T _J =125°C Exponential waveform, Gate open circuit		50		V/μs
Gate Controlled Turn-on Time	t _{gt}	I _{TM} =16A, V _D =V _{DRM(max)} , I _G =0.1A dI _G /dt=5A/μs		2		μs

■ TYPICAL CHARACTERISTICS

Figure 1. Maximum On-State Dissipation. P_{tot} vs RMS On-state Current, $I_{T(RMS)}$, Where α =Conduction Angle.

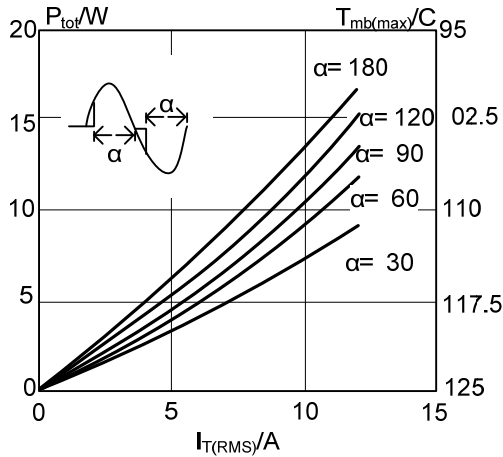


Figure 2. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM} , vs Pulse Width t_p , for Sinusoidal Currents, $t_p \leq 20ms$.

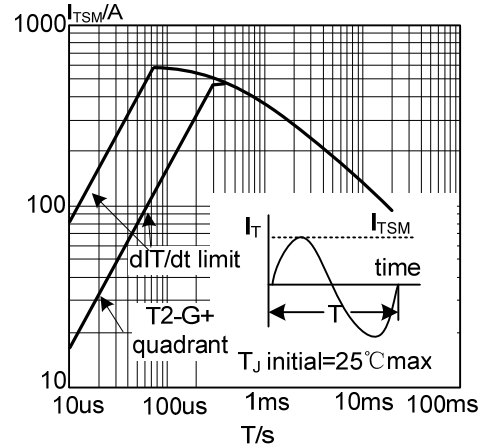


Figure 3. Maximum Permissible Non-Repetitive Peak On-State Current I_{TSM} , vs Number of Cycles, for Sinusoidal Currents, $f=50Hz$.

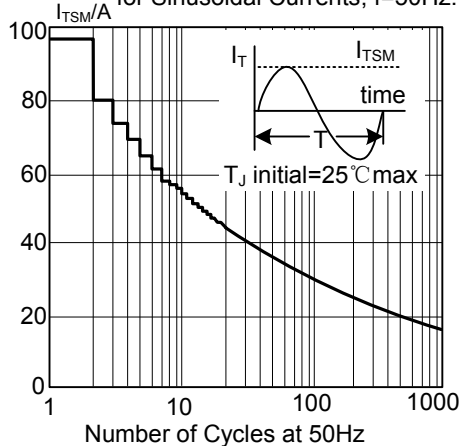


Figure 4. Maximum Permissible RMS Current $I_{T(RMS)}$ vs Mounting Base Temperature T_{mb}

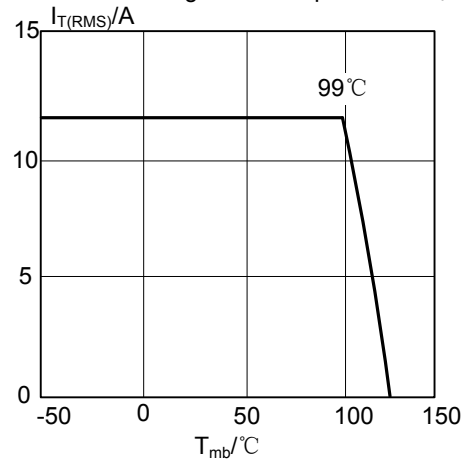


Figure 5. Maximum Permissible Repetitive RMS On-State Current $I_{T(RMS)}$, vs Surge Duration, for Sinusoidal Currents, $f=50Hz$, $T_{mb} \leq 99^\circ C$

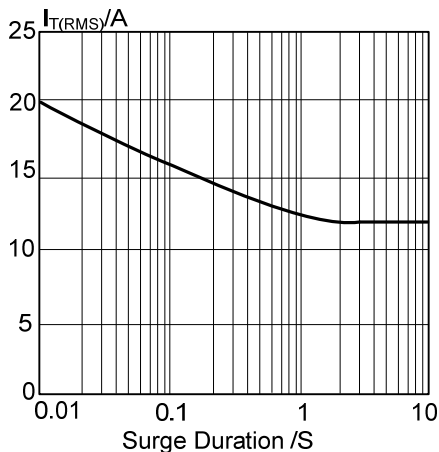
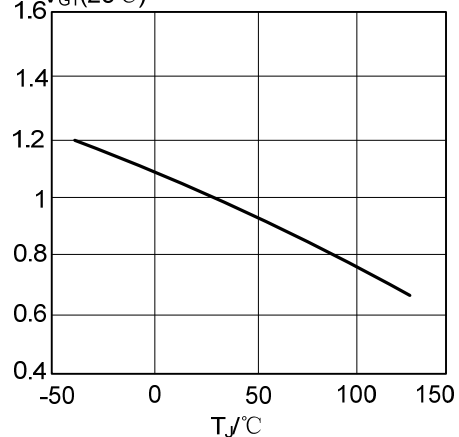


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_J)/V_{GT}(25^\circ C)$, vs Junction Temperature T_J



■ TYPICAL CHARACTERISTICS (Cont.)

Figure 7. Normalised Gate Trigger Current $I_{GT}(T_J)/I_{GT}(25^\circ\text{C})$, vs Junction Temperature T_J .

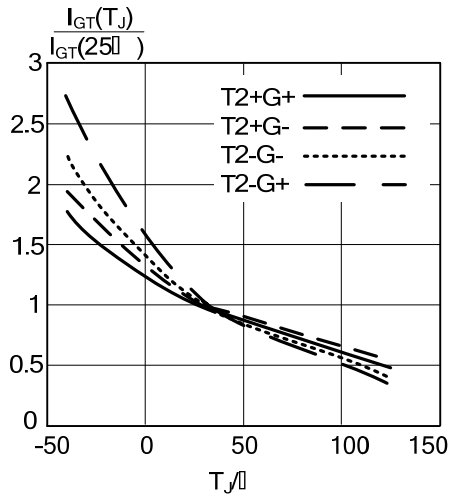


Figure 9. Normalised Holding Current $I_H(T_J)/I_H(25^\circ\text{C})$, vs Junction Temperature T_J .

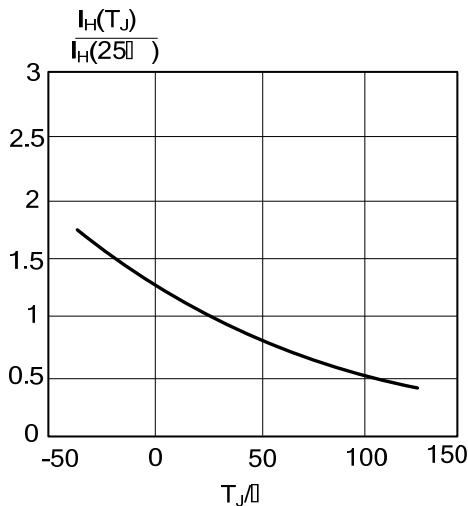


Figure 11. Transient Thermal Impedance $Z_{th\ i-mb}$, vs Pulse Width t_p

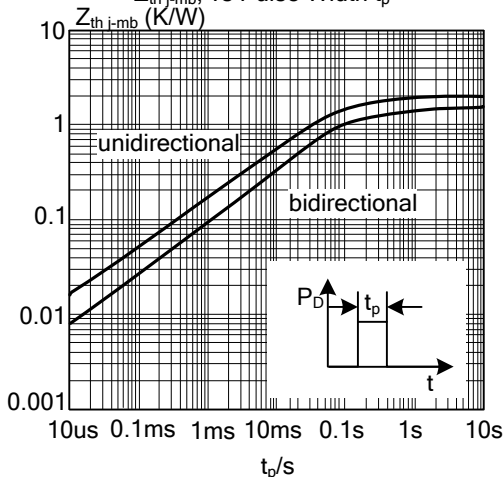


Figure 8. Normalised Latching Current $I_L(T_J)/I_L(25^\circ\text{C})$, vs Junction Temperature T_J .

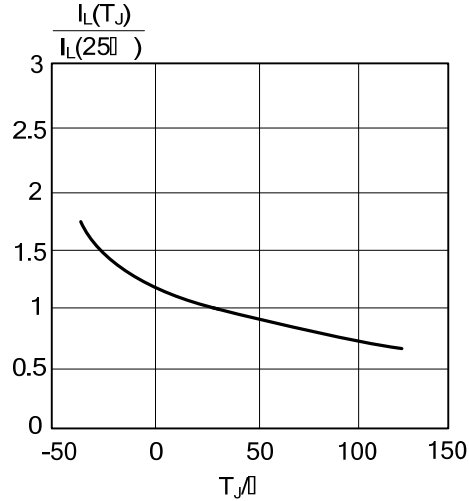


Figure 10. Typical and Maximum On-state Characteristic

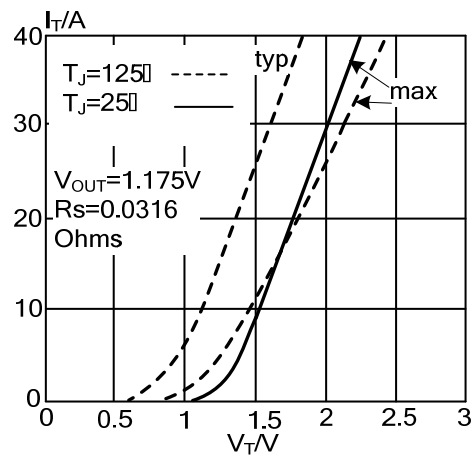
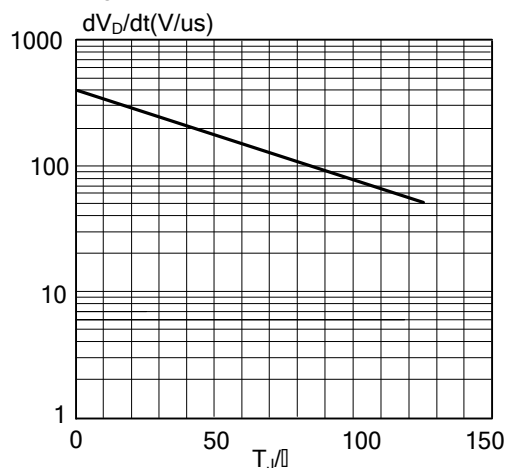


Figure 12. Typical Critical Rate of Rise of Off-State Voltage, dV_D/dt Versus Junction Temperature T_J



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