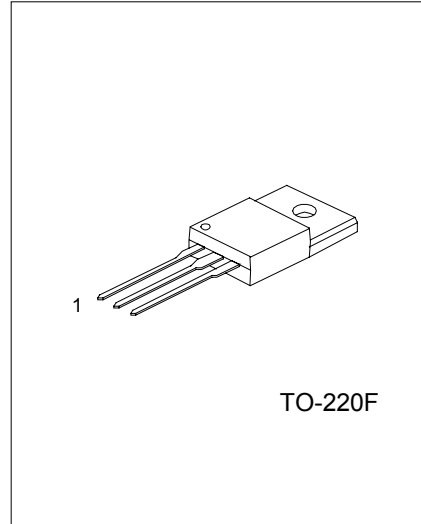
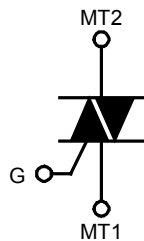


TRIACS

DESCRIPTION

Glass passivated triacs in a full pack plastic envelope, intended for use in applications requiring high bidirectional transient and blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS (Tj=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltages UT138FF/FG-5 UT138FF/FG-6 UT138FF/FG-8	V _{DRM}	500* 600* 800	V
RMS On-state Current (Full sine wave, T _{hs} ≤ 56°C)	I _{T(RMS)}	12	A
Non-repetitive Peak. On-State Current (Full sine wave, T _j = 125°C prior to surge, with reapplied V _{DRM(max)}) t = 20ms t = 16.7ms	I _{TSM}	90 100	A
I ² t For Fusing (t = 10ms)	I ² t	40	A ² s
Repetitive Rate of Rise of On-state Current after Triggering (I _{TM} = 20A, I _G = 0.2A, dI _G /dt = 0.2A/μs) T2+ G+ T2+ G- T2- G- T2- G+	dI _T /dt	50 50 50 10	A/μs
Peak Gate Voltage	V _{GM}	5	V
Peak Gate Current	I _{GM}	2	A
Peak Gate Power	P _{GM}	5	W
Average Gate Power (over any 20ms period)	P _{G(AV)}	0.5	W
Operating Junction Temperature	T _j	125	°C
Storage Temperature	T _{stg}	-40~150	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC (T_{HS}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
R.M.S. isolation voltage from all three terminals to external heatsink (f=50-60Hz, sinusoidal waveform R.H. ≤ 65%, clean and dustfree)	Visol			1500	V
Capacitance from MT2 to external heatsink (f=1MHz)	Cisol		12		pF

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to heatsink (full or half cycle) with heatsink compound without heatsink compound	Rthj-hs			4.0 5.5	K/W
Thermal Resistance, Junction to Ambient In free air	Rthj-a		55		K/W

STATIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX		UNIT
					UT138FF	UT138FG	
Gate trigger current	IGT	V _D =12V, I _T =0.1A T2+ G+ T2+ G- T2- G- T2- G+		5	25	50	mA
				8	25	50	
				10	25	50	
				22	70	100	
Latching current	IL	V _D =12V, I _{GT} =0.1A T2+ G+ T2+ G- T2- G- T2- G+		7	40	60	mA
				20	60	90	
				8	40	60	
				10	60	90	
Holding current	I _H	V _D = 12 V, I _{GT} = 0.1 A		6	30	60	mA
On-state voltage	V _T	I _T =15A		1.4	1.65		V
Gate trigger voltage	V _{GT}	V _D =12V, I _T =0.1A		0.7	1.5		V
		V _D =400V, I _T =0.1A, T _J =125°C	0.25	0.4			V
Off-state leakage current	I _D	V _D =V _{DRM(max)} , T _J =125°C		0.1	0.5		mA

DYNAMIC CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN		TYP	MAX	UNIT
			UT138FF	UT138FG			
Critical rate of change of Off-state voltage	dV _D /dt	V _{DM} = 67% V _{DRM(max)} , T _J =125°C; exponential waveform, gate open circuit	100	200	250		V/μs
Critical rate of change of Commutating voltage	dV _{com} /dt	V _{DM} =400V; T _J =95°C, I _{T(RMS)} =12A; dI _{com} /dt =5.4A/ms, gate open circuit			20		V/μs
Gate controlled turn-on time	t _{gt}	I _{TM} =16 A, V _D = V _{DRM(max)} , I _G =0.1A; dI _G /dt=5A/μs			2		μs

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation, P_{tot} vs rms On-state Current, $I_T(RMS)$, Where α = conduction Angle.

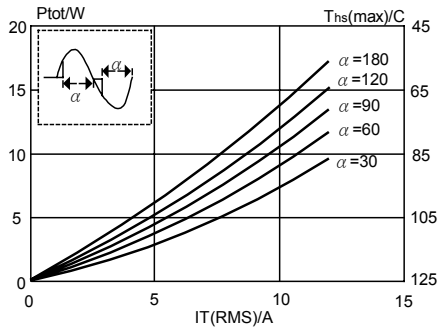


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current I_{TSM} , vs Pulse Width t_p , for Sinusoidal Currents, $t_p \leq 20ms$

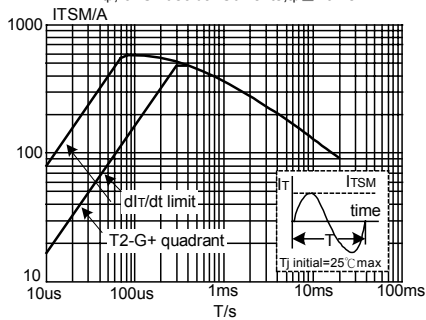


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current I_{TSM} , vs Number of Cycles, for Sinusoidal Currents, $f=50Hz$

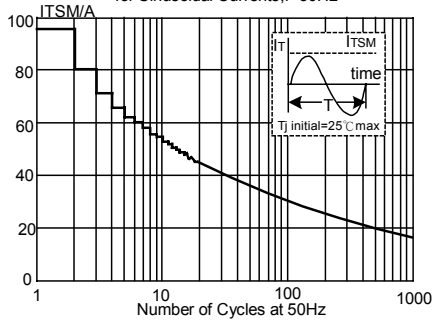


Figure 4. Maximum Permissible RMS Current $I_T(RMS)$ vs heatsink temperature T_{hs}

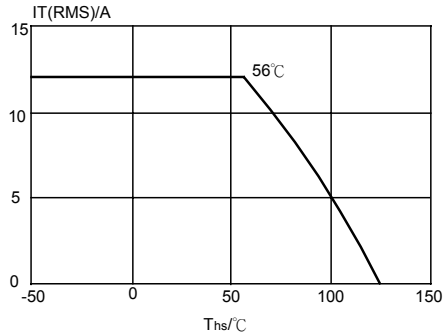


Figure 5. Maximum Permissible Repetitive rms on-state Current $I_T(RMS)$, vs Surge Duration, for Sinusoidal Currents, $f=50Hz$, $T_{hs} \leq 56^\circ C$

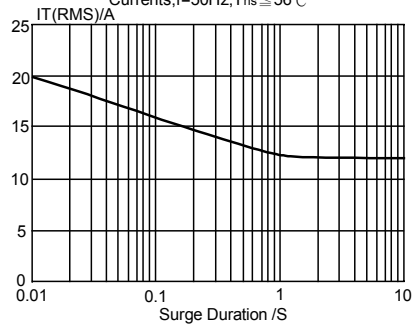
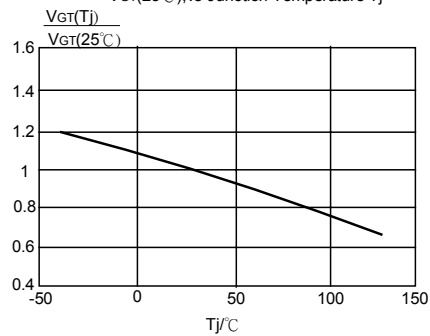
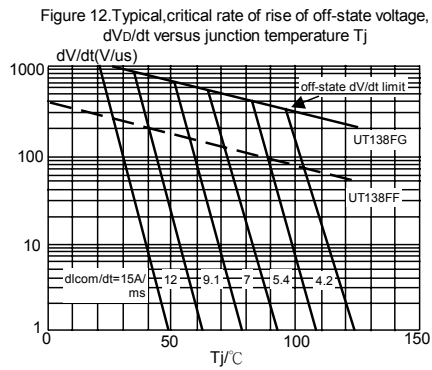
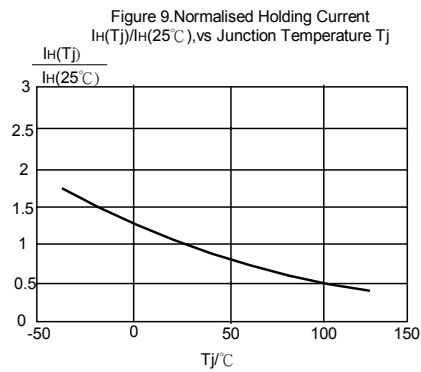
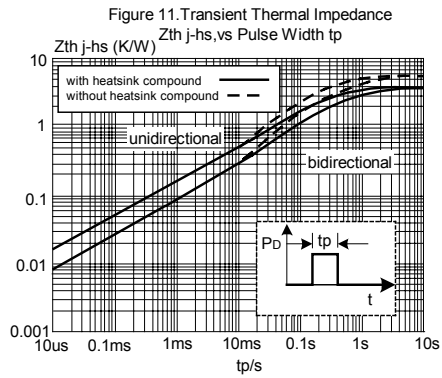
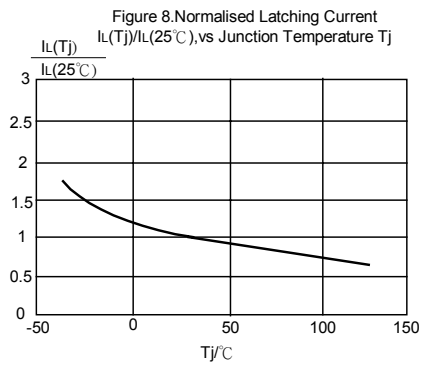
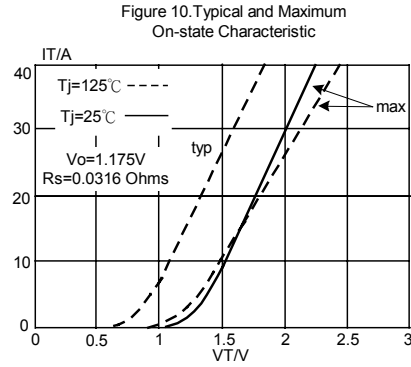
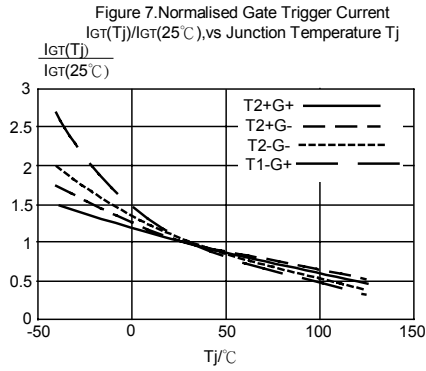


Figure 6. Normalised Gate Trigger Voltage $V_{GT}(T_j)/V_{GT}(25^\circ C)$, vs Junction Temperature T_j





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