



FEATURES

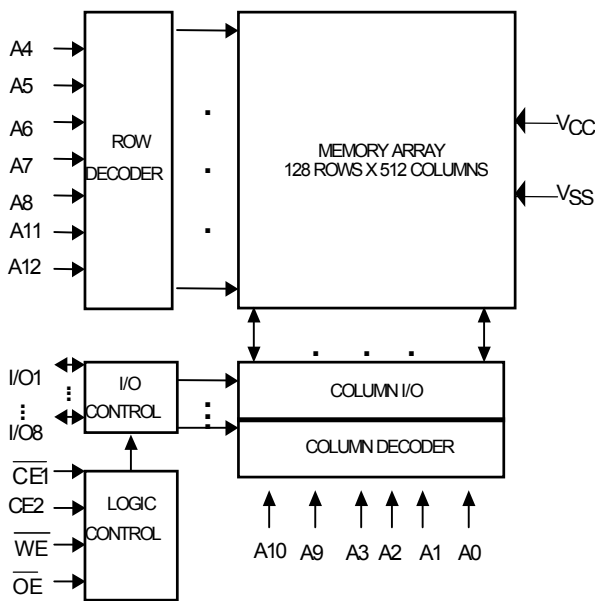
- Fast access time : 10/12/15 ns (max.)
- Low operating power consumption : 80 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil SOJ  
28-pin 8mm×13.4mm STSOP

The UT6164C is a 65,536-bit high-speed CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

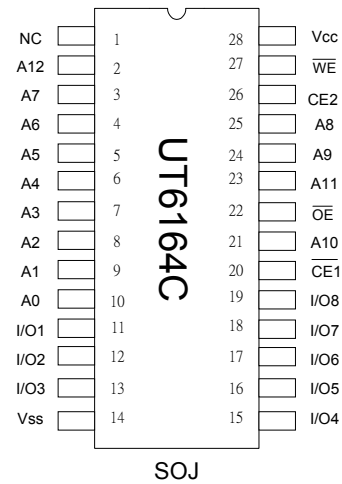
The UT6164C is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT6164C operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM

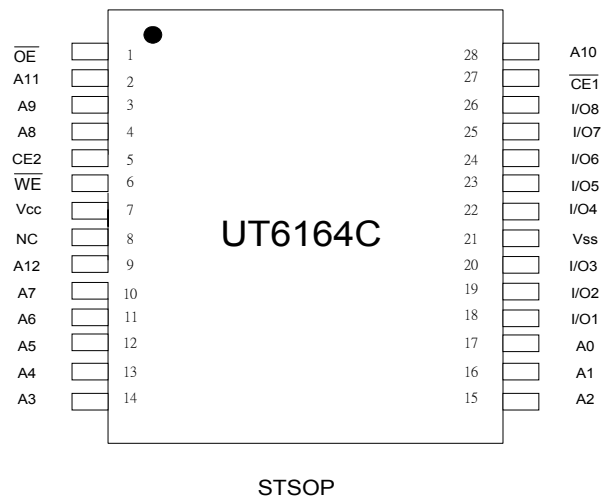


PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1, CE2	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground



GENERAL DESCRIPTION

**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V <sub>SS</sub>	V <sub>TERM</sub>	-0.5 to +6.5	V
Operating Temperature	T <sub>A</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-65 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>solder</sub>	260	°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
Standby	X	L	X	X	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	High - Z	I <sub>CC</sub>
Read	L	H	L	H	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	H	X	L	D <sub>IN</sub>	I <sub>CC</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V <sub>IH</sub>		2.2	V <sub>CC</sub> +0.5	V	
Input Low Voltage	V <sub>IL</sub>		- 0.5	0.8	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	- 1	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub> $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	- 1	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 4mA	2.4	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	0.4	V	
Operating Power Supply Current	I <sub>CC</sub>	Cycle time=Min. $\overline{CE1} = V_{IL}$ , CE2= V <sub>IH</sub> I <sub>I/O</sub> = 0mA	- 10	-	180	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Current (TTL)	I <sub>SB</sub>	$\overline{CE1} = V_{IH}$ or CE2= V <sub>IL</sub>	-	30	mA	
Standby Current (CMOS)	I <sub>SB1</sub>	$\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V	-	5	mA	

**CAPACITANCE** ( $T_A=25^{\circ}\text{C}$ ,  $f=1.0\text{MHz}$ )

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	$C_{IN}$	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$ , $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ )**(1) READ CYCLE**

PARAMETER	SYMBOL	UT6164C-10		UT6164C-12		UT6164C-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	$t_{RC}$	10	-	12	-	15	-	ns
Address Access Time	$t_{AA}$	-	10	-	12	-	15	ns
Chip Enable Access Time	$t_{ACE}$	-	10	-	12	-	15	ns
Output Enable Access Time	$t_{OE}$	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	$t_{CLZ}^*$	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	$t_{OLZ}^*$	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	$t_{CHZ}^*$	-	5	-	6	-	7	ns
Output Disable to Output in High Z	$t_{OHZ}^*$	-	5	-	6	-	7	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	3	-	ns

**(2) WRITE CYCLE**

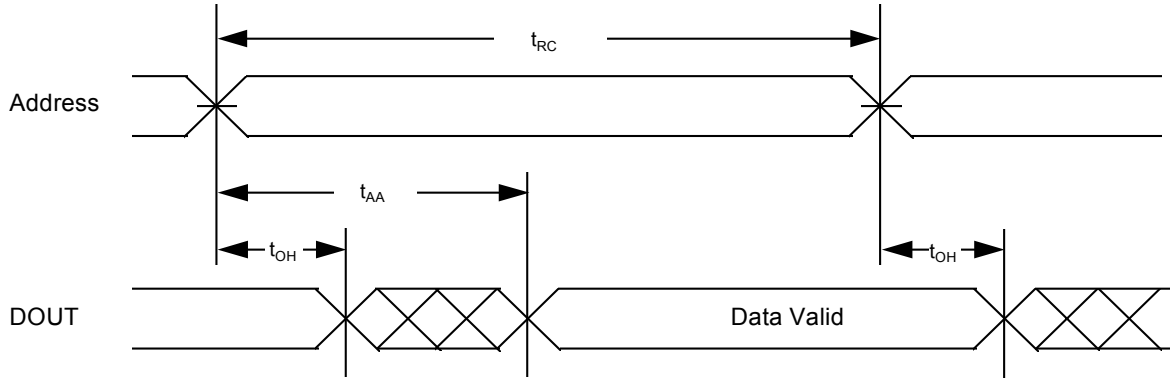
PARAMETER	SYMBOL	UT6164C-10		UT6164C-12		UT6164C-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	$t_{WC}$	10	-	12	-	15	-	ns
Address Valid to End of Write	$t_{AW}$	8	-	10	-	12	-	ns
Chip Enable to End of Write	$t_{CW}$	8	-	10	-	12	-	ns
Address Set-up Time	$t_{AS}$	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	8	-	9	-	10	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	ns
Data to Write Time Overlap	$t_{DW}$	6	-	7	-	8	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	0	-	0	-	ns
Output Active from End of Write	$t_{OW}^*$	2	-	3	-	4	-	ns
Write to Output in High Z	$t_{WHZ}^*$	-	6	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

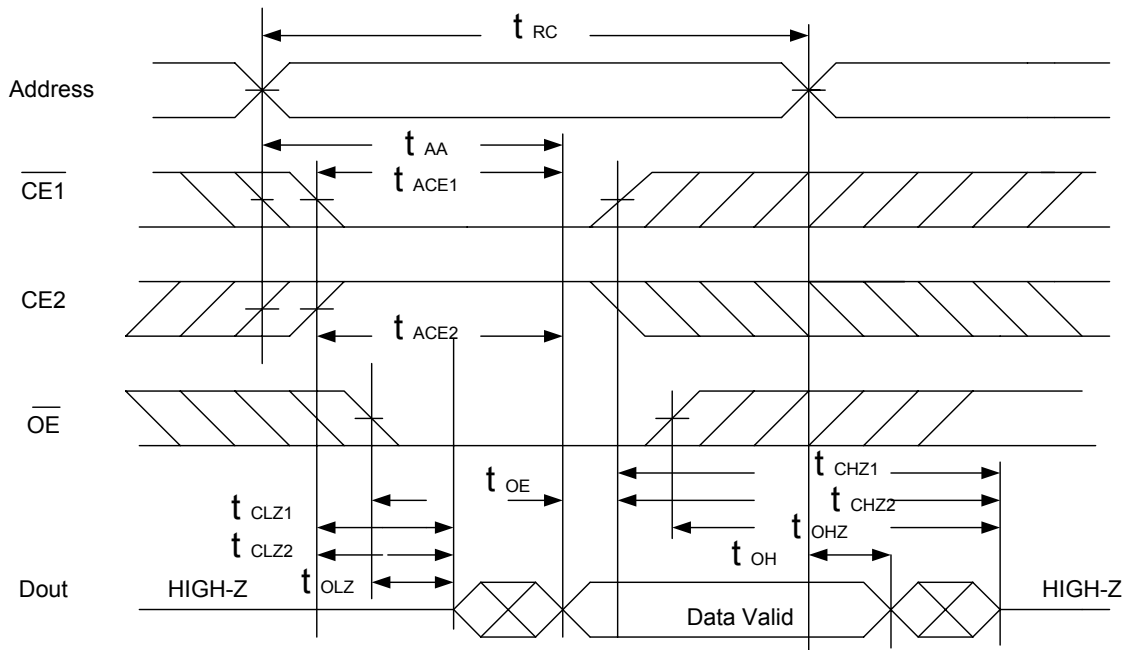


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ( $\overline{CE1}$ ,  $\overline{CE2}$  and  $\overline{OE}$  Controlled) (1,3,5,6)

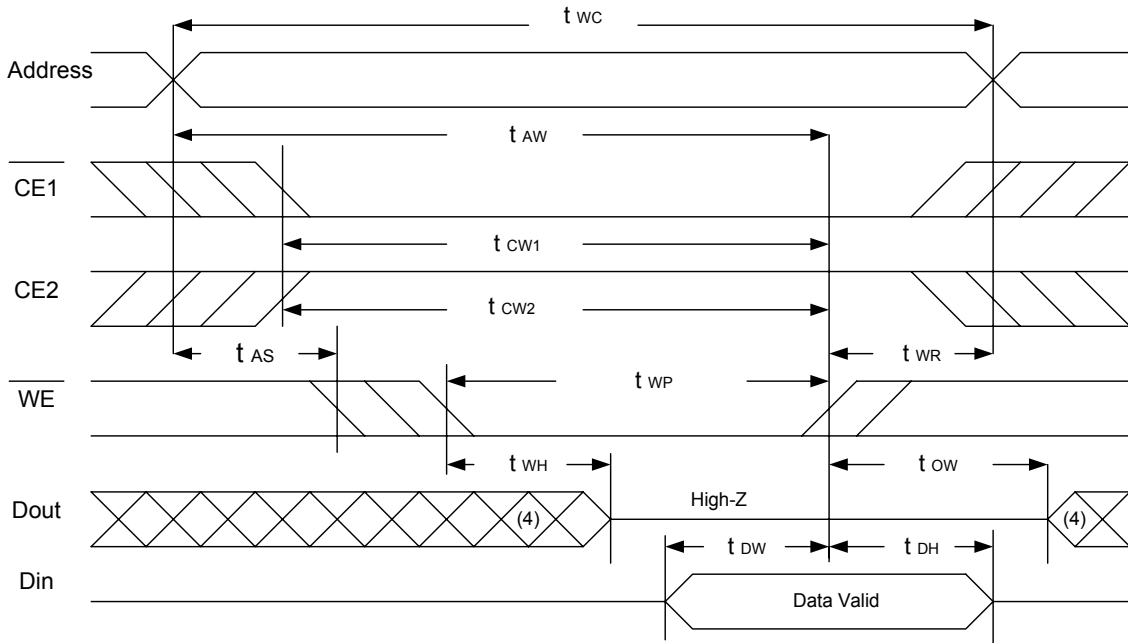


Notes :

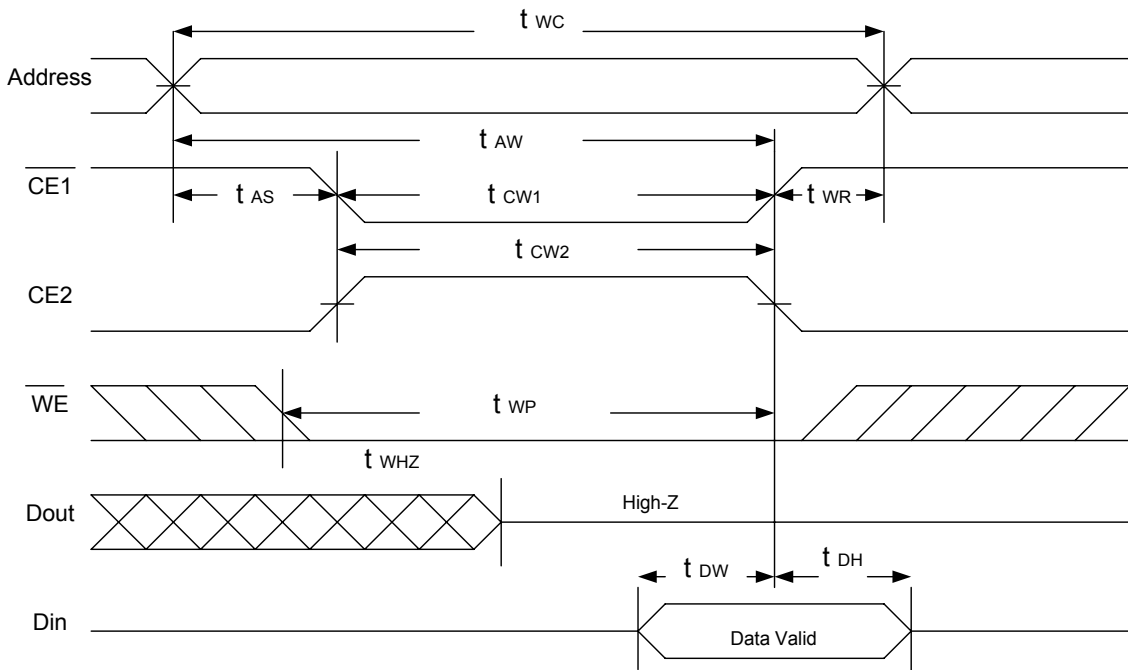
1.  $\overline{WE}$  is high for read cycle.
2. Device is continuously selected  $\overline{CE1} = V_{IL}$  and  $\overline{CE2} = V_{IH}$ .
3. Address must be valid prior to or coincident with  $\overline{CE1}$  and  $\overline{CE2}$  transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is low.
5.  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ1}$  is less than  $t_{CLZ1}$ ,  $t_{CHZ2}$  is less than  $t_{CLZ2}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



**WRITE CYCLE 1 ( $\overline{WE}$  Controlled) (1,2,3,5)**



**WRITE CYCLE 2 ( $\overline{CE1}$  ,  $\overline{CE2}$  Controlled) (1,2,5)**



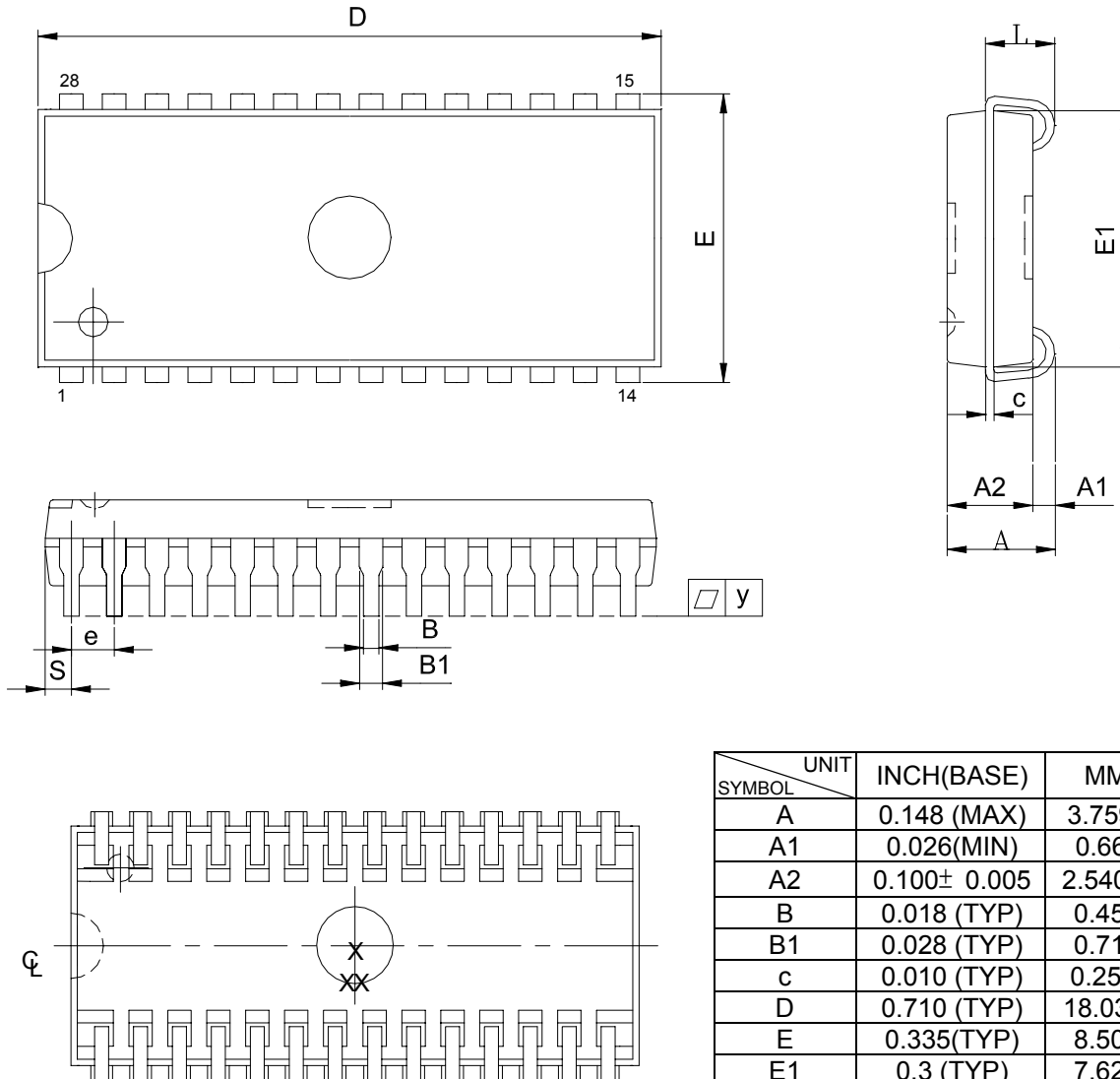
Notes :

1.  $\overline{WE}$  or  $\overline{CE1}$  must be high or  $\overline{CE2}$  must be low during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE1}$ , a high  $\overline{CE2}$  and a low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled with write cycle with  $\overline{OE}$  low,  $t_{WP}$  must be greater than  $t_{WHZ}+t_{DW}$  to allow the I/O drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE1}$  low and  $\overline{CE2}$  high transition occurs simultaneously with or after  $\overline{WE}$  low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L=5pF$ . Transition is measured  $\pm 500mV$  from steady state.



PACKAGE OUTLINE DIMENSION

28 pin 300 mil SOJ Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026(MIN)	0.660(MIN)
A2	0.100± 0.005	2.540± 0.127
B	0.018 (TYP)	0.457(TYP)
B1	0.028 (TYP)	0.711(TYP)
c	0.010 (TYP)	0.254 (TYP)
D	0.710 (TYP)	18.034 (TYP)
E	0.335(TYP)	8.509(TYP)
E1	0.3 (TYP)	7.620(TYP)
e	0.050 (TYP)	1.270 (TYP)
L	0.087± 0.010	2.210± 0.254
S	0.030 (TYP)	0.762 (TYP)
Y	0.003(MAX)	0.076(MAX)

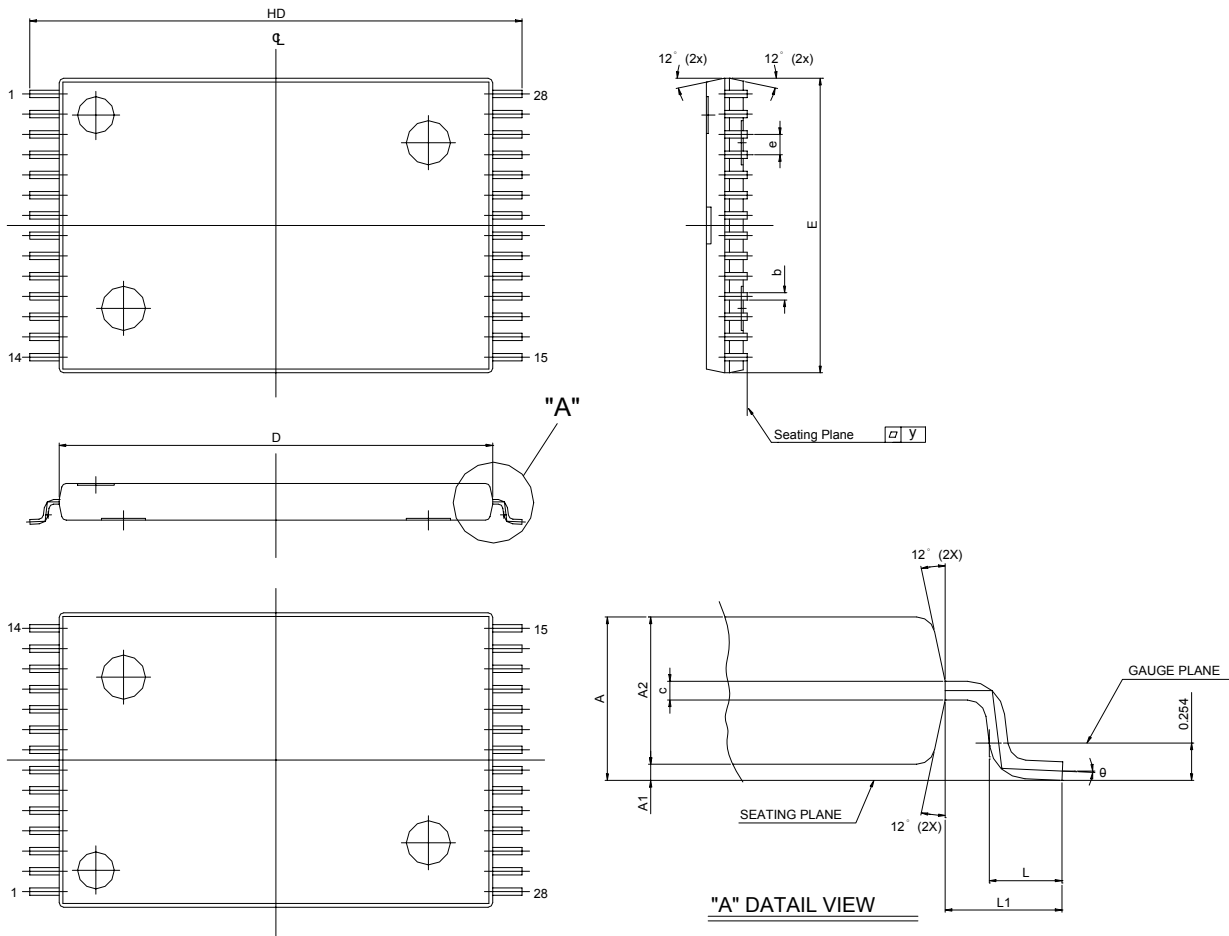
Note:

1. S/E/D DIM NOT INCLUDEING MOLD FLASH.
2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THAN 10 MILS EACH SIDE

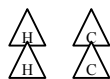




28 pin 8x13.4mm STSOP PACKAGE OUTLINE DIMENSION



Note :  
E dimension is not including end flash  
the total of both sides' end flash  
is not above 0.3mm.



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.008± 0.001	0.200± 0.025
c	0.005 (TYP)	0.127(TYP)
Db	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528± 0.008	13.40± 0.20
L	0.0236± 0.004	0.50± 0.10
L1	0.0315± 0.004	0.80± 0.10
y	0.003(MAX)	0.076(MAX)
θ	0°~5°	0°~5°



UTRON

Rev. 1.0

UT6164C

8K X 8 BIT HIGH SPEED CMOS SRAM

**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>PACKAGE</b>
UT6164CJC-10	10	28 PIN SOJ
UT6164CJC-12	12	28 PIN SOJ
UT6164CJC-15	15	28 PIN SOJ
UT6164CLS-10	10	28 PIN STSOP
UT6164CLS-12	12	28 PIN STSOP
UT6164CLS-15	15	28 PIN STSOP





**UTRON**

Rev. 1.0

**UT6164C**  
**8K X 8 BIT HIGH SPEED CMOS SRAM**

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**REVISION HISTORY**

<b>REVISION</b>	<b>DESCRIPTION</b>	<b>DATE</b>
Rev. 1.0	Original	Oct 15,2001



UTRON

Rev. 1.0

UT6164C

8K X 8 BIT HIGH SPEED CMOS SRAM

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