



REVISION HISTORY

REVISION	DESCRIPTION	Release Date
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev. 1.0	<ol style="list-style-type: none"> The symbols CE# and OE# and WE# are revised as \overline{CE} and \overline{OE} and \overline{WE}. Separate Industrial and Consumer SPEC. Add access time 55ns range. The power supply is revised: 3.3V\Rightarrow3.6V 	Jul 4,2001
Rev. 1.1	<ol style="list-style-type: none"> Revised PIN CONFIGURATION Rev 1.0 : No A17 pin\rightarrowtyping error Rev 1.1 : add A17 pin. <ol style="list-style-type: none"> TFBGA package : ball D3 : NC\rightarrowA17 TSOP package : pin18 : A16\rightarrowA17 pin19 : A15\rightarrowA16 pin20 : A14\rightarrowA15 pin21 : A13\rightarrowA14 pin22 : A12\rightarrowA13 pin23 : NC\rightarrowA12 	Oct 18,2001
Rev. 1.2	<ol style="list-style-type: none"> Revised AC ELECTRICAL CHARACTERISTICS t_{OH} : 5ns\rightarrow10ns (Min.) t_{BLZ} : 0ns\rightarrow10ns (Min.) Revised FUNCTIONAL BLOCK DIAGRAM 	Mar 19,2002
Rev. 1.3	<ol style="list-style-type: none"> Revised DC ELECTRICAL CHARACTERISTICS : Revised V_{IH} as 2.2V Revised 48-pin TFBGA package outline dimension : Rev. 1.2 : ball diameter=0.3mm Rev. 1.3 : ball diameter=0.35mm 	Apr 17,2002
Rev. 1.4	<ol style="list-style-type: none"> Revised Standby current (LL-Version) : 3uA(typ)\rightarrow2uA(typ) Revised operating current (Iccmax) : 45/35/25mA\rightarrow40/30/25mA Revised DC CHARACTERISTICS : <ol style="list-style-type: none"> Operating Power Supply Current (Icc) 55ns (max) : 45\rightarrow40mA 70ns (typ) : 25\rightarrow20mA, 70ns (max) : 35\rightarrow30mA 100ns (Typ) : 20\rightarrow16mA Standby current(CMOS) : LL-version (typ) : 3\rightarrow2uA, 25\rightarrow20uA 	Dec 18,2002
Rev. 1.5	<ol style="list-style-type: none"> Revised V_{OH}(Typ) : NA\rightarrow2.7V Add V_{IH}(max)=V_{CC}+2.0V for pulse width less than 10ns. V_{IL}(min)=V_{SS}-2.0V for pulse width less than 10ns. Add order information for lead free product 	May 06,2003



FEATURES

- Fast access time : 55/70/100ns
- CMOS Low power operating
Operating current: 40/30mA (Icc max.)
Standby current: 20uA (typ.) L-version
2uA (typ.) LL-version
- Single 2.7V~3.6V power supply
- Operating temperature:
Industrial : -40 ~85
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Data byte control : \overline{LB} (I/O1~I/O8)
 \overline{UB} (I/O9~I/O16)
- Package : 44-pin 400mil TSOP-
48-pin 6mm x 8mm TFBGA

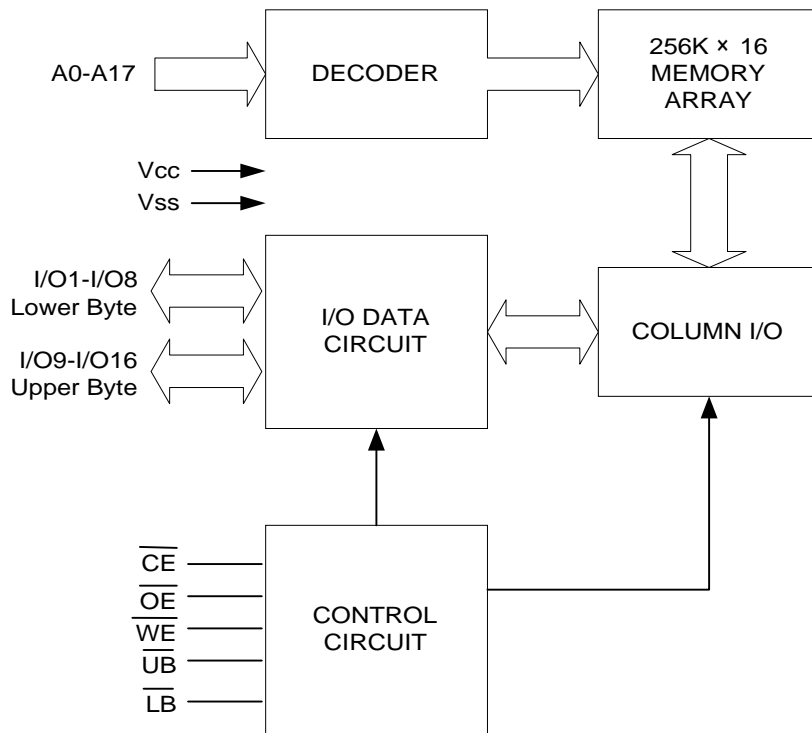
GENERAL DESCRIPTION

The UT62L25616(I) is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

The UT62L25616(I) operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

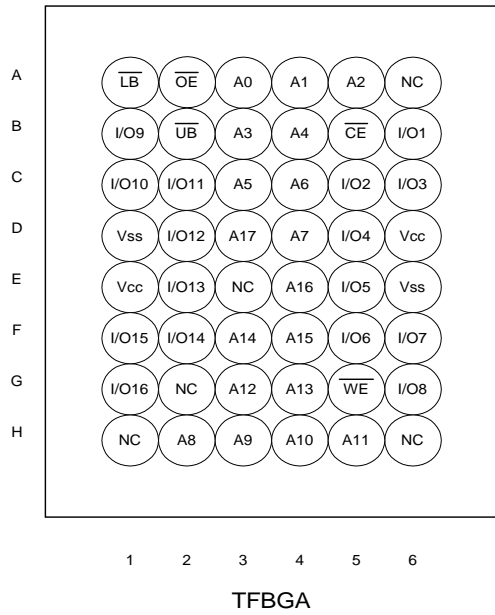
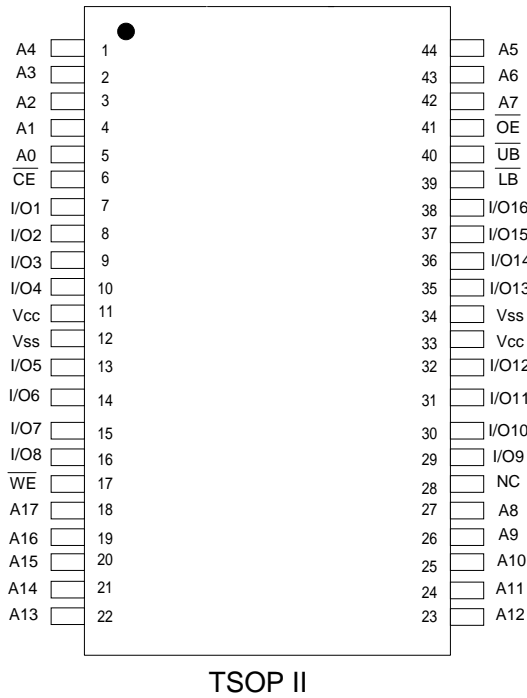
The UT62L25616(I) is designed for low power system applications.

FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
CE	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
LB	Lower Byte Control
UB	Upper Byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	CE	OE	WE	LB	UB	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	H	H	X	L	High - Z	High - Z	
Read	L	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	L	H	H	L	High - Z	D _{OUT}	
	L	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	X	L	H	L	High - Z	D _{IN}	
	L	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	T_A	-40 to 85	
Storage Temperature	T_{STG}	-65 to 150	
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = -40$ to 85 (I))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Power Voltage	V_{CC}		2.7	3.0	3.6	V	
Input High Voltage	$V_{IH}^{1)}$		2.2	-	$V_{CC}+0.3$	V	
Input Low Voltage	$V_{IL}^{2)}$		-0.2	-	0.6	V	
Input Leakage Current	I_{LI}	V_{SS} V_{IN} V_{CC}	-1	-	1	μA	
Output Leakage Current	I_{LO}	V_{SS} V_{IO} V_{CC} ; Output Disable	-1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	2.7	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V	
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty $I_{IO}=0mA$, $\overline{CE}=V_{IL}$	55	-	30	40	mA
			70	-	20	30	mA
			100	-	16	25	mA
Average Operation Current	I_{CC1}	100%duty, $I_{IO}=0mA$, $\overline{CE} = 0.2V$, other pins at 0.2V or $V_{CC}-0.2V$	$T_{cycle}=1\mu s$	-	4	5	mA
	I_{CC2}		$T_{cycle}=500ns$	-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}=V_{IH}$, other pins = V_{IL} or V_{IH}	-	0.3	0.5	mA	
Standby Current (CMOS)	I_{SB1}	$\overline{CE}=V_{CC}-0.2V$ other pins at 0.2V or $V_{CC}-0.2V$	-L	-	20	80	μA
			-LL	-	2	20	μA

Notes:

1. Overshoot : $V_{CC}+2.0v$ for pulse width less than 10ns.
2. Undershoot : $V_{SS}-2.0v$ for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

**CAPACITANCE** ($T_A=25^\circ\text{C}$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF}$, $I_{OH}/I_{OL} = -1\text{mA} / 2.1\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=2.7\text{V}\sim 3.6\text{V}$, $T_A = -40^\circ\text{C}$ to 85°C (I))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L25616(I)-55		UT62L25616(I)-70		UT62L25616(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
\overline{LB} , \overline{UB} Access Time	t_{BA}	-	55	-	70	-	100	ns
\overline{LB} , \overline{UB} to High-Z Output	t_{BHZ}	-	25	-	30	-	40	ns
\overline{LB} , \overline{UB} to Low-Z Output	t_{BLZ}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

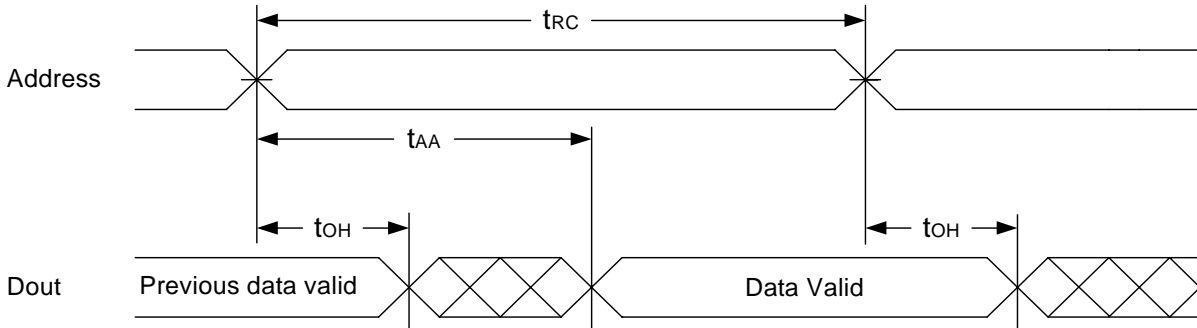
PARAMETER	SYMBOL	UT62L25616(I)-55		UT62L25616(I)-70		UT62L25616(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}^*	-	30	-	30	-	40	ns
\overline{LB} , \overline{UB} Valid to End of Write	t_{BW}	45	-	60	-	80	-	ns

*These parameters are guaranteed by device characterization, but not production tested.

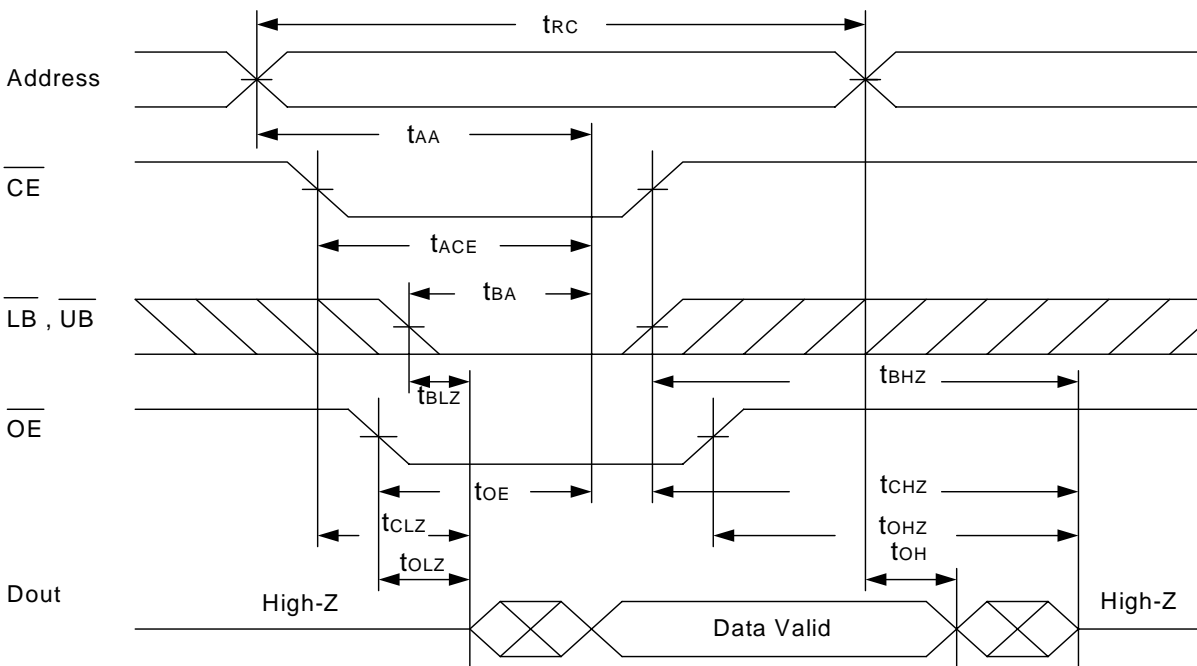


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,4,5)



Notes :

1. \overline{WE} is high for read cycle.
2. Device is continuously selected $\overline{OE} = \text{low}$, $\overline{CE} = \text{low}$, \overline{LB} or $\overline{UB} = \text{low}$.
3. Address must be valid prior to or coincident with $\overline{CE} = \text{low}$, \overline{LB} or $\overline{UB} = \text{low}$ transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

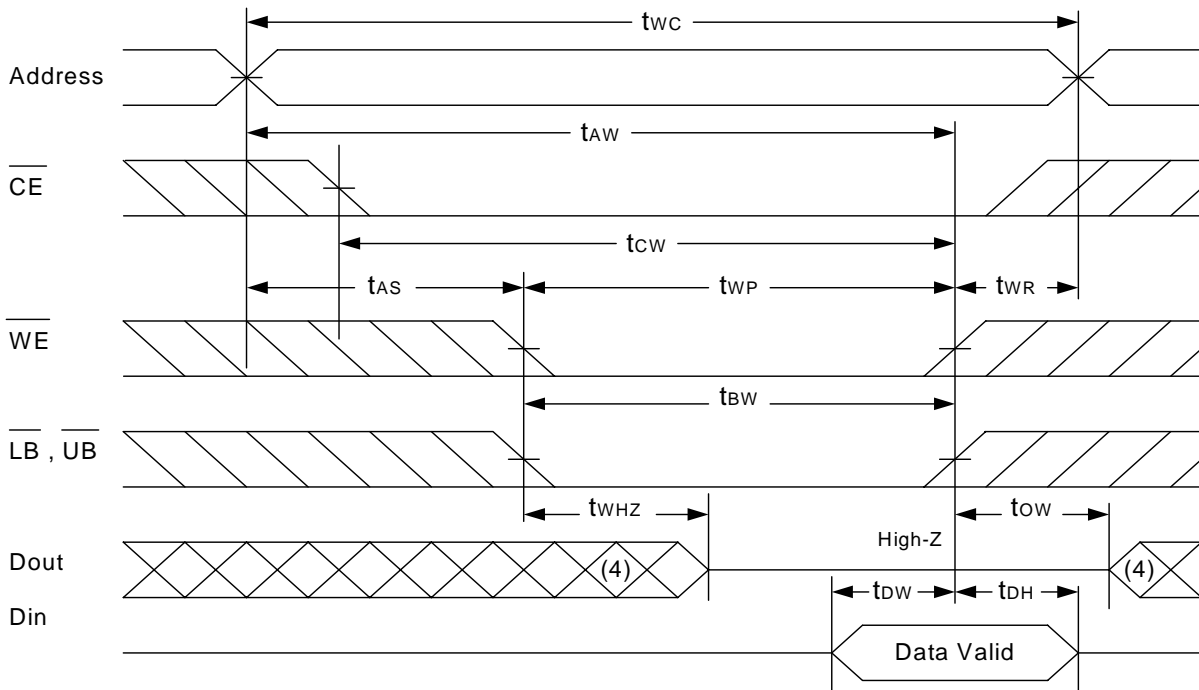


Rev. 1.5

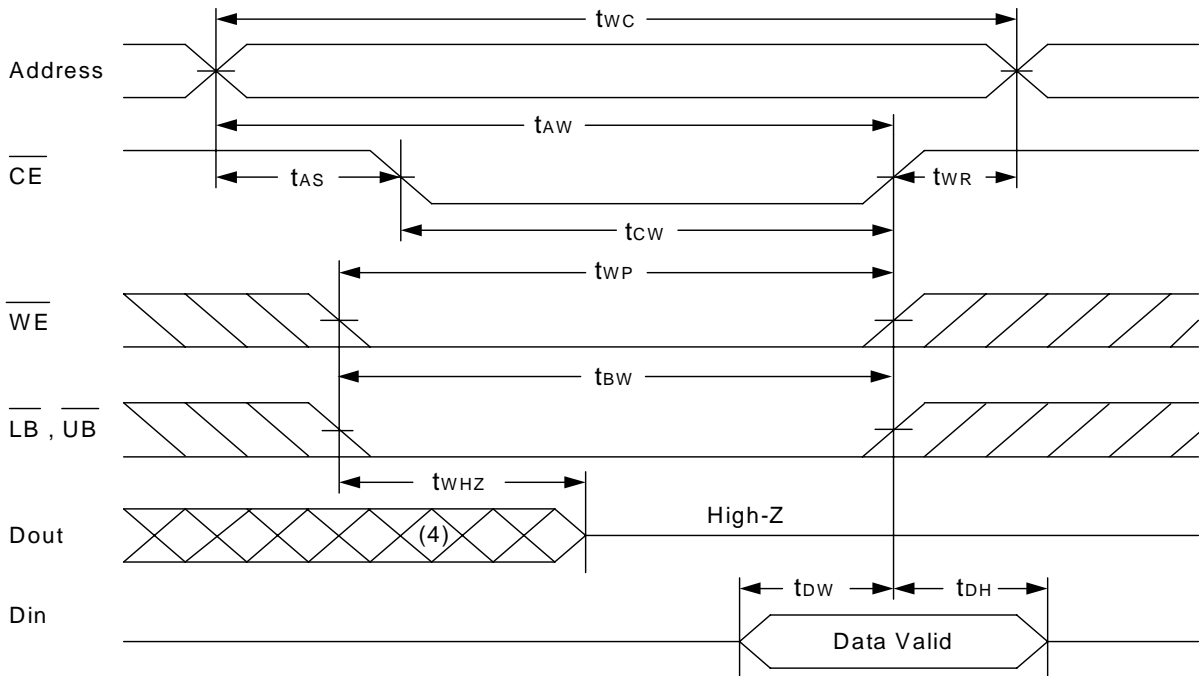
UTRON

UT62L25616(I) 256K X 16 BIT LOW POWER CMOS SRAM

WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5,6)

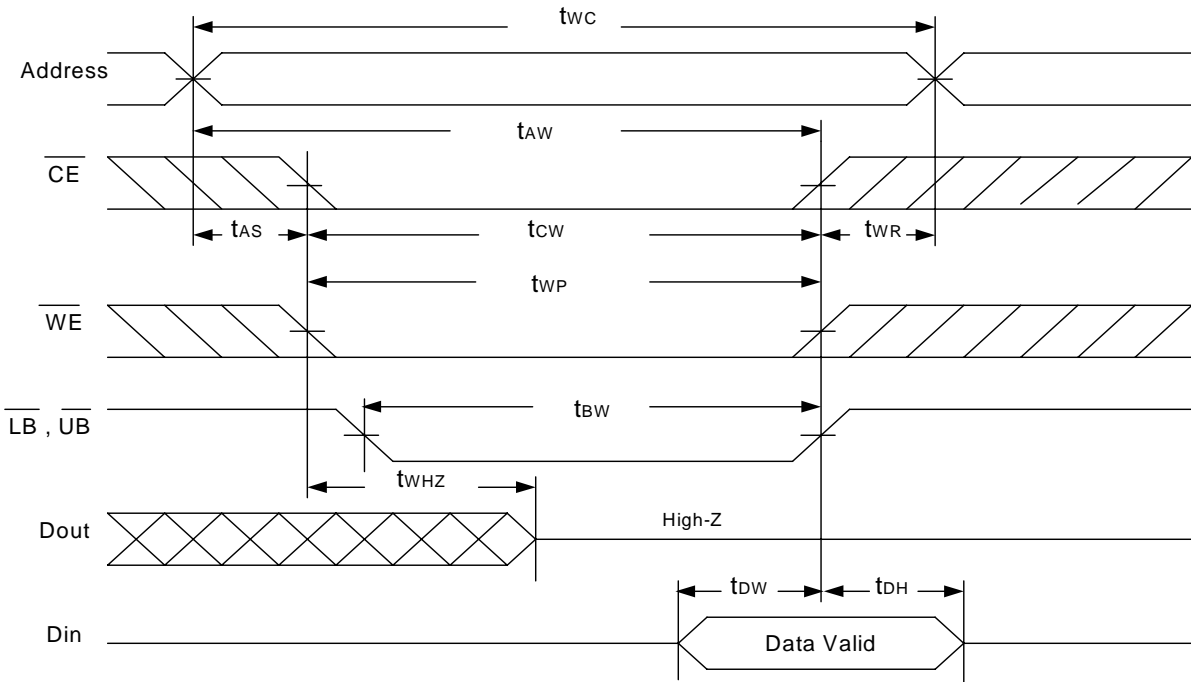


WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5,6)





WRITE CYCLE 3 (\overline{LB} , \overline{UB} Controlled) (1,2,5,6)



Notes :

1. \overline{WE} , \overline{CE} , \overline{LB} , \overline{UB} must be high during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} , low \overline{WE} , \overline{LB} or \overline{UB} = low.
3. During a \overline{WE} controlled write cycle with \overline{OE} low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} , \overline{LB} , \overline{UB} low transition occurs simultaneously with or after \overline{WE} low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

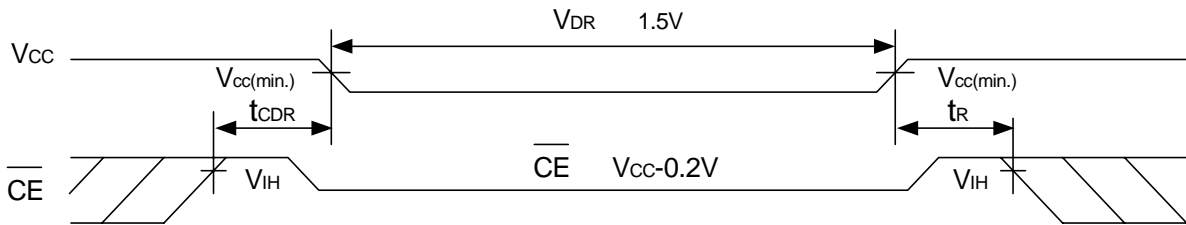


DATA RETENTION CHARACTERISTICS (T_A = -40 to 85 (I))

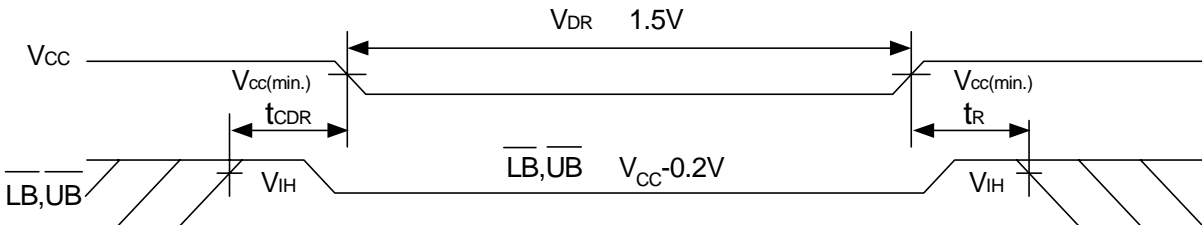
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{cc} for Data Retention	V _{DR}	\overline{CE} V _{CC} -0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =1.5V	- L	1	50	μA
		\overline{CE} V _{CC} -0.2V	- LL	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t _R		5	-	-	ms

DATA RETENTION WAVEFORM

Low V_{cc} Data Retention Waveform (1) (\overline{CE} controlled)



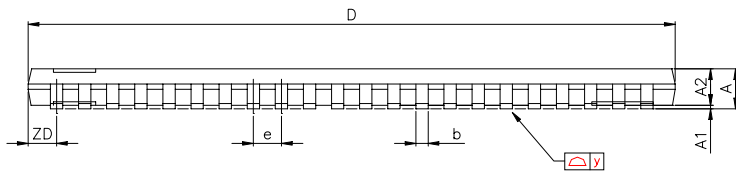
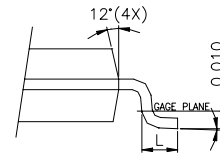
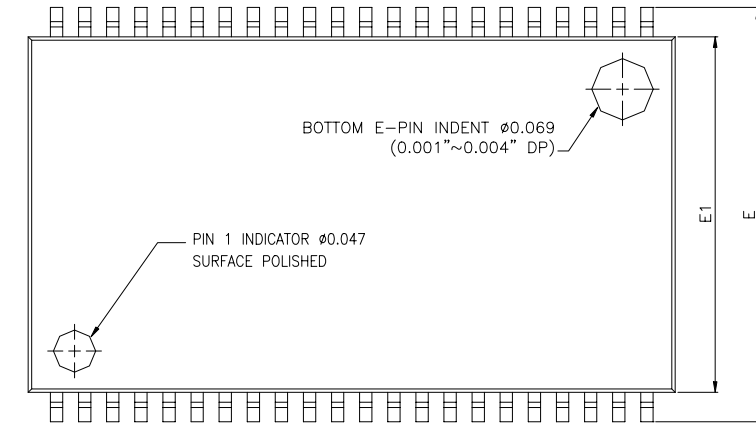
Low V_{cc} Data Retention Waveform (2) (\overline{LB} , \overline{UB} controlled)





PACKAGE OUTLINE DIMENSION

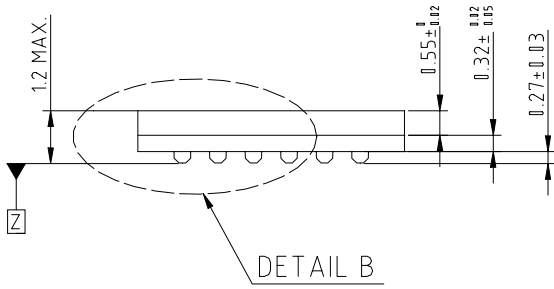
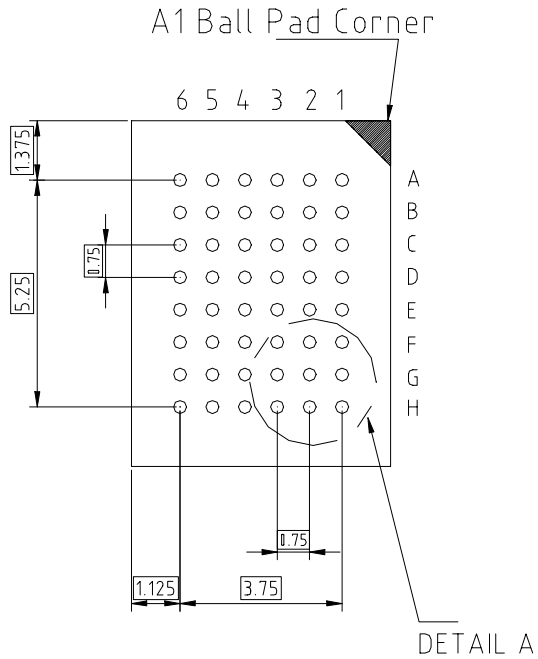
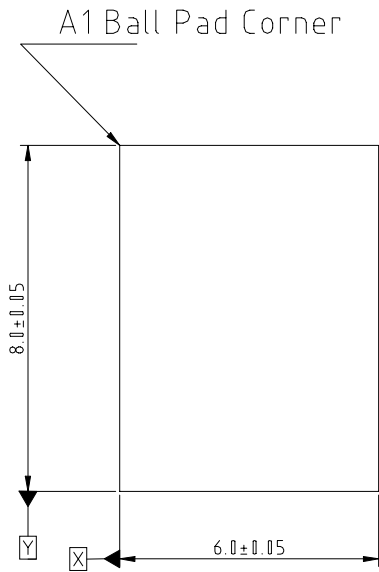
44-pin 400mil TSOP- Package Outline Dimension



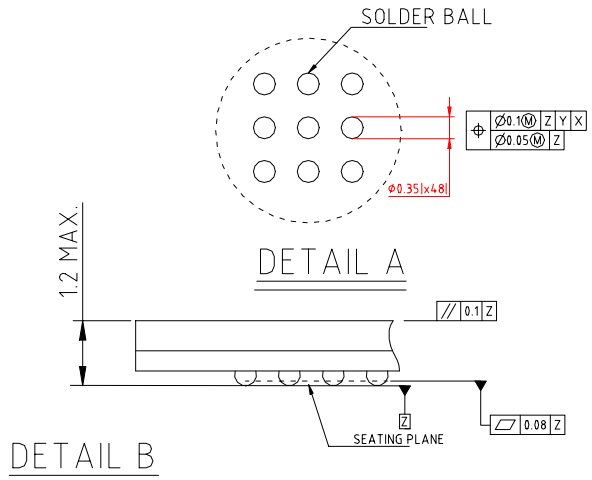
SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
	0°	-	5°	0°	-	5°



48-pin 6mm x 8mm TFBGA Package Outline Dimension



SIDE VIEW



DETAIL B



ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (µA) typ.	PACKAGE
UT62L25616MC-55LI	55	20	44 PIN TSOP-
UT62L25616MC-55LLI	55	2	44 PIN TSOP-
UT62L25616MC-70LI	70	20	44 PIN TSOP-
UT62L25616MC-70LLI	70	2	44 PIN TSOP-
UT62L25616BS-55LI	55	20	48 PIN TFBGA
UT62L25616BS-55LLI	55	2	48 PIN TFBGA
UT62L25616BS-70LI	70	20	48 PIN TFBGA
UT62L25616BS-70LLI	70	2	48 PIN TFBGA

ORDERING INFORMATION (for lead free product)

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (µA) typ.	PACKAGE
UT62L25616MCL-55LI	55	20	44 PIN TSOP-
UT62L25616MCL-55LLI	55	2	44 PIN TSOP-
UT62L25616MCL-70LI	70	20	44 PIN TSOP-
UT62L25616MCL-70LLI	70	2	44 PIN TSOP-
UT62L25616BSL-55LI	55	20	48 PIN TFBGA
UT62L25616BSL-55LLI	55	2	48 PIN TFBGA
UT62L25616BSL-70LI	70	20	48 PIN TFBGA
UT62L25616BSL-70LLI	70	2	48 PIN TFBGA



Rev. 1.5

UTRON

UT62L25616(I)
256K X 16 BIT LOW POWER CMOS SRAM

This page is left blank intentionally.