

REVISION HISTORY

REVISION	DESCRIPTION	Draft Date
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev.1.0	1. Separate Industrial and Commercial SPEC. 2. New waveforms. 3. Add access time 55ns range. 4. The symbols CE1# and OE# and WE# are revised as $\overline{CE1}$ and \overline{OE} and \overline{WE} .	Aug 7, 2001
Rev.1.1	1. Revised access time $\rightarrow 55/70/100$ ns - Rev 1.0: 55ns(max) for $V_{CC}=3.0V\sim 3.6V$ 70/100 ns(max) for $V_{CC}=2.7V\sim 3.6V$ 2. Revised "SYMBOL" : $\overline{CE1} \rightarrow \overline{CE}$ 3. Revised ABSOLUTE MAXIMUM RATINGS - V_{TERM} : -0.3 to 4.6 \rightarrow -0.5 to 4.6V - P_D : 1.0~1.5 \rightarrow 1W - I_{OUT} : 50 \rightarrow 20mA 4. Revised DC CHARACTERISTICS - V_{IH} : 2.0 \rightarrow 2.2V 5. Revised AC CHARACTERISTICS - t_{OH} & t_{BLZ} : 5 \rightarrow 10ns 6. Revised 48-pin TFBGA package outline dimension : - ball diameter : 0.3mm \rightarrow 0.35mm	Nov 8 , 2002
Rev.1.2	1. Revised Standby current (LL-Version) : 3uA(typ) \rightarrow 2uA(typ) 2. Revised operating current (I_{CCmax}) : 45/35/25mA \rightarrow 40/30/25mA 3. Revised DC CHARACTERISTICS : a. Operating Power Supply Current (I_{CC}) 55ns (max) : 45 \rightarrow 40mA 70ns (typ) : 25 \rightarrow 20mA, 70ns (max) : 35 \rightarrow 30mA 100ns (Typ) : 20 \rightarrow 16mA b. Standby current (CMOS) : LL-version (typ) : 3 \rightarrow 2uA, 25 \rightarrow 20uA	Dec 3, 2002
Rev.1.3	1. Revised V_{OH} (Typ) : NA \rightarrow 2.7V 2. Add $V_{IH}(max)=V_{CC}+2.0V$ for pulse width less than 10ns. $V_{IL}(min)=V_{SS}-2.0V$ for pulse width less than 10ns. 3. Add order information for lead free product	May 6, 2003



FEATURES

- Fast access time : 55/70/100ns
- CMOS low power operating
Operating current : 40/30/25 (Icc,max.)
Standby current : 20uA (TYP.) L-version
2uA (TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operation temperature:
Industrial : -40 ~85
- All TTL compatible inputs and outputs
- Fully static operation
- Three state outputs
- Data retention voltage:1.5V (min.)
- Data byte control : \overline{LB} (I/O1~I/O8)
 \overline{UB} (I/O9~I/O16)
- Package : 48-pin 6mm x 8mm TFBGA

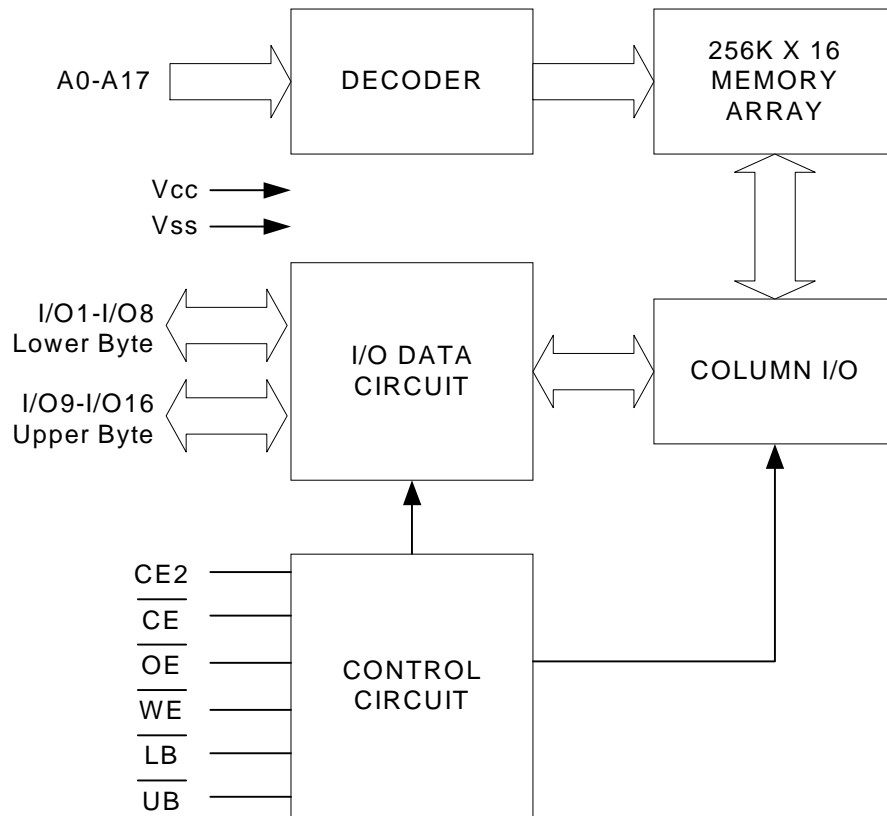
GENERAL DESCRIPTION

The UT62L25716(I) is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

The UT62L25716(I) operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L25716(I) is designed for low power system applications. It is particularly well suited for use in high-density low power system applications.

FUNCTIONAL BLOCK DIAGRAM



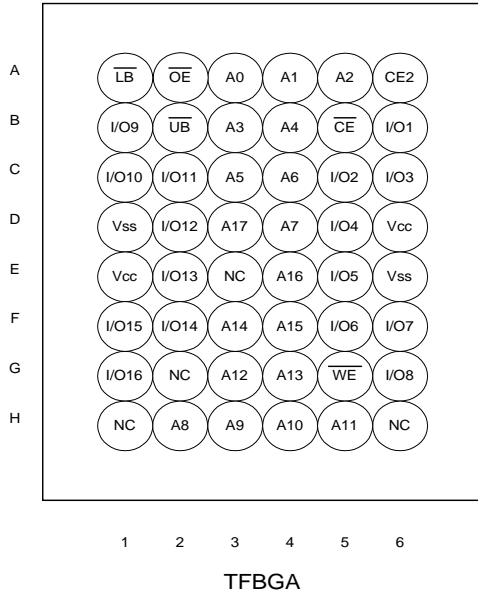


UTRON

Rev. 1.3
SRAM

UT62L25716(I)
256K X 16 BIT LOW POWER CMOS

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
\overline{CE} , CE2	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB}	Lower-byte Control
\overline{UB}	Upper-byte Control
V _{CC}	Power Supply
V _{SS}	Ground
NC	No Connection

TRUTH TABLE

MODE	\overline{CE}	CE2	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O OPERATION		SUPPLY CURRENT
							I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	L	X	X	X	X	High - Z	High - Z	
	X	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	H	H	H	X	L	High - Z	High - Z	
Read	L	H	L	H	L	H	D _{OUT}	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	H	L	H	H	L	High - Z	D _{OUT}	
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	
Write	L	H	X	L	L	H	D _{IN}	High - Z	I _{CC} , I _{CC1} , I _{CC2}
	L	H	X	L	H	L	High - Z	D _{IN}	
	L	H	X	L	L	L	D _{IN}	D _{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Industrial	T_A	-40 to 85
Storage Temperature	T_{STG}	-65 to 150	
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 secs)	T_{solder}	260	

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7V \sim 3.6V$, $T_A = -40$ to 85 (I))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Power Voltage	V_{CC}		2.7	3.0	3.6	V	
Input High Voltage	V_{IH}^{*1}		2.2	-	$V_{CC}+0.3$	V	
Input Low Voltage	V_{IL}^{*2}		-0.2	-	0.6	V	
Input Leakage Current	I_{LI}	$V_{SS} \quad V_{IN} \quad V_{CC}$	-1	-	1	μA	
Output Leakage Current	I_{LO}	$V_{SS} \quad V_{IO} \quad V_{CC}$; Output Disable	-1	-	1	μA	
Output High Voltage	V_{OH}	$I_{OH} = -1mA$	2.2	2.7	-	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V	
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty $I/O=0mA$, $\overline{CE}=V_{IL}$	55	-	30	40	mA
			70	-	20	30	mA
			100	-	16	25	mA
Average Operation Current	I_{CC1}	100%duty, $I_{IO}=0mA$, $\overline{CE} = 0.2V$, other pins at 0.2V or $V_{CC}-0.2V$	$T_{cycle}=1\mu s$	-	4	5	mA
	I_{CC2}		$T_{cycle}=500ns$	-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}=V_{IH}$, other pins = V_{IL} or V_{IH}	-	0.3	0.5	mA	
Standby Current (CMOS)	I_{SB1}	$\overline{CE}=V_{CC}-0.2V$ other pins at 0.2V or $V_{CC}-0.2V$	-L	-	20	80	μA
			-LL	-	2	20	μA

Notes:

1. Overshoot : $V_{CC}+2.0v$ for pulse width less than 10ns.
2. Undershoot : $V_{SS}-2.0v$ for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

**CAPACITANCE** ($T_A=25$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF}$, $I_{OH}/I_{OL} = -1\text{mA}/2.1\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 2.7\text{V}\sim 3.6\text{V}$, $T_A = -40$ to 85 (I))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L25716(I)-55		UT62L25716(I)-70		UT62L25716(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns
\overline{LB} , \overline{UB} Access Time	t_{BA}	-	55	-	70	-	100	ns
\overline{LB} , \overline{UB} to High-Z Output	t_{BHZ}	-	25	-	30	-	40	ns
\overline{LB} , \overline{UB} to Low-Z Output	t_{BLZ}	10	-	10	-	10	-	ns

(2) WRITE CYCLE

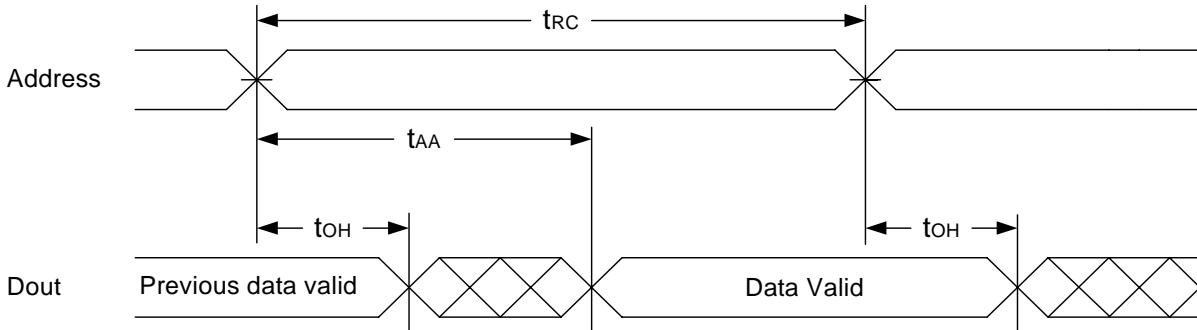
PARAMETER	SYMBOL	UT62L25716(I)-55		UT62L25716(I)-70		UT62L25716(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}^*	-	30	-	30	-	40	ns
\overline{LB} , \overline{UB} Valid to End of Write	t_{BW}	45	-	60	-	80	-	ns

* These parameters are guaranteed by device characterization, but not production tested.

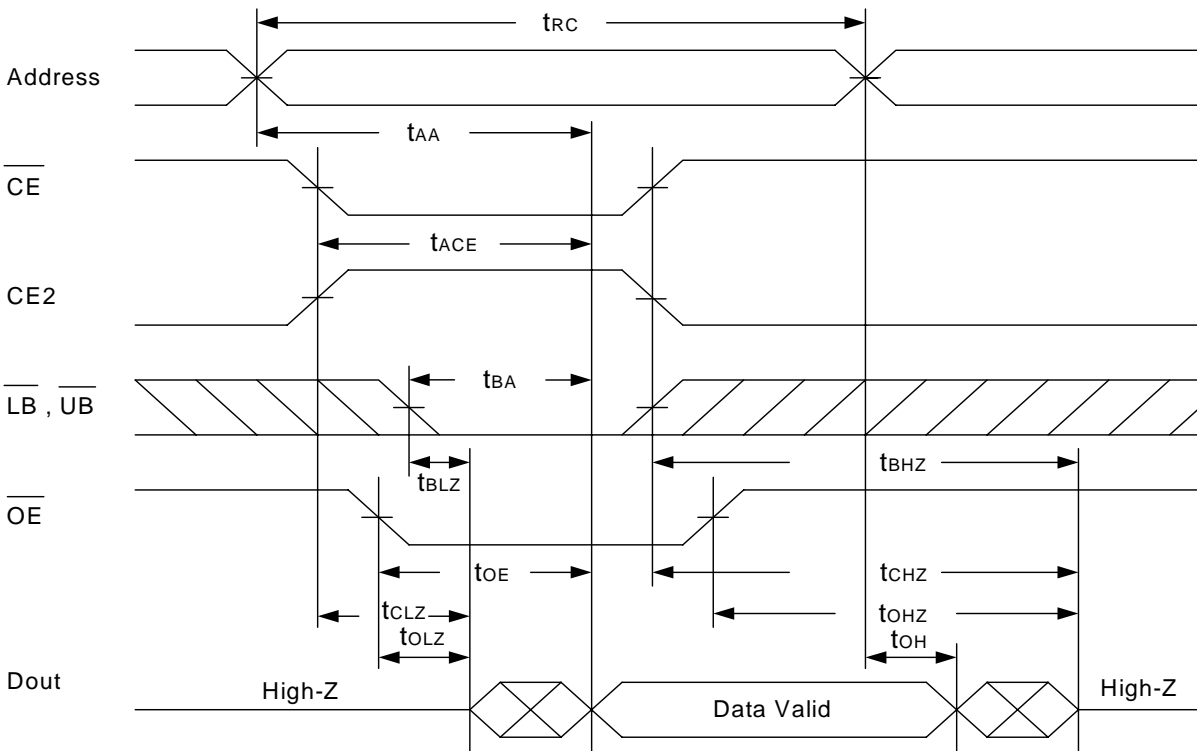


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (\overline{CE} and CE2 and \overline{OE} Controlled) (1,3,4,5)

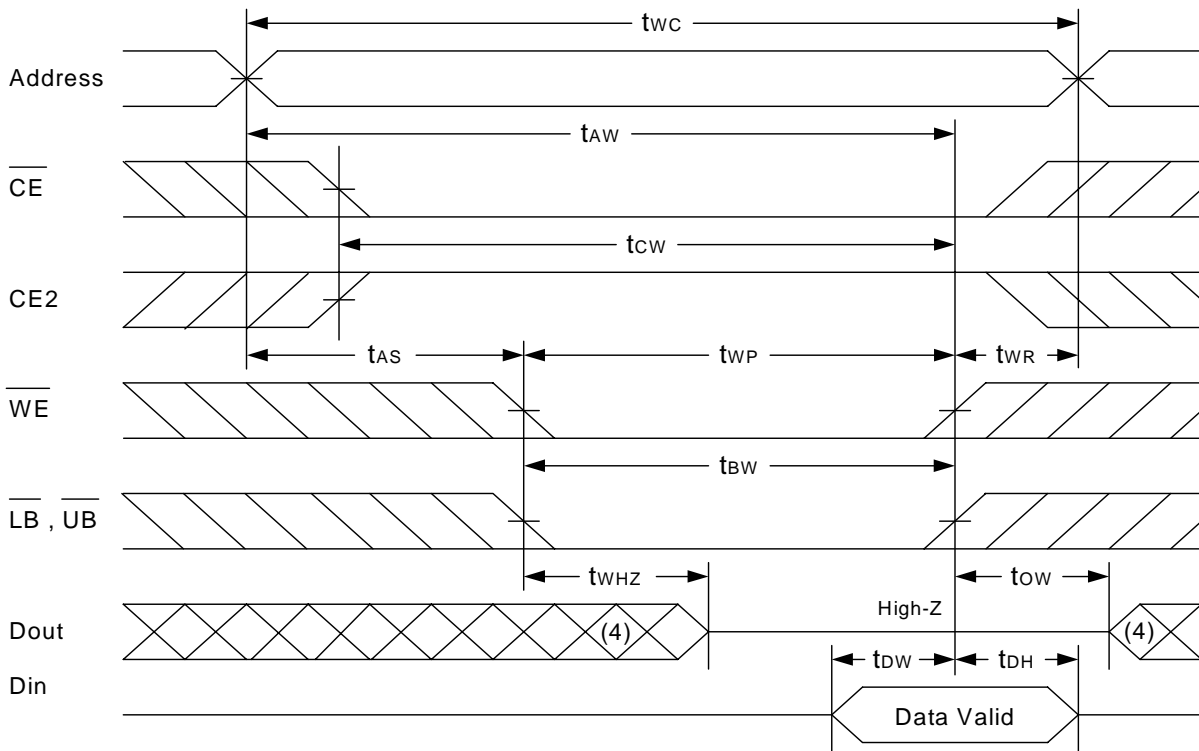


Notes :

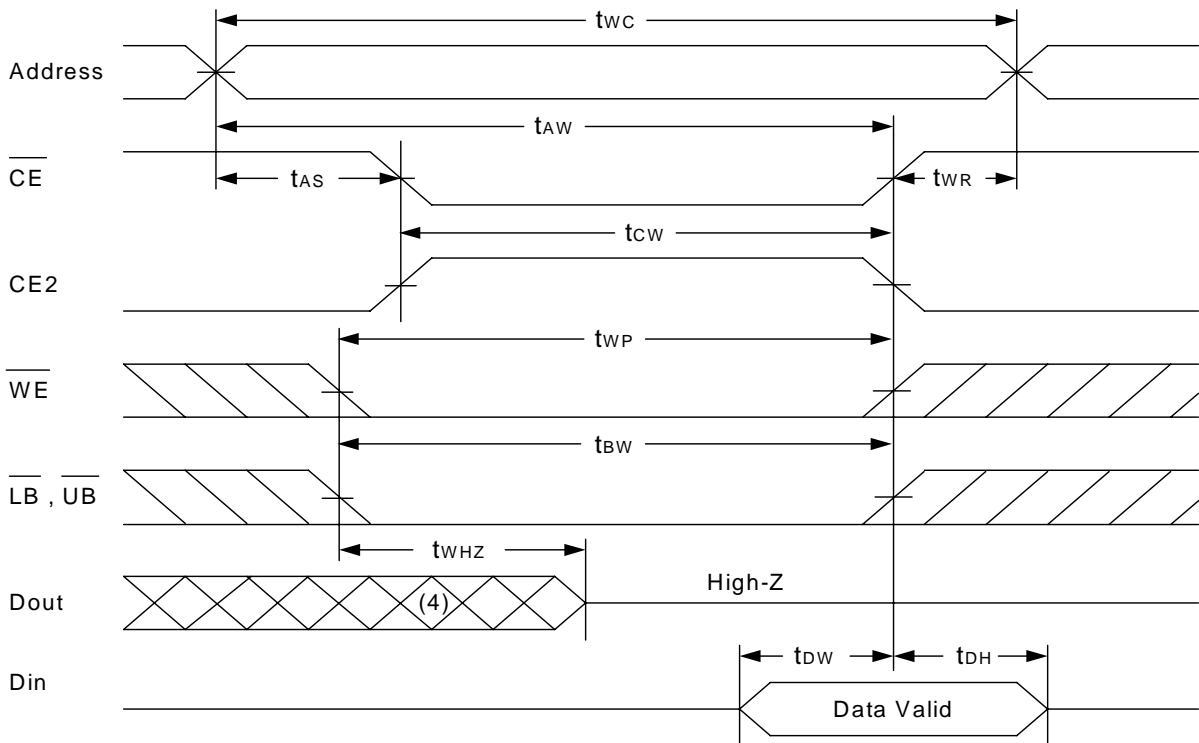
1. \overline{WE} is high for read cycle.
2. Device is continuously selected \overline{OE} =low, \overline{CE} =low, CE2=high, \overline{LB} or \overline{UB} =low.
3. Address must be valid prior to or coincident with \overline{CE} =low, CE2=high, \overline{LB} or \overline{UB} =low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5,6)

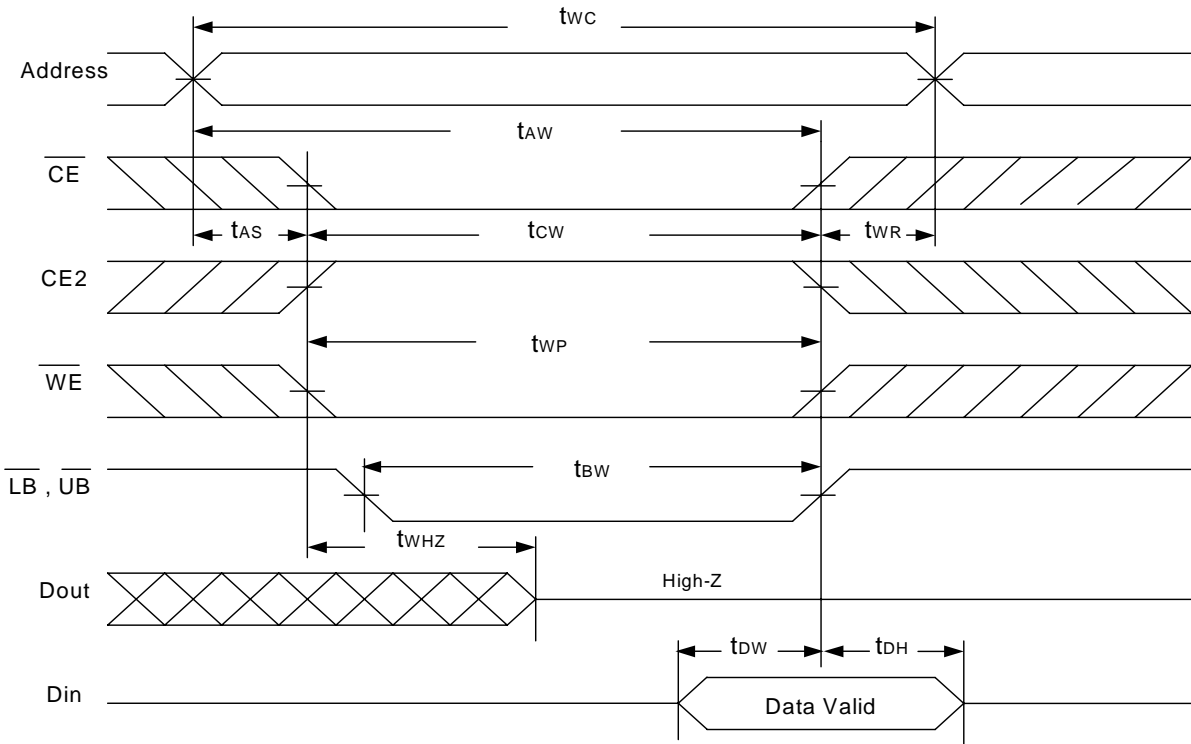


WRITE CYCLE 2 (\overline{CE} and $\overline{CE2}$ Controlled) (1,2,5,6)





WRITE CYCLE 3 (\overline{LB} , \overline{UB} Controlled) (1,2,5,6)



Notes :

1. \overline{WE} , \overline{CE} , \overline{LB} , \overline{UB} must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} , high CE2, low \overline{WE} , \overline{LB} or \overline{UB} = low.
3. During a \overline{WE} controlled write cycle with \overline{OE} low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} , \overline{LB} , \overline{UB} low transition and CE2 high transition occurs simultaneously with or after \overline{WE} low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

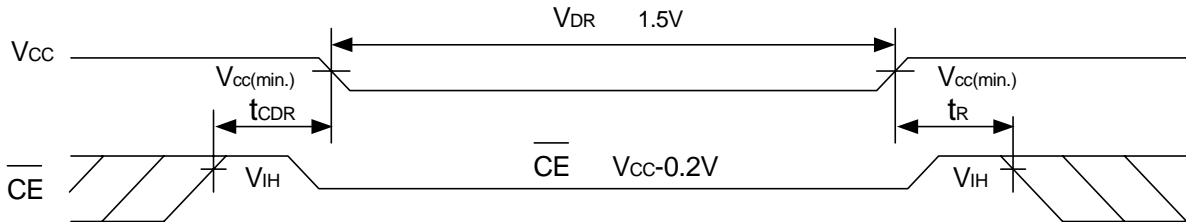


DATA RETENTION CHARACTERISTICS ($T_A = -40$ to 85 (I))

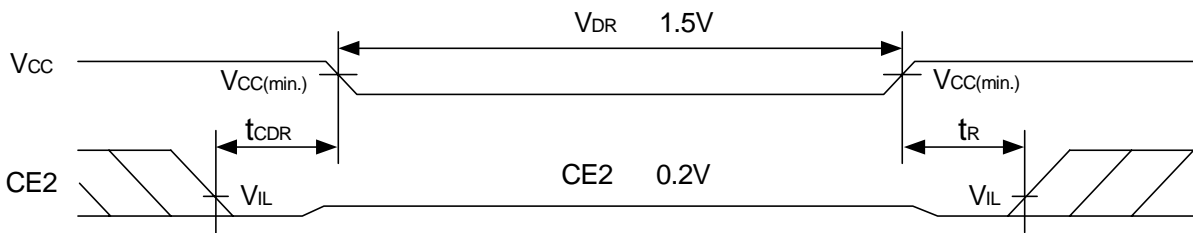
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V _{DR}	\overline{CE} V _{CC} -0.2V or CE2 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} =1.5V	- L	1	50	μ A
		\overline{CE} V _{CC} -0.2V or CE2 0.2V	- LL	0.5	20	μ A
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms
Recovery Time	t _R		5	-	-	ms

DATA RETENTION WAVEFORM

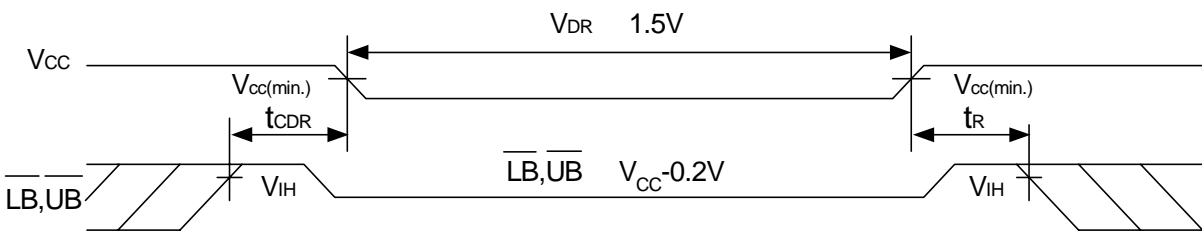
Low Vcc Data Retention Waveform (1) (\overline{CE} controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)



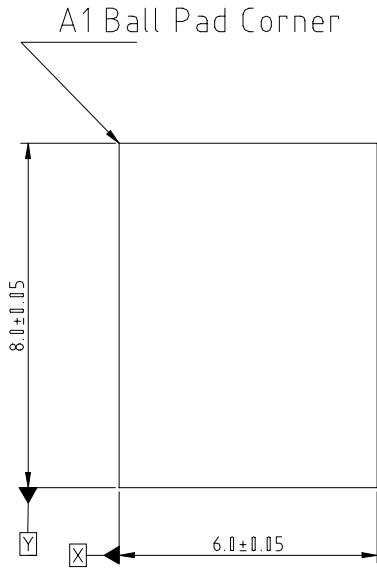
Low Vcc Data Retention Waveform (3) ($\overline{LB}, \overline{UB}$ controlled)



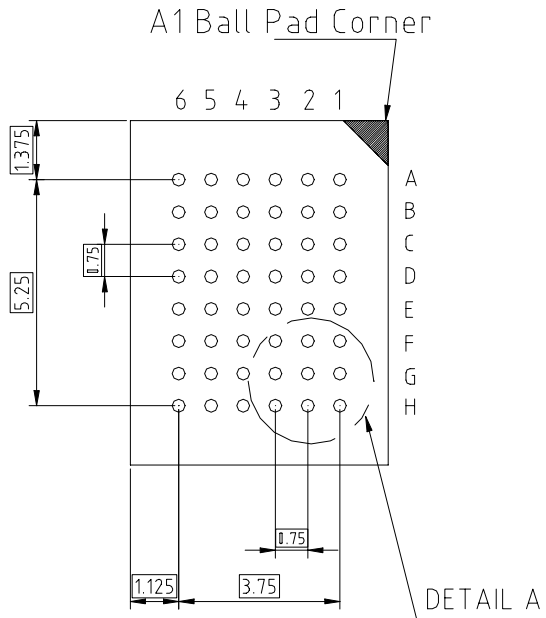


PACKAGE OUTLINE DIMENSION

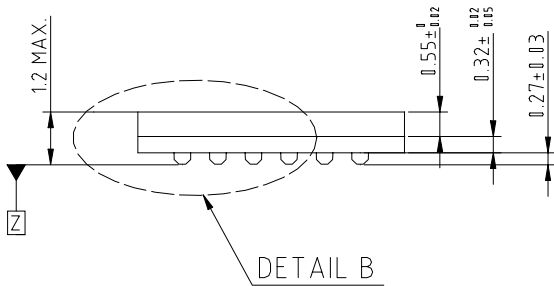
48 pin 6.0mmX8.0mm TFBGA Package Outline Dimension



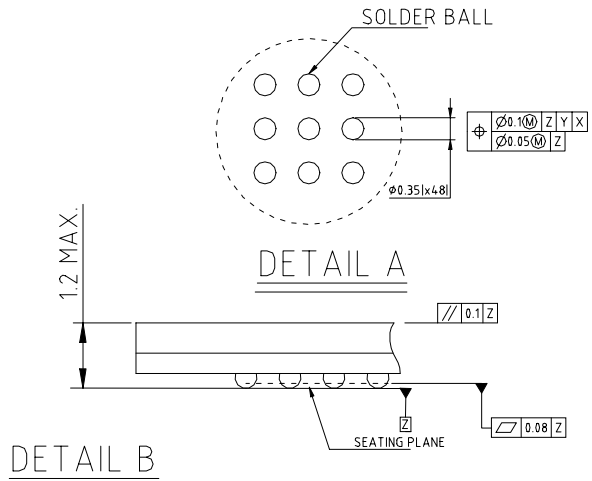
TOP VIEW (DIE VIEW)



BOTTOM VIEW (BALL SIDE)



SIDE VIEW



DETAIL B



UTRON

UT62L25716(I)

Rev. 1.3

256K X 16 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L25716BS-55LI	55	20	48 PIN BGA
UT62L25716BS-55LLI	55	2	48 PIN BGA
UT62L25716BS-70LI	70	20	48 PIN BGA
UT62L25716BS-70LLI	70	2	48 PIN BGA
UT62L25716BS-100LI	100	20	48 PIN BGA
UT62L25716BS-100LLI	100	2	48 PIN BGA

ORDERING INFORMATION (for lead free product)

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μ A) typ.	PACKAGE
UT62L25716BSL-55LI	55	20	48 PIN BGA
UT62L25716BSL-55LLI	55	2	48 PIN BGA
UT62L25716BSL-70LI	70	20	48 PIN BGA
UT62L25716BSL-70LLI	70	2	48 PIN BGA
UT62L25716BSL-100LI	100	20	48 PIN BGA
UT62L25716BSL-100LLI	100	2	48 PIN BGA



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