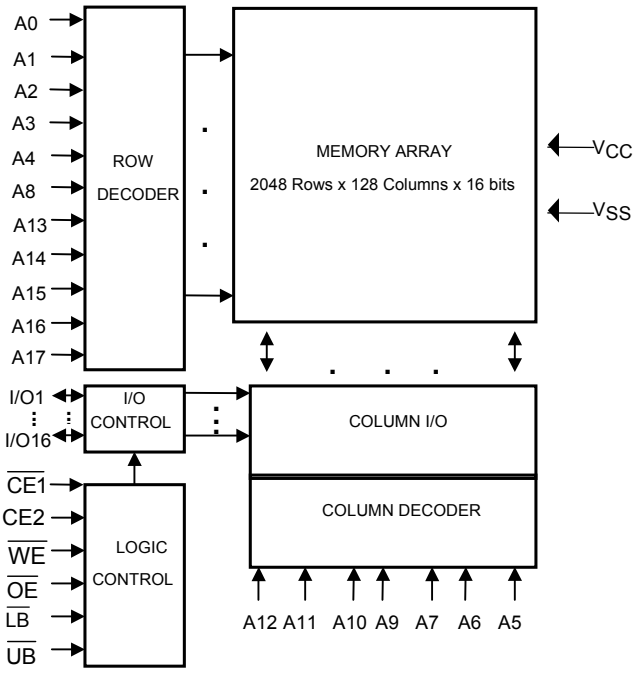
FEATURES

- High speed access time :
  55ns(max) for Vcc=3.0V~3.6V
  70/100 ns(max) for Vcc=2.7V~3.6V
- CMOS Low power consumption
- Operation current : 45/35/25 (Icc,max.)
- Standby: 20uA (TYP.) L-version
  3uA (TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operation temperature:
  Commercial : 0℃~70℃
  Extended : -20℃~80℃
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage:1.5V (min.)
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
  $\overline{UB}$ (I/O9~I/O16)
- Package : 48-pin 6mm × 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The UT62L25716 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

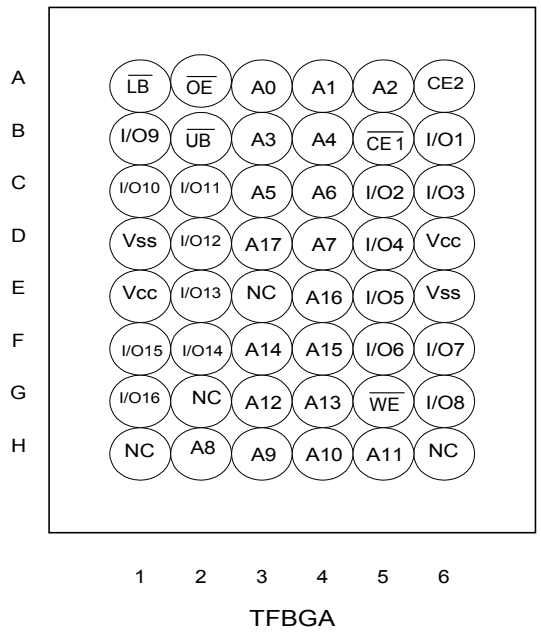
The UT62L25716 operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L25716 is designed for low power system applications. It is particularly well suited for use in high-density low power system applications.

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	High-Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION



TFBGA

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.3 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70	℃
	Extended	T_A	-20 to 80	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1.0~1.5	W
DC Output Current		I_{OUT}	20	mA
Soldering Temperature (under 10 secs)		Tsolder	260.10	℃.sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1-I/O8	I/O9-I/O16	SUPPLY CURRENT
Standby	H	X	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	L	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	X	X	X	H	H	High – Z	High – Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	L	X	High – Z	High – Z	I_{CC1},I_{CC2}
	L	H	H	H	X	L	High – Z	High – Z	
Read	L	H	L	H	L	H	D_{OUT}	High – Z	I_{CC1},I_{CC2}
	L	H	L	H	H	L	High – Z	D_{OUT}	
	L	H	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	H	X	L	L	H	D_{IN}	High – Z	I_{CC1},I_{CC2}
	L	H	X	L	H	L	High – Z	D_{IN}	
	L	H	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.(Must be low or high state)

DC ELECTRICAL CHARACTERISTICS (Vcc = 2.7V~3.6V, TA = 0℃ to 70℃ / -20℃ to 80℃(E))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	Vcc			2.7	3.0	3.6	V
Input High Voltage	V_{IH}			2.0	-	Vcc+0.3	V
Input Low Voltage	V_{IL}			- 0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq$Vcc		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq$Vcc, Output Disabled		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH}= - 1.0mA		2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time =min,100% duty, $I_{I/O}$=0mA, CE2=V_{IH}, $\overline{CE1}$=V_{IL}, V_{IN}=V_{IH} or V_{IL},	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
	Icc1	Cycle time = 1us,100% duty, $I_{I/O}$=0mA, $\overline{CE1} \leqq$0.2V, CE2$\geqq$Vcc-0.2V other pins at 0.2V or Vcc-0.2V,		-	4	5	mA
	Icc2	Cycle time =500ns,100% duty, $I_{I/O}$=0mA, $\overline{CE1} \leqq$0.2V, CE2$\geqq$Vcc-0.2V other pins at 0.2V or Vcc-0.2V,		-	8	10	mA
Standby Current	I_{SB}	$\overline{CE1}$=V_{IH},or CE2=V_{IH},other pins =V_{IH} or V_{IL},		-	0.3	0.5	mA
Standby Current	I_{SB1}	$\overline{CE1} \geqq V_{CC}$-0.2V,or CE2 $\leqq$0.2V, other pins at 0.2V or Vcc-0.2V,	-L	-	20	80	μA
			-LL	-	3	25	μA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS (VCC = 2.7V~3.6V , TA = 0℃ to 70℃ / -20℃ to 80℃(E))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L25716-55*		UT62L25716-70		UT62L25716-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	55	-	70	-	100	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{HZB}	-	25	-	30	0	40	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{LZB}	0	-	0	-	0	-	ns

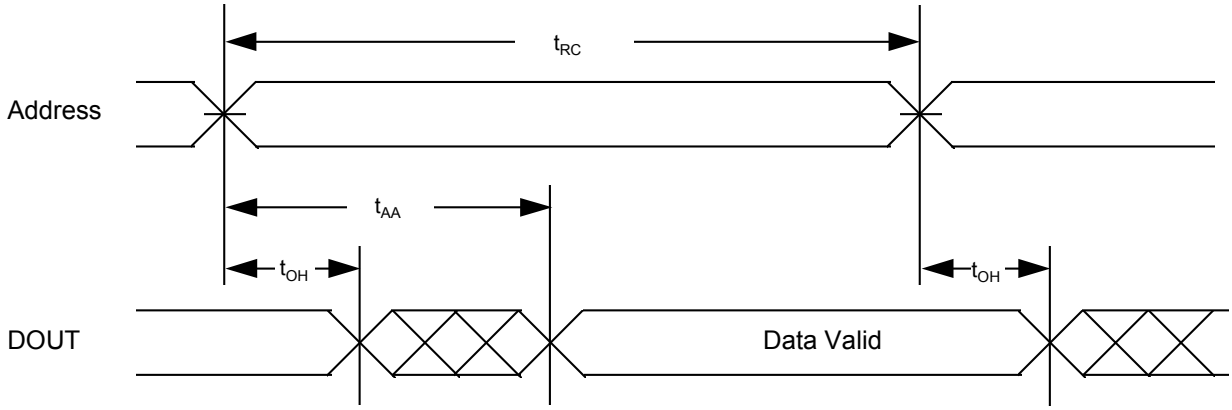
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L25716-55*		UT62L25716-70		UT62L25716-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{PWB}	45	-	60	-	80	-	ns

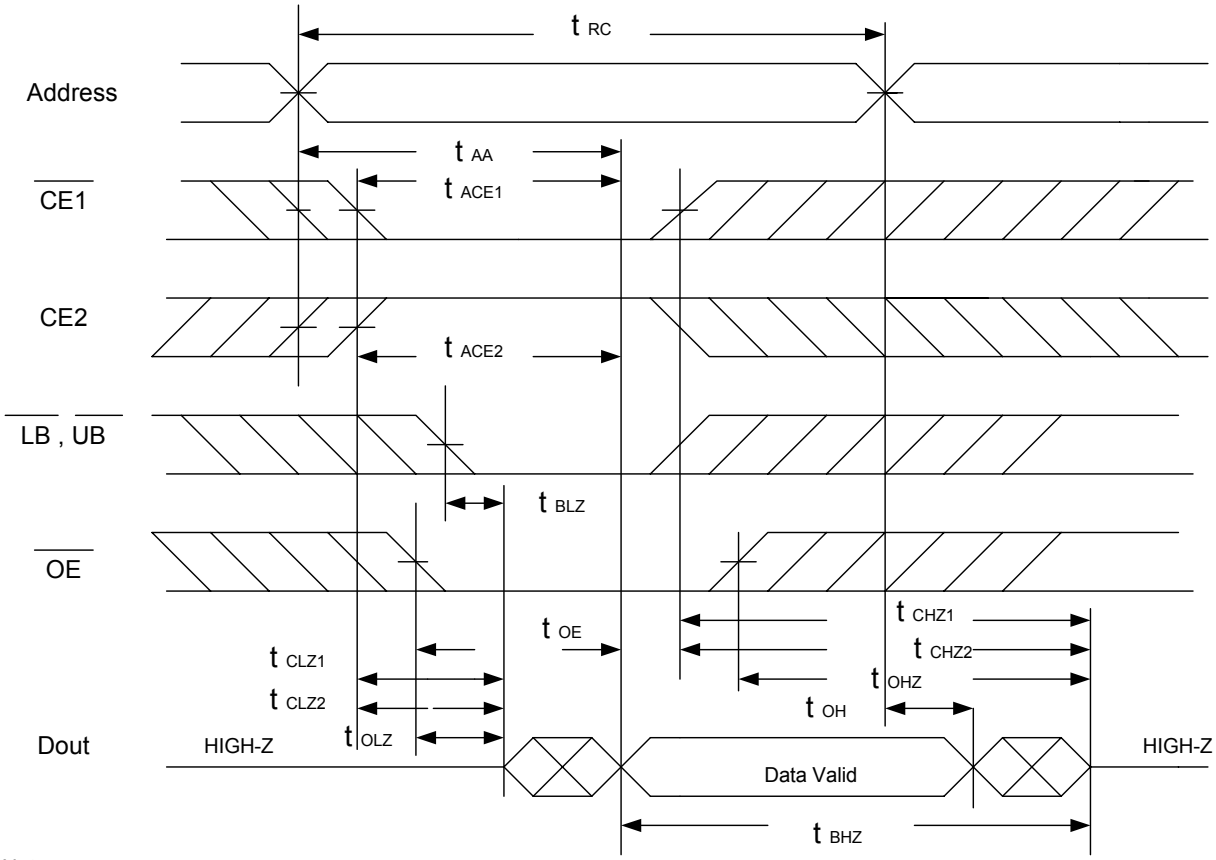
* These parameters are guaranteed by device characterization, but not production tested.
* 55ns for 3.0V~3.6V.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



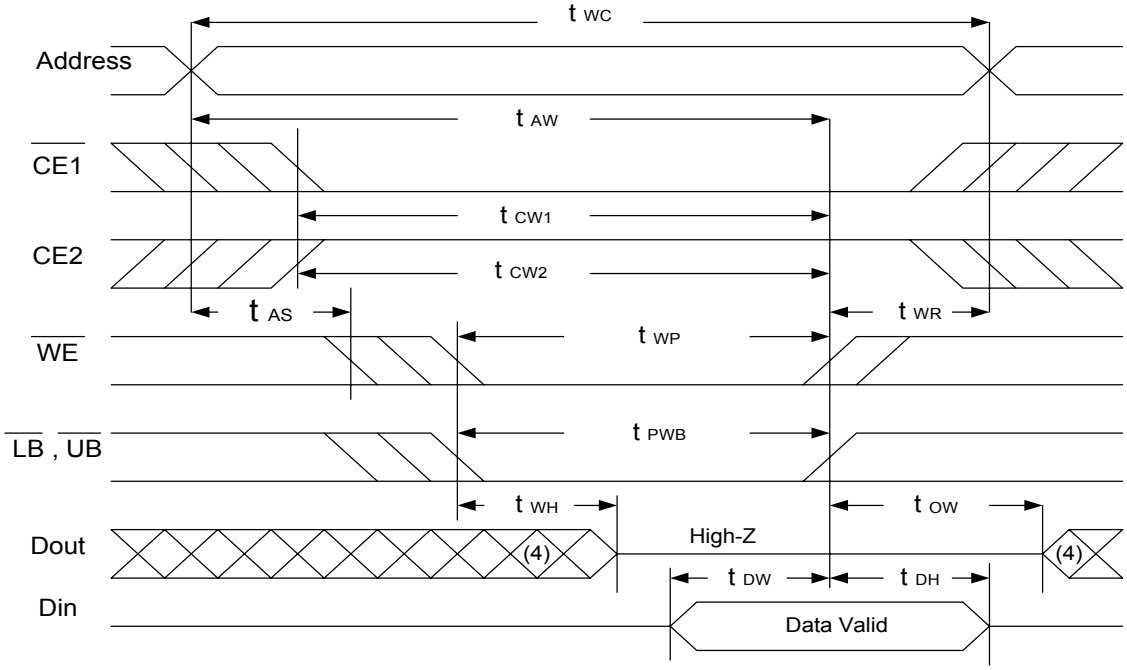
READ CYCLE 2 ($\overline{CE1}$ and CE2 and $\overline{OE}$ Controlled) (1,3,5,6)



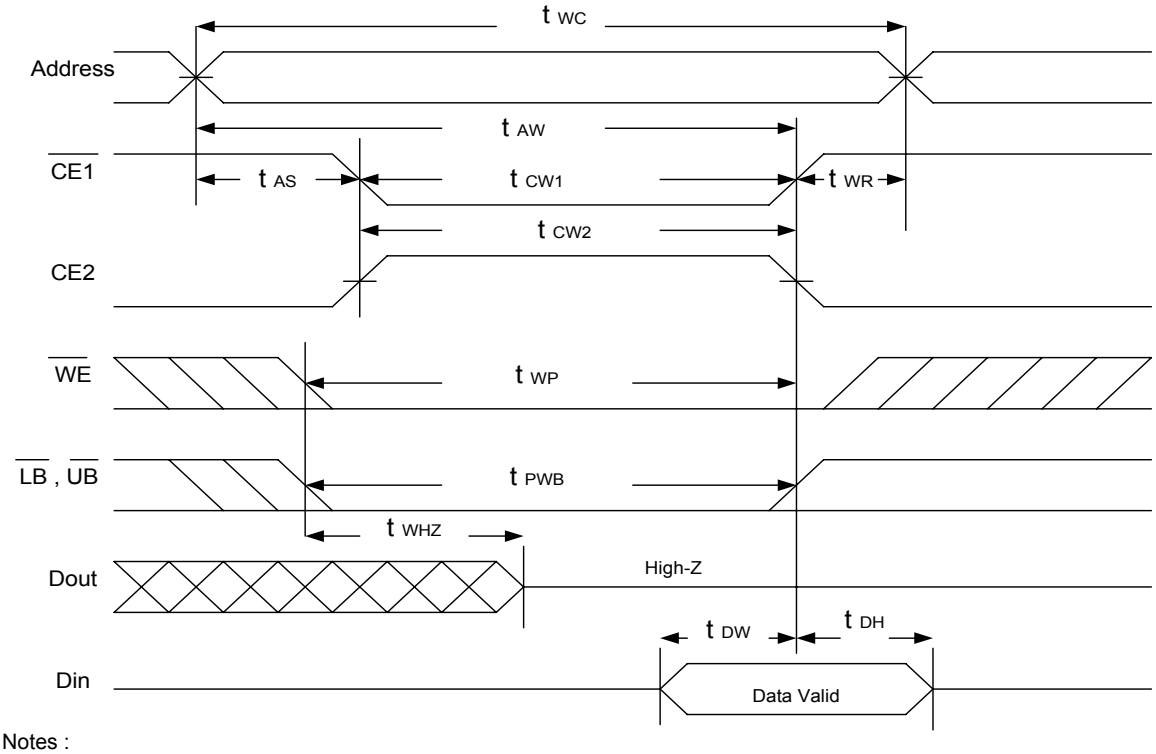
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE1}$ =V_{IL} and CE2=V_{IH}. and $\overline{LB}$ =V_{IL} and $\overline{UB}$ =V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ and CE2 and $\overline{LB}$ and $\overline{UB}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



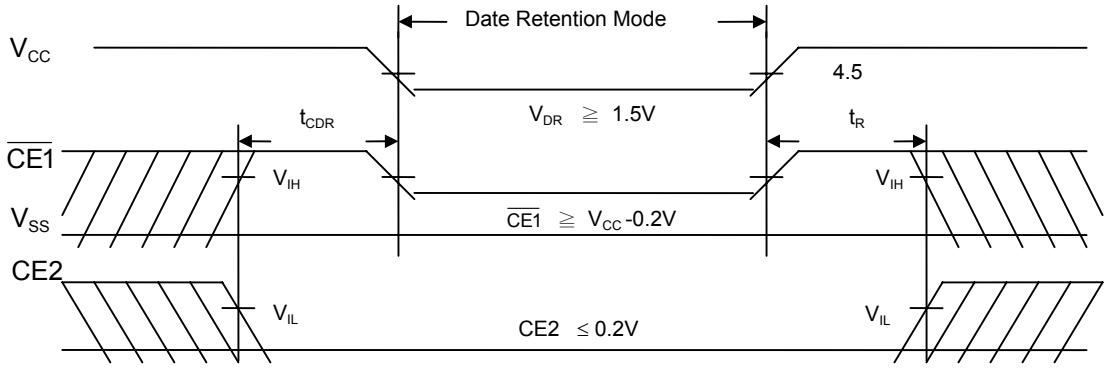
Notes :

1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (TA = 0℃ to 70℃ / -20℃ to 80℃(E))

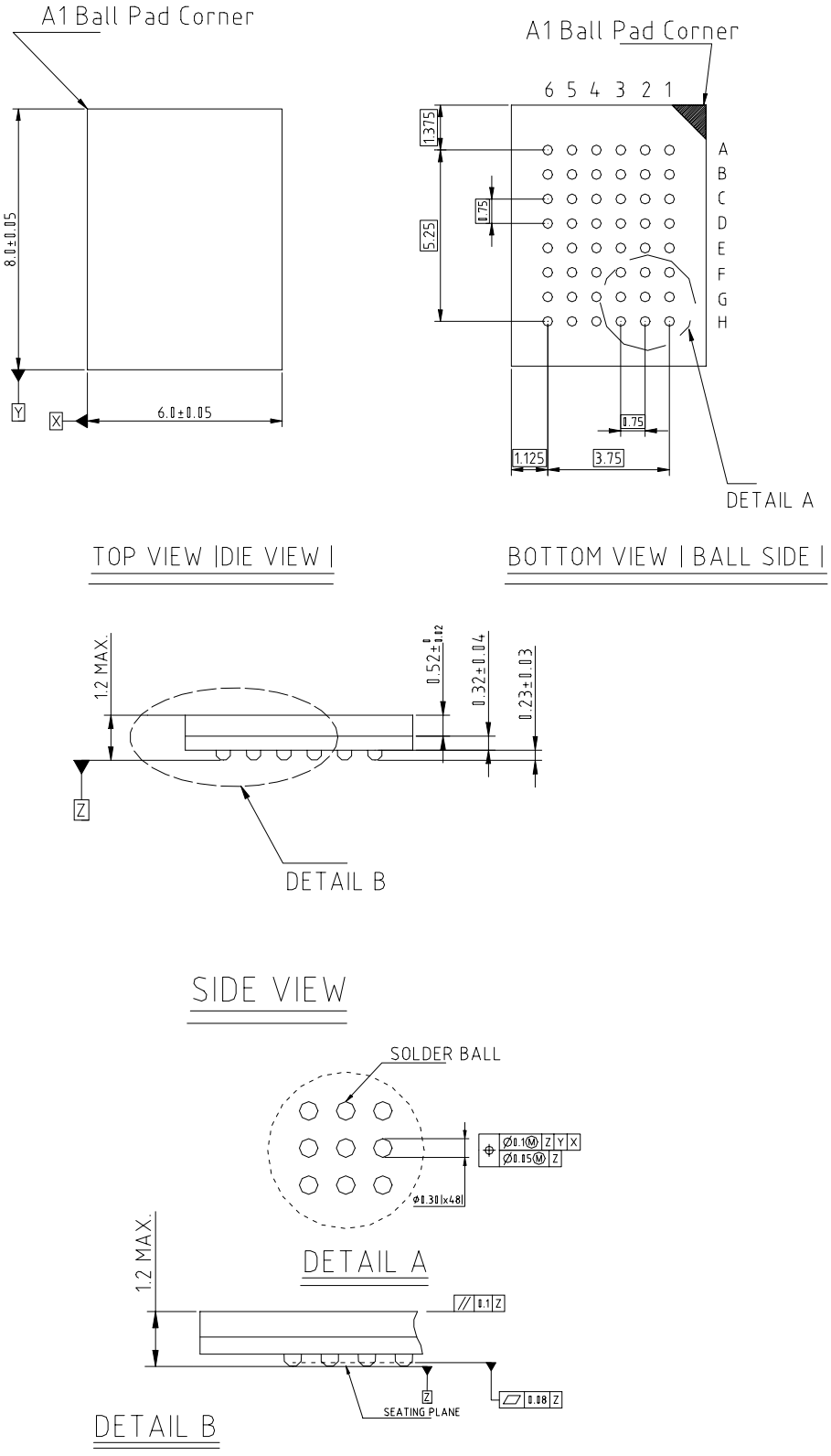
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2≦0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-	1	50	µA
		$\overline{CE1} \geqq V_{CC}$-0.2V or CE2≦0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

48 pin 6.0mmX8.0mm TFBGA Package Outline Dimension



ORDERING INFORMATION

COMMERCIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA max)	PACKAGE
UT62L25716BS-55L	55	20	48 PIN BGA
UT62L25716BS-55LL	55	3	48 PIN BGA
UT62L25716BS-70L	70	20	48 PIN BGA
UT62L25716BS-70LL	70	3	48 PIN BGA

EXTENDED TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA max)	PACKAGE
UT62L25716BS-55LE	55	20	48 PIN BGA
UT62L25716BS-55LLE	55	3	48 PIN BGA
UT62L25716BS-70LE	70	20	48 PIN BGA
UT62L25716BS-70LLE	70	3	48 PIN BGA

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev.1.0	1. Separate Industrial and Commercial SPEC. 2. New waveforms. 3. Add access time 55ns range. 4. The symbols CE1# and OE# and WE# are revised as. $\overline{CE1}$ and $\overline{OE}$ and $\overline{WE}$.	Jul. 12,2001

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