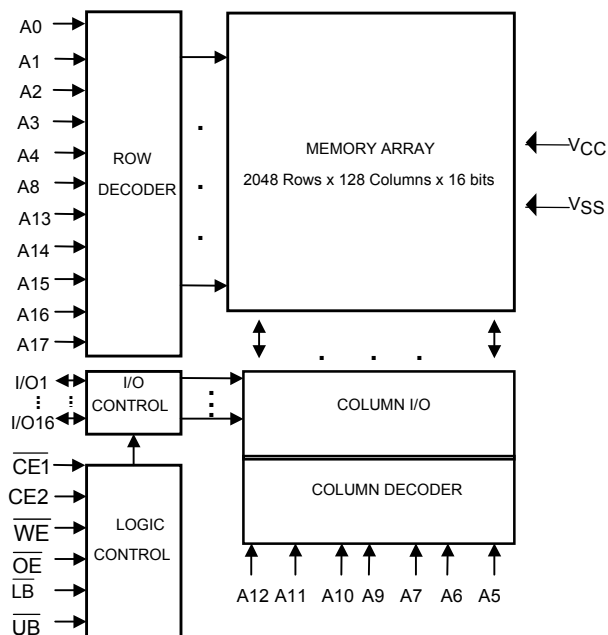




### FEATURES

- Fast access time :70/100 ns
- CMOS Low power consumption  
Operation current : 30/20 (Icc,max.)  
Standby: 20uA (TYP.) L-version  
2uA (TYP.) LL-version
- Single 2.3V~2.7V power supply
- Operation temperature:  
Commercial : 0°C~70°C  
Extended : -20°C~80°C
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Data byte control :  $\overline{LB}$  (I/O1~I/O8)  
 $\overline{UB}$  (I/O9~I/O16)
- Package : 48-pin 6mm × 8mm TFBGA

### FUNCTIONAL BLOCK DIAGRAM



### GENERAL DESCRIPTION

The UT62V25716 is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

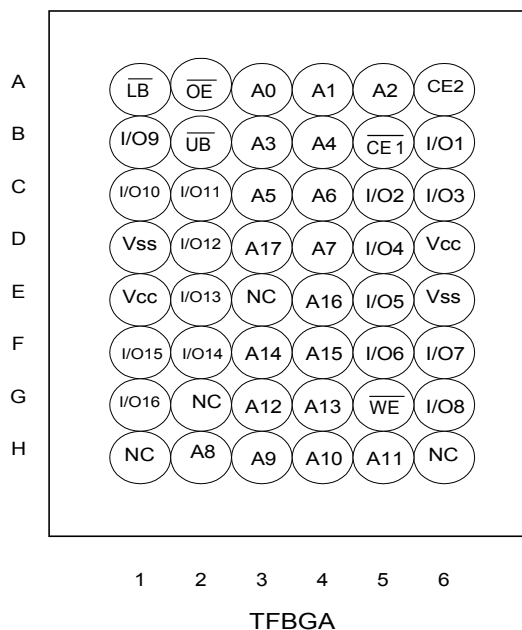
The UT62V25716 operates from a single 2.3V~2.7V power supply and all inputs and outputs are fully TTL compatible.

The UT62V25716 is designed for low power system applications. It is particularly well suited for use in high-density low power system applications.

### PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE1}$ , CE2	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	High-Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection

### PIN CONFIGURATION



**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V <sub>SS</sub>	V <sub>TERM</sub>	-0.3 to 4.6	V
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70
	Extended	T <sub>A</sub>	-20 to 80
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1.0~1.5	W
DC Output Current	I <sub>OUT</sub>	20	mA
Soldering Temperature (under 10 secs)	T <sub>solder</sub>	260.10	°C.sec

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	CE1	CE2	OE	WE	LB	UB	I/O1-I/O8	I/O9-I/O16	SUPPLY CURRENT
Standby	H	X	X	X	X	X	High - Z	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	L	X	X	X	X	High - Z	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
	X	X	X	X	H	H	High - Z	High - Z	I <sub>SB</sub> , I <sub>SB1</sub>
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
	L	H	H	H	X	L	High - Z	High - Z	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
Read	L	H	L	H	L	H	D <sub>OUT</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
	L	H	L	H	H	L	High - Z	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
	L	H	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
Write	L	H	X	L	L	H	D <sub>IN</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
	L	H	X	L	H	L	High - Z	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>
	L	H	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub> , I <sub>CC1</sub> , I <sub>CC2</sub>

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care. (Must be low or high state)

**DC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 2.3V~2.7V, T<sub>A</sub> = 0°C to 70°C / -20°C to 80°C(E))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Power Voltage	V <sub>CC</sub>		2.3	2.5	2.7	V	
Input High Voltage	V <sub>IH</sub>		2.0	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub>		-0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>SS</sub> ≤ V <sub>I/O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -0.5mA	2.0	-	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 0.5mA	-	-	0.4	V	
Operating Power Supply Current	I <sub>CC</sub>	Cycle time = min, 100% duty, I <sub>I/O</sub> = 0mA, CE2 = V <sub>IH</sub> , CE1 = V <sub>IL</sub> , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> ,	70	-	20	30	mA
			100	-	15	20	mA
	I <sub>CC1</sub>	Cycle time = 1us, 100% duty, I <sub>I/O</sub> = 0mA, CE1 ≤ 0.2V, CE2 ≥ V <sub>CC</sub> -0.2V, other pins at 0.2V or V <sub>CC</sub> -0.2V,	-	3	4	mA	
I <sub>CC2</sub>	Cycle time = 500ns, 100% duty, I <sub>I/O</sub> = 0mA, CE1 ≤ 0.2V, CE2 ≥ V <sub>CC</sub> -0.2V, other pins at 0.2V or V <sub>CC</sub> -0.2V,	-	6	8	mA		
Standby Current (TTL)	I <sub>SB</sub>	CE1 = V <sub>IH</sub> , or CE2 = V <sub>IH</sub> , other pins = V <sub>IH</sub> or V <sub>IL</sub> ,	-	0.3	0.5	mA	
Standby Current (CMOS)	I <sub>SB1</sub>	CE1 ≥ V <sub>CC</sub> -0.2V, or CE2 ≤ 0.2V, other pins at 0.2V or V <sub>CC</sub> -0.2V,	-L	-	20	80	μA
			-LL	-	2	15	μA

**CAPACITANCE** (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 2.2V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.2V
Output Load	C <sub>L</sub> = 30pF, I <sub>OH</sub> /I <sub>OL</sub> = -0.5mA/0.5mA

**AC ELECTRICAL CHARACTERISTICS** (VCC = 2.3V~2.7V, TA = 0°C to 70°C / -20°C to 80°C(E))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62V25716-70		UT62V25716-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	70	-	100	-	ns
Address Access Time	t <sub>AA</sub>	-	70	-	100	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	70	-	100	ns
Output Enable Access Time	t <sub>OE</sub>	-	35	-	50	ns
Chip Enable to Output in Low Z	t <sub>CLZ*</sub>	10	-	10	-	ns
Output Enable to Output in Low Z	t <sub>OLZ*</sub>	5	-	5	-	ns
Chip Disable to Output in High Z	t <sub>CHZ*</sub>	-	25	-	30	ns
Output Disable to Output in High Z	t <sub>OHZ*</sub>	-	25	-	30	ns
Output Hold from Address Change	t <sub>OH</sub>	5	-	5	-	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Access Time	t <sub>BA</sub>	-	70	-	100	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ to High-Z Output	t <sub>HZB</sub>	-	30	0	40	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ to Low-Z Output	t <sub>LZB</sub>	0	-	0	-	ns

**(2) WRITE CYCLE**

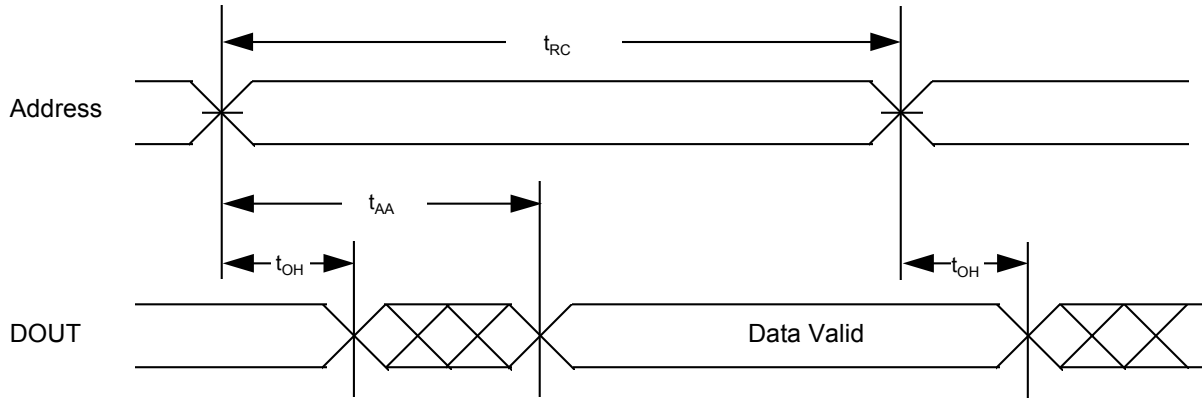
PARAMETER	SYMBOL	UT62V25716-70		UT62V25716-100		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	70	-	100	-	ns
Address Valid to End of Write	t <sub>AW</sub>	60	-	80	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	60	-	80	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	55	-	70	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	30	-	40	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	ns
Output Active from End of Write	t <sub>OW*</sub>	5	-	5	-	ns
Write to Output in High Z	t <sub>WHZ*</sub>	-	30	-	40	ns
$\overline{\text{LB}}, \overline{\text{UB}}$ Valid to End of Write	t <sub>PWB</sub>	60	-	80	-	ns

\* These parameters are guaranteed by device characterization, but not production tested.

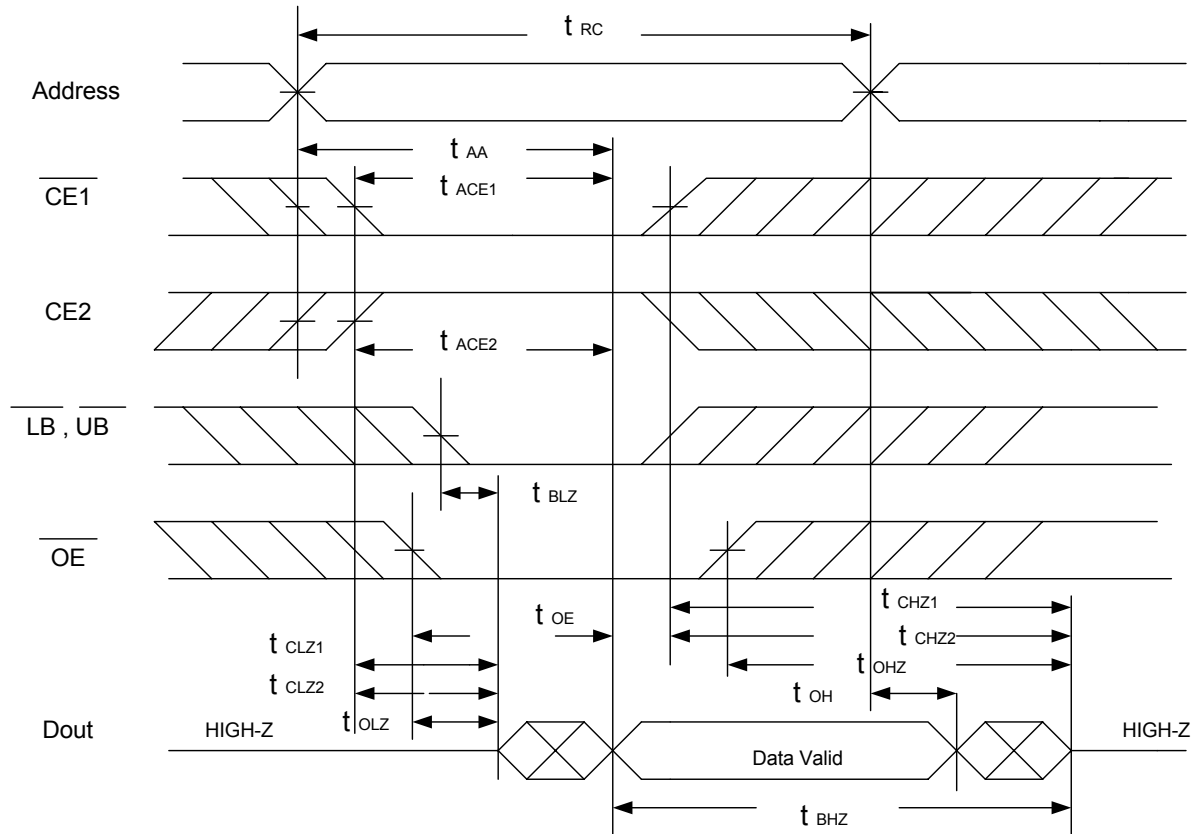


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ( $\overline{CE1}$  and  $\overline{CE2}$  and  $\overline{OE}$  Controlled) (1,3,5,6)

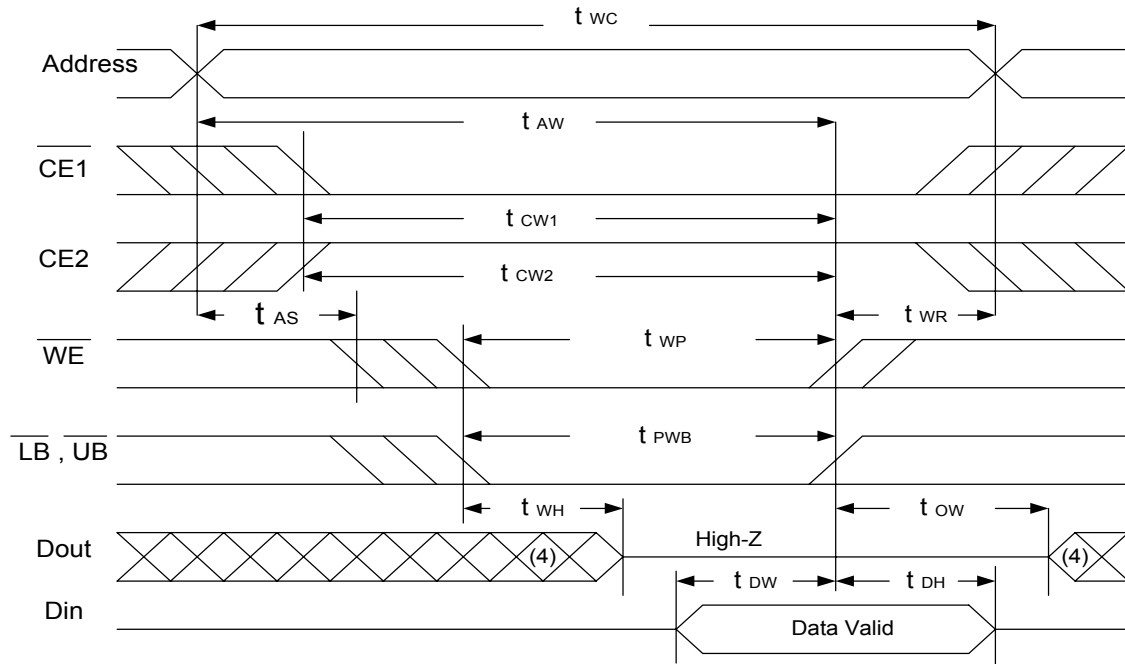


Notes :

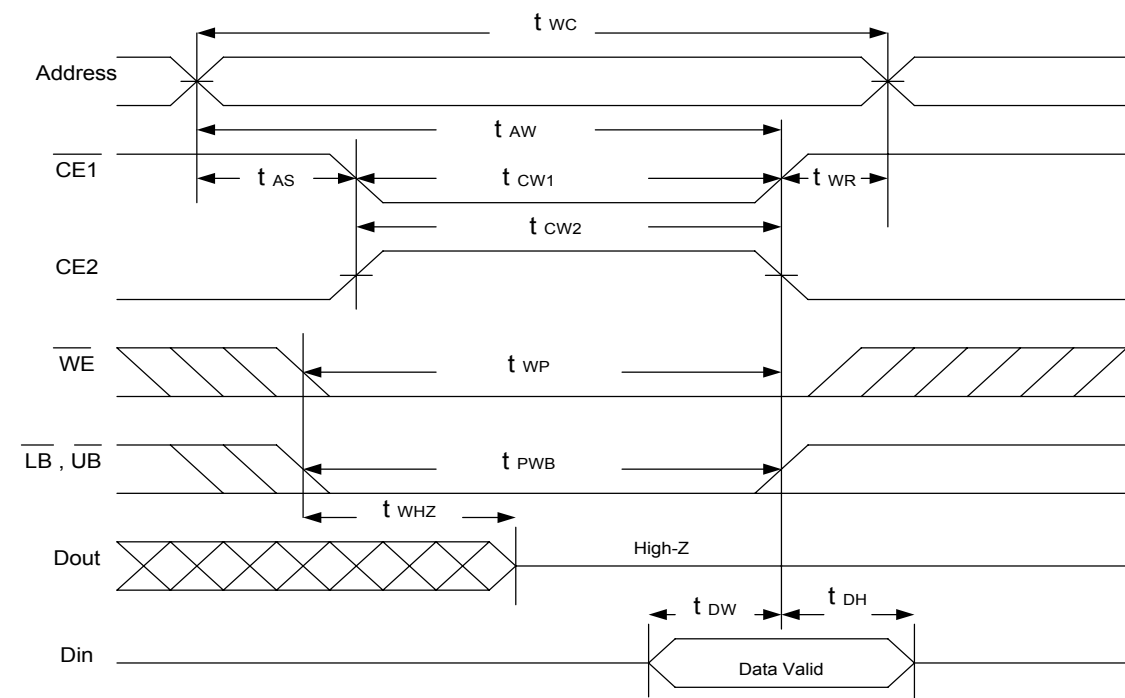
1.  $\overline{WE}$  is HIGH for read cycle.
2. Device is continuously selected  $\overline{CE1}=V_{IL}$  and  $\overline{CE2}=V_{IH}$ . and  $\overline{LB}=V_{IL}$  and  $\overline{UB}=V_{IH}$ .
3. Address must be valid prior to or coincident with  $\overline{CE1}$  and  $\overline{CE2}$  and  $\overline{LB}$  and  $\overline{UB}$  transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is low.
5.  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$  and  $t_{OHZ}$  are specified with  $C_L=5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ1}$  is less than  $t_{CLZ1}$ ,  $t_{CHZ2}$  is less than  $t_{CLZ2}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



WRITE CYCLE 1 ( $\overline{WE}$  Controlled) (1,2,3,5)



WRITE CYCLE 2 ( $\overline{CE1}$  and  $\overline{CE2}$  Controlled) (1,2,5)



Notes :

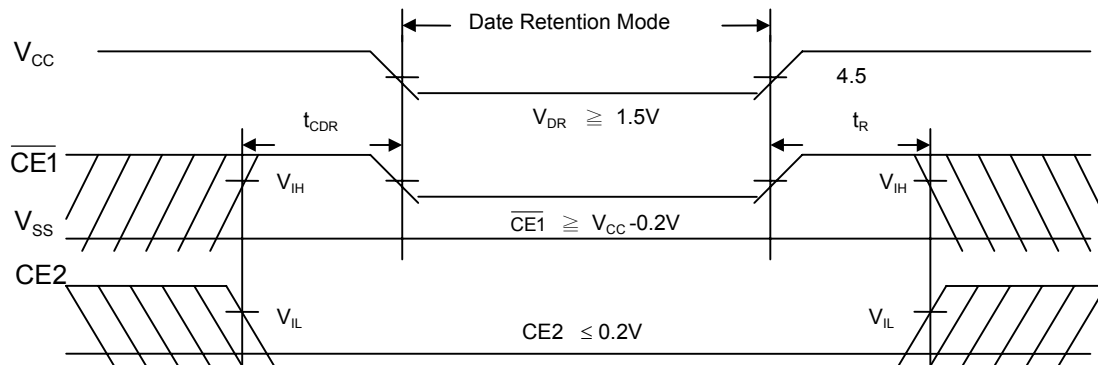
1.  $\overline{WE}$  or  $\overline{CE1}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE1}$  and a low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled with write cycle with  $\overline{OE}$  LOW,  $t_{wp}$  must be greater than  $t_{whz}+t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE1}$  LOW transition occurs simultaneously with or after  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



**DATA RETENTION CHARACTERISTICS (TA = 0°C to 70°C / -20°C to 80°C(E))**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V <sub>DR</sub>	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	1.5	-	3.6	V	
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> =1.5V $\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	- L	-	1	50	μA
			- LL	-	0.5	15	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ms	
Recovery Time	t <sub>R</sub>		5	-	-	ms	

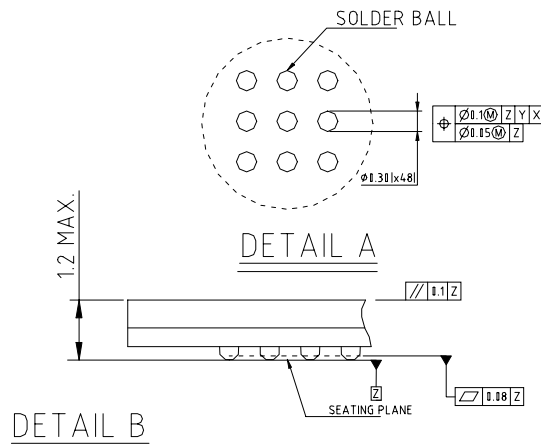
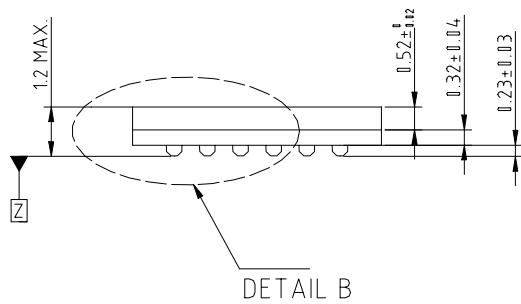
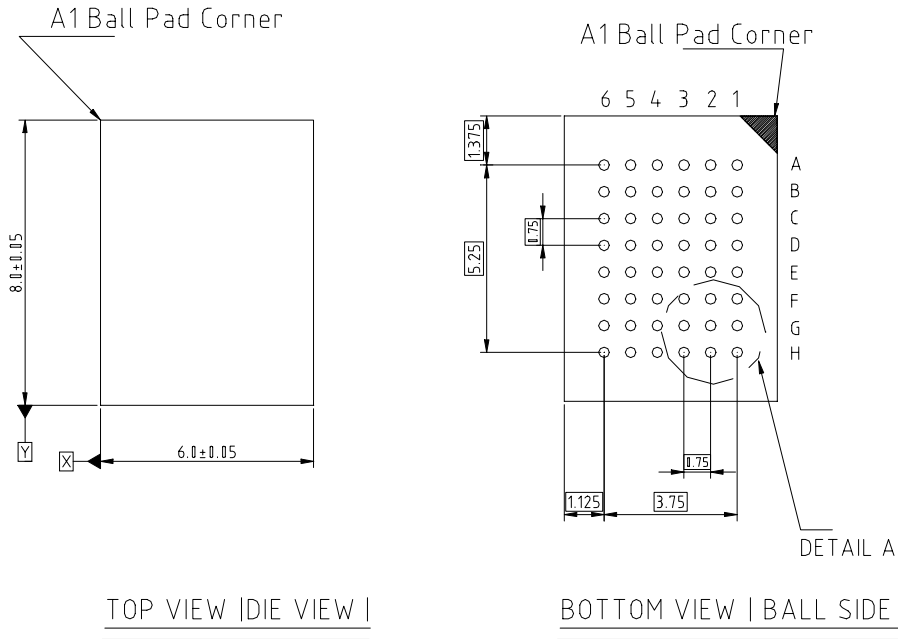
**DATA RETENTION WAVEFORM**





PACKAGE OUTLINE DIMENSION

48 pin 6.0mmX8.0mm TFBGA Package Outline Dimension





UTRON

UT62V25716

Rev. 1.0

256K X 16 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

**COMMERCIAL TEMPERATURE**

<b>PART NO.</b>	<b>ACCESS TIME ( ns )</b>	<b>STANDBY CURRENT ( <math>\mu</math>A max )</b>	<b>PACKAGE</b>
UT62V25716BS-70L	70	20	48 PIN BGA
UT62V25716BS-70LL	70	2	48 PIN BGA
UT62V25716BS-100L	100	20	48 PIN BGA
UT62V25716BS-100LL	100	2	48 PIN BGA

**EXTENDED TEMPERATURE**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>STANDBY CURRENT ( <math>\mu</math>A max )</b>	<b>PACKAGE</b>
UT62V25716BS-70LE	70	20	48 PIN BGA
UT62V25716BS-70LLE	70	2	48 PIN BGA
UT62V25716BS-100LE	100	20	48 PIN BGA
UT62V25716BS-100LLE	100	2	48 PIN BGA





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**REVISION HISTORY**

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev.1.0	1. Separate Industrial and Commercial SPEC. 2. New waveforms. 3. Add access time 55ns range. 4. The symbols CE1# and OE# and WE# are revised as $\overline{CE1}$ and $\overline{OE}$ and $\overline{WE}$ .	Aug 7,2001



Rev. 1.0

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