V363EPC A0 Local Bus to PCI Bridge

for Embedded Processors

1.0 About the V363EPC

- Direct interface to these processors:
  - AMD® AM29030/40™
  - IBM® PowerPC 401™ Gx
  - Intel® i960® Cx/Hx/Jx/Sx
- Fully compliant with PCI Local Bus Specification, Revision 2.1
- Configurable for system master, PCI bus master, or PCI target operation
- Type 0 and Type 1 PCI configuration cycles
- Up to 1 kB burst access on the PCI or the local bus
- 640 bytes of programmable FIFO storage with *Dynamic Bandwidth Allocation*™ architecture
- 64-byte read FIFO in each direction
- Enhanced support for 8-bit/16-bit local bus devices with programmable region sizes
- Dual bi-directional address space remapping
- 10-bit bus watch timer
- On-the-fly byte order (endian) conversion
- I_2O-Ready™ ATU and messaging unit, including hardware controlled circular queues
- Two-channel DMA, multiprocessor DMA chaining, and demand mode DMA
- Hot Swap Capable™ according to the PICMG® Hot Swap Specification, version 2.1
- Sixteen 8-bit bi-directional mailbox registers with doorbell interrupts
- Support for real-mode MS-DOS® holes
- Flexible PCI and local interrupt management
- Optional power-on serial EEPROM initialization
- Up to 50 MHz on both PCI and local bus clocks
- 3.3 V operation; 5 V tolerant input
- Industrial temperature range (–40°C to +85°C)
- Low-cost 160-pin EIAJ PQFP package (Electronic Industries Association of Japan Plastic Quad Flat Pack)

About the V363EPC

The V363EPC offers the highest performance, most flexible, and most economical solution for interfacing either 32-bit or 16-bit local bus applications to the PCI bus. It is also an ideal candidate for a variety of high-performance applications based on Motorola, IBM, DEC, Hitachi, and other popular embedded processors where only a minimal amount of glue logic is needed.

V363EPC is the 3.3 V enhanced version of the V350EPC and V360EPC Rev A1 devices and supports powerful features like Hot Swap and DMA chaining. The PCI bus operates at up to 50 MHz, independent of local bus clock frequency. The overall throughput of the system is dramatically improved by using our unique *Dynamic Bandwidth Allocation*™ architecture.

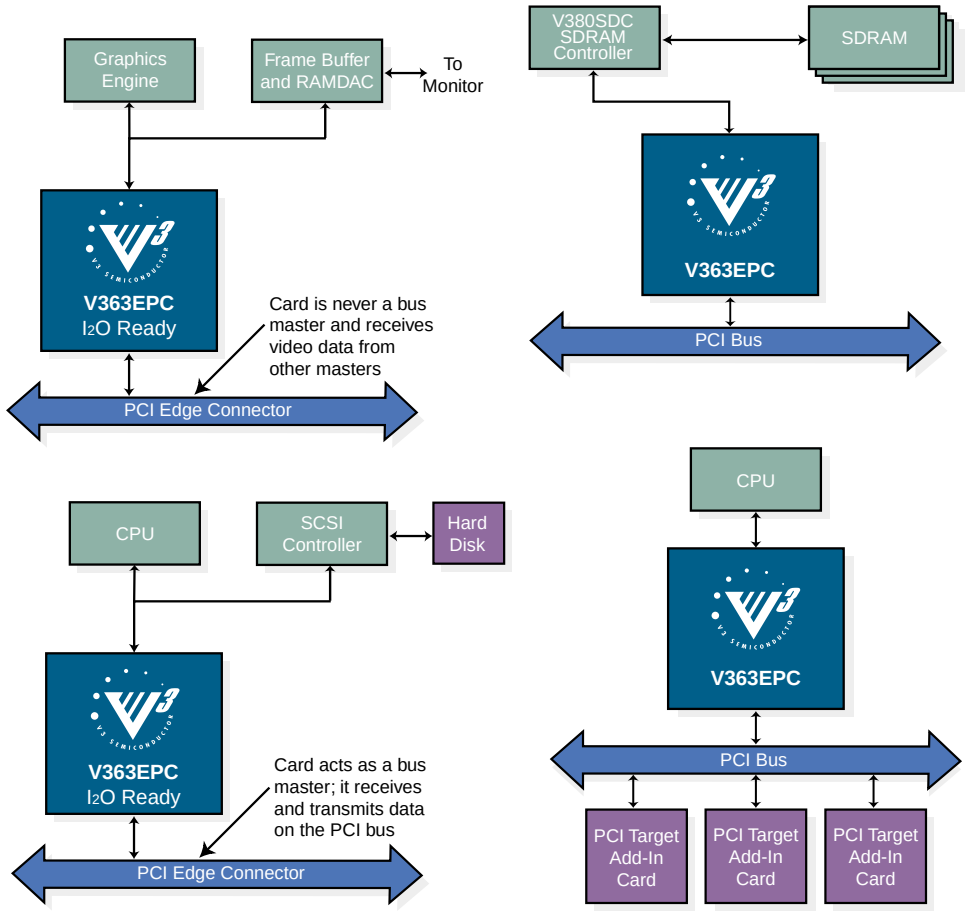
Access to the PCI bus can be performed through two programmable address apertures. Two more apertures are provided for PCI-to-local bus accesses. There are 64 bytes of read FIFOs in each direction, 32 bytes dedicated for each aperture.

Two high-performance DMA channels with chaining and demand mode capabilities provide a powerful data transfer engine for bulk data transfers. Mailbox registers and flexible PCI interrupt controllers also provide a simple mechanism to emulate PCI device control ports. The part is available in a 160-pin, low-cost PQFP package.

This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V363EPC. Detailed functional information is contained in the User's Manual.

> **Note:** V3 Semiconductor retains the rights to change documentation, specifications, or device functionality at any time without notice. Please verify that you have the latest copy of all documents before finalizing a design.

Figure 1: Example Applications



2.0 Product Codes

Table 1: Product Codes

Product Code	Package	Frequency
V363EPC-50 REV A0	160-pin EIAJ PQFP	50 MHz

3.0 Pin Descriptions and Pinouts

Table 2 lists the pin types found on the V363EPC. Together, Table 3 and Table 4 describe the function of each pin on the V363EPC. Table 5 lists the RESET state for test mode pins. Section 3.2 lists processor-mode-specific pin assignments and shows the pinouts for the 160-pin EIAJ PQFP package. Figure 6 shows the mechanical dimensions of the package.

Table 2: Pin Types

Pin Type	Description
PCI I	PCI input only pin.
PCI O	PCI output only pin.
PCI I/O	PCI tri-state I/O pin.
PCI I/O_D	PCI input with open drain output.
I/O_4	TTL I/O pin with 4 mA output drive.
I	TTL input only pin.
O_4	TTL output pin with 4 mA output drive.

Table 3: Signal Descriptions: Non-Processor Mode Dependent

Signal	Type	Reset State	Description
PCI Bus Interface Signals			
AD[31:0]	PCI I/O	Z	**Address and Data** multiplexed on the same pins.
C/$\overline{BE}$[3:0]	PCI I/O	Z	**Bus Command and Byte Enables** multiplexed on the same pins.
PAR	PCI I/O	Z	**Parity** represents even parity across AD[31:0] and C/$\overline{BE}$[3:0].
$\overline{FRAME}$	PCI I/O	Z	**Cycle Frame** indicates the beginning and burst length of an access.
$\overline{IRDY}$	PCI I/O	Z	**Initiator Ready** indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction.
$\overline{TRDY}$	PCI I/O	Z	**Target Ready** indicates the target agent's (selected device's) ability to complete the current data phase of the transaction.
$\overline{STOP}$	PCI I/O	Z	**Stop** indicates that the current target is requesting the master to stop the current transaction (retry or disconnect).
$\overline{DEVSEL}$	PCI I/O	Z	**Device Select**, when actively driven by a target, indicates the driving device has decoded its address as the target of the current access. As an input to the initiator, $\overline{DEVSEL}$ indicates whether any device on the bus has been selected.

Table 3: Signal Descriptions: Non-Processor Mode Dependent

Signal	Type	Reset State	Description
IDSEL	PCI I		**Initialization Device Select** is used as a chip select during configuration read and write transactions. It must be driven high in order to access the chip's internal configuration space.
$\overline{\text{REQ}}$	PCI O	Z	**Request** indicates to the arbiter that this agent requests use of the bus.
$\overline{\text{GNT}}$	PCI I		**Grant** indicates to the agent that access to the bus has been granted.
PCLK	PCI I		**PCI Clock** provides timing for all transactions on the PCI bus.
$\overline{\text{PRST}}$	PCI I/O	Z/L	**PCI Reset** acts as an input when RDIR is high, an output when RDIR is low. As an input it is asserted low to bring all internal EPC operation to a reset state.
$\overline{\text{PERR}}$	PCI I/O	Z	**Parity Error** is used to report data parity errors during all PCI transactions except a Special Cycle.
$\overline{\text{SERR}}$	PCI I/OD	Z	**System Error** is used to report address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
$\overline{\text{INT[A:D]}}$	PCI I/OD	Z	**Interrupt** is used to receive or generate level-sensitive interrupt requests.
Serial EEPROM Interface Signals			
SCL/$\overline{\text{LPERR}}$	O_4	X	**EEPROM Clock, Local Parity Error**.
SDA	I/O_4	X	**EEPROM Data**.
Configuration Signal			
RDIR	I		**Reset Direction**: tie low to drive $\overline{\text{PRST}}$ out and $\overline{\text{LRST}}$ in; tie high to drive $\overline{\text{LRST}}$ out and $\overline{\text{PRST}}$ in.
Power and Ground Signals			
V_{CC}	—		**Power** leads for external connection to a 3.3 V V_{CC} board plane.
GND	—		**Ground** leads for external connection to a GND board plane.

Table 4: Signal Descriptions: Processor Mode Dependent

De-Multiplexed A/D		Multiplexed A/D		Type	Reset State	Description
AM29030/40	i960Cx/Hx	i960Jx	i960Sx			
ID[31:0]	LD[31:0]	LAD[31:0]	LAD[15:0]	I/O_4	Z	De-multiplexed data bus. Multiplexed address and data bus.
LA[31:2]	LA[31:2]	LA[5:2]	LA[31:16] LA[5:2]	I/O_4	Z	**Address Bus** LA[5:2] are output only in Multiplexed A/D mode.
$\overline{BWE}$[3:0]	$\overline{BE}$[3:0]	$\overline{BE}$[3:0]	$\overline{BE}$[1:0]	I/O_4	Z	**Byte Enables**
R/$\overline{W}$	W/$\overline{R}$	W/$\overline{R}$	W/$\overline{R}$	I/O_4	Z	**Read-Write** strobe.
—	—	ALE	ALE	I/O_4	Z	**Address Latch Enable**
$\overline{LREQ}$	$\overline{ADS}$	$\overline{ADS}$	$\overline{AS}$	**I/O_4**	Z	**Address Strobe** is asserted low to indicate the beginning of a bus cycle; interpreted as $\overline{LREQ}$ in AM29030/40 mode.
$\overline{RDY}$	$\overline{READY}$	$\overline{RDYRCY}$	$\overline{READY}$	I/O_4	Z	**Data Ready**
$\overline{LBREQ}$	HOLD	HOLD	HOLD	O_4	L[1]	**Bus Mastership Request**
$\overline{LBGRT}$	HOLDA	HOLDA	HOLDA	I		**Bus Mastership Grant**
LPAR[3:0]	LPAR[3:0]	LPAR[3:0]	LPAR[1:0]	I/O_4	Z	**Data Parity**
$\overline{BURST}$	$\overline{BLAST}$	$\overline{BLAST}$	$\overline{BLAST}$	I/O_4	Z	$\overline{BURST}$: **Burst Request** $\overline{BLAST}$: **Burst Last**
$\overline{ERR}$	$\overline{BTERM}$	$\overline{BTERM}$	—	**I/O_4**	Z	$\overline{ERR}$: **Bus Time-out** $\overline{BTERM}$: **Burst Terminate**
$\overline{LINT}$	$\overline{LINT}$	$\overline{LINT}$	$\overline{LINT}$	O_4	H	**Local Interrupt Request**
$\overline{LRST}$	$\overline{LRST}$	$\overline{LRST}$	$\overline{LRST}$	I/O_4	L/Z	**Local Bus RESET**
MEMCLK	LCLK	LCLK	LCLK	I		**Local Bus Clock**

1. The reset state is ‘H’ in AM29030/40 mode.

3.1 Test Mode Pins

Several device pins are used during the manufacturing test to put the V363EPC device into various test modes.

> **Note:** These pins must be maintained at proper levels during reset to insure proper operation.

This is typically handled through pull-up or pull-down resistors (typically 1–10 kΩ) on the signal pins if they are not guaranteed to be at the proper level during reset. Table 5 shows the reset states for test mode pins.

Table 5: RESET State for Test Mode Pins

Mode	Pin 134	Pin 135	Pin 153
i960 Cx/Hx	Pull up	Pull up	Pull up
AMD 2930/40	Pull down	Pull up	Pull up
i960 Jx	Pull down	Pull up	Pull down
i960 Sx	Pull down	Pull down	Pull down

3.2 Processor-mode Specific Pin Assignments

The following tables and diagrams describe the pin assignments for the V363EPC A0 in its various processor modes.

- AM29030/040 mode: Table 6 and Figure 2
- i960 Cx/Hx mode: Table 7 and Figure 3
- i960 Jx mode: Table 8 and Figure 4
- i960 Sx mode: Table 9 and Figure 5

Pin Descriptions and Pinouts

Processor-mode Specific Pin Assignments

Table 6: Pin Assignments for AM29030/40 Mode

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	LA23	122	LA6
3	$\overline{PRST}$	43	AD13	83	ID8	123	ID25
4	PCLK	44	AD12	84	LA22	124	LA5
5	$\overline{GNT}$	45	AD11	85	ID9	125	ID26
6	$\overline{REQ}$	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	ID10	127	ID27
8	AD30	48	AD8	88	LA20	128	LA3
9	AD29	49	C/$\overline{BE0}$	89	ID11	129	ID28
10	AD28	50	V_{CC}	90	LA19	130	LA2
11	GND	51	GND	91	ID12	131	ID29
12	AD27	52	AD7	92	LA18	132	ID30
13	AD26	53	AD6	93	ID13	133	ID31
14	AD25	54	AD5	94	LA17	134	'0'
15	AD24	55	AD4	95	ID14	135	$\overline{ERR}$
16	C/$\overline{BE3}$	56	AD3	96	LA16	136	$\overline{RDY}$
17	IDSEL	57	AD2	97	ID15	137	$\overline{LBREQ}$
18	AD23	58	AD1	98	LA15	138	$\overline{LBGNT}$
19	AD22	59	AD0	99	ID16	139	$\overline{LREQ}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	ID0	102	LA14	142	MEMCLK
23	AD20	63	LA31	103	ID17	143	NC
24	AD19	64	ID1	104	LA13	144	V_{CC}
25	AD18	65	LA30	105	ID18	145	$\overline{BWE3}$
26	AD17	66	ID2	106	LA12	146	$\overline{BWE2}$
27	AD16	67	LA29	107	ID19	147	$\overline{BWE1}$
28	C/$\overline{BE2}$	68	ID3	108	LA11	148	$\overline{BWE0}$
29	$\overline{FRAME}$	69	LA28	109	ID20	149	$\overline{BURST}$
30	GND	70	ID4	110	LA10	150	R/$\overline{W}$
31	$\overline{IRDY}$	71	LA27	111	ID21	151	RDIR
32	$\overline{TRDY}$	72	ID5	112	LA9	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	LA26	113	ID22	153	'1'
34	$\overline{STOP}$	74	ID6	114	LA8	154	$\overline{LINT}$
35	$\overline{PERR}$	75	LA25	115	ID23	155	SDA
36	$\overline{SERR}$	76	ID7	116	LA7	156	SCL/$\overline{LPERR}$
37	PAR	77	LA24	117	LPAR2	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	LPAR3	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	ID24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

Figure 2: Pinout for AM29030/40 Mode (top view)

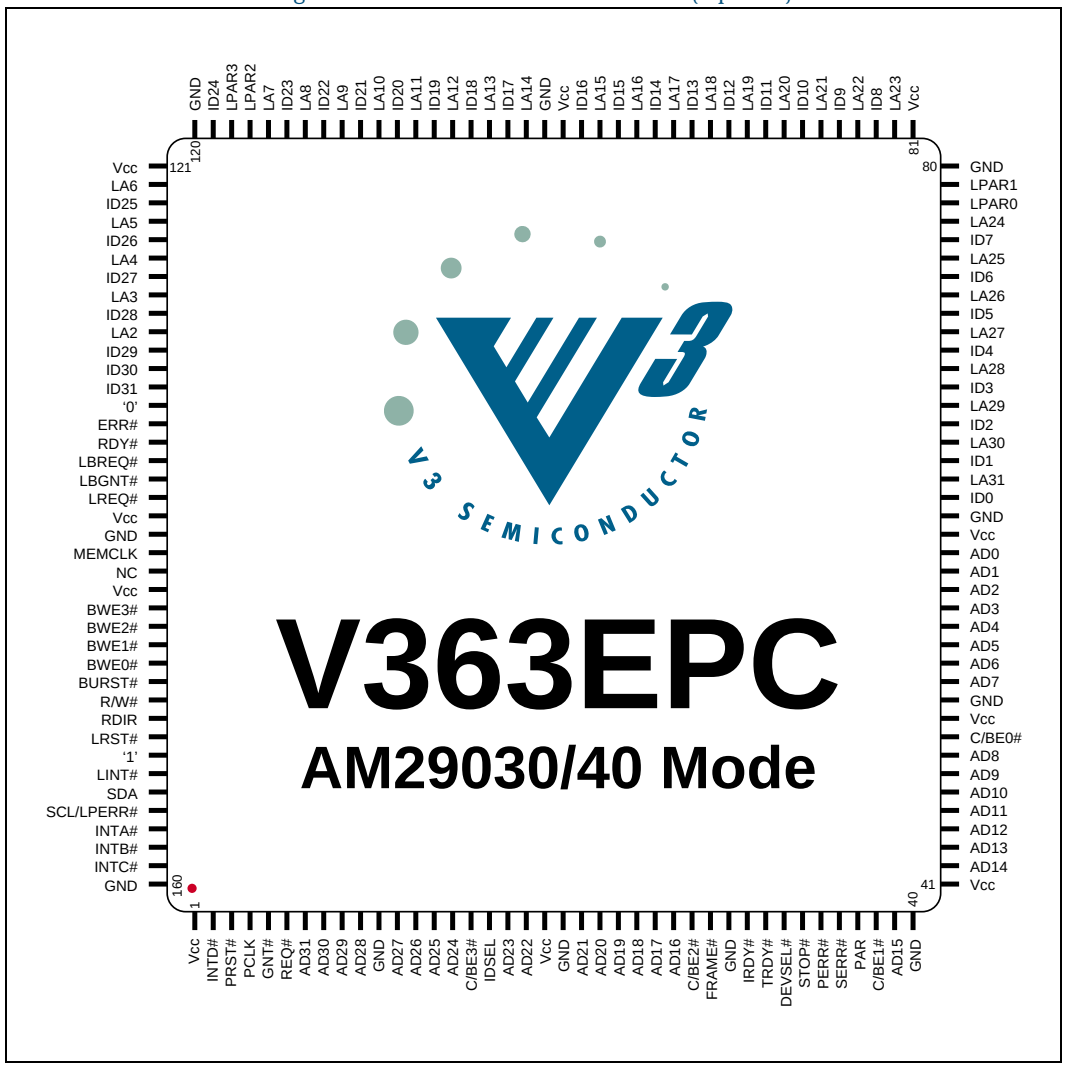


Table 7: Pin Assignments for i960 Cx/Hx Mode

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	LA23	122	LA6
3	$\overline{PRST}$	43	AD13	83	LD8	123	LD25
4	PCLK	44	AD12	84	LA22	124	LA5
5	$\overline{GNT}$	45	AD11	85	LD9	125	LD26
6	$\overline{REQ}$	46	AD10	86	LA21	126	LA4
7	AD31	47	AD9	87	LD10	127	LD27
8	AD30	48	AD8	88	LA20	128	LA3
9	AD29	49	C/$\overline{BE0}$	89	LD11	129	LD28
10	AD28	50	V_{CC}	90	LA19	130	LA2
11	GND	51	GND	91	LD12	131	LD29
12	AD27	52	AD7	92	LA18	132	LD30
13	AD26	53	AD6	93	LD13	133	LD31
14	AD25	54	AD5	94	LA17	134	'1'
15	AD24	55	AD4	95	LD14	135	$\overline{BTERM}$
16	C/$\overline{BE3}$	56	AD3	96	LA16	136	$\overline{READY}$
17	IDSEL	57	AD2	97	LD15	137	HOLD
18	AD23	58	AD1	98	LA15	138	HOLDA
19	AD22	59	AD0	99	LD16	139	$\overline{ADS}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LD0	102	LA14	142	LCLK
23	AD20	63	LA31	103	LD17	143	NC
24	AD19	64	LD1	104	LA13	144	V_{CC}
25	AD18	65	LA30	105	LD18	145	$\overline{BE3}$
26	AD17	66	LD2	106	LA12	146	$\overline{BE2}$
27	AD16	67	LA29	107	LD19	147	$\overline{BE1}$
28	C/$\overline{BE2}$	68	LD3	108	LA11	148	$\overline{BE0}$
29	$\overline{FRAME}$	69	LA28	109	LD20	149	$\overline{BLAST}$
30	GND	70	LD4	110	LA10	150	W/$\overline{R}$
31	$\overline{IRDY}$	71	LA27	111	LD21	151	RDIR
32	$\overline{TRDY}$	72	LD5	112	LA9	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	LA26	113	LD22	153	'1'
34	$\overline{STOP}$	74	LD6	114	LA8	154	$\overline{LINT}$
35	$\overline{PERR}$	75	LA25	115	LD23	155	SDA
36	$\overline{SERR}$	76	LD7	116	LA7	156	SCL/$\overline{LPERR}$
37	PAR	77	LA24	117	LPAR2	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	LPAR3	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	LD24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

Figure 3: Pinout for i960 Cx/Hx Mode (top view)

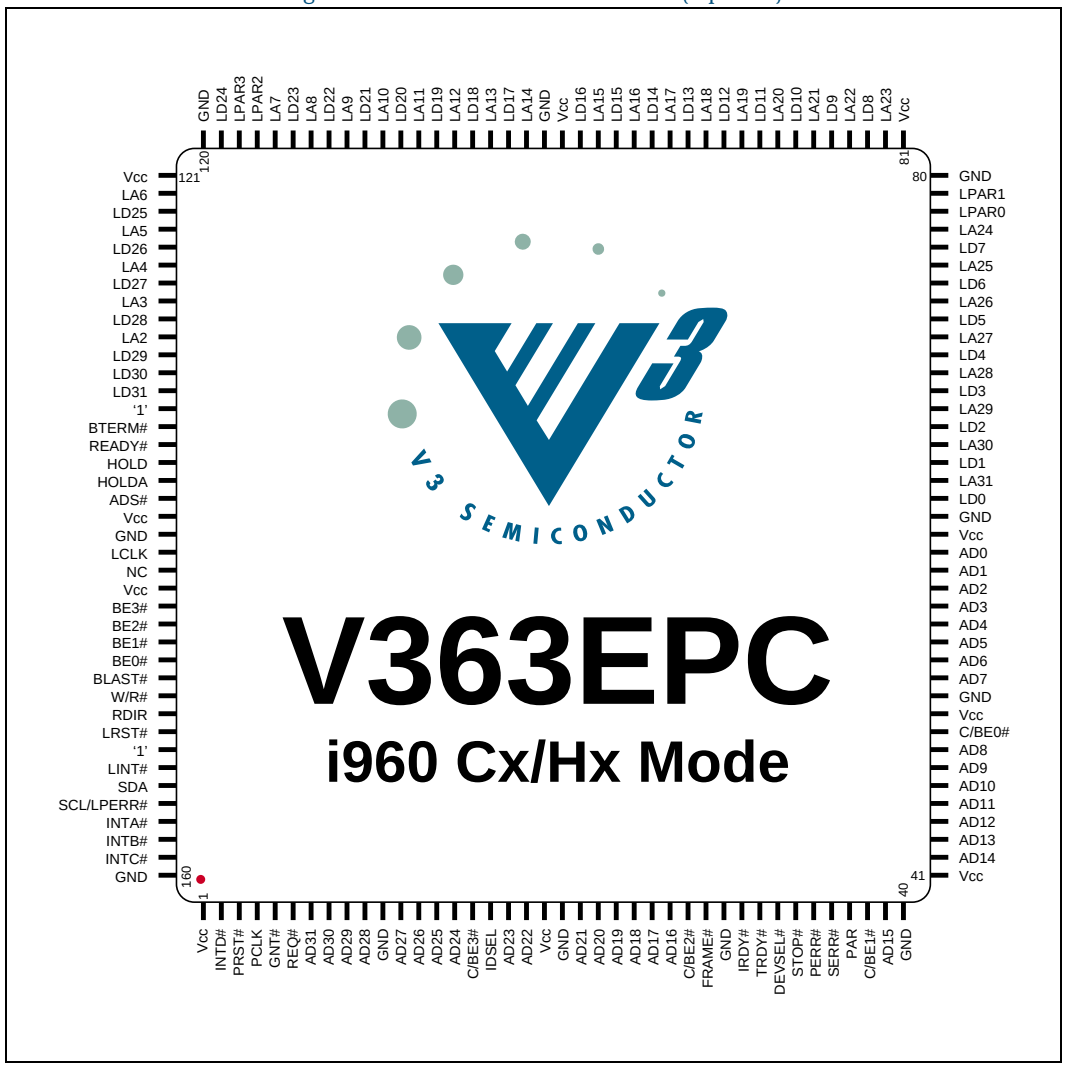


Table 8: Pin Assignments for i960 Jx Mode

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	NC	122	NC
3	$\overline{PRST}$	43	AD13	83	LAD8	123	LAD25
4	PCLK	44	AD12	84	NC	124	LA5
5	$\overline{GNT}$	45	AD11	85	LAD9	125	LAD26
6	$\overline{REQ}$	46	AD10	86	NC	126	LA4
7	AD31	47	AD9	87	LAD10	127	LAD27
8	AD30	48	AD8	88	NC	128	LA3
9	AD29	49	C/$\overline{BE0}$	89	LAD11	129	LAD28
10	AD28	50	V_{CC}	90	NC	130	LA2
11	GND	51	GND	91	LAD12	131	LAD29
12	AD27	52	AD7	92	NC	132	LAD30
13	AD26	53	AD6	93	LAD13	133	LAD31
14	AD25	54	AD5	94	NC	134	ALE
15	AD24	55	AD4	95	LAD14	135	$\overline{BTERM}$
16	C/$\overline{BE3}$	56	AD3	96	NC	136	$\overline{RDYRCV}$
17	IDSEL	57	AD2	97	LAD15	137	HOLD
18	AD23	58	AD1	98	NC	138	HOLDA
19	AD22	59	AD0	99	LAD16	139	$\overline{ADS}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LAD0	102	NC	142	LCLK
23	AD20	63	NC	103	LAD17	143	NC
24	AD19	64	LAD1	104	NC	144	V_{CC}
25	AD18	65	NC	105	LAD18	145	$\overline{BE3}$
26	AD17	66	LAD2	106	NC	146	$\overline{BE2}$
27	AD16	67	NC	107	LAD19	147	$\overline{BE1}$
28	C/$\overline{BE2}$	68	LAD3	108	NC	148	$\overline{BE0}$
29	$\overline{FRAME}$	69	NC	109	LAD20	149	$\overline{BLAST}$
30	GND	70	LAD4	110	NC	150	W/$\overline{R}$
31	$\overline{IRDY}$	71	NC	111	LAD21	151	RDIR
32	$\overline{TRDY}$	72	LAD5	112	NC	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	NC	113	LAD22	153	'0'
34	$\overline{STOP}$	74	LAD6	114	NC	154	$\overline{LINT}$
35	$\overline{PERR}$	75	NC	115	LAD23	155	SDA
36	$\overline{SERR}$	76	LAD7	116	NC	156	SCL/$\overline{LPERR}$
37	PAR	77	NC	117	LPAR2	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	LPAR3	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	LAD24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

Figure 4: Pinout for i960 Jx Mode (top view)

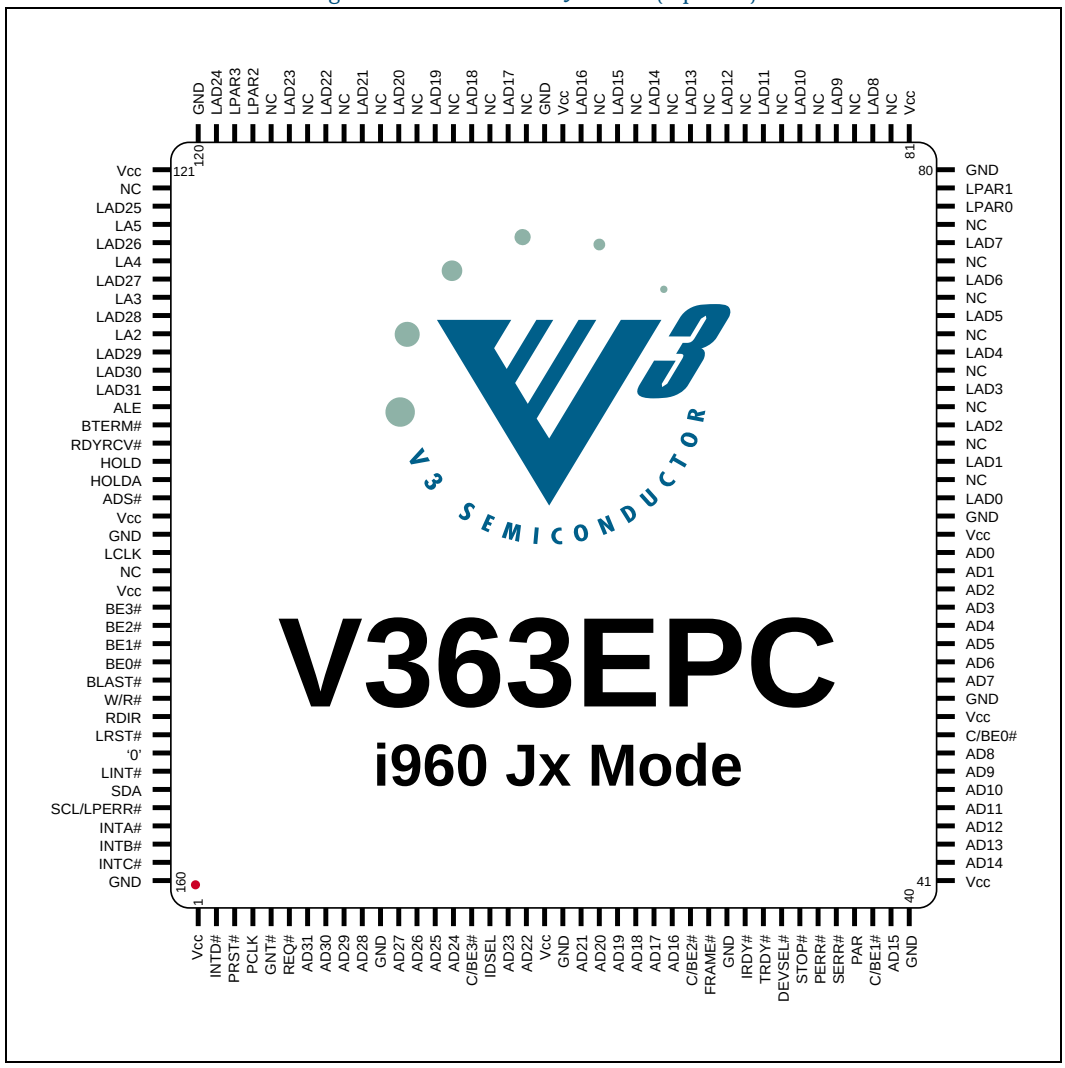
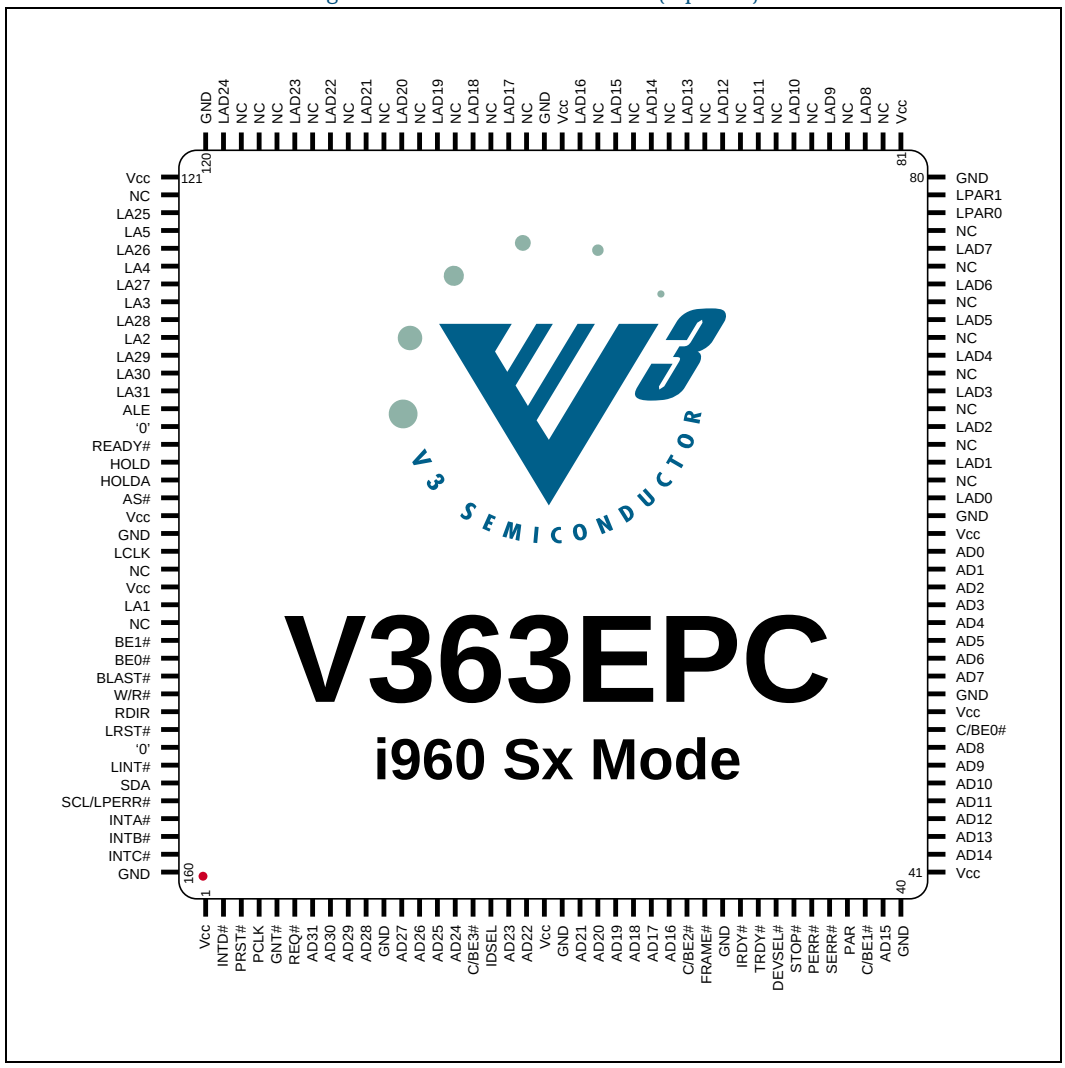


Table 9: Pin Assignments for i960 Sx Mode

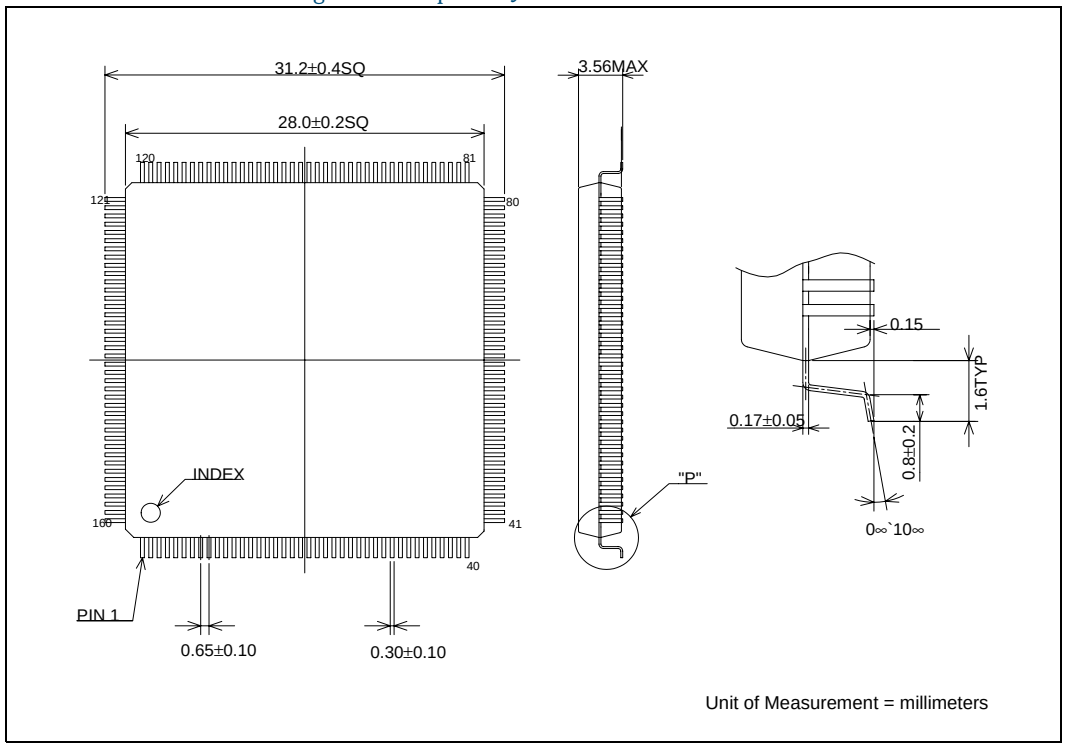
PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	V_{CC}	41	V_{CC}	81	V_{CC}	121	V_{CC}
2	$\overline{INTD}$	42	AD14	82	NC	122	NC
3	$\overline{PRST}$	43	AD13	83	LAD8	123	LA25
4	PCLK	44	AD12	84	NC	124	LA5
5	$\overline{GNT}$	45	AD11	85	LAD9	125	LA26
6	$\overline{REQ}$	46	AD10	86	NC	126	LA4
7	AD31	47	AD9	87	LAD10	127	LA27
8	AD30	48	AD8	88	NC	128	LA3
9	AD29	49	C/$\overline{BE0}$	89	LAD11	129	LA28
10	AD28	50	V_{CC}	90	NC	130	LA2
11	GND	51	GND	91	LAD12	131	LA29
12	AD27	52	AD7	92	NC	132	LA30
13	AD26	53	AD6	93	LAD13	133	LA31
14	AD25	54	AD5	94	NC	134	ALE
15	AD24	55	AD4	95	LAD14	135	'0'
16	C/$\overline{BE3}$	56	AD3	96	NC	136	$\overline{READY}$
17	IDSEL	57	AD2	97	LAD15	137	HOLD
18	AD23	58	AD1	98	NC	138	HOLDA
19	AD22	59	AD0	99	LA16	139	$\overline{AS}$
20	V_{CC}	60	V_{CC}	100	V_{CC}	140	V_{CC}
21	GND	61	GND	101	GND	141	GND
22	AD21	62	LAD0	102	NC	142	LCLK
23	AD20	63	NC	103	LA17	143	NC
24	AD19	64	LAD1	104	NC	144	V_{CC}
25	AD18	65	NC	105	LA18	145	LA1
26	AD17	66	LAD2	106	NC	146	NC
27	AD16	67	NC	107	LA19	147	$\overline{BE1}$
28	C/$\overline{BE2}$	68	LAD3	108	NC	148	$\overline{BE0}$
29	$\overline{FRAME}$	69	NC	109	LA20	149	$\overline{BLAST}$
30	GND	70	LAD4	110	NC	150	W/$\overline{R}$
31	$\overline{IRDY}$	71	NC	111	LA21	151	RDIR
32	$\overline{TRDY}$	72	LAD5	112	NC	152	$\overline{LRST}$
33	$\overline{DEVSEL}$	73	NC	113	LA22	153	'0'
34	$\overline{STOP}$	74	LAD6	114	NC	154	$\overline{LINT}$
35	$\overline{PERR}$	75	NC	115	LA23	155	SDA
36	$\overline{SERR}$	76	LAD7	116	NC	156	SCL/$\overline{LPERR}$
37	PAR	77	NC	117	NC	157	$\overline{INTA}$
38	C/$\overline{BE1}$	78	LPAR0	118	NC	158	$\overline{INTB}$
39	AD15	79	LPAR1	119	LA24	159	$\overline{INTC}$
40	GND	80	GND	120	GND	160	GND

Figure 5: Pinout for i960 Sx Mode (top view)



3.3 Mechanical Details

Figure 6: 160-pin EIAJ PQFP mechanical details



4.0 DC Specifications

The DC specifications for the PCI bus signals reference those given in the *PCI Local Bus Specification*, Revision 2.1, Section 4.2.2.1. For more information on the PCI DC specifications, see the *PCI Local Bus Specification*.

Table 10: Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage	–0.3 to 3.8	V
V_{IN}	DC input voltage	–0.3 to 5.75	V
T_{STG}	Storage temperature range	–55 to 125	°C

Table 11: Guaranteed Operating Conditions

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage 3.3 volt	3.0 to 3.6	V
J_{max}	Maximum Junction temperature	125	°C
θ_{JA}	Junction-to-ambient thermal resistance	50	°C/w
θ_{JC}	Junction-to-case thermal resistance	11	°C/w
T_A	Ambient temperature range	–40 to 85	°C

4.1 PCI Bus DC Specifications

Table 12: PCI Bus Signals DC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{IH}	Input high voltage		0.5 V_{CC}	5.75	V	1
V_{IL}	Input low voltage		–0.5	0.3 V_{CC}	V	
I_{IL}	Input leakage current	0 < V_{IN} < V_{CC}		±10	µA	2
V_{OH}	Output high voltage	I_{OUT} = –500 µA	0.9 V_{CC}		V	
V_{OL}	Output low voltage	I_{OUT} = 1500 µA		0.1 V_{CC}	V	
C_{IN}	Input pin capacitance			10	pF	3
C_{CLK}	PCLK pin capacitance		5	12	pF	
C_{IDSEL}	IDSEL pin capacitance			8	pF	4

1. Custom 5 V tolerant PCI buffers are used in the design.
2. Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
3. Absolute maximum pin capacitance for a PCI unit is 10 pF (except for CLK).
4. Lower capacitance on this input-only pin allows for non-resistive coupling to AD[xx].

4.2 Local Bus DC Specifications

Table 13: Local Bus Signals DC Operating Specifications

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage			0.8	V
V_{IH}	High level input voltage		2.0		V
I_{IL}	Low level input current	V_{IN} = GND	–10		µA
I_{IH}	High level input current	V_{IN} = V_{CC}		10	µA
V_{OL4}	Low level output voltage for 4 mA outputs and I/O pins	I_{OL} = 4 mA		0.4	V
V_{OH4}	High level output voltage for 4 mA outputs and I/O pins	I_{OH} = –4 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = GND	–10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{CC}		10	µA
I_{CC} (max)	Maximum supply current	V_{CC} = 3.6 V PCLK = LCLK = 33 MHz		55	mA
I_{CC} (typ)	Typical supply current	V_{CC} = 3.3 V PCLK = LCLK = 33 MHz		44	mA
C_{IO}	Input and output capacitance			10	pF

5.0 AC Specifications

The AC specifications for the PCI bus signals match those given in the *PCI Local Bus Specification,* Revision 2.1, Section 4.2.2.2. For more information on the PCI AC specifications, including the V/I curves for 3.3 V signalling, see the *PCI Local Bus Specification.*

5.1 PCI Bus Timings

Table 14: PCI Bus Signals AC Operating Specifications

Symbol	Parameter	Condition	Min	Max	Units
$I_{OH(AC)}$	Switching current high	$0 < V_{OUT} \leq 0.3\ V_{CC}$	$-12\ V_{CC}$		mA
		$0.3\ V_{CC} < V_{OUT} < 0.9\ V_{CC}$	$-17.1\ (V_{CC} - V_{OUT})$		mA
		$0.7\ V_{CC} < V_{OUT} < V_{CC}$		Equation C	
	(Test point)	$V_{OUT} = 0.7\ V_{CC}$		$-32\ V_{CC}$	mA
$I_{OL(AC)}$	Switching current low	$V_{CC} > V_{OUT} \geq 0.6\ V_{CC}$	$16\ V_{CC}$		mA
		$0.6\ V_{CC} > V_{OUT} > 0.1\ V_{CC}$	$26.7\ V_{OUT}$		mA
		$0.18\ V_{CC} > V_{OUT} > 0$		Equation D	
	(Test point)	$V_{OUT} = 0.18\ V_{CC}$		$38\ V_{CC}$	mA
I_{CL}	Low clamp current	$-3 < V_{IN} \leq -1$	$-25 + (V_{IN} + 1) / 0.015$		mA
I_{CH}	High clamp current	$V_{CC} + 4 > V_{IN} \geq V_{CC} + 1$	$25 + (V_{IN} - V_{CC} - 1) / 0.015$		mA
t_R	Unloaded output rise time	$0.2\ V_{CC} - 0.6\ V_{CC}$ load	1	4	V/ns
t_F	Unloaded output fall time	$0.6\ V_{CC} - 0.2\ V_{CC}$ load	1	4	V/ns

5.2 Local Bus Timings

Table 15: Local Bus AC Test Conditions

Symbol	Parameter	Limits	Units
V_{CC}	Supply voltage, 3.3 volt operation	3.0 to 3.60	V
V_{IN}	Input low and high voltages	0.4 and 2.0	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

Table 16: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply voltage	Derating
4 mA	3.3 volt	+0.046 ns/pF for loads > 50pF

Figure 7: Clock and Synchronous Signals

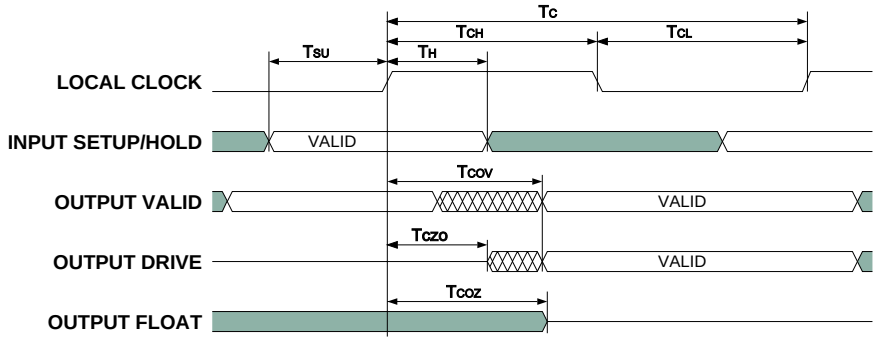


Table 17: Local Bus Timing Parameters for V_{CC} = 3.3 Volts ± 10%

#	Symbol	Description	Notes	Min	Max	Units
1	T_C	LCLK/MEMCLK period		20		ns
2	**T_{CH}**	LCLK/MEMCLK high time	1	9		ns
3	T_{CL}	LCLK/MEMCLK low time	2	9		ns
4	T_{SU}	Synchronous input setup	3	6		ns
4a	T_{SU}	Synchronous input setup ($\overline{AS}$/$\overline{ADS}$/$\overline{LREQ}$)		4		ns
4b	T_{SU}	Synchronous input setup for HOLDA ($\overline{LBGRT}$)		3		ns
5	T_H	Synchronous input hold		2		ns
6	T_{COV}	LCLK/MEMCLK to output valid delay	4	4	11	ns
6a	T_{COV}	LCLK/MEMCLK to output valid delay (address, data)		4	12	ns
7	T_{CZO}	LCLK/MEMCLK to output driving delay		4	11	ns
8	T_{COZ}	LCLK/MEMCLK to output float delay	5	4	11	ns
9	T_{RST}	Reset period when $\overline{LRST}$ used as input		16 T_C		ns

1. Measured at 1.5 V.
2. Measured at 1.5 V.
3. All local bus signals except those in 4a and 4b.
4. All local bus signals except those in 6a.
5. $\overline{READY}$, $\overline{BLAST}$, $\overline{ADS}$ are driven to high impedance at the falling edge of LCLK.

Table 18: PCI Bus Timing Parameters for V_{CC} = 3.3 Volts ± 10%

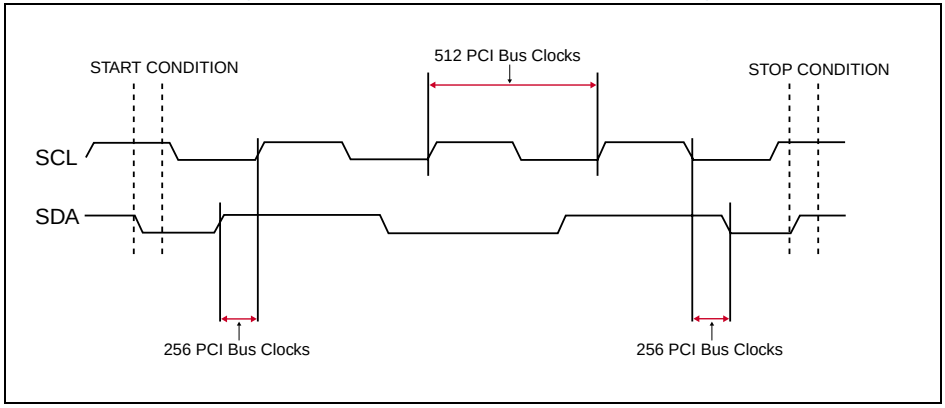
#	Symbol	Description	Notes	Min	Max	Units
1	T_C	PCLK period		20		ns
2	T_{SU}	Synchronous input setup to PCLK	1	7		ns
2a	T_{SU}	Synchronous input setup to PCLK ($\overline{GNT}$)		9		ns
3	T_H	Synchronous input hold from PCLK		0		ns
4	T_{COV}	PCLK to output valid delay	2	3	11	ns
4a	T_{COV}	PCLK to output valid delay ($\overline{REQ}$)		3	12	ns
5	T_{CZO}	PCLK to output driving delay		3	11	ns
6	T_{COZ}	PCLK to output float delay		4	18	ns
7	T_{RST}	Reset period when PRST used as input		16 T_C		

1. All PCI bus signals except those in 2a.
2. All PCI bus signals except those in 4a.

5.3 Serial EEPROM Port TImings

The clock for the serial EEPROM interface is derived by dividing the PCI bus clock. The waveforms generated are shown in Figure 8.

Figure 8: Serial EEPROM Waveforms and Timings



6.0 Getting Help from V3 Semiconductor

If you need assistance with a technical question, please contact us. E-mail is the quickest and most efficient way to get technical support from V3. The V3 Web site also contains much technical support information as well as the most up-to-date technical documents. Visit us on the Web at: http://www.vcubed.com.

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7.0 Revision History

Table 19: Revision History

Revision Number	Date	Comments and Changes
1.01	10/00	Updated power consumption & θ_{JC}.
1.00	07/00	Preliminary presilicon revision of data sheet.