Supertex inc.

T-39-13

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
40V	0.3Ω	20A	VN1204N1	VN1204N2	VN1204N5	VN1204ND
60V	0.3Ω	20A	VN1206N1	VN1206N2	VN1206N5	VN1206ND
100V	0.3Ω	20A	VN1210N1	VN1210N2	VN1210N5	VN1210ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

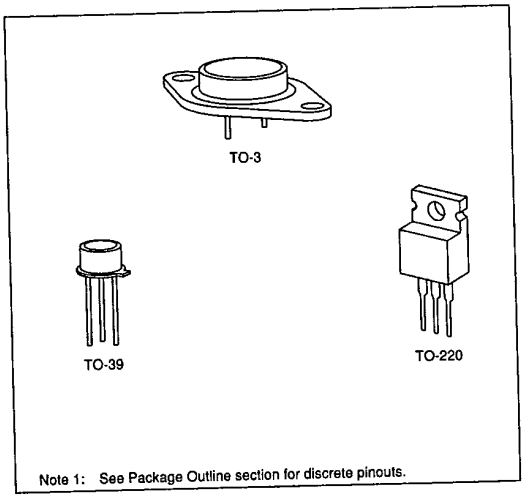
*Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}	I_{DRM}*
TO-3	12A	35A	100W	30	1.25	12A	35A
TO-39	3.5A	15A	6.5W	125	20	3.5A	15A
TO-220	9A	35A	45W	70	2.75	9A	35A

*I_D (continuous) is limited by max rated T_j.

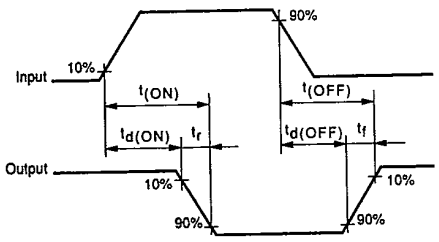
Electrical Characteristics (@ 25°C unless otherwise specified)

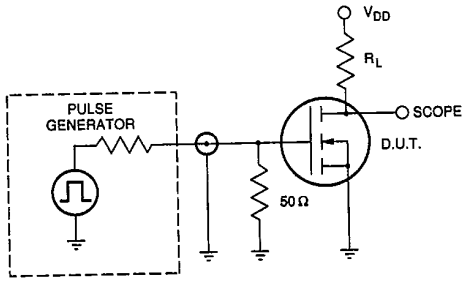
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN1210	100			V	V_{GS} = 0, I_D = 10mA
		VN1206	60				
		VN1204	40				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.3	-5.5	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage			1	100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		5	10		A	V_{GS} = 5V, V_{DS} = 25V
			20	35			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.22	0.45	Ω	V_{GS} = 5V, I_D = 2A
				0.2	0.3		V_{GS} = 10V, I_D = 10A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	V_{GS} = 10V, I_D = 10A
G_{FS}	Forward Transconductance		4.0	4.5		℧	V_{DS} = 25V, I_D = 2A
C_{ISS}	Input Capacitance			600	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			300	350		
C_{RSS}	Reverse Transfer Capacitance			50	75		
$t_{d(ON)}$	Turn-ON Delay Time			8	20	ns	V_{DD} = 25V, I_D = 5A, R_S = 50Ω
t_r	Rise Time			8	20		
$t_{d(OFF)}$	Turn-OFF Delay Time			70	90		
t_f	Fall Time			40	60		
V_{SD}	Diode Forward Voltage Drop			1.2	1.4	V	V_{GS} = 0, I_{SD} = 10A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = 1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

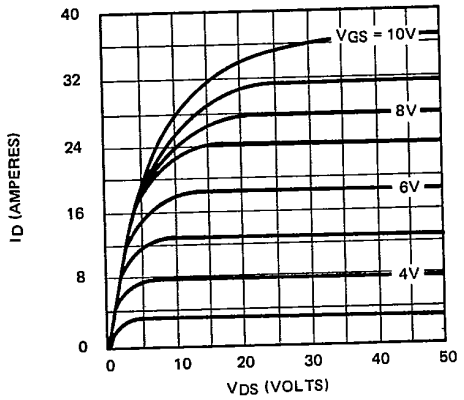




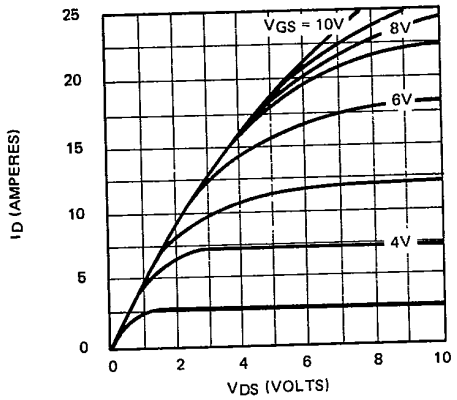
Typical Performance Curves

T-39-13

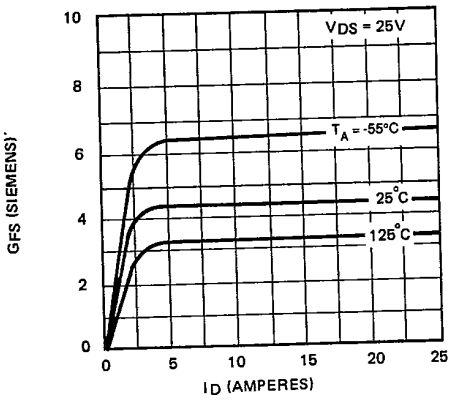
Output Characteristics



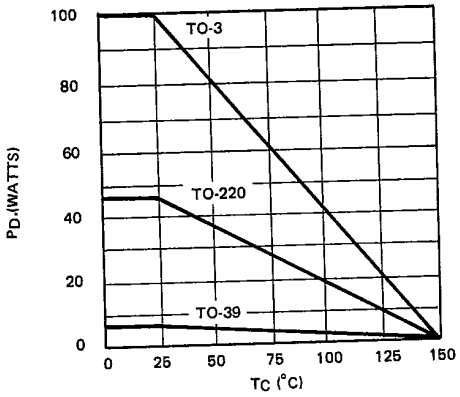
Saturation Characteristics



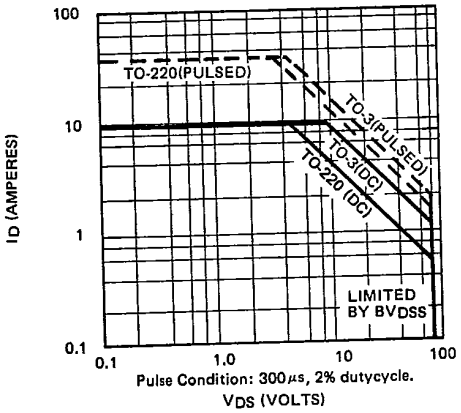
Transconductance Vs. Drain Current



Power Dissipation Vs. Case Temperature

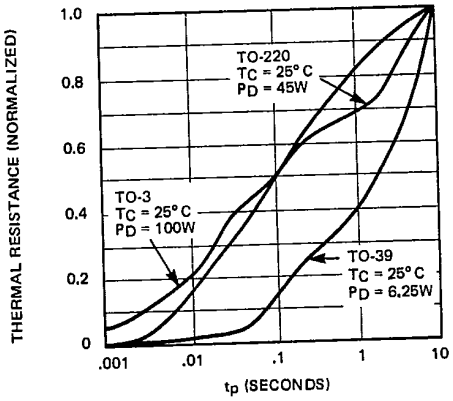


Maximum Rated Safe Operating Area

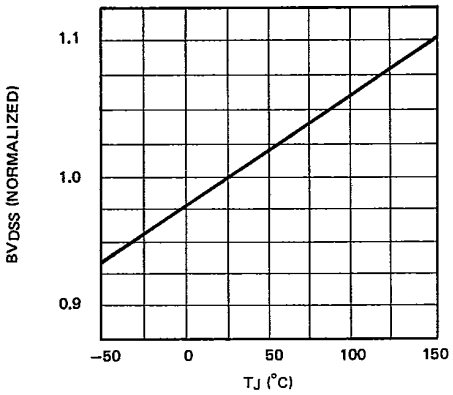


Pulse Condition: 300μs, 2% dutycycle.
VDS (VOLTS)

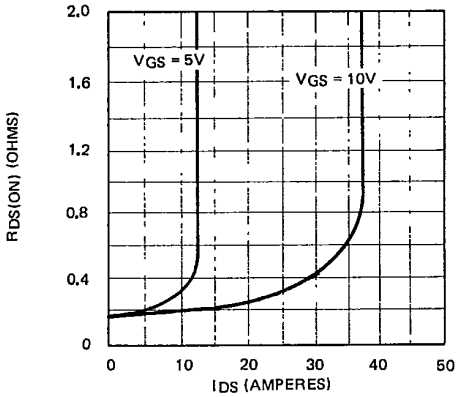
Thermal Response Characteristics



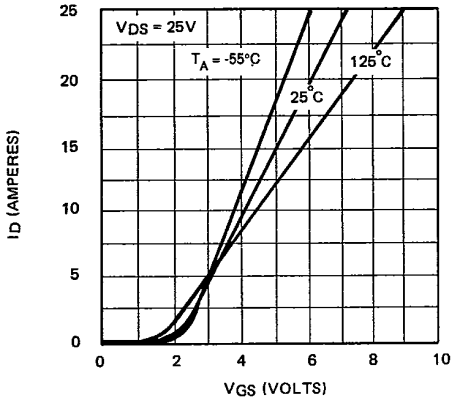
BVDSS Variation with Temperature



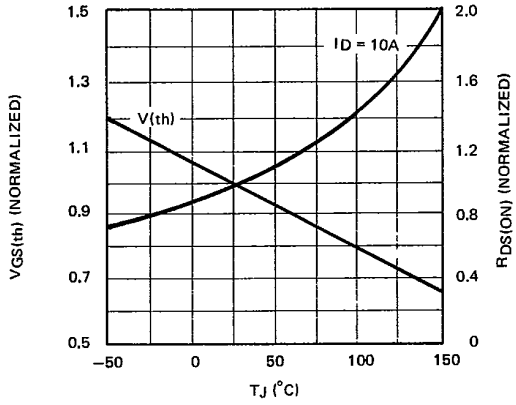
ON - Resistance Vs. Drain Current



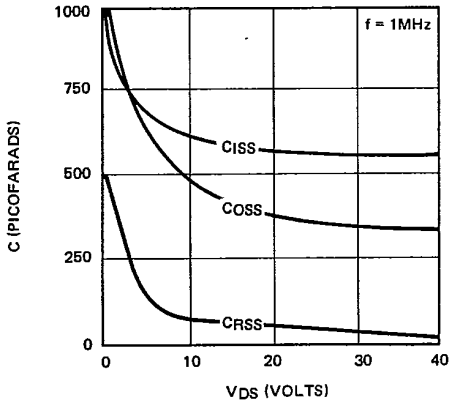
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics