Applications

- Gigabit Ethernet Up-links
- High Speed Proprietary interface
- Backplane Serialization
- Bus Extender

General Description

The VN16118 is a single chip,1.25 Gigabits per second Ethernet transceiver. It performs all the functions of the Physical Medium Attachment (PMA) portion of the Physical layer, as specified by. the IEEE 802.3z Gigabit Ethernet standard. These functions include parallel-to-serial and serial-to-parallel conversion, clock generation, clock data recovery, and word synchronization. In addition, an internal loopback function is provided for system debugging.

The VN16118 is ideal for Gigabit Ethernet, serial backplane and proprietary point-to-point applications. The device supports both 1000BASE-LX and 1000BASE-SX fiber-optic media, and 1000BASE-CX copper media.

The transmitter section of the VN16118 accepts 10-bit wide parallel TTL data and converts it to a high speed serial data stream. The parallel data is encoded in 8b/10b format. This incoming parallel data is latched into an input register, and synchronized on the rising edge of the 125 MHz reference clock supplied by the user. A phase locked loop (PLL) locks to the 125 MHz clock. The clock is then multiplied by 10 to produce a 1.25 GHz serial clock that is used to provide the high speed serial data output. The output is sent through a Pseudo Emitter Coupled Logic (PECL) driver. This output connects directly to a copper cable in the case of 1000BASE-CX medium, or to a fiber optic module in the case of 1000BASE-LX or 1000BASE SX fiber optic medium.

The receiver section of the VN16118 accepts a serial PECL-compatible data stream at a 1.25 Gbps rate, recovers the original 10-bit wide parallel data format, and retimes the data. A Phase Lock Loop (PLL) locks on to the incoming serial data stream, and recovers the 1.25 GHz high speed serial clock and data. This is accomplished by continually frequency locking on to the 125 MHz reference clock, and by phase locking on to the incoming data stream. The serial data is converted back to parallel data format. The ‘comma’ character is used to establish byte alignment. Two 62.5 MHz clocks, 180 degrees out of phase, are recovered. These clocks are alternately used to clock out the parallel data on the rising edge. This parallel data is sent to the user in TTL-compatible form.

Features

- IEEE 802.3z Gigabit Ethernet Compliant
- Supports 1.25 Gbps Using NRZ Coding over uncompensated twin-coax cable
- Fully integrated CMOS IC
- Low Power Consumption
- ESD rating >2000V (Human Body Model) or >200V (Machine Model)
- 5-Volt Input Tolerance
- Fully Compatible with HP HDMP-1636/HDMP-1646 and Vitesse VCS7135 transceivers
- Available in both 10 mm x 10 mm and 14 mm x 14 mm LQFP Packages

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Figure 1. Functional Block Diagram

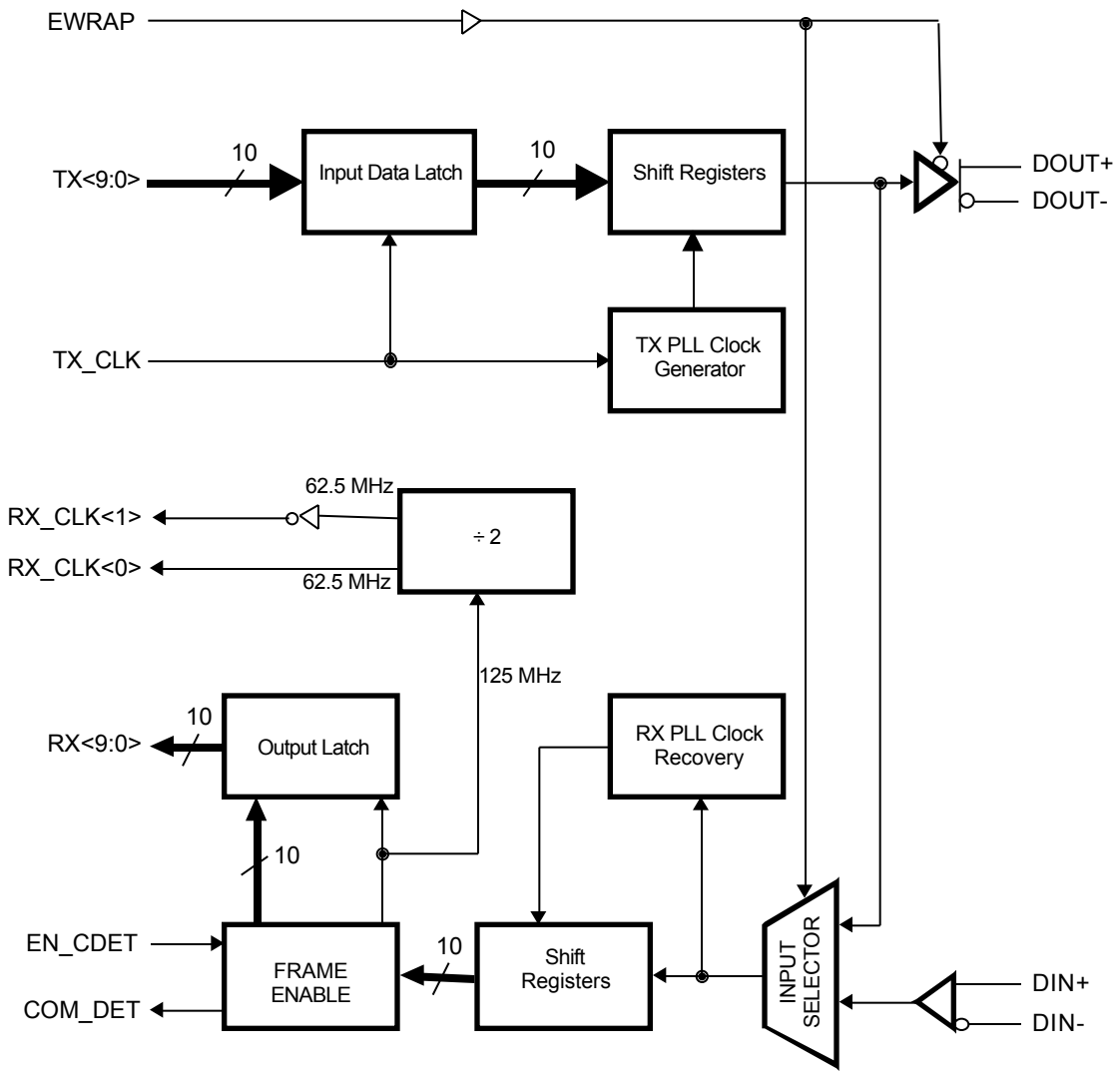

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Figure 2. Pin Configuration (Top View)

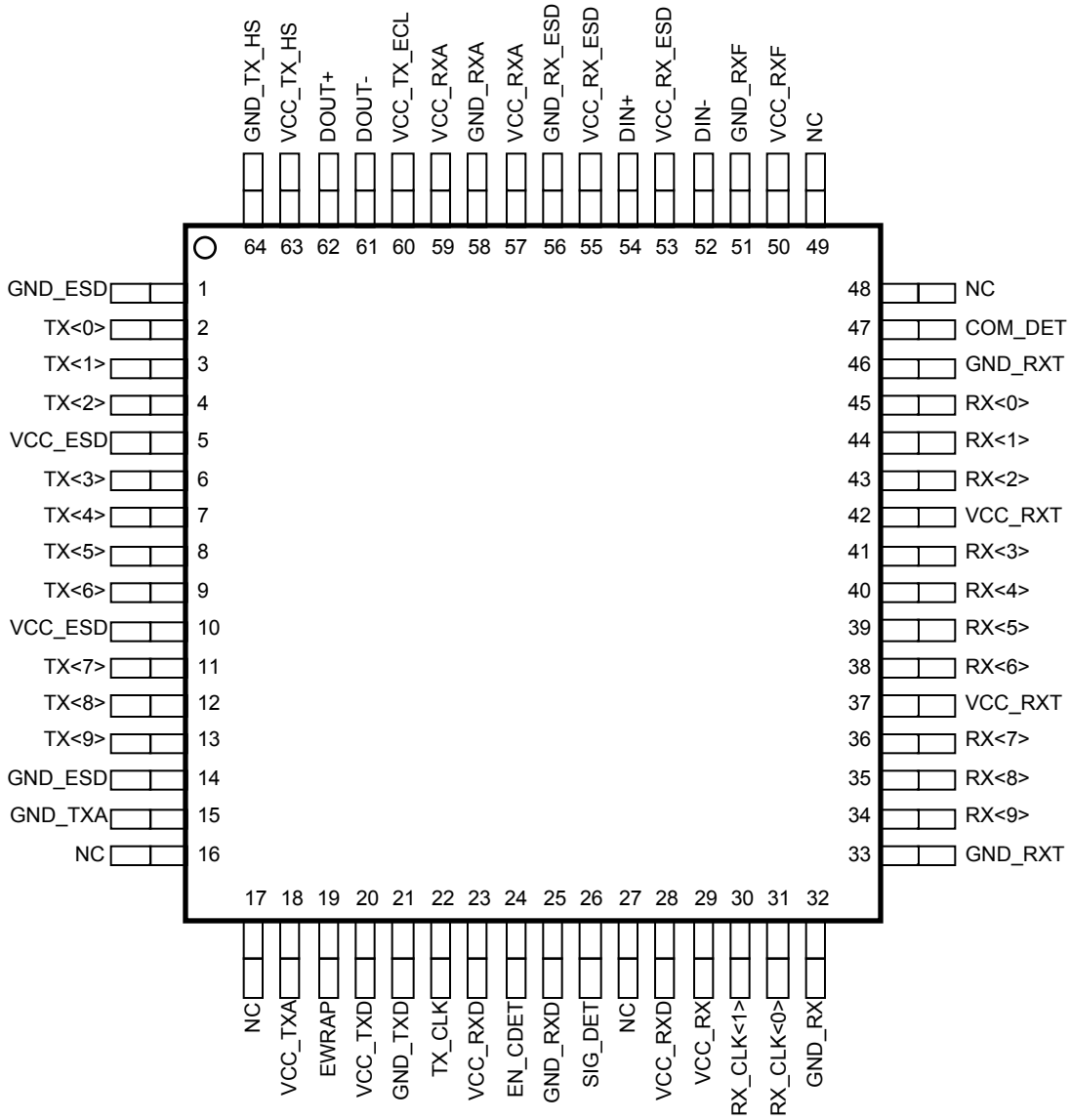

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Table 1. Pin Description

Name	Pin #	Type	Description
GND_ESD VCC_ESD	1, 14 5, 10	Power	Power and ground pairs for pad ESD structure.
TX<0> TX<1> TX<2> TX<3> TX<4> TX<5> TX<6> TX<7> TX<8> TX<9>	2 3 4 6 7 8 9 11 12 13	TTL Input	10-bit parallel data input pins. This data should be 10b/8b encoded. The least significant bit is TX<0> and is transmitted first.
GND_TXA VCC_TXA	15 18	Power	Power and ground pair for TX PLL analog circuits.
NC	16, 17, 27, 48, 49	No Connect	These pins are bonded to isolated pads and have no connection to internal circuits.
EWRAP	19	TTL Input	Wrap Enable. This pin is active HIGH. When asserted, the high-speed serial data are internally wrapped from the transmitter serial data output back to the receiver data input. Also, when asserted, DOUT± are held static at logic 1. When deasserted, DOUT± and DIN± are active.
VCC_TXD GND_TXD	20 21	Power	Power and ground pair for TX digital circuits.
TX_CLK	22	TTL Input	Reference clock and transmit byte clock. This is a 125 MHz system clock supplied by the host system. On the positive edge of the clock, the input data, TX<9:0>, are latched into the register. This clock is multiplied by 10 internally, to generate the transmit serial bit clock.
VCC_RXD GND_RXD	23 28, 25	Power	Power and ground pair for digital circuits in the receiver portion.
EN_CDET	24	TTL Input	Comma Detect Enable. This pin is active HIGH. When asserted, the internal byte alignment function is turned on, to allow the clock to synchronize with the comma character (0011111XXX). When de-asserted, the function is disabled and will not align the clock and data. In this mode COM_DET is set to LOW.
SIG_DET	26	TTL Output	Signal Detect. This pin is active HIGH. It indicates the loss of input signal on the high-speed serial inputs, DIN±. SIG_DET is set to LOW when differential inputs are less than 50 mV.
VCC_RX GND_RX	29 32	Power	Power and ground pair for the clock signal of the receiver portion.
RX_CLK<1> RX_CLK<0>	30 31	TTL Output	Receiver Byte Clocks. Two 180 degrees out-of-phase 62.5 MHz clock signals that are recovered by the receiver section. The received bytes are alternately clocked by the rising edges of these signals. The rising edge of RX_CLK<1> aligns with a comma character when detected.

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Table1. (Continued)

Name	Pin#	Type	Description
GND_RXT VCC_RXT	33 46, 37, 42	Power	Power and ground pairs for ESD structure.
RX<9> RX<8> RX<7> RX<6> RX<5> RX<4> RX<3> RX<2> RX<1> RX<0>	34 35 36 38 39 40 41 43 44 45	TTL Output	Received Parallel Data Output. RX<0> is the least significant bit and is received first. When DIN± lose input data, all RX pins will be held HIGH.
COM_DET	47	TTL Output	Comma detect. This pin is active HIGH. When asserted, it indicates the detection of comma character (0011111XXX). It is active only when EN_CEDT is enabled.
VCC_RXF GND_RXF	50 51	Power	Power and ground pair for the front-end of the receiver section.
DIN+ DIN-	52 54	Input	High-speed serial data input. Serial data input is received when EWRAP is disabled.
VCC_RXESD GND_RXESD	53,55 56	Power	Power and ground pair for ESD structure.
VCC_RXA GND_RXA	57, 59 58	Power	Power and ground pair for analog circuits of the receiver section.
VCC_TX_ECL	60	Power	Power supply to line driver circuits. Ground supply is from pin 64.
DOUT- DOUT+	61 62	Output	High-speed serial data output. These pins are active when EWRAP is disabled and are held static at logic 1 when EWRAP is enable.
VCC_TX_HS GND_TX_HS	63 64	Power	Power and ground pair for high-speed transmit logic in the parallel-to-serial section.

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Functional Block Description

Input Data Latch

The input data latch block latches the 10-bit TTL input parallel byte, TX<9:0>, on the rising edge of the 125 MHz user-provided TX_CLK into the holding registers.

Parallel-to-Serial Converter

The received 10-bit TTL parallel input byte is converted to serial PECL level data stream by the parallel-to-serial block, and is transmitted differentially to the line driver block at 1.25 Gbps. The 8b/10b encoded data is transmitted sequentially with bit 0 being sent first.

Clock Generator

The 1250 MHz signal used for clocking the serial outputs is generated by the TX PLL block based on the user-provided TX_CLK. This clock should have a ±100 ppm tolerance.

Internal Loopback

When EWRAP is set to a logic HIGH, the serial data stream generated by the transmitter is looped back to the receiver path, instead of going out to the DOUT± pins. When in loopback mode, a static logic 1 is transmitted at the line driver (DOUT+ is HIGH and DOUT- is LOW).

Signal Detect

Signal detect block is used to sense the serial input data stream at pins DIN±. If the serial input is lower than 50 mV differentially, this block deasserts SIG_DET and sets the output, RX<9:0>, to all logic ones. When the serial input at pins DIN± is greater than 50 mV, the signal is directed to the receive path.

Equalizer and Slicer

The signal received from the line (DIN± pins) is distorted by the cable bandwidth. In order to maintain a low bit-error rate, an equalizer is used to compensate for the signal loss. The slicer recovers the differential low-level signal to a CMOS-level single-ended signal, for clock recovery and data re-timing.

Clock Recovery

The serial input data stream contains both data and clock. The clock recovery block is used to extract both data and clocks from this input. In addition to data, two clocks of 62.5 MHz are recovered.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{cc}	Supply voltage	-0.5	5.0	V
$V_{IN,TTL}$	TTL Input Voltage	-0.7	Vcc + 2.8	V
V_{IN,HS_IN}	HS_IN Input Voltage	2.0	Vcc	V
$I_{O,TTL}$	TTL Output Source Current		13	mA
T_{stg}	Storage Temperature	-65	+150	°C
T_j	Junction Operating Temperature	0	+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

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Table 3. Guaranteed Operating Rates

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Parallel Clock Rate (MHz)		Serial Baud Rate (Mbaud)	
Min.	**Max.**	**Min.**	**Max.**
124.0	126.0	1240	1260

Table 4. AC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_{r,REFCLK}$	REFCLK Rise Time, 0.8 to 2.0 Volts			2.4	nsec
$t_{f,REFCLK}$	REFCLK Fall Time, 2.0 to 0.8 Volts			2.4	nsec
$t_{r,TTLin}$	Input TTL Rise Time, 0.8 to 2.0 Volts		2		nsec
$t_{f,TTLin}$	Input TTL Fall Time, 2.0 to 0.8 Volts		2		nsec
$t_{r,TTLout}$	Output TTL Rise Time, 0.8 to 2.0 Volts, 10 pF Load		1.5	2.4	nsec
$t_{f,TTLout}$	Output TTL Fall Time, 2.0 to 0.8 Volts, 10 pF Load		1.1	2.4	nsec
t_{rs,HS_OUT}	HS_OUT Single-Ended (DOUT+) Rise Time	85	225	327	psec
t_{fs,HS_OUT}	HS_OUT Single-Ended (DOUT+) Fall Time	85	200	327	psec
t_{rd,HS_OUT}	HS_OUT Differential Rise Time	85		327	psec
t_{fd,HS_OUT}	HS_OUT Differential Fall Time	85		327	psec
V_{IP,HS_IN}	HS_IN Input Peak-to-Peak Differential Voltage	200	1200	2000	mV
V_{OP,HS_OUT} (1)	HS_OUT Output Peal-to-Peak Differential Voltage	1200	1600	2000	mV

Note:
1. Output Peak-to-Peak Differential Voltage specified as DOUT+ minus DOUT-

Table 5. DC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed High Signal for All Inputs	2		5.5	V
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed Low Signal for All Inputs	0		0.8	V
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = -400 µA	2.2		V_{CC}	V
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 1 mA	0		0.6	V
$I_{IH,TTL}$	Input High Current, V_{IN} = 2.4 V, V_{CC} = 3.45 V			40	µA
$I_{IL,TTL}$	Input Low Current, V_{IN} = 0.4 V, V_{CC} = 3.45 V			-600	µA
$I_{CC,TRX}$[1,2]	Transceiver V_{CC} Supply Current, TA = 25°C		220		mA

Notes:
1. Measurement Conditions: Tested sending 1250 MBd PRBS 2^7-1 sequence from a serial Bit Error Rate Tester (BERT) with DOUT± outputs terminated with 150 Ω resistors to GND.
2. Typical values are at Vcc = 3.3 volts.

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Table 6. Transceiver Reference Clock Requirements

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
f	Nominal Frequency (for gigabit Ethernet Compliance)		125		MHz
F_{tol}	Frequency Tolerance	-100		+100	ppm
Symm	Symmetry (Duty Cycle)	40		60	%

Table 7. Transmitter Timing Characteristics

T_A = 0°C to +70°C, V_{CC} = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{setup}	Setup Time to Rising Edge of REFCLK	1.5			nsec
t_{hold}	Hold Time to Rising Edge of REFCLK	1.0			nsec
t_txlat[1]	Transmitter Latency		3.5		nsec
			4.4		bits

Note:
1. The transmitter latency, as shown in Figure 4, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit by clock, REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

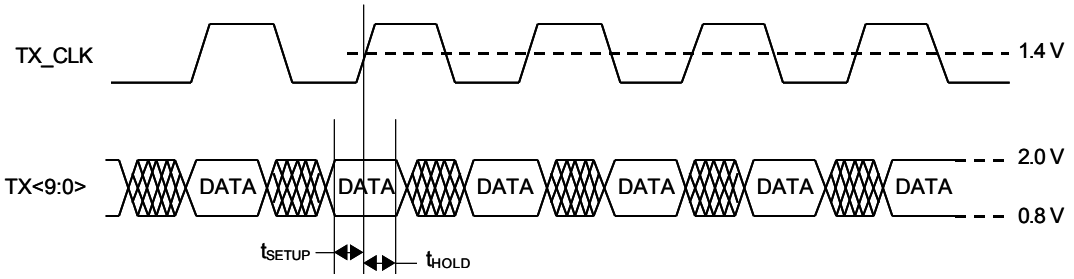

Figure 3. Transmitter Section Timing

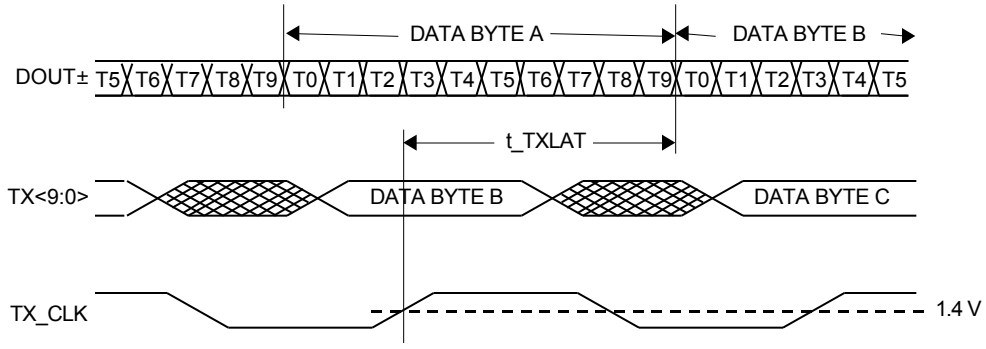

Figure 4. Transmitter Latency

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Table 8. Receiver Timing Characteristics

TA = 0°C to +70°C, Vcc = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
b_sync[1]	Bit Sync Time			2500	bits
f_lock	Frequency Lock at Powerup			500	µs
t_{SETUP}	Data Setup Before Rising Edge of RX_CLK	2.5			nsec
t_{HOLD}	Data Hold After Rising Edge of RX_CLK	1.5			nsec
t_{DUTY}	RX_CLK Duty Cycle	40		60	%
t_{A-B}	RX_CLK Skew	7.5		8.5	nsec
T_rxlat[2]	Receiver Latency		22.4		nsec
			28.0		bits

Notes:
1. This is the recovery for input phase jumps.
2. The receiver latency as shown in Figure 6, is defined as the time between receiving the first serial bit of a parallel data word (defined as the first edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC1 or RBC0).

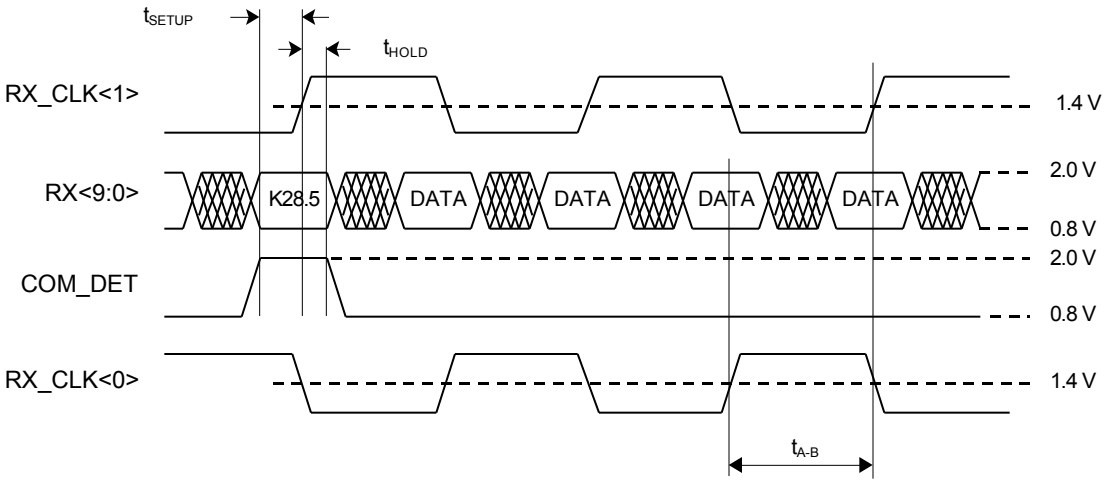

Figure 5. Receiver Section Timing

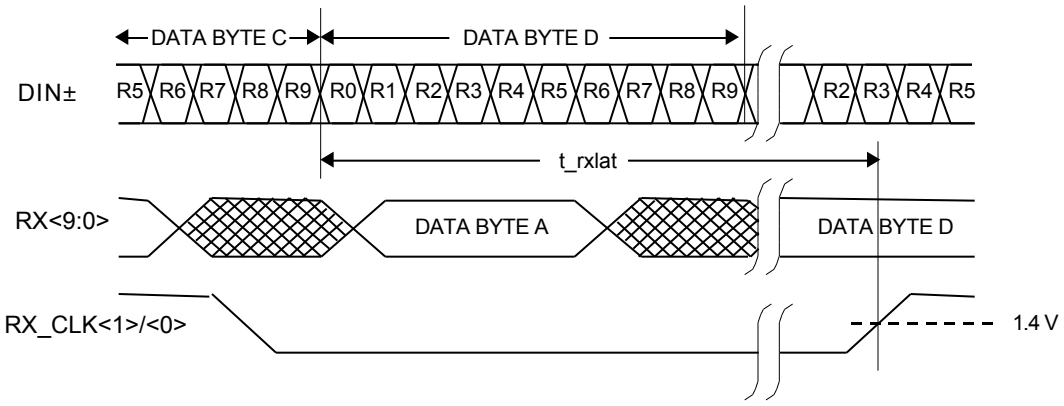

Figure 6. Receiver Latency

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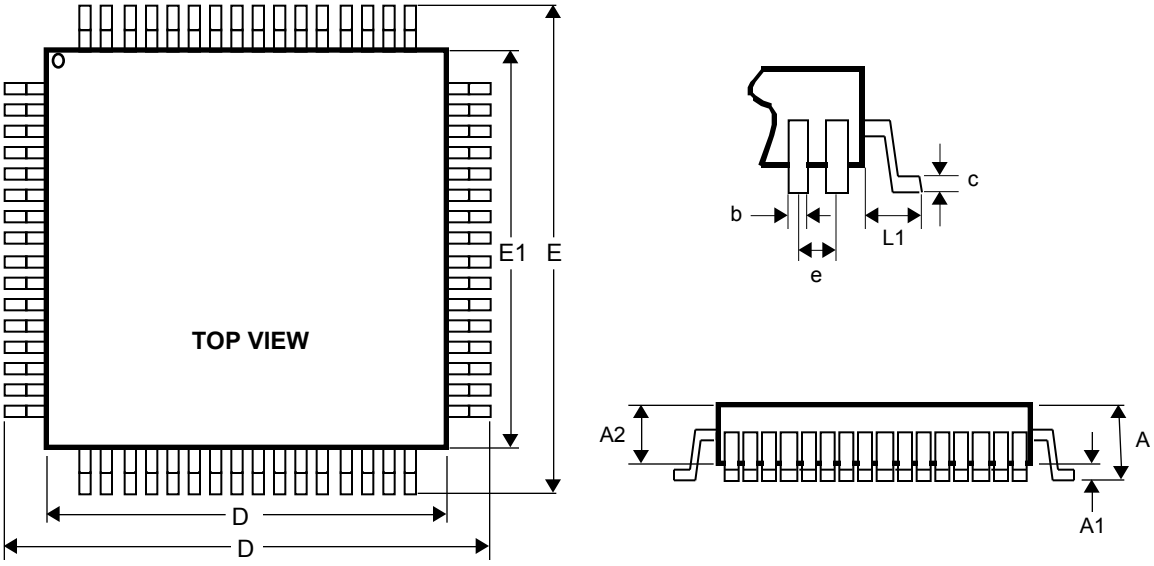

Figure 7. Mechanical Dimensions

All dimensions are in millimeters

PART NUMBER	D1/E1	D/E	b	e	L1	c	A2	A1	A
VN16118L1	10	12	0.2	0.5	1.0	0.127	1.4	0.1	1.5
VN16118L2	14	16	0.35	0.8	1.0	0.127	1.4	0.1	1.5

Package follows JEDEC Standards

Ordering Information

Part Number	No. of Pins	Package	Temperature
VN16118L1	64	LQFP	0°C to +70°C
VN16118L2	64	LQFP	0°C to +70°C

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