Vaishali Semiconductor

VN16218

2.5 Gigabit SERDES Transceiver

Applications

- Fast serial backplane transceiver
- High-speed point-to-point links

General Description

The VN16218 is a low power single chip, 2.5GBd transceiver. It provides a 2.5GBd serial link interface in the physical layer and includes a Serialize/Deserialize (SERDES) capability. Other functions include clock generation, clock data recovery, and word synchronization. In addition, an internal loopback function is provided for system debugging.

The VN16218 is ideal for 2.5 Gigabit, serial backplane and proprietary point-to-point applications. The device supports both fiber-optic and copper media.

The transmitter section of the VN16218 accepts 20-bit wide TTL data and latches it on the rising edge of the incoming Transmit Byte Clock (TBC) and serializes the data onto the TX± differential outputs, at a baud rate that is twenty times the TBC frequency. The data is converted to a high-speed serial data stream. The transmit PLL locks to the 125 MHz TBC. This clock is then multiplied by 20 to supply a 2.5 GHz serial clock for parallel-to-serial conversion. The high-speed serial outputs can interface directly with copper cables or PCB traces. Where optical transmission is required, the outputs can connect to a separate optical module. When copper lines are the medium, equalization is available for improved performance.

The receiver section of the VN16218 accepts a serial data stream of 2.5 GBd and recovers 20 bit parallel data. The receiver PLL locks on to the incoming serial signal and recovers the high-speed incoming clock and data. The serial data is converted back into 20-bit parallel data format. Byte alignment is accomplished by optional recognition of the K28.5+ comma character.

The recovered parallel data is sent to CMOS outputs, together with two 125 MHz clocks, RBC and RBCN, that are 180 degrees out of phase from each other.

Features

- 20-bit wide parallel Tx, Rx busses
- 20-bit LVTTL interface for transmit and receive data at 125 MHz
- 125 MHz complementary receive and byte clocks
- Low Power Consumption
- ESD rating >2000V (Human Body Model) or >200V (Machine Model)
- Parallel loopback mode
- Available in 14 mm x 14 mm LQFP package
- Differential PECL serial output
- I/O power supply 3.3V
- Core power supply 1.8 V

www.vaishali.com
Vaishali Semiconductor ● 747 Camden Avenue, Suite C ● Campbell ● CA 95008 ● Ph. 408.377.6060 ● Fax 408.377.6063

Figure 1. Functional Block Diagram

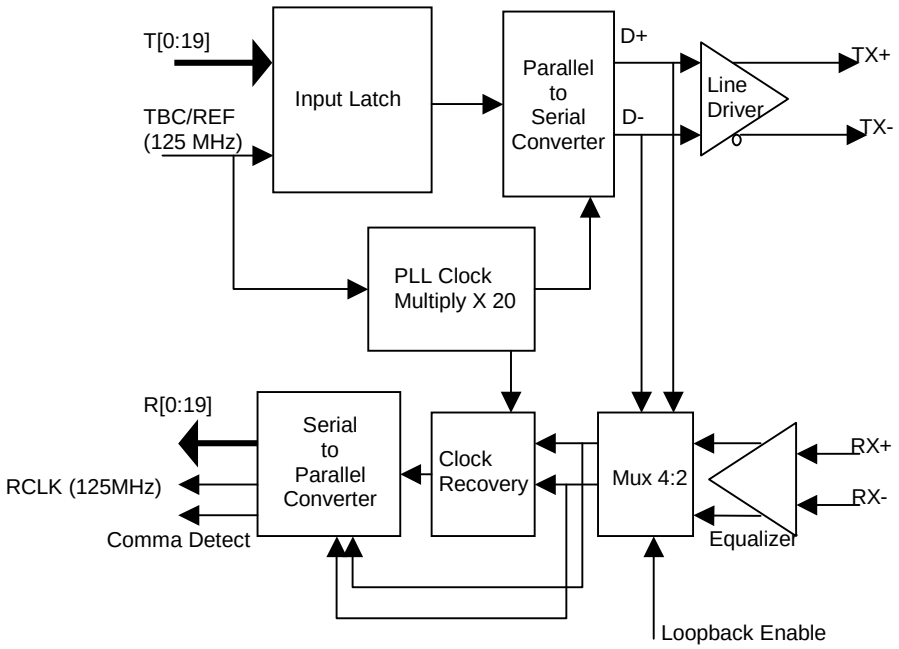
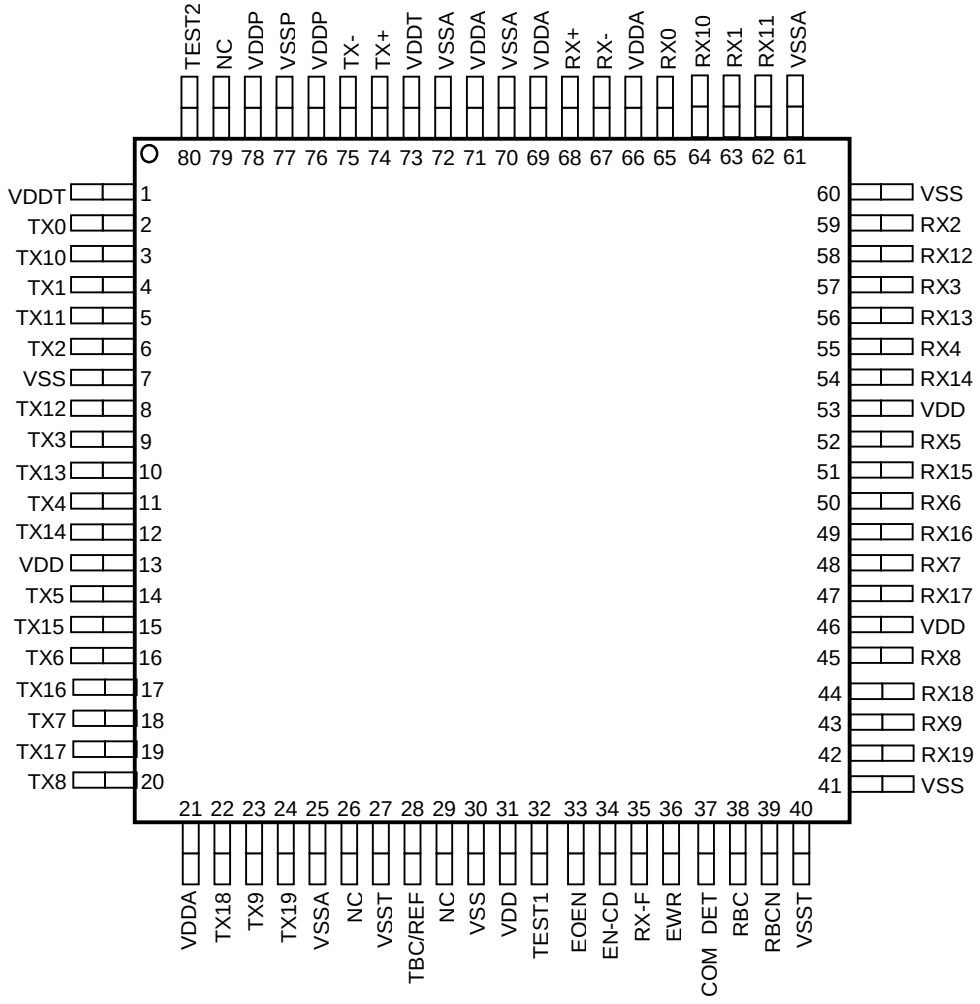


Figure 2. Pin Configuration



www.vaishali.com
Vaishali Semiconductor ● 747 Camden Avenue, Suite C ● Campbell ● CA 95008 ● Ph. 408.377.6060 ● Fax 408.377.6063

Table 1. Pin Description

Name	Pin #	Type	Description
VDDT	1, 73	P	3.3V power supply
VSS	7, 30, 41, 60	P	Digital Ground. 0V
VDD	13, 31, 46, 53	P	Digital Power Supply. Connect to 1.8V
VDDA	21, 66, 69, 71	P	Analog Power Supply. Connect to 1.8V
TX[0:19]	2, 4, 6 9,11, 14 16, 18, 20 23, 3, 5 8,10,12 15, 17, 19 22, 24	I-TTL	Transmit Data Bus (bits 0 through 19). 20 bit transmit character. Parallel data on this bus is clocked in on the rising edge of TBC. The data bit corresponding to T0 is transmitted first
VSSA	25, 61, 70, 72	P	Analog Ground. 0V
NC	26, 29, 79		No Connection
VSST	27, 40	P	TTL ground
TBC/REF	28	I-TTL	Transmit Byte Clock / Reference Clock . A 125 MHz clock supplied by the host system. The transmitter section accepts this signal as the frequency reference clock. It is multiplied by 20 to generate the serial bit clock and other internal clocks. The transmit side also uses this clock as the transmit byte clock for the incoming parallel data TX0 …. TX19. It also serves as the reference clock for the receive portion of the transceiver
TEST1	32	I-TTL	Test pin. For Vaishali use only. User should connect to V_{DD}
EQEN	33	I-TTL	Equalizer enable
EN_CD	34	I-TTL	Enables comma detect
RX-F	35	O	Receiver filter pin. For Vaishali use only.
EWR	36	I-TTL	Enable Internal WRAP mode. This pin is LOW in normal operation. When enabled High, an internal loop-back path from the transmitter to the receiver is enabled, TX+ is HIGH and TX- is LOW
COM_DET	37	O-TTL	Comma Detect. This output goes HIGH to signify that R0:6 contains a comma character (0011111). COM_DET can be sampled on the rising edge of TBC
RBC, RBCN	38, 39	O-TTL	Recovered Byte Clock. Recovered clock and its complement derived from the RX± data rate divided by 20. The rising edge of RBC corresponds to a new word on RX[0:19]

Name	Pin #	Type	Description
RX[0:19]	65, 63, 59 57, 55, 52 50, 48, 45 43, 64 ,62 58, 56, 54 51,49,47 44, 42	O-TTL	Receive Data Bus, Bits 0 through 19. 20 bit received data character. Parallel data on this bus can be sampled on the rising edge of RBC. R0 is the first bit received on RX+/RX-
RX+, RX-	68, 67	I-diff	Receiver serial inputs. The device recognizes receiver inputs when EWR is LOW
TX+, TX-	74, 75	O diff	Transmitter serial ouputs. When EWR is LOW, the serialized transmit data is available on these pins. When EWR is HIGH, TX+ is HIGH and TX- is LOW
VDDP	76,78	P	High-speed output driver power supply. Connect to 1.8V
VSSP	77	P	High speed output driver ground. 0V
TEST2	80	I-TTL	Test pin for Vaishali internal use only. User should tie this pin to GND for normal operation

Legend: I = Input
O = Output
P = Power supply connection

Functional Block Description

PLL Clock Multiplier

The VN16218 employs a user-supplied 125 MHz clock both as a reference clock and as a Transmit Byte Clock (TBC). The PLL Clock Multiplier multiplies the TBC by 20 to generate a baud rate clock of 2.5 GHz. The TBC also clocks in the incoming parallel data.

Serializer (Parallel-to-Serial Converter)

Input data arrives at the T[0:19] bus as two parallel 10 bit characters and is latched into the input latch on the rising edge of TBC. The data is serialized and transmitted on the TX differential outputs at a baud rate of twenty times the frequency of TBC. Bit T0 is transmitted first. Incoming data is already encoded for transmission using either the 8B/10B block code, as specified in the Fibre Channel specification, or an equivalent edge-rich, DC-balanced code. If EWR is HIGH, the transmitter will be disabled, with TX+ HIGH and TX- LOW. If EWR is LOW, the transmitter outputs serialized data. According to the fibre channel specification, a transmission character is an encoded byte of 10 bits. The 20 bit interface of the VN16218 corresponds to two transmission characters, as shown in Table 2 below.

Table 2. Transmission Sequence and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Valid Comma Pos.														1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Vaishali Semiconductor ● 747 Camden Avenue, Suite C ● Campbell ● CA 95008 ● Ph. 408.377.6060 ● Fax 408.377.6063

Equalizer

When EQEN is HIGH, the equalizer at the receiver is enabled, in order to correct for the frequency response of the cable or other system components. The equalizer compensates for distortion introduced by the cable, in order to maintain a low bit-error rate.

Input Latch

The transmitter accepts 20 bits wide single-ended parallel input T[0:19]. The TBC provided by the sender of the transmit data is used as the transmit byte clock. The T[0:19] and TBC signals must be aligned as shown in Figure 5. The T[0:19] data is latched on the rising edge of TBC.

Clock Recovery

When EWR is LOW, the VN16218 accepts differential high-speed inputs on the RX+ and RX- pins, extracts the clock and retimes the data. The serial bit stream should be encoded in a Fibre Channel compatible 8B/10B, or equivalent format, in order to accomplish DC-balance and limited run length. Clock recovery circuitry is self-contained and does not require external components. The baud rate of the data stream to be recovered should be within 200 ppm of twenty times the TBC frequency. This allows oscillators at either end of the link to be 125 MHz $\pm$ 100ppm.

Deserializer (Serial-to-Parallel Converter)

The re-timed serial bit stream is converted into two 10-bit parallel output characters. The VN16218 provides a TTL recovered clock (RBC) at one-twentieth the serial baud rate. This is accomplished by dividing down the high-speed clock that is phase locked to the serial data. The serial data is re-timed by the internal high-speed clock and deserialized. Parallel data results, and is captured by the adjoining protocol logic on the rising edge of RBC

Word Alignment

The VN16218 has 7-bit Fibre Channel comma character recognition, and data word alignment. Word synchronization (with EN_CD HIGH), causes the VN16218 to constantly search the serial data for the presence of the Fibre Channel ‘comma’ character. This pattern is ‘0011111XX’: the leading zero corresponds to the first bit received. The comma sequence occurs only within special characters (K28.1, K28.5 and K28.7) that are defined specifically for synchronization in Fibre Channel systems.
Improper alignment condition of the comma character is defined as;

1. The comma is not aligned within the 10 bit transmission character such that T0…T6 = ‘0011111’
2. The comma straddles the boundary between two 10-bit transmission characters.

When EN_CD is HIGH and an improperly aligned comma is encountered, the internal data is shifted so that the comma character is aligned properly in R0:6, as shown in Table 2. The result is proper character and word alignment. When an improperly aligned comma pattern causes changes in parallel data alignment, some data that would have been presented at the parallel output port may be lost. However, the synchronization character and subsequent data will be sent correctly and properly aligned. With EN_CD LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.
A ‘comma’ character drives COM_DET HIGH to notify the user that realignment of the parallel data field may have occurred. The COM_DET pulse occurs simultaneously with the ‘comma’ character and has a duration equal to that of the data. The COM_DET pulse is timed so that it is captured by the adjoining protocol logic, on the rising edge of RBC. Figures 3 and 4 show functional waveforms for synchronization. Figure 3 illustrates the situation when a ‘comma’ character is detected, but no phase adjustment is necessary. The position of the COM_DET pulse is shown in relation to the ‘comma’ character on R0:6. Figure 4 illustrates the situation when K28.5 is detected, but is out- of-phase, and a change in the output data alignment is required. It should be noted that up to three characters before the ‘comma’ character may be corrupted by the realignment process.

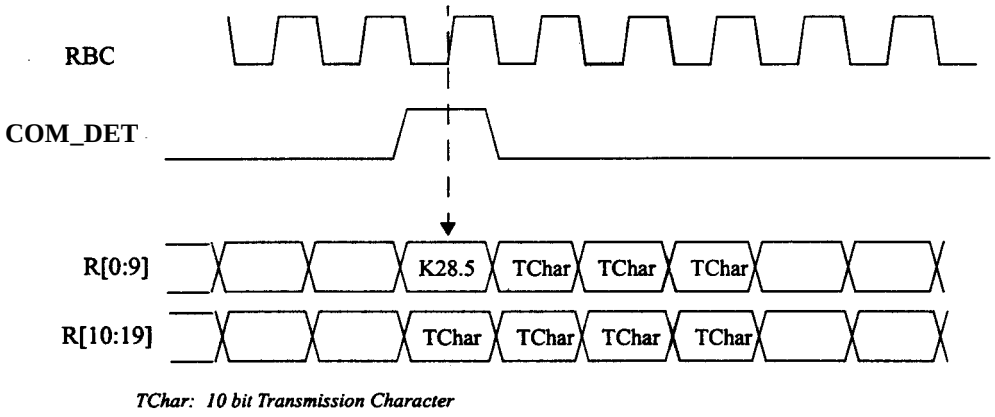


Figure 3. Detection of a Properly Aligned Comma Character

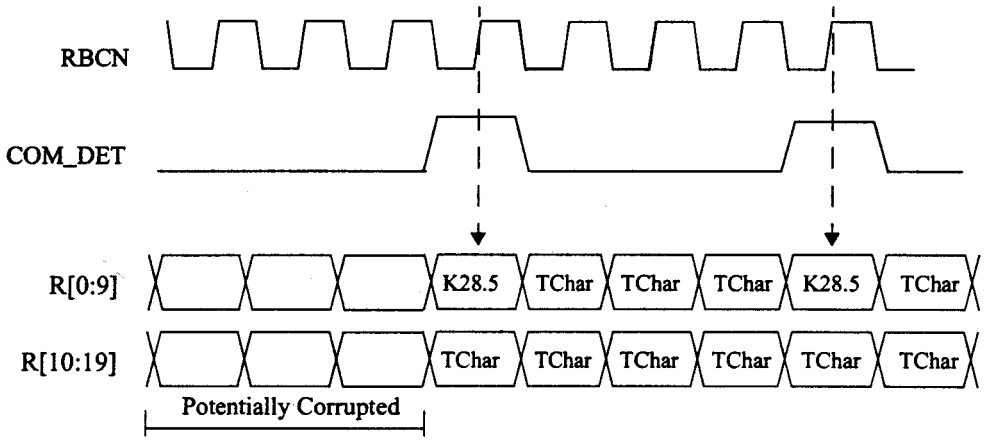


Figure 4. Detection and Resynchronization of an Improperly Aligned Comma Character

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Units
VDDT	3.3V Supply voltage		-0.5	4.6	V
VDD	1.8V Power Supply voltage		-0.5	2.5	V
V_{IN}	Differential Input Voltage		-0.5	V_{DD} + 0.5	V
T_C	Case temperature		0	95	°C
T_{stg}	Storage Temperature		-65	+150	°C
T_j	Junction Operating Temperature		0	+125	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4. Guaranteed Operating Rates

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Parallel Clock Rate (MHz)		Serial Baud Rate (GBd)		Serial Baud Rate (GBd)	
Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
124.0	126.0	1.24	1.26	2.48	2.52

Table 5. AC Electrical Characteristics

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rd}	TX+, TX- Differential Rise Time, 20 % - 80%			160		psec
t_{fd}	TX+, TX- Differential Fall Time 20% - 80%			160		psec

Table 6. DC Electrical Characteristics

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IPD}	TX+, TX- Input peak-to-peak differential voltage		200		2000	mV
V_{OP} (1)	TX+, TX- Output Peak-to-Peak Differential Voltage (Zo=50Ω)		800	1050	2000	mV
V_{OP} (1)	TX+, TX- Output Peak-to-Peak Differential Voltage (Zo=75Ω)		1100	1400	2000	mV

Note:
1. Output Peak-to-Peak Differential Voltage specified as TX+ minus TX.

Table 7. Transceiver Reference Clock and TBC Requirements

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f	Nominal Frequency (for gigabit Ethernet Compliance)			125		MHz
F_{tol}	Frequency Tolerance		-100		+100	ppm
Symm	Symmetry (Duty Cycle)		40		60	%

Table 8. Transceiver DC Electrical Specifications

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC} (1)	Transceiver supply Current (Total of all Supplies)			220		mA
P_D (1)	Transceiver Total Power Dissipation			450		mW

Note: 1. Measurement conditions: Tested sending 2.5GBd 2^7 –1 PRBS from a serial BERT with TX± outputs terminated with 100 ohm resistors.

Table 9. DC Electrical Specifications for Differential Inputs (Rx+, Rx-)

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IHD}	Input High Voltage Level		2.1		2.6	V
V_{ILD}	Input Low Voltage Level		1.3		1.8	V

Table 10. DC Electrical Specifications for LVTTL Inputs

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V. VDD = 1.7V to 1.9V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage Level		2.00			V
V_{IL}	Input Low Voltage Level				0.80	V

Table 11. Transmitter Timing Characteristics

T_A = 0°C to +70°C, VDDT = 3.15 V to 3.45 V, VDD = 1.7V to 1.9V

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{setup}	Setup Time to Rising Edge of TBC	1.5			nsec
t_{hold}	Hold Time to Rising Edge of TBC	1.0			nsec
t_txlat[1]	Transmitter Latency		3.5		nsec
			0.8ns+ 8.5 bits		

Note:
The transmitter latency, as shown in Figure 6, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock, TBC) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

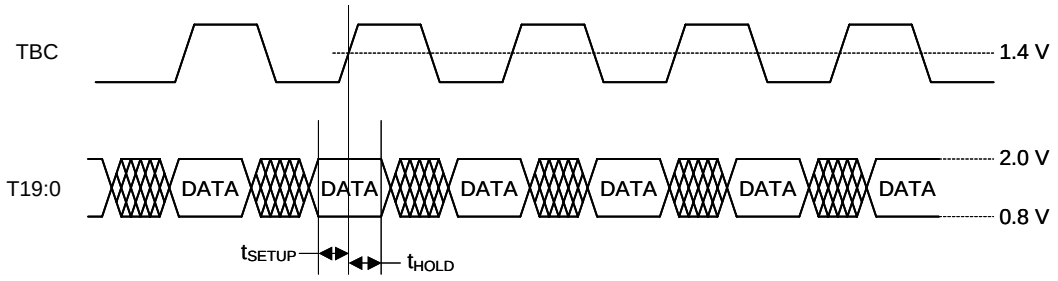


Figure 5. Transmitter Section Timing

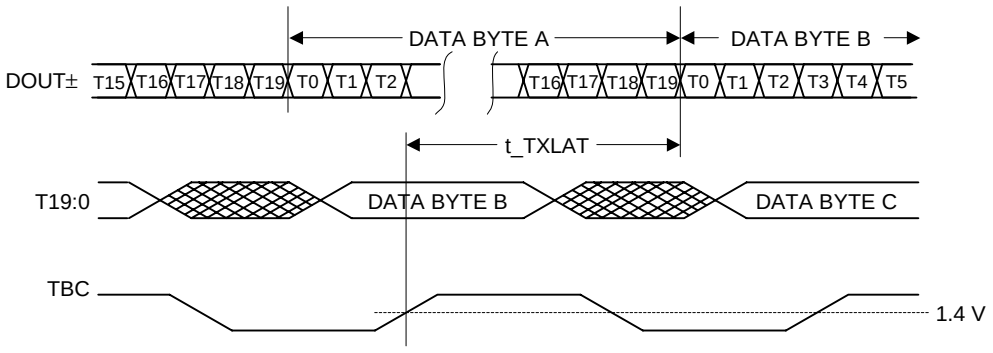


Figure 6. Transmitter Latency

Table 12. Receiver Timing Characteristics

TA = 0°C to +70°C, Vcc = 3.15 V to 3.45 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
b_sync[1]	Bit Sync Time			2500	bits
f_lock	Frequency Lock at Powerup			500	µs
t_{SETUP}	Data Setup Before Rising Edge of RBC,RBCN	2.5			nsec
t_{HOLD}	Data Hold After Rising Edge of RBC,RBCN	1.5			nsec
t_{DUTY}	RBC,RBCN Duty Cycle	40		60	%
t_{A-B}	RBC,RBCN Skew	7.5		8.5	nsec
T_rxlat[2]	Receiver Latency		22.4		nsec
			28.0		bits

Notes:
1. This is the recovery for input phase jumps.
2. The receiver latency as shown in Figure 8, is defined as the time between receiving the first serial bit of a parallel data word (defined as the first edge of the first serial bit) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, either RBC or RBCN).

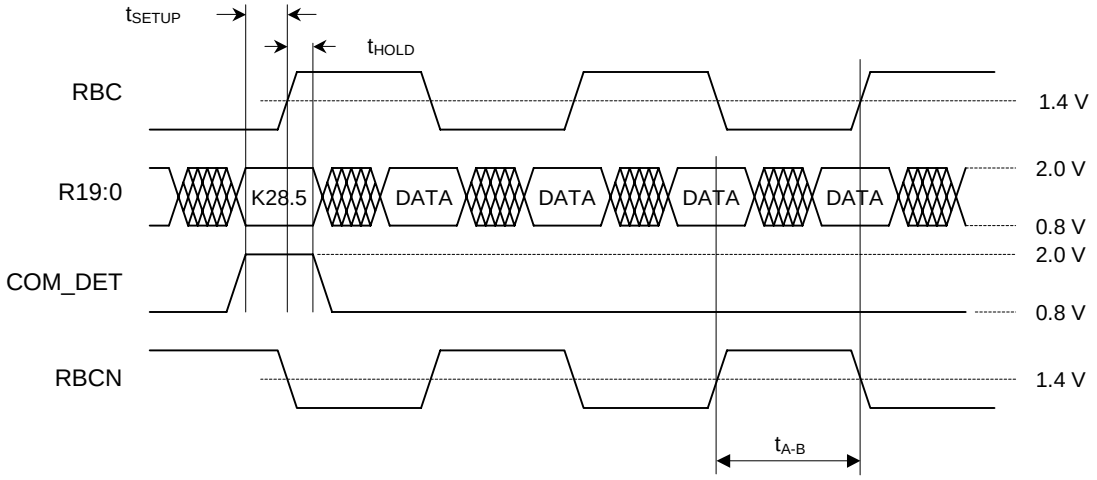


Figure 7. Receiver Section Timing

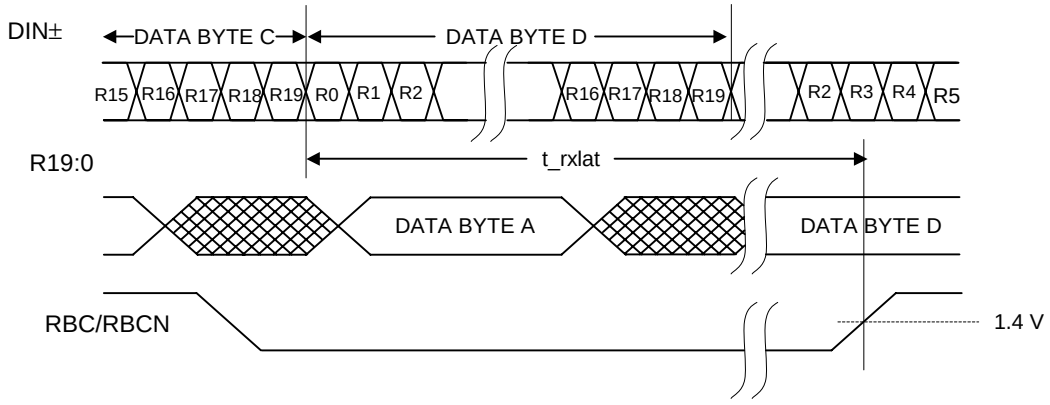
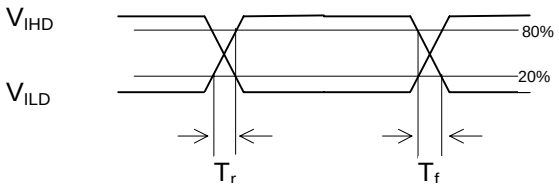


Figure 8. Receiver Latency

Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

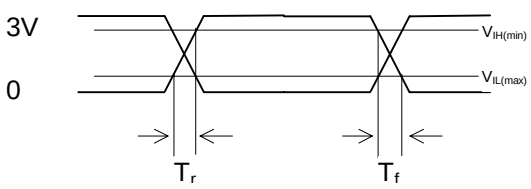


Figure 9. Parametric Measurement Information

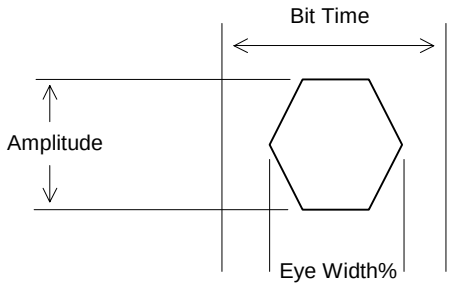
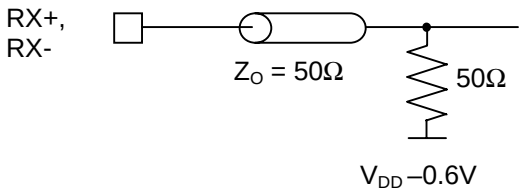


Figure 10. Receiver Input Eye Jitter Tolerance Mask Diagram

Serial Output Load



Serial Output Load

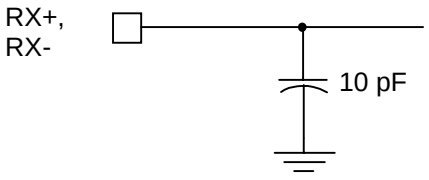
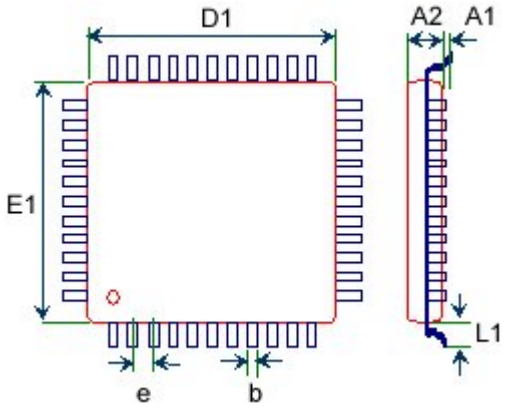


Figure 11. Parametric Test Load Circuit

Figure 12. Mechanical Dimensions

80 Pin LQFP



A1	stand-off
A2	body thickness
L1	lead length
b	lead width
c	lead thickness
e	lead pitch

All dimensions are in millimeters

D1/E1	b	e	L1	c	A2	A1	A
14	0.3	0.65	1.0	0.127	1.4	0.1	1.5

Package follows JEDEC Standards

Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
VN16218L2	VN16218L2	Trays	80	LQFP	0°C to +70°C