N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	Order Number / Package			
			TO-92	14-Pin P-DIP	TO-243AA*	Die†
50V	0.3Ω	2.4V	VN3205N3	VN3205N6	VN3205N8	VN3205ND

* Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

† MIL visual screening available

Product marking for TO-243AA:

VN2L❋

Where ❋ = 2-week alpha date code

Features

- ❏ Free from secondary breakdown
- ❏ Low power drive requirement
- ❏ Ease of paralleling
- ❏ Low C_{ISS} and fast switching speeds
- ❏ Excellent thermal stability
- ❏ Integral Source-Drain diode
- ❏ High input impedance and high gain
- ❏ Complementary N- and P-channel devices

Applications

- ❏ Motor controls
- ❏ Converters
- ❏ Amplifiers
- ❏ Switches
- ❏ Power supply circuits
- ❏ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

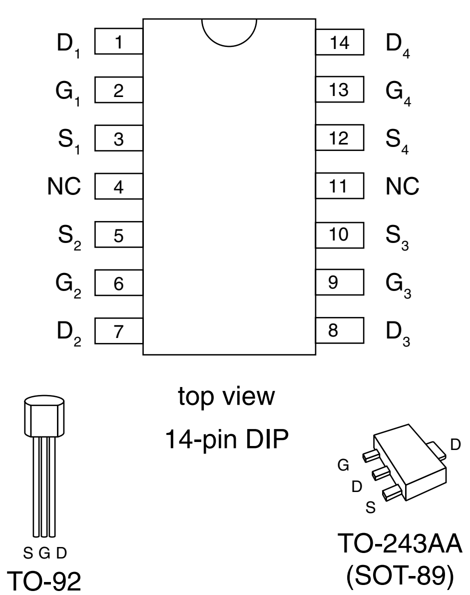
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note: See Package Outline section for dimensions.

11/12/01

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	1.2A	8.0A	1.0W	125	170	1.2A	8.0A
SOT-89	1.5A	8.0A	1.6W ($T_A = 25°C$)	15	78†	1.5A	8.0A
Plastic DIP	1.5A	8.0A	3.0W‡	41.6‡	83.3‡	1.5A	8.0A

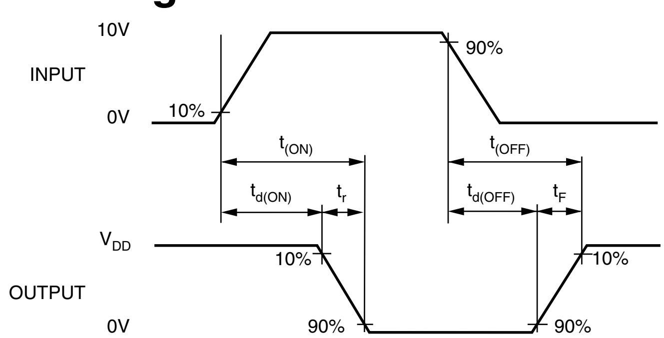
* I_D (continuous) is limited by max rated T_j. $T_A = 25°C$.
† Mounted on FR5 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.
‡ Total for package.

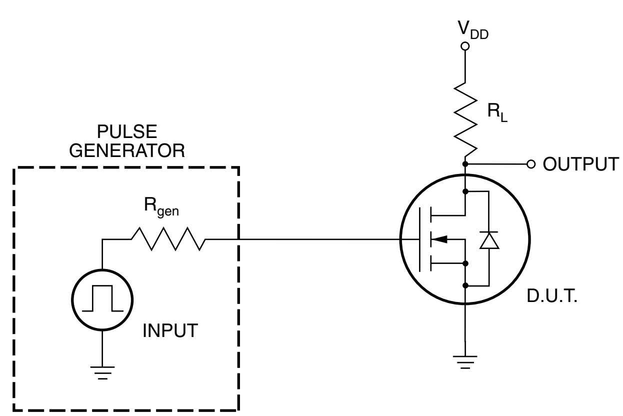
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	50			V	$V_{GS} = 0V$, $I_D = 10mA$
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 10mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.3	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 10mA$
I_{GSS}	Gate Body Leakage		1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			10	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
				1	mA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current	3.0	14		A	$V_{GS} = 10V$, $V_{DS} = 5V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance — TO-92 and P-DIP			0.45	Ω	$V_{GS} = 4.5V$, $I_D = 1.5A$
	SOT-89			0.45	Ω	$V_{GS} = 4.5V$, $I_D = 0.75A$
	TO-92 and P-DIP			0.3	Ω	$V_{GS} = 10V$, $I_D = 3A$
	SOT-89			0.3	Ω	$V_{GS} = 10V$, $I_D = 1.5A$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.85	1.2	%/°C	$V_{GS} = 10V$, $I_D = 3A$
G_{FS}	Forward Transconductance	1.0	1.5		℧	$V_{DS} = 25V$, $I_D = 2A$
C_{ISS}	Input Capacitance		220	300	pF	$V_{GS} = 0V$, $V_{DS} = 25V$ f = 1 MHz
C_{OSS}	Common Source Output Capacitance		70	120		
C_{RSS}	Reverse Transfer Capacitance		20	30		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V$ $I_D = 2A$ $R_{GEN} = 10\Omega$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			25		
t_f	Fall Time			25		
V_{SD}	Diode Forward Voltage Drop			1.6	V	$V_{GS} = 0V$, $I_{SD} = 1.5A$
t_{rr}	Reverse Recovery Time		300		ns	$V_{GS} = 0V$, $I_{SD} = 1A$

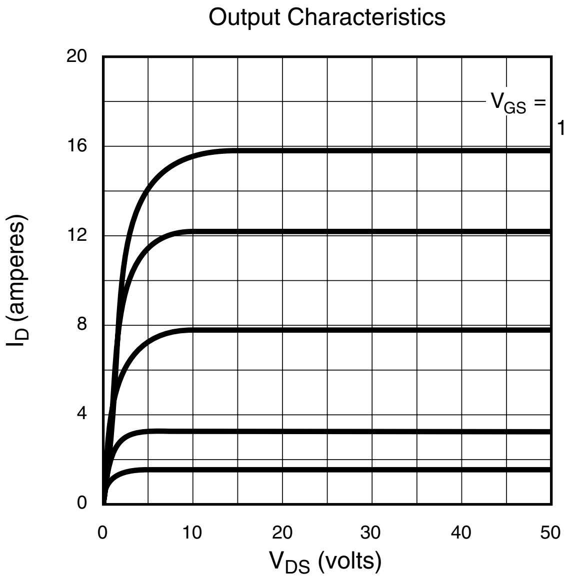
Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

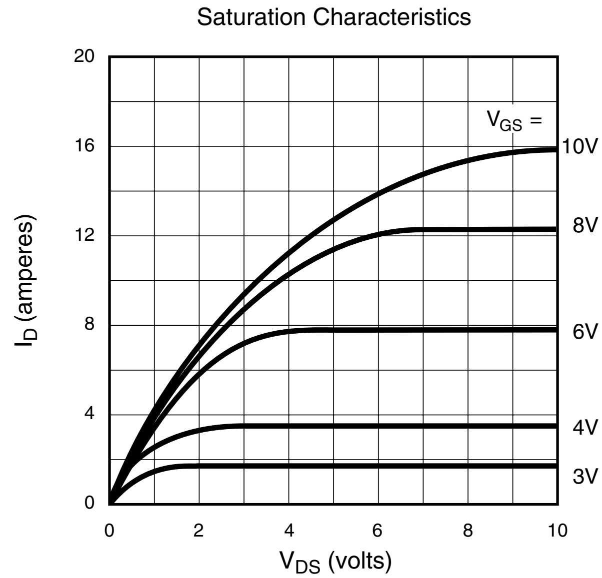
Switching Waveforms and Test Circuit

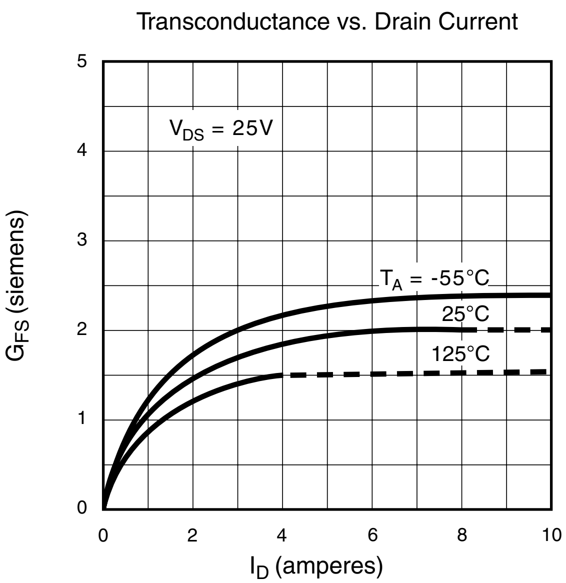


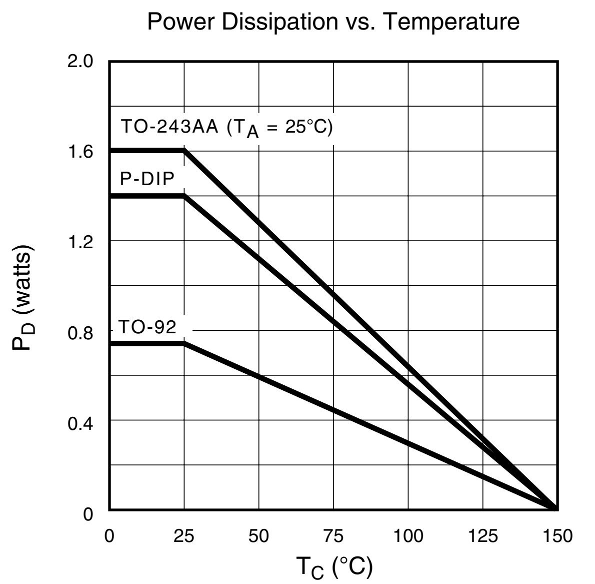


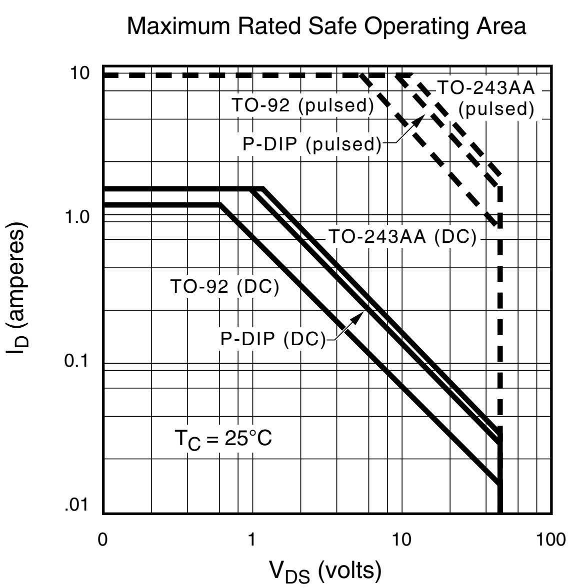
Typical Performance Curves

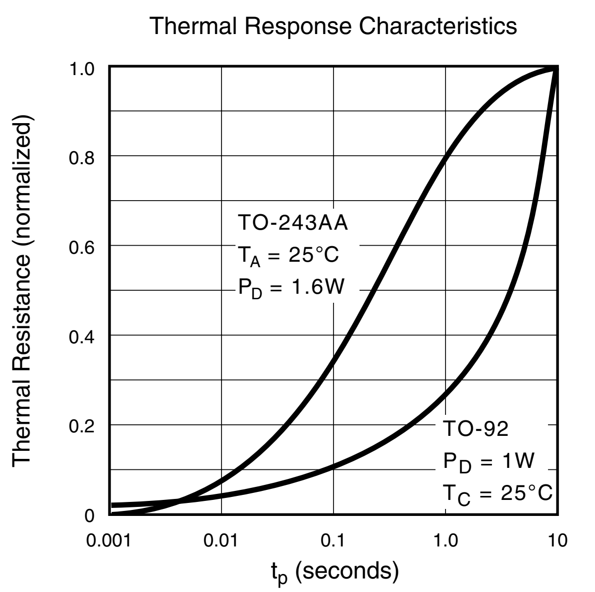






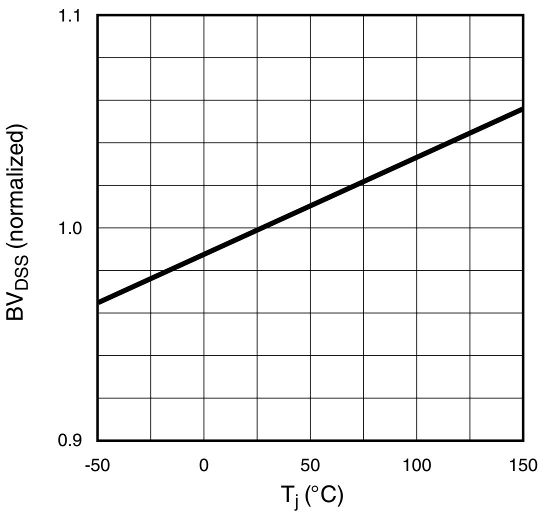




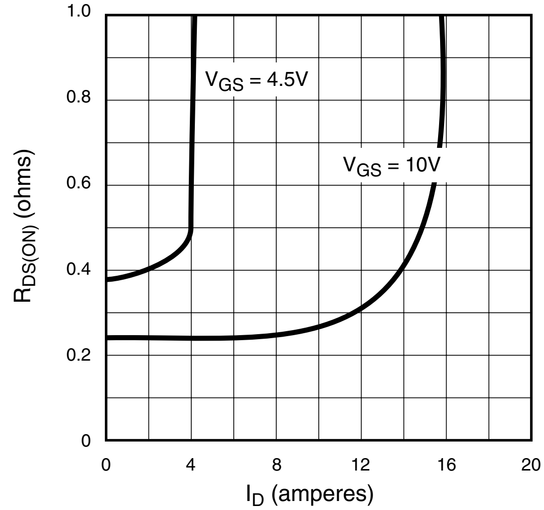


Typical Performance Curves

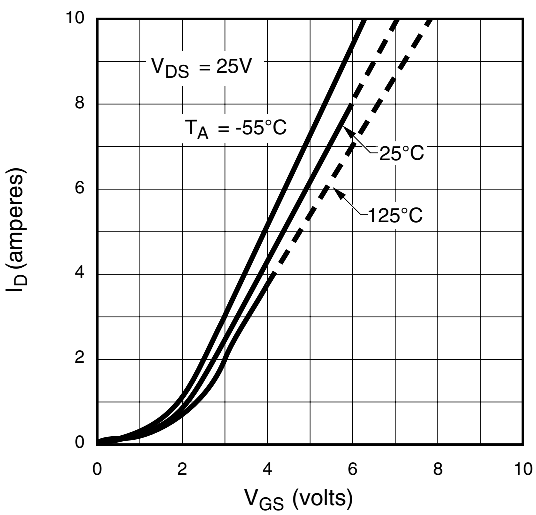
BV_{DSS} Variation with Temperature



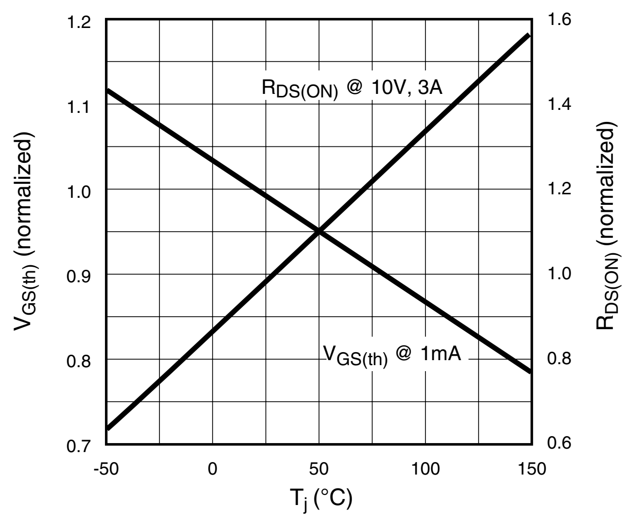
On-Resistance vs. Drain Current



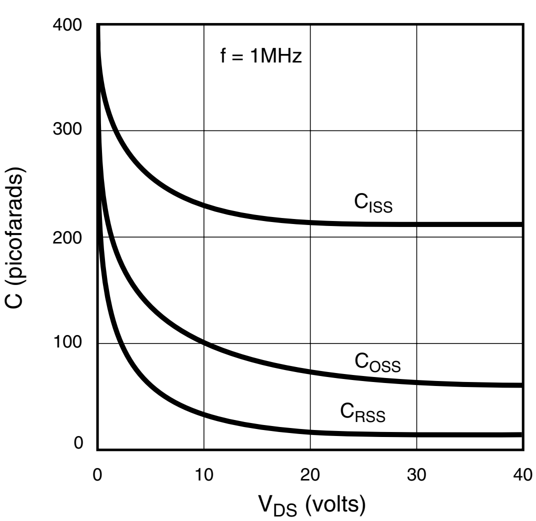
Transfer Characteristics



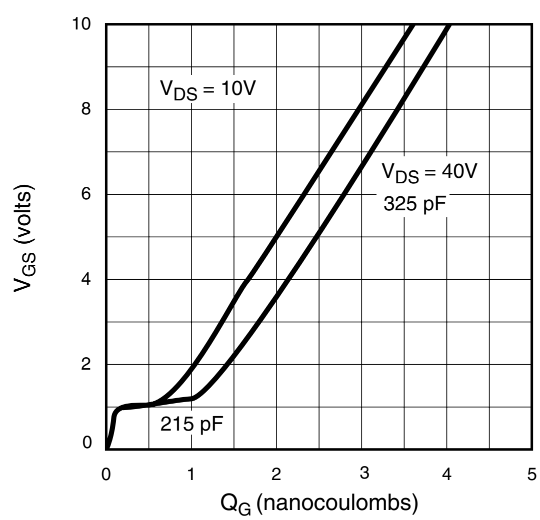
$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



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