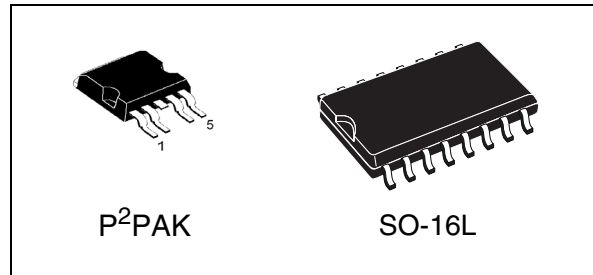


### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VN920D-B5 VN920DSO	18 m $\Omega$	30 A	36 V

- CMOS-compatible input
- On-state open load detection
- Off-state open load detection
- Shorted load protection
- Under-voltage and over-voltage shutdown
- Protection against loss of ground
- Very low standby current
- Reverse battery protected (see [Application schematic](#))



### Description

The VN920D-B5 and VN920DSO are monolithic devices designed in STMicroelectronics VIPower M0-3 technology. The VN920D-B5 and VN920DSO are intended for driving any type of load with one side connected to ground. The active  $V_{CC}$  pin voltage clamp protects the devices against low energy spikes (see ISO7637 transient compatibility table).

Active current limitation combined with thermal shutdown and automatic restart protects the devices against overload. The devices detect the open load condition in both the on and off-state. In the off-state the devices detect if the output is shorted to  $V_{CC}$ . The devices automatically turn-off in the case where the ground pin becomes disconnected.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
P <sup>2</sup> PAK	VN920D-B5	VN920D-B513TR
SO-16L	VN920DSO	VN920DSO13TR

# Contents

<b>1</b>	<b>Block diagram and pin description</b> .....	<b>5</b>
<b>2</b>	<b>Electrical specifications</b> .....	<b>6</b>
2.1	Absolute maximum ratings .....	6
2.2	Thermal data .....	7
2.3	Electrical characteristics .....	8
2.4	Electrical characteristics curves .....	13
<b>3</b>	<b>Application information</b> .....	<b>16</b>
3.1	GND protection network against reverse battery .....	16
3.1.1	Solution 1: resistor in the ground line (RGND only) .....	16
3.1.2	Solution 2: diode (DGND) in the ground line .....	17
3.2	Load dump protection .....	17
3.3	MCU I/Os protection .....	17
3.4	P <sup>2</sup> PAK maximum demagnetization energy (VCC = 13.5V) .....	18
3.5	SO-16L maximum demagnetization energy (VCC = 13.5V) .....	19
<b>4</b>	<b>Package and PCB thermal data</b> .....	<b>20</b>
4.1	SO-16L thermal data .....	20
4.2	P <sup>2</sup> PAK thermal data .....	22
<b>5</b>	<b>Package and packing information</b> .....	<b>25</b>
5.1	ECOPACK <sup>®</sup> packages .....	25
5.2	P <sup>2</sup> PAK mechanical data .....	27
5.3	SO-16L packing information .....	29
5.4	P <sup>2</sup> PAK packing information .....	30
<b>6</b>	<b>Revision history</b> .....	<b>31</b>

## List of tables

Table 1.	Device summary . . . . .	1
Table 2.	Suggested connections for unused and not connected pins . . . . .	5
Table 3.	Absolute maximum ratings . . . . .	6
Table 4.	Thermal data . . . . .	7
Table 5.	Power . . . . .	8
Table 6.	Switching ( $V_{CC}=13V$ ) . . . . .	8
Table 7.	Input pin . . . . .	9
Table 8.	$V_{CC}$ output diode. . . . .	9
Table 9.	Status pin . . . . .	9
Table 10.	Protections . . . . .	9
Table 11.	Open load detection . . . . .	10
Table 12.	Truth table. . . . .	11
Table 13.	Electrical transient requirements . . . . .	11
Table 14.	SO-16L thermal parameters . . . . .	22
Table 15.	P <sup>2</sup> PAK thermal parameters . . . . .	24
Table 16.	SO-16L mechanical data . . . . .	25
Table 17.	P <sup>2</sup> PAK mechanical data . . . . .	28
Table 18.	Document revision history . . . . .	31

## List of figures

Figure 1.	Block diagram . . . . .	5
Figure 2.	Configuration diagram (top view) . . . . .	5
Figure 3.	Current and voltage conventions . . . . .	6
Figure 4.	Status timings . . . . .	10
Figure 5.	Switching time waveforms . . . . .	10
Figure 6.	Waveforms . . . . .	12
Figure 7.	Off-state output current. . . . .	13
Figure 8.	High-level input current. . . . .	13
Figure 9.	Input clamp voltage. . . . .	13
Figure 10.	Status leakage current . . . . .	13
Figure 11.	Status low output voltage . . . . .	13
Figure 12.	Status clamp voltage . . . . .	13
Figure 13.	On-state resistance Vs $T_{case}$ . . . . .	14
Figure 14.	On-state resistance Vs $V_{CC}$ . . . . .	14
Figure 15.	Over-voltage shutdown. . . . .	14
Figure 16.	Input high-level . . . . .	14
Figure 17.	Input low-level. . . . .	14
Figure 18.	Input hysteresis voltage . . . . .	14
Figure 19.	$I_{lim}$ Vs $T_{case}$ . . . . .	15
Figure 20.	Turn-on voltage slope . . . . .	15
Figure 21.	Turn-off voltage slope . . . . .	15
Figure 22.	Application schematic. . . . .	16
Figure 23.	P <sup>2</sup> PAK maximum turn-off current versus inductance . . . . .	18
Figure 24.	SO-16L maximum turn-off current versus inductance . . . . .	19
Figure 25.	SO-16L PC board . . . . .	20
Figure 26.	SO-16L $R_{thj-amb}$ Vs PCB copper area in open box free air condition . . . . .	20
Figure 27.	SO-16L thermal impedance junction ambient single pulse . . . . .	21
Figure 28.	Thermal fitting model of a single channel HSD in SO-16L . . . . .	21
Figure 29.	P <sup>2</sup> PAK PC board . . . . .	22
Figure 30.	P <sup>2</sup> PAK $R_{thj-amb}$ Vs. PCB copper area in open box free air condition . . . . .	23
Figure 31.	P <sup>2</sup> PAK thermal impedance junction ambient single pulse . . . . .	23
Figure 32.	Thermal fitting model of a single channel HSD in P <sup>2</sup> PAK. . . . .	24
Figure 33.	SO-16L package dimensions . . . . .	25
Figure 34.	P <sup>2</sup> PAK package dimensions. . . . .	27
Figure 35.	SO-16L tube shipment (no suffix) . . . . .	29
Figure 36.	SO-16L tape and reel shipment (suffix "TR") . . . . .	29
Figure 37.	P <sup>2</sup> PAK tube shipment (no suffix) . . . . .	30
Figure 38.	P <sup>2</sup> PAK tape and reel (suffix "13TR"). . . . .	30

# 1 Block diagram and pin description

Figure 1. Block diagram

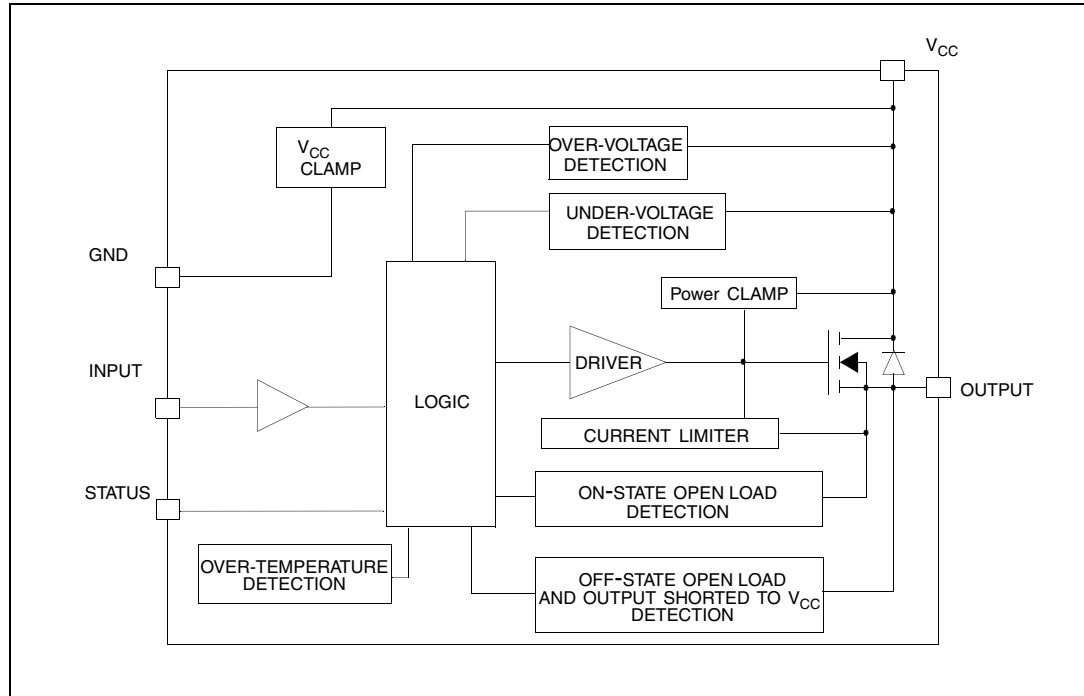


Figure 2. Configuration diagram (top view)

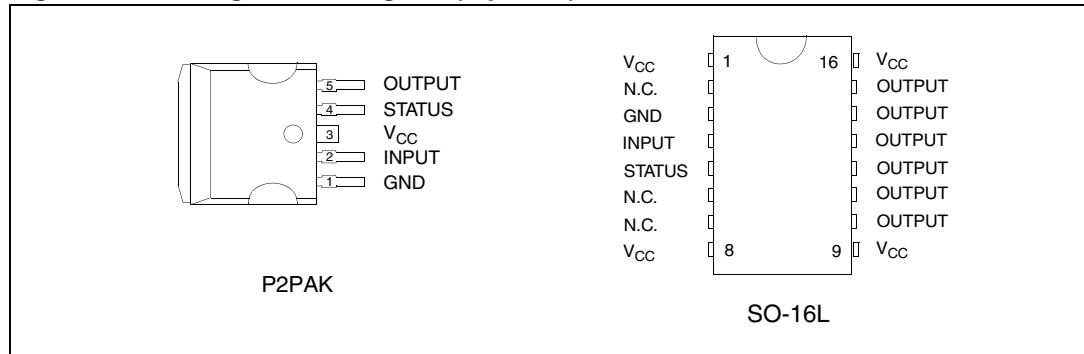
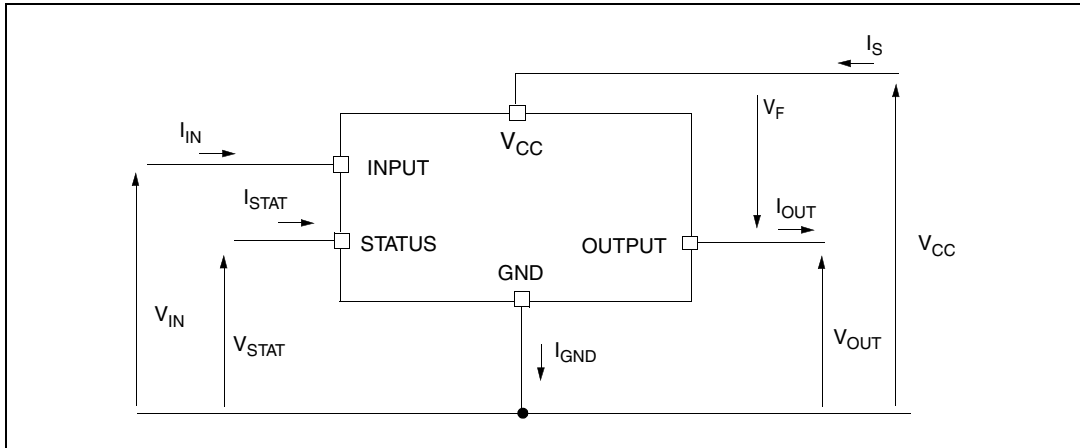


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics sure program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SO-16L	P <sup>2</sup> PAK	
V <sub>CC</sub>	DC supply voltage	41		V
- V <sub>CC</sub>	Reverse DC supply voltage	- 0.3		V
- I <sub>gnd</sub>	DC reverse ground pin current	- 200		mA
I <sub>OUT</sub>	DC output current	Internally limited		A
- I <sub>OUT</sub>	Reverse DC output current	- 25		A
I <sub>IN</sub>	DC input current	+/- 10		mA
I <sub>STAT</sub>	DC Status current	+/- 10		mA
V <sub>ESD</sub>	Electrostatic discharge (human body model: R = 1.5KΩ, C = 100pF)			
	- INPUT	4000		V
	- STATUS	4000		V
	- OUTPUT	5000		V
	- V <sub>CC</sub>	5000		V

**Table 3. Absolute maximum ratings (continued)**

Symbol	Parameter	Value		Unit
		SO-16L	P <sup>2</sup> PAK	
E <sub>MAX</sub>	Maximum switching energy (L = 0.25mH; R <sub>L</sub> = 0Ω; V <sub>bat</sub> = 13.5V; T <sub>Jstart</sub> = 150°C; I <sub>L</sub> = 45A)	352	364	mJ
P <sub>tot</sub>	Power dissipation T <sub>C</sub> = 25°C	8.3	96.1	W
T <sub>j</sub>	Junction operating temperature	Internally limited		°C
T <sub>C</sub>	Case operating temperature	- 40 to 150		°C
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C

## 2.2 Thermal data

**Table 4. Thermal data**

Symbol	Parameter	Max. value		Unit
		SO-16L	P <sup>2</sup> PAK	
R <sub>thj-case</sub>	Thermalresistance junction-case	-	1.3	°C/W
R <sub>thj-lead</sub>	Thermalresistance junction-lead	15	-	°C/W
R <sub>thj-amb</sub>	Thermalresistance junction-ambient	65 <sup>(1)</sup>	51.3 <sup>(2)</sup>	°C/W

1. When mounted on FR4 printed circuit board with 0.5cm<sup>2</sup> of Cu (at least 35μm thick) connected to all V<sub>CC</sub> pins.
2. When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35μm thick).

## 2.3 Electrical characteristics

Values specified in this section are for  $8V < V_{CC} < 36V$ ;  $-40^{\circ}C < T_j < 150^{\circ}C$ , unless otherwise stated.

**Table 5. Power**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Under-voltage shutdown		3	4	5.5	V
$V_{USDhyst}$	Under-voltage shutdown hysteresis			0.5		V
$V_{OV}$	Over-voltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 10A$ ; $T_j = 25^{\circ}C$ ;			18	m $\Omega$
		$I_{OUT} = 10A$ ;			36	m $\Omega$
		$I_{OUT} = 3A$ ; $V_{CC} = 6V$			50	m $\Omega$
$I_S$	Supply current	Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$		10	25	$\mu A$
		Off-state; $V_{CC} = 13V$ ; $V_{IN} = V_{OUT} = 0V$ ; $T_j = 25^{\circ}C$		10	20	$\mu A$
		On-state; $V_{CC} = 13V$ ; $V_{IN} = 5V$ ; $I_{OUT} = 0A$			3.5	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$	0		50	$\mu A$
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V$ ; $V_{OUT} = 3.5V$	-75		0	$\mu A$
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 125^{\circ}C$			5	$\mu A$
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0V$ ; $V_{CC} = 13V$ ; $T_j = 25^{\circ}C$			3	$\mu A$

**Table 6. Switching ( $V_{CC}=13V$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 1.3\Omega$		50		$\mu s$
$t_{d(off)}$	Turn-off delay time	$R_L = 1.3\Omega$		50		$\mu s$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 1.3\Omega$		See <a href="#">Figure 20.</a>		V/ $\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 1.3\Omega$		See <a href="#">Figure 21.</a>		V/ $\mu s$



**Table 7. Input pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low-level				1.25	V
$I_{IL}$	Low-level input current	$V_{IN} = 1.25V$	1			$\mu A$
$V_{IH}$	Input high-level		3.25			V
$I_{IH}$	High-level input current	$V_{IN} = 3.25V$			10	$\mu A$
$V_{hyst}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$ $I_{IN} = -1mA$	6	6.8 - 0.7	8	V V

**Table 8.  $V_{CC}$  output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT} = 5.5A; T_j = 150^\circ C$			0.7	V

**Table 9. Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6mA$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5V$			10	$\mu A$
$C_{STAT}$	Status pin input capacitance	Normal operation; $V_{STAT} = 5V$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1mA$ $I_{STAT} = -1mA$	6	6.8 - 0.7	8	V V

**Table 10. Protections<sup>(1)</sup>**

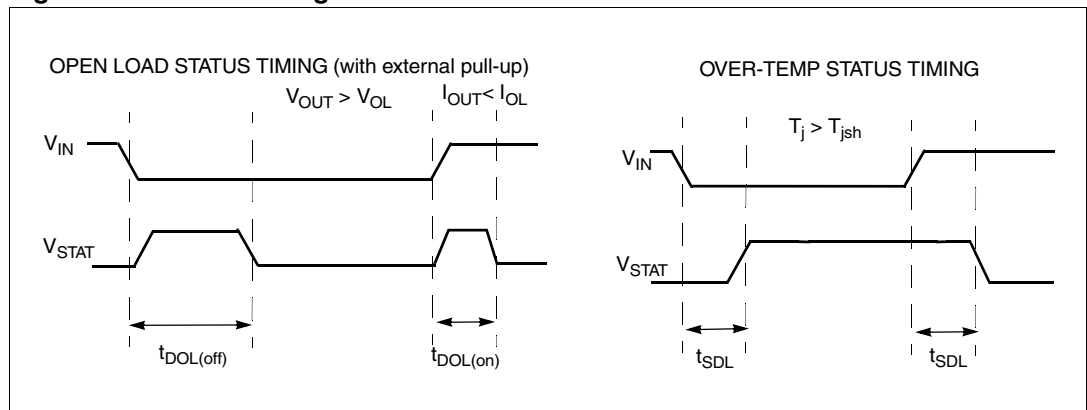
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	$^\circ C$
$T_R$	Reset temperature		135			$^\circ C$
$T_{hyst}$	Thermal hysteresis		7	15		$^\circ C$
$t_{SDL}$	Status delay in overload condition	$T_j > T_{jsh}$			20	ms
$I_{lim}$	Current limitation	$5.5V < V_{CC} < 36V$	30	45	75 75	A A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2 A;$ $V_{IN} = 0V;$ $L = 6mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

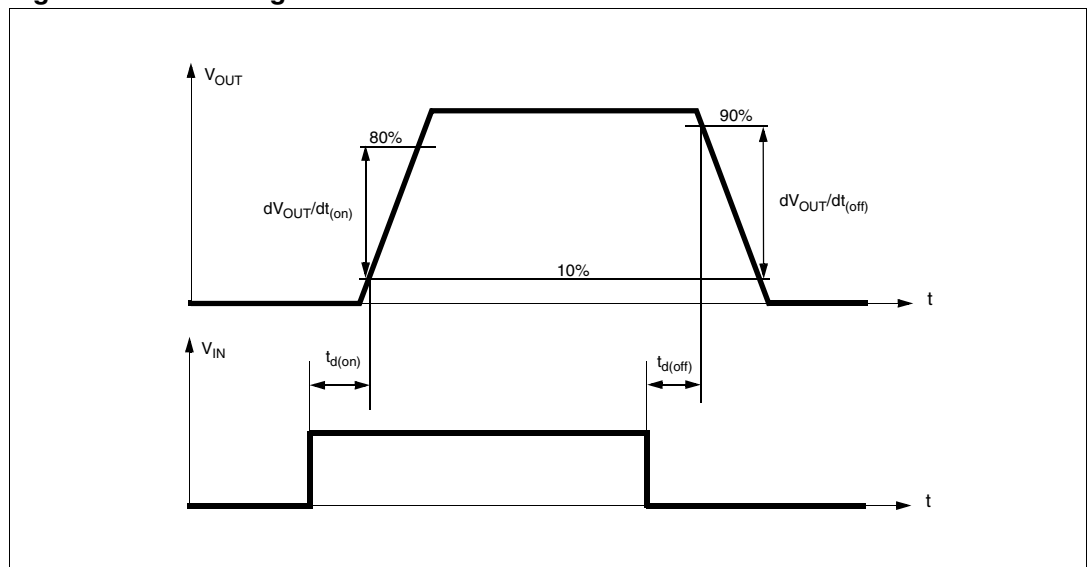
**Table 11. Open load detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Open load on-state detection threshold	$V_{IN} = 5V$	300	500	700	mA
$t_{DOL(on)}$	Open load on-state detection delay	$I_{OUT} = 0A$			250	$\mu s$
$V_{OL}$	Open load off-state voltage detection threshold	$V_{IN} = 0V$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open load detection delay at turn-off				1000	$\mu s$

**Figure 4. Status timings**



**Figure 5. Switching time waveforms**



**Table 12. Truth table**

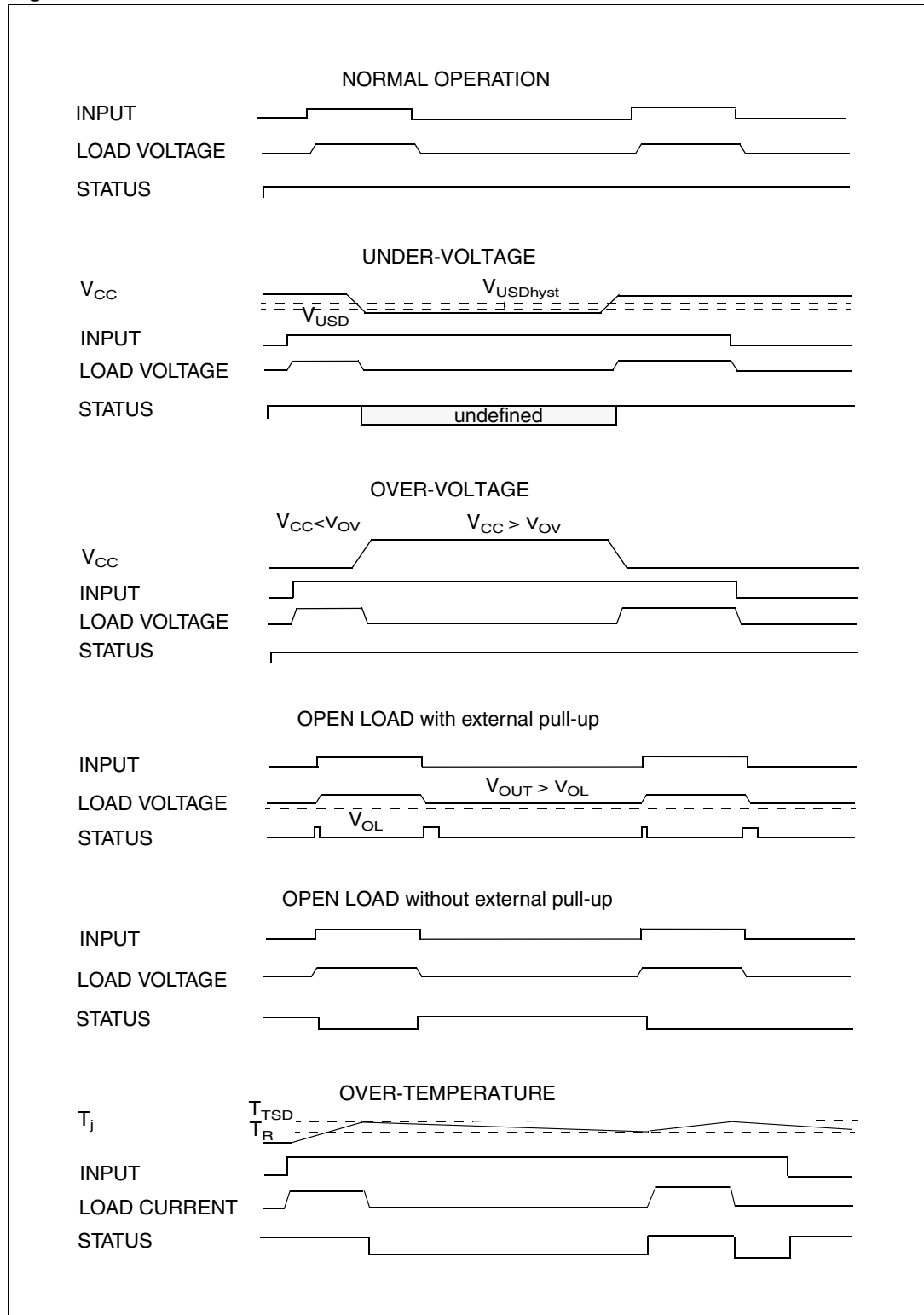
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H
	H	X	( $T_j > T_{TSD}$ ) L
Over-temperature	L	L	H
	H	L	L
Under-voltage	L	L	X
	H	L	X
Over-voltage	L	L	H
	H	L	H
Output voltage > $V_{OL}$	L	H	L
	H	H	H
Output current < $I_{OL}$	L	L	H
	H	H	L

**Table 13. Electrical transient requirements**

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25V <sup>(1)</sup>	- 50V <sup>(1)</sup>	- 75V <sup>(1)</sup>	- 100V <sup>(1)</sup>	2ms, 10Ω
2	+ 25V <sup>(1)</sup>	+ 50V <sup>(1)</sup>	+ 75V <sup>(1)</sup>	+ 100V <sup>(1)</sup>	0.2ms, 10Ω
3a	- 25V <sup>(1)</sup>	- 50V <sup>(1)</sup>	- 100V <sup>(1)</sup>	- 150V <sup>(1)</sup>	0.1μs, 50Ω
3b	+ 25V <sup>(1)</sup>	+ 50V <sup>(1)</sup>	+ 75V <sup>(1)</sup>	+ 100V <sup>(1)</sup>	0.1μs, 50Ω
4	- 4V <sup>(1)</sup>	- 5V <sup>(1)</sup>	- 6V <sup>(1)</sup>	- 7V <sup>(1)</sup>	100ms, 0.01Ω
5	+ 26.5V <sup>(1)</sup>	+ 46.5V <sup>(2)</sup>	+ 66.5V <sup>(2)</sup>	+ 86.5V <sup>(2)</sup>	400ms, 2Ω

1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms



## 2.4 Electrical characteristics curves

Figure 7. Off-state output current

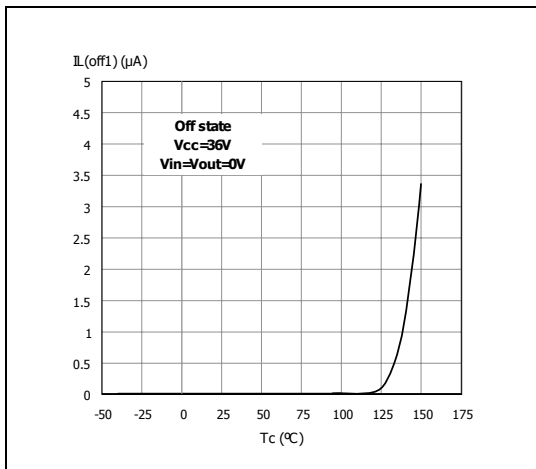


Figure 8. High-level input current

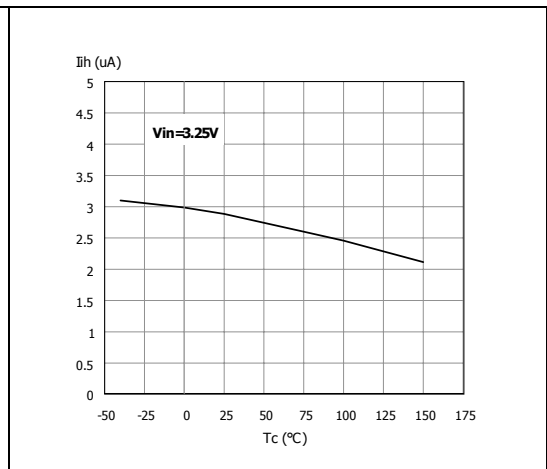


Figure 9. Input clamp voltage

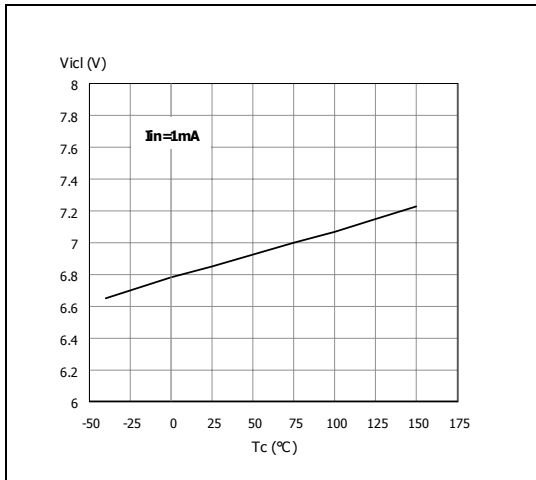


Figure 10. Status leakage current

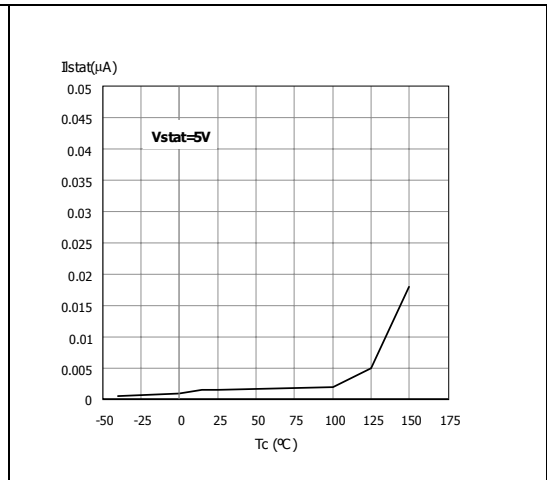


Figure 11. Status low output voltage

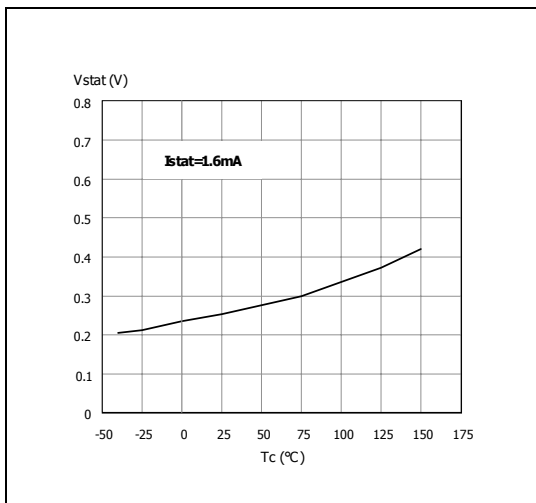


Figure 12. Status clamp voltage

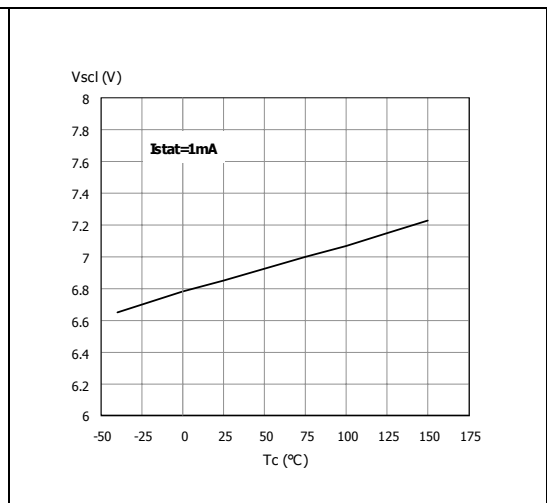


Figure 13. On-state resistance Vs  $T_{case}$

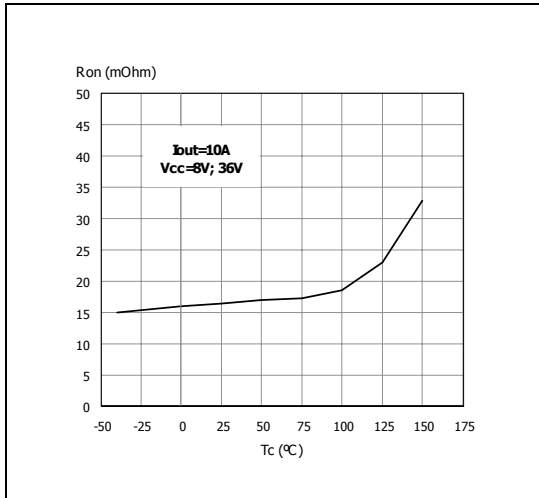


Figure 14. On-state resistance Vs  $V_{CC}$

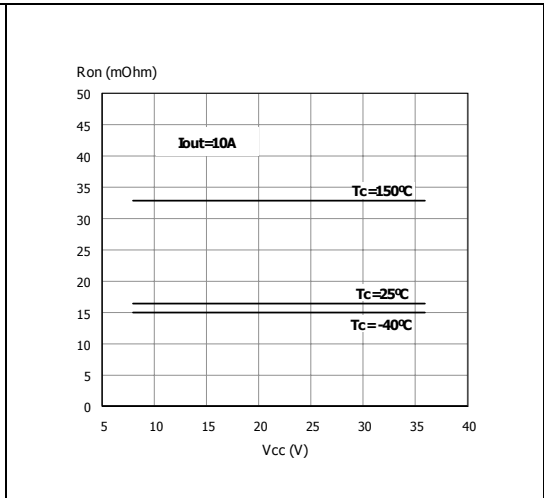


Figure 15. Over-voltage shutdown

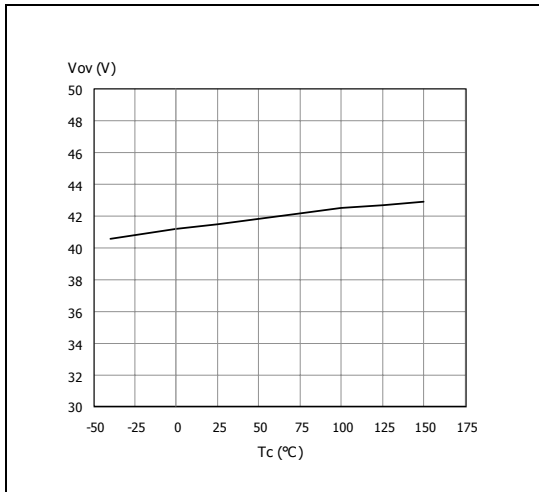


Figure 16. Input high-level

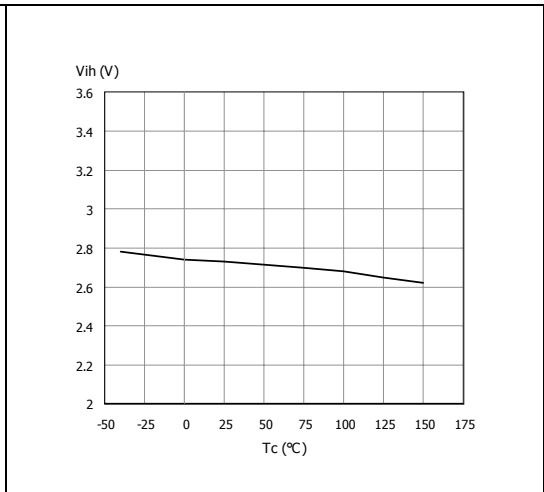


Figure 17. Input low-level

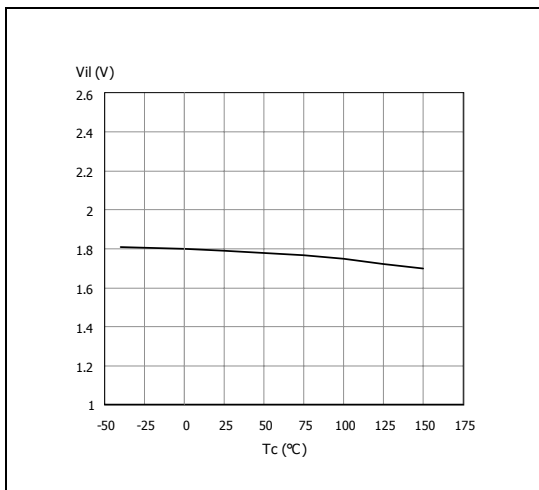


Figure 18. Input hysteresis voltage

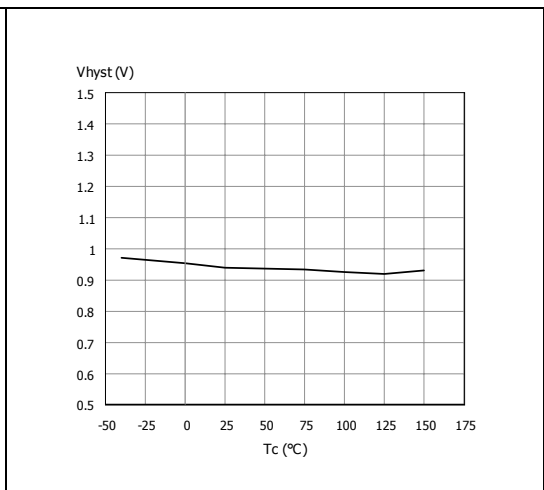


Figure 19.  $I_{lim}$  Vs  $T_{case}$

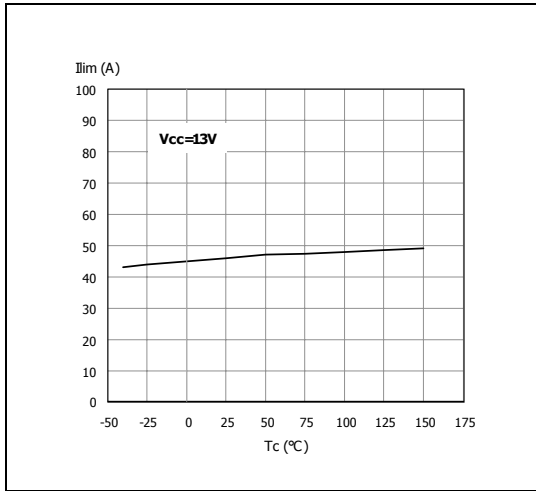


Figure 20. Turn-on voltage slope

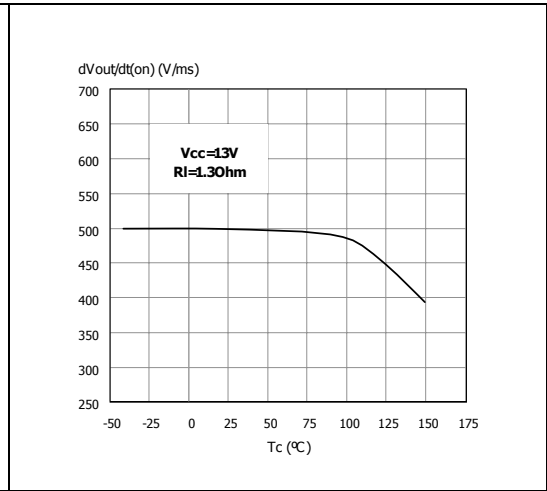
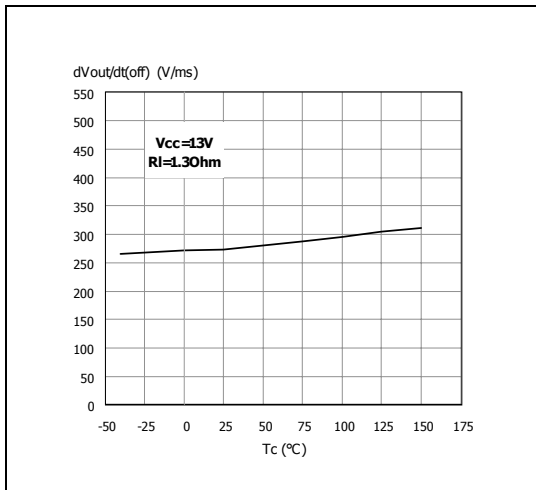
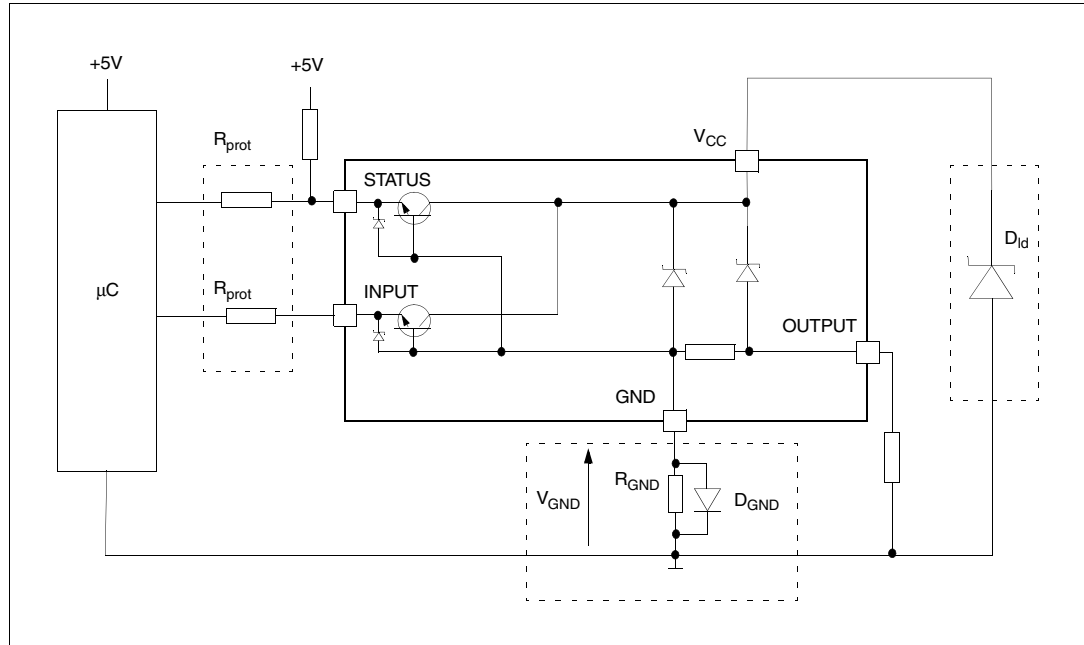


Figure 21. Turn-off voltage slope



### 3 Application information

Figure 22. Application schematic



#### 3.1 GND protection network against reverse battery

##### 3.1.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to dimension the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600\text{mV} / (I_{S(ON)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(ON)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> will produce a shift ( $I_{S(ON)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high-side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).



### 3.1.2 Solution 2: diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1k\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ( $\approx 600mV$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

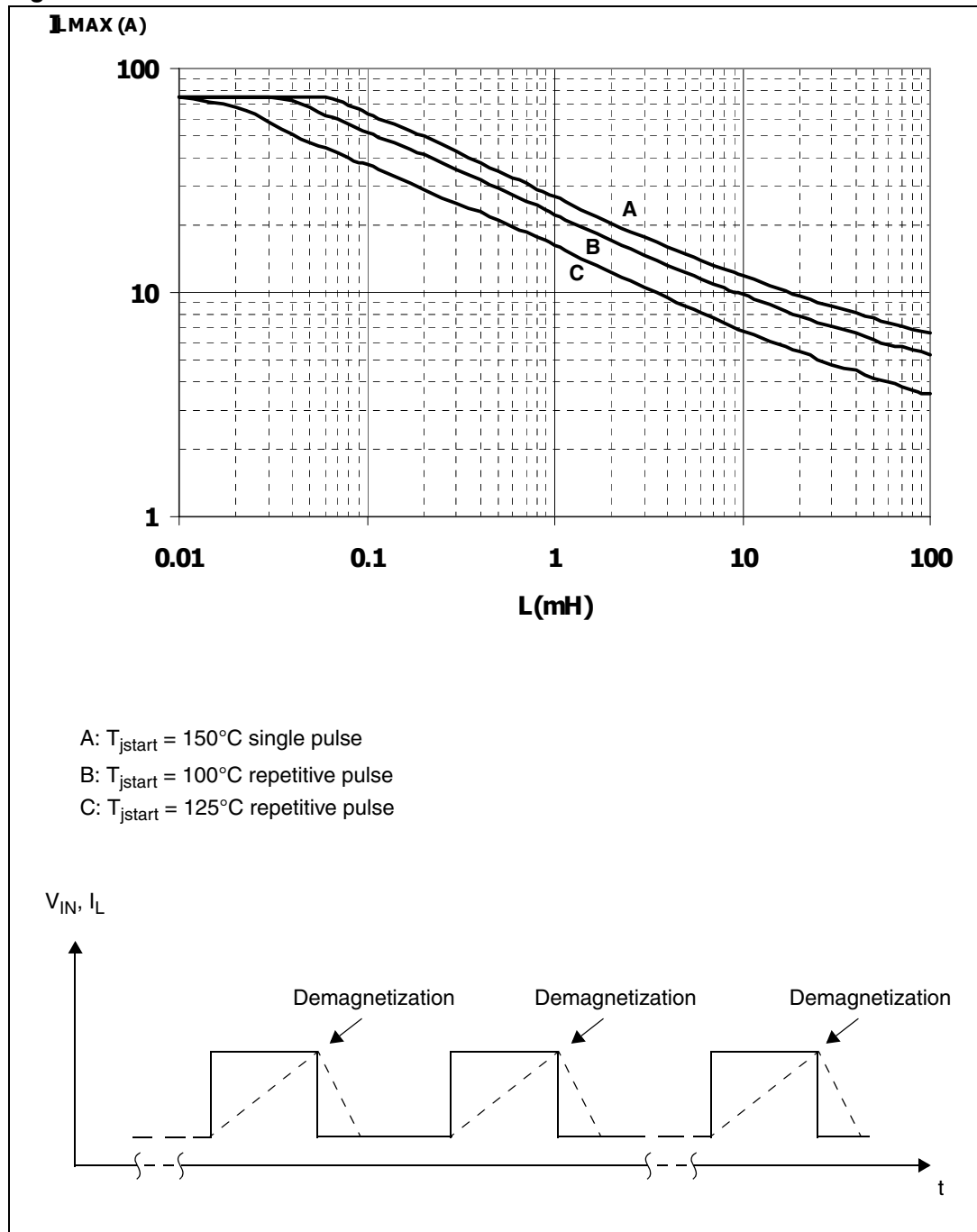
For  $V_{CCpeak} = -100V$  and  $I_{latchup} \geq 20mA$ ;  $V_{OH\mu C} \geq 4.5V$

$$5k\Omega \leq R_{prot} \leq 65k\Omega$$

Recommended values:  $R_{prot} = 10k\Omega$ .

### 3.4 P<sup>2</sup>PAK maximum demagnetization energy ( $V_{CC} = 13.5V$ )

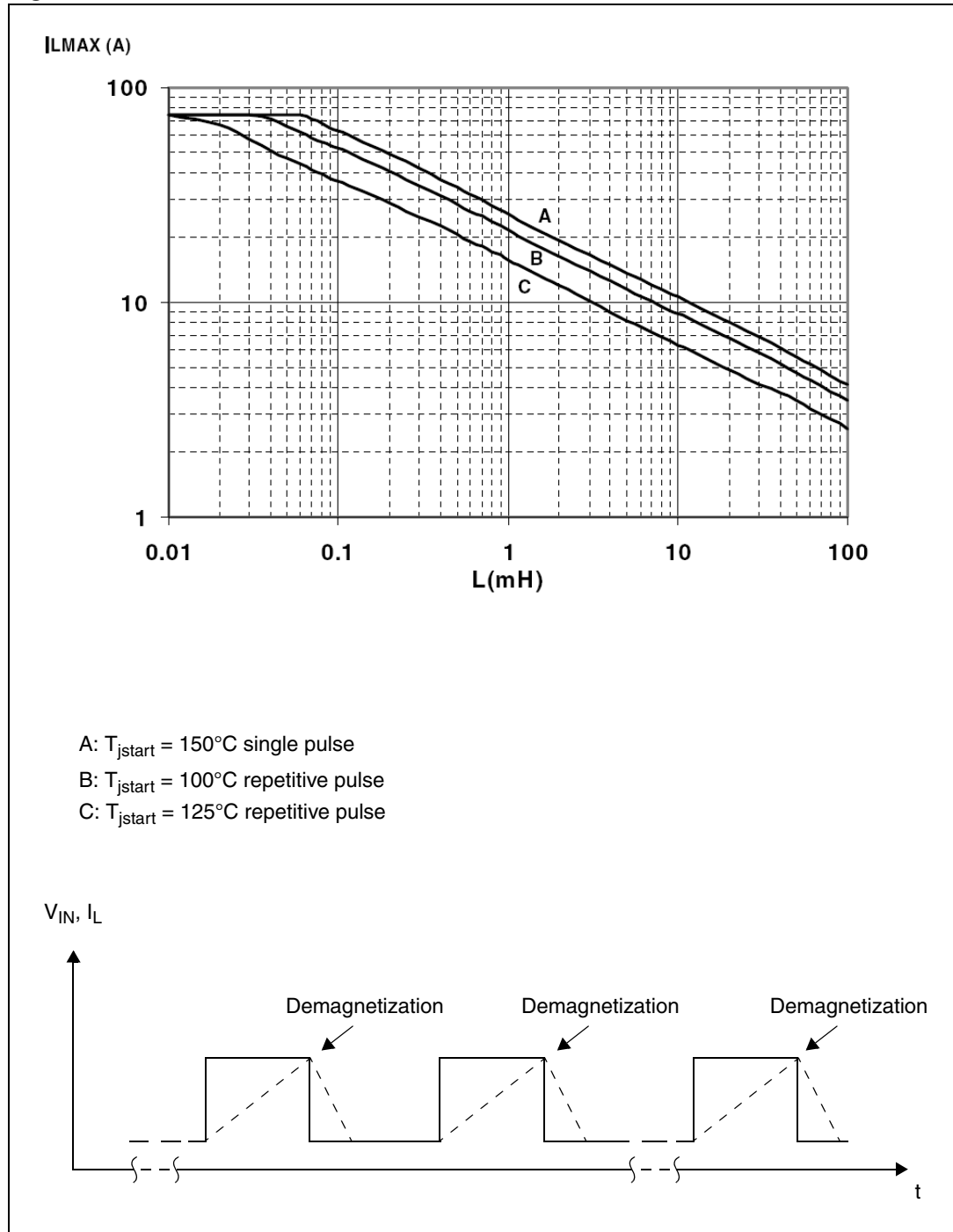
Figure 23. P<sup>2</sup>PAK maximum turn-off current versus inductance



Note: Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

### 3.5 SO-16L maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 24. SO-16L maximum turn-off current versus inductance

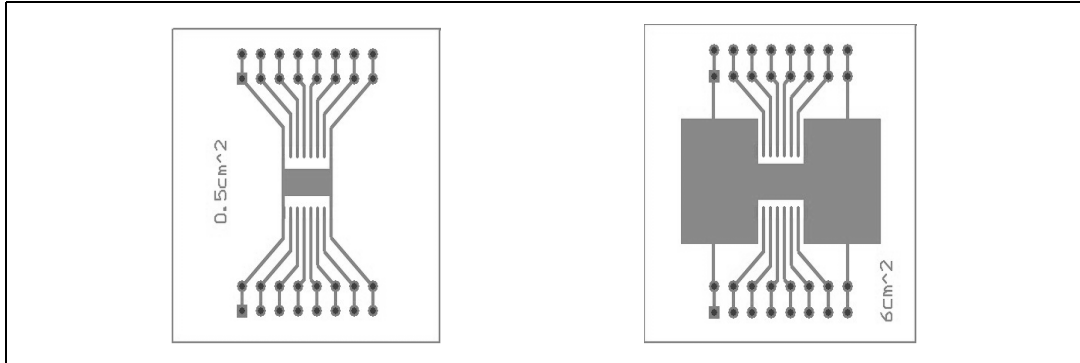


Note: Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

### 4.1 SO-16L thermal data

Figure 25. SO-16L PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 41mm x 48mm, PCB thickness = 2mm, Cu thickness = 35 $\mu$ m, Copper areas: 0.5cm<sup>2</sup>, 6cm<sup>2</sup>).

Figure 26. SO-16L  $R_{thj-amb}$  Vs PCB copper area in open box free air condition

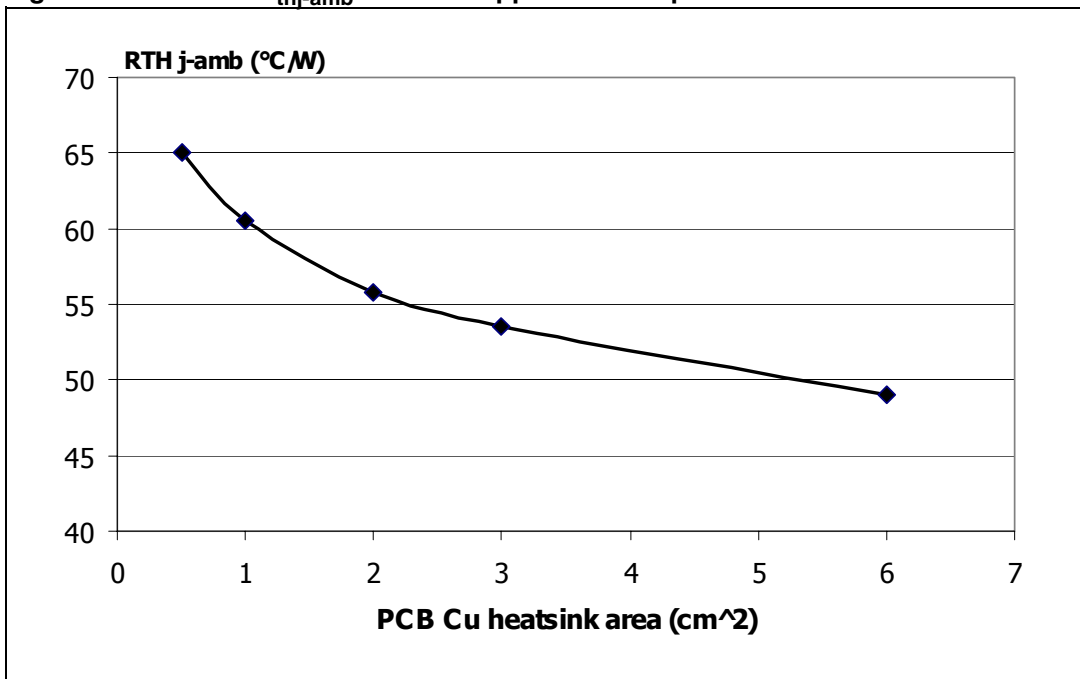
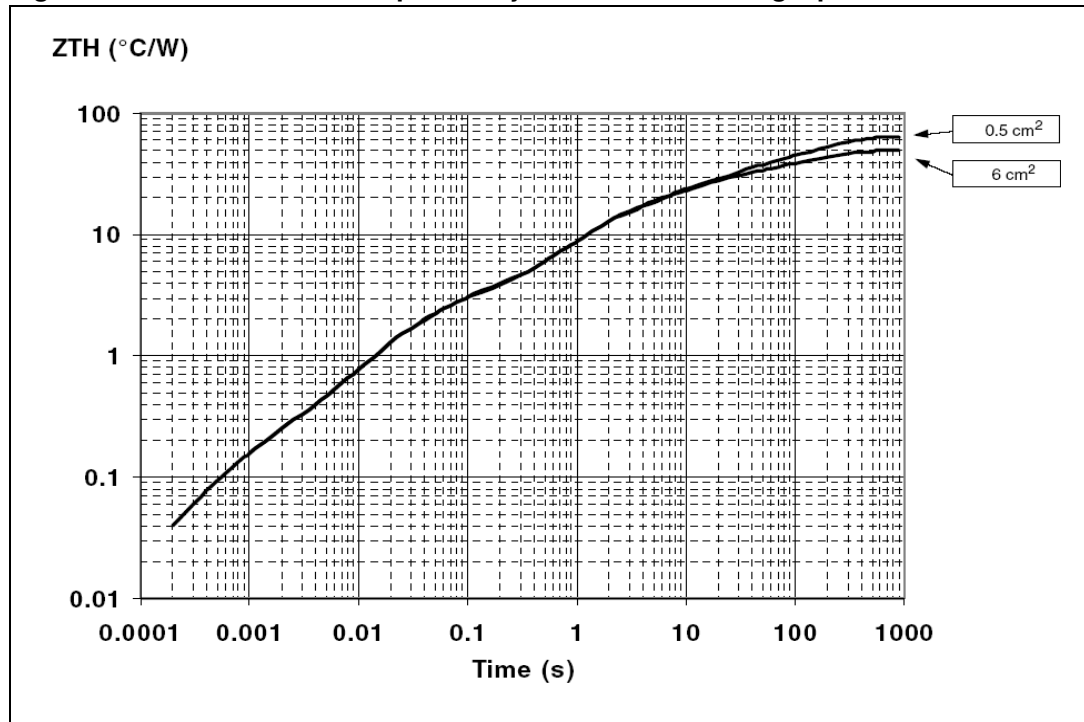


Figure 27. SO-16L thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p / T$

Figure 28. Thermal fitting model of a single channel HSD in SO-16L

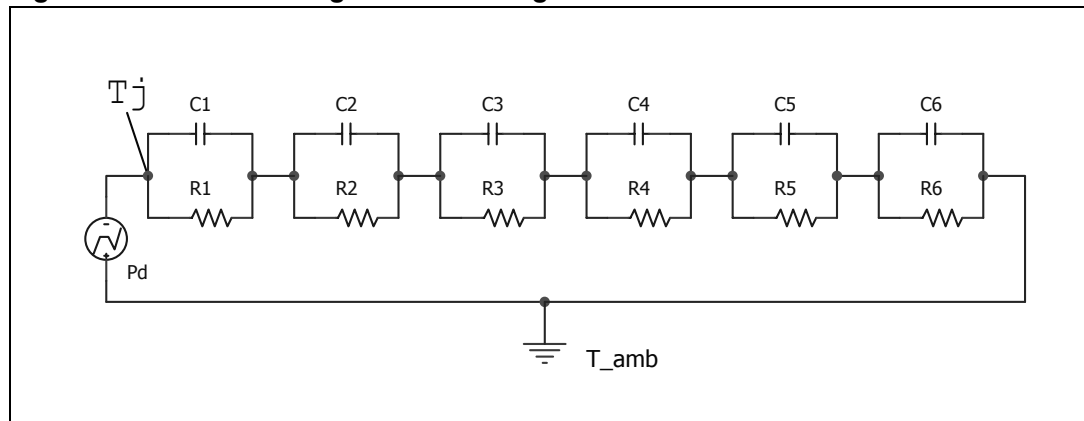
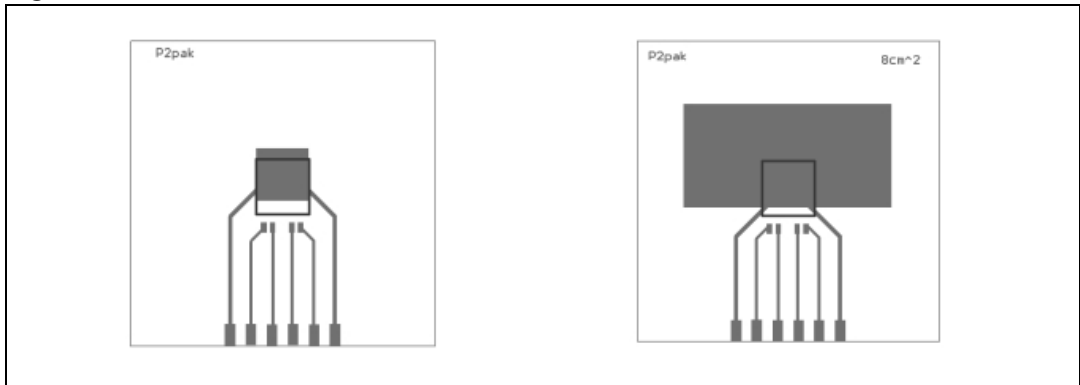


Table 14. SO-16L thermal parameters

Area / island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	2.2	
R4 (°C/W)	12	
R5 (°C/W)	15	
R6 (°C/W)	35	20
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7E-03	
C3 (W.s/°C)	1.5E-02	
C4 (W.s/°C)	0.14	
C5 (W.s/°C)	1	
C6 (W.s/°C)	5	8

## 4.2 P<sup>2</sup>PAK thermal data

Figure 29. P<sup>2</sup>PAK PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area = 60mm x 60mm, PCB thickness = 2 mm, Cu thickness = 35µm, Copper areas: 0.97cm<sup>2</sup>, 8cm<sup>2</sup>).

Figure 30. P<sup>2</sup>PAK R<sub>thj-amb</sub> Vs. PCB copper area in open box free air condition

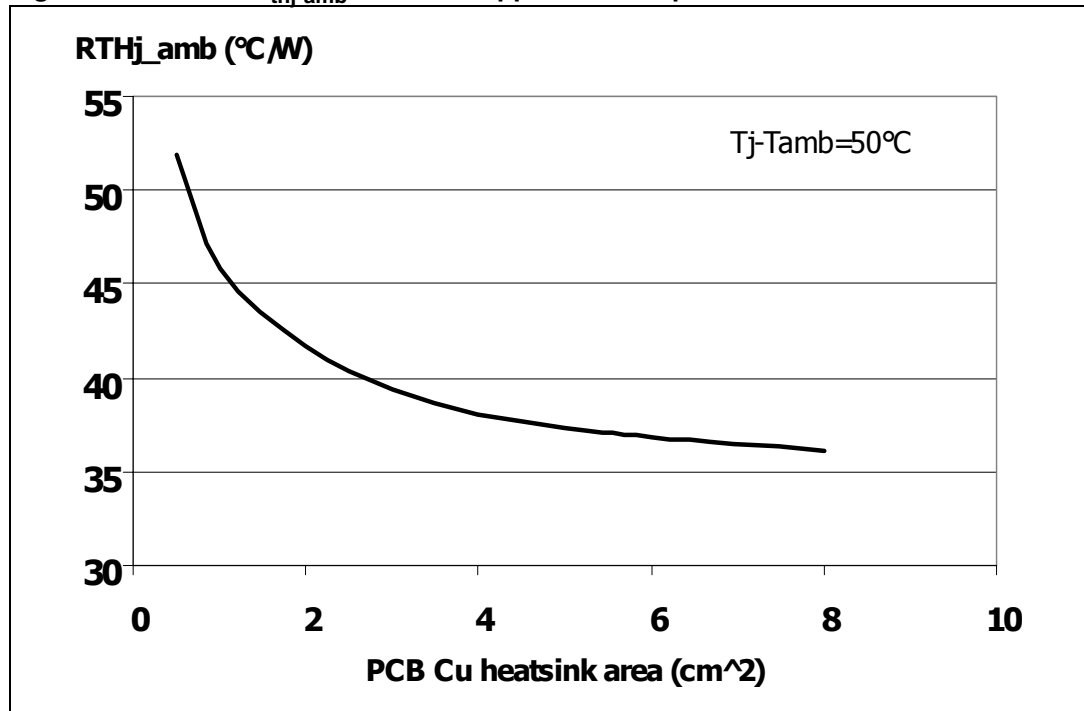
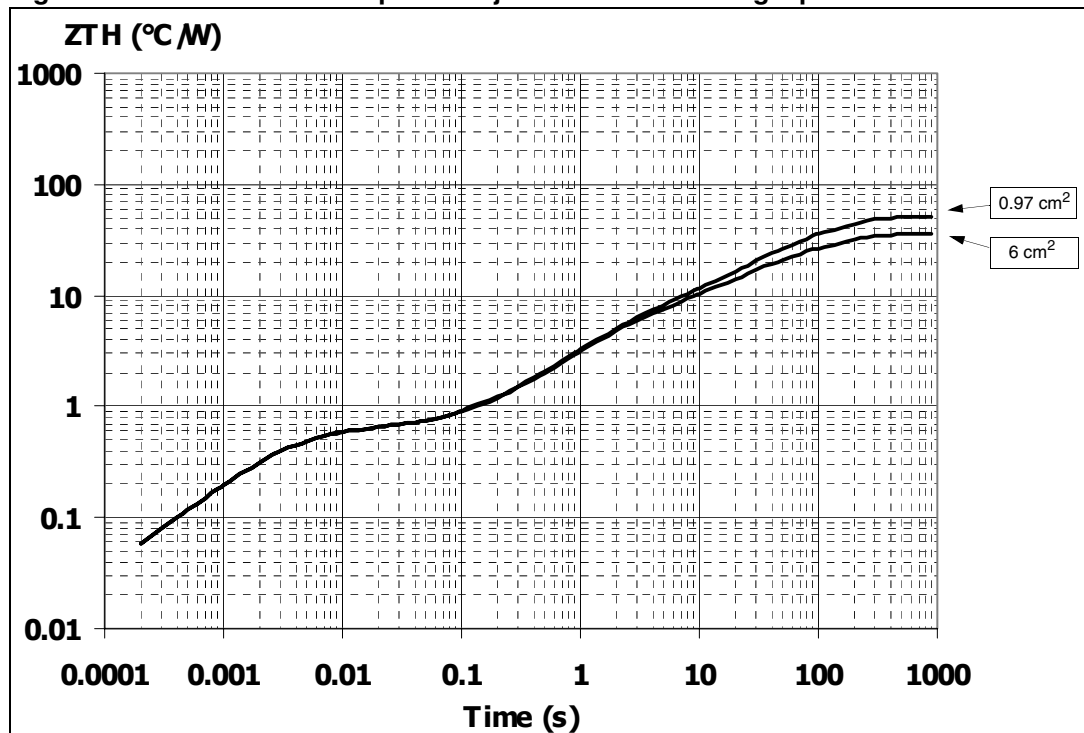


Figure 31. P<sup>2</sup>PAK thermal impedance junction ambient single pulse

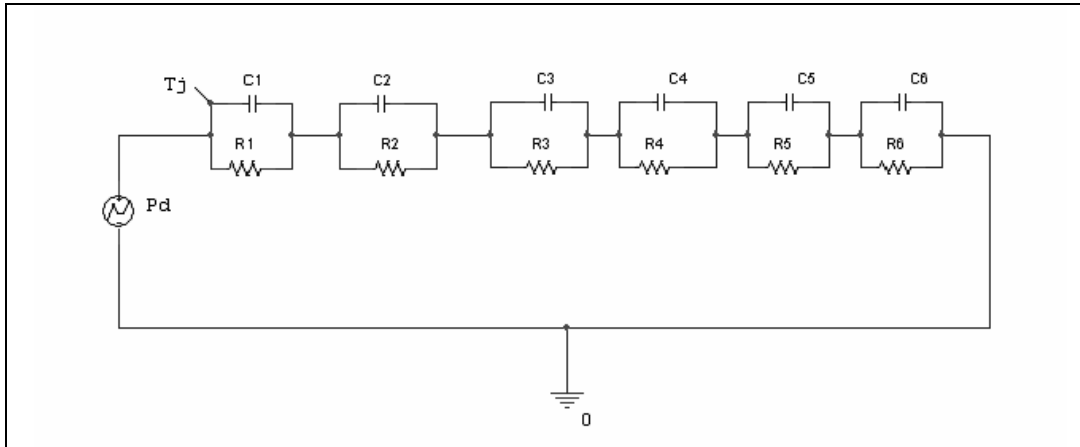


**Equation 2: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

**Figure 32. Thermal fitting model of a single channel HSD in P<sup>2</sup>PAK**



**Table 15. P<sup>2</sup>PAK thermal parameters**

Area/island (cm <sup>2</sup> )	0.97	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.22	
R4 (°C/W)	4	
R5 (°C/W)	9	
R6 (°C/W)	37	22
C1 (W·s/°C)	0.0015	
C2 (W·s/°C)	0.007	
C3 (W·s/°C)	0.015	
C4 (W·s/°C)	0.4	
C5 (W·s/°C)	2	
C6 (W·s/°C)	3	5



## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 33. SO-16L package dimensions

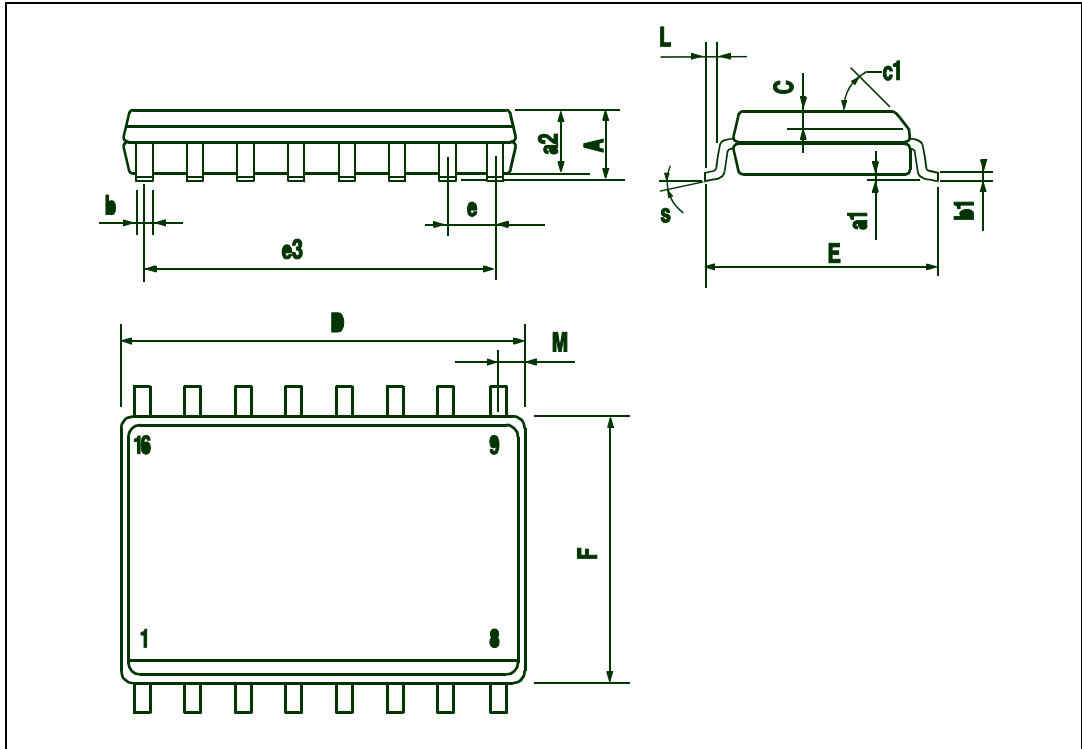


Table 16. SO-16L mechanical data

DIM.	mm.		
	Min.	Typ.	Max.
A			2.65
a1	0.1		0.2
a2			2.45
b	0.35		0.49
b1	0.23		0.32
C		0.5	
c1	45° (typ.)		

Table 16. SO-16L mechanical data (continued)

DIM.	mm.		
	Min.	Typ.	Max.
D	10.1		10.5
E	10.0		10.65
e		1.27	
e3		8.89	
F	7.4		7.6
L	0.5		1.27
M			0.75
S	8° (max.)		

### 5.2 P<sup>2</sup>PAK mechanical data

Figure 34. P<sup>2</sup>PAK package dimensions

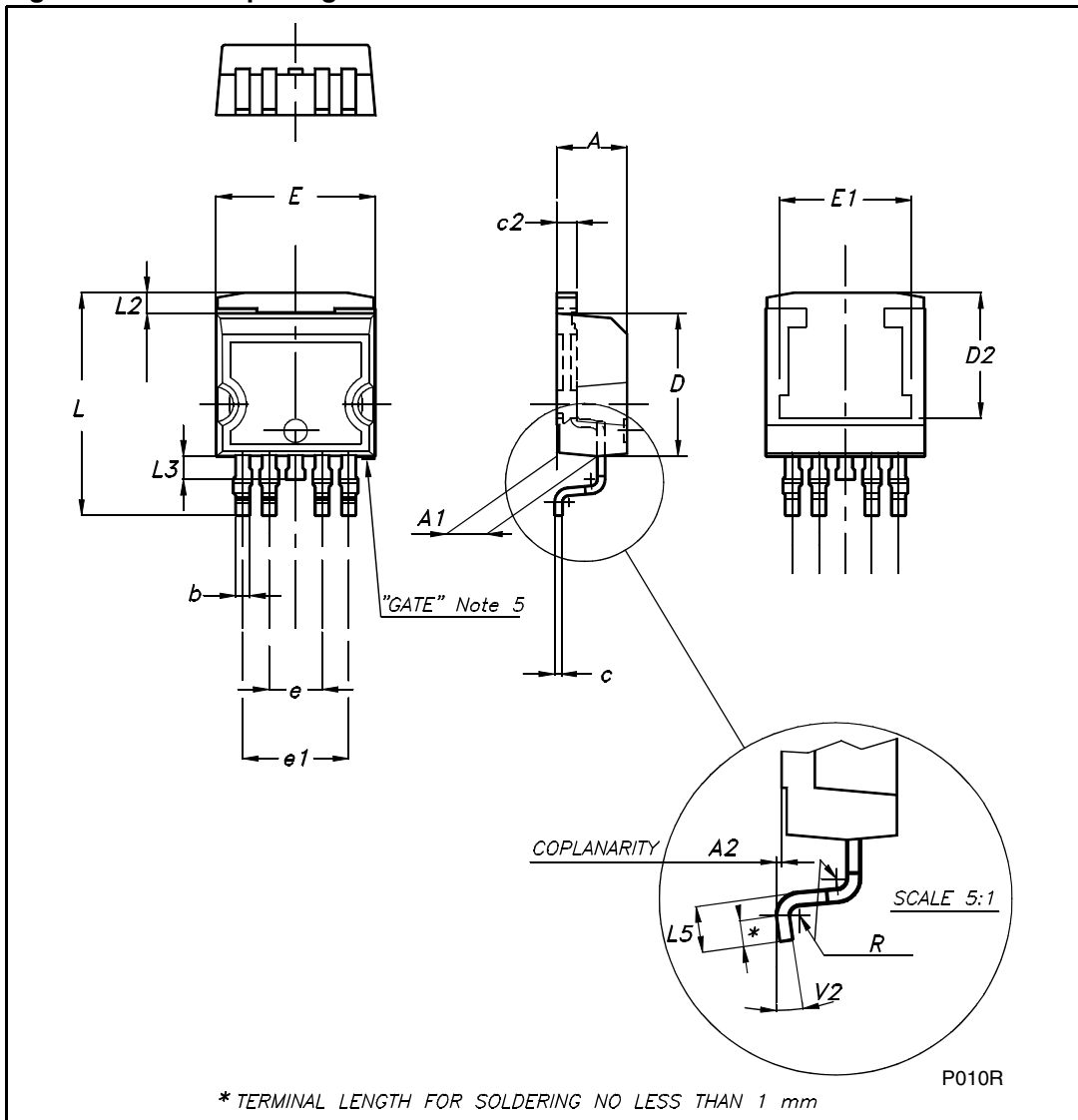


Table 17. P<sup>2</sup>PAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	2.40		2.80
A2	0.03		0.23
b	0.80		1.05
c	0.45		0.60
c2	1.17		1.37
D	8.95		9.35
D2		8.00	
E	10.00		10.40
E1		8.50	
e	3.20		3.60
e1	6.60		7.00
L	13.70		14.50
L2	1.25		1.40
L3	0.90		1.70
L5	1.55		2.40
R		0.40	
V2	0°		8°
Package weight	1.40 Gr (typ)		

### 5.3 SO-16L packing information

Figure 35. SO-16L tube shipment (no suffix)

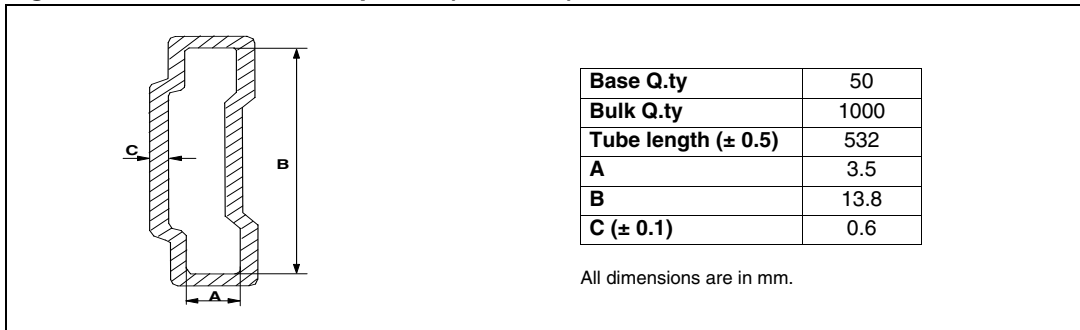
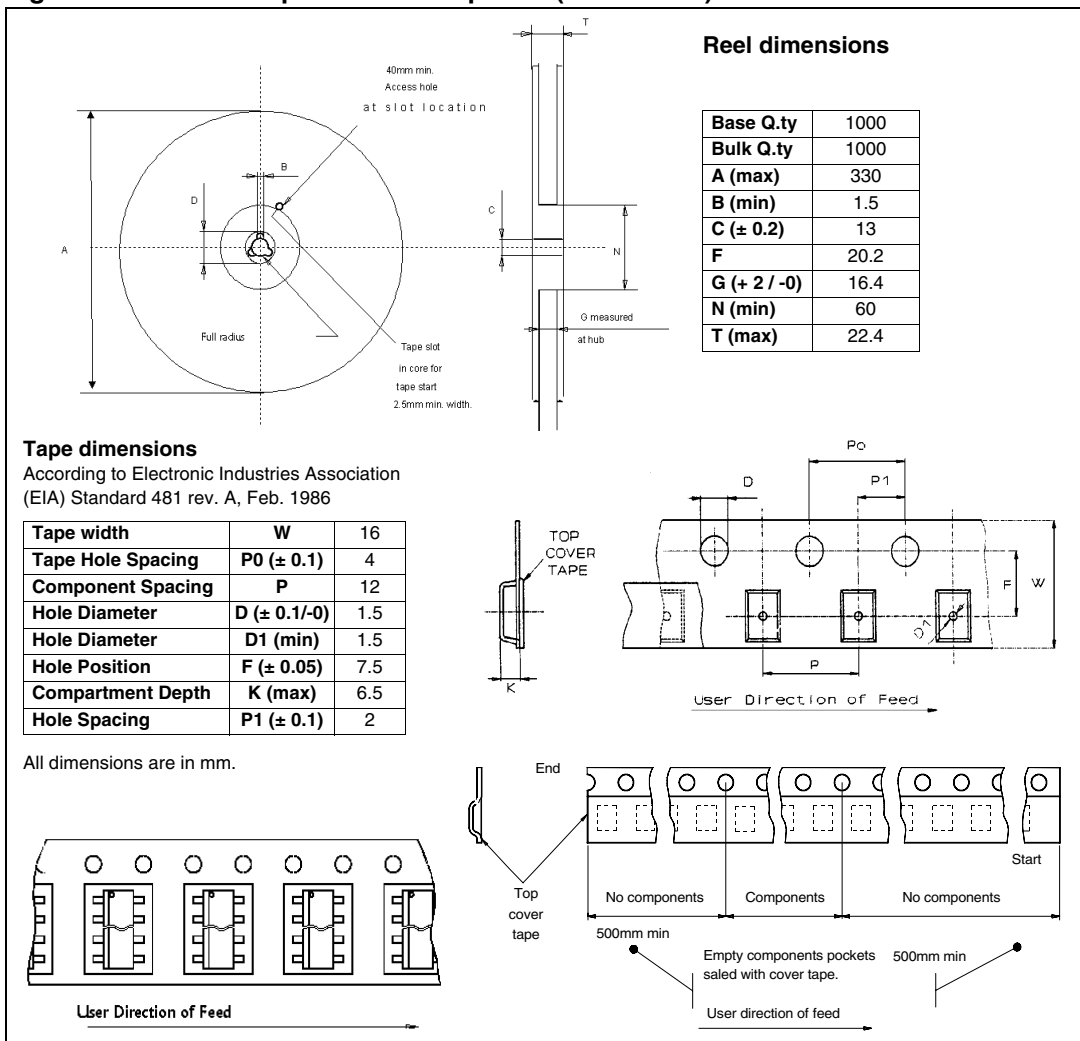


Figure 36. SO-16L tape and reel shipment (suffix "TR")



### 5.4 P<sup>2</sup>PAK packing information

Figure 37. P<sup>2</sup>PAK tube shipment (no suffix)

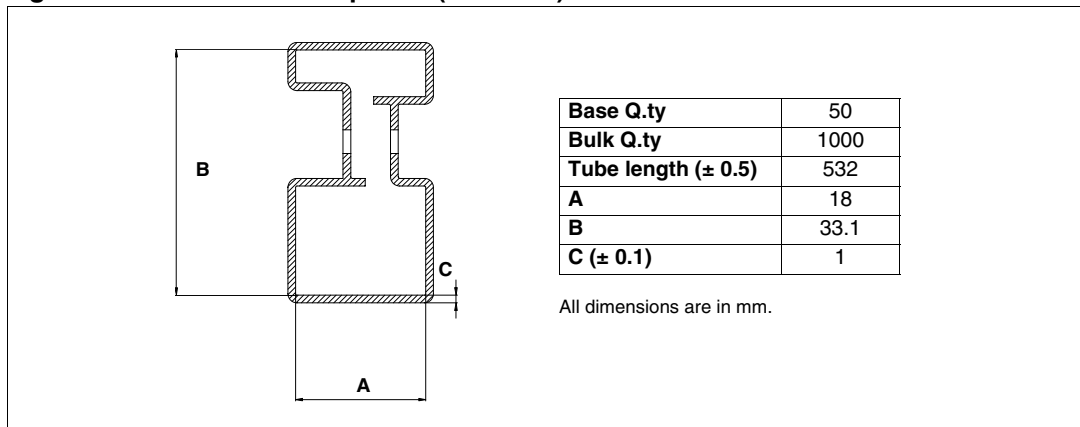
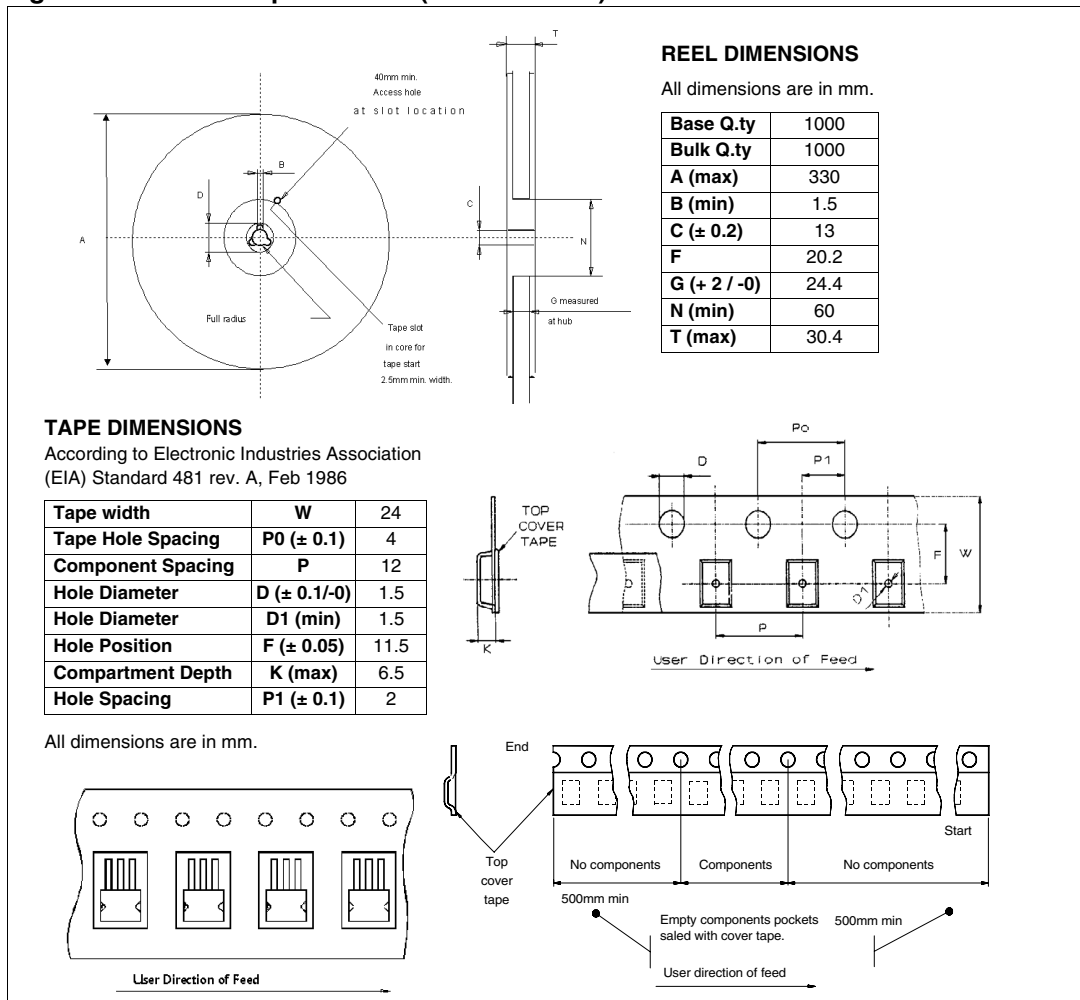


Figure 38. P<sup>2</sup>PAK tape and reel (suffix “13TR”)



## 6 Revision history

**Table 18. Document revision history**

Date	Revision	Changes
09-Sep-2004	1	Initial release.
03-May-2006	2	Suggested connections for unused and n.c.pins correction (page 2).
19-Dec-2008	3	Document reformatted and restructured. Added content, list of figures and tables. Added <i>ECOPACK® packages</i> information. Updated <i>Figure 38.: P<sup>2</sup>PAK tape and reel (suffix "13TR")</i> : changed component spacing (P) in tape dimensions table from 16 mm to 12 mm.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2008 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)