



# VN920DSP

## HIGH SIDE DRIVER

**Table 1. General Features**

Type	R <sub>DS(on)</sub>	I <sub>out</sub>	V <sub>CC</sub>
VN920DSP	16 mΩ	25 A	36 V

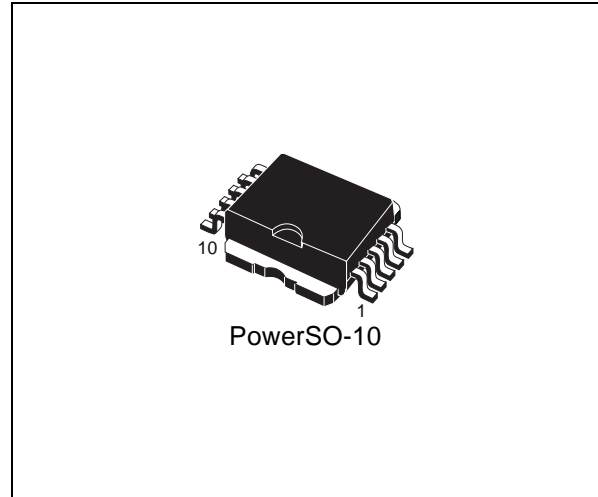
- CMOS COMPATIBLE INPUT
- ON STATE OPEN LOAD DETECTION
- OFF STATE OPEN LOAD DETECTION
- SHORTED LOAD PROTECTION
- UNDERVOLTAGE AND OVERVOLTAGE SHUTDOWN
- PROTECTION AGAINST LOSS OF GROUND
- VERY LOW STAND-BY CURRENT
- REVERSE BATTERY PROTECTION (\*)

### DESCRIPTION

The VN920DSP is a monolithic device made by using STMicroelectronics VIPower M0-3 Technology, intended for driving any kind of load with one side connected to ground.

Active V<sub>CC</sub> pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

**Figure 1. Package**



Active current limitation combined with thermal shutdown and automatic restart protect the device against overload.

The device detects open load condition both is on and off state. Output shorted to V<sub>CC</sub> is detected in the off state. Device automatically turns off in case of ground pin disconnection.

**Table 2. Order Codes**

Package	Tube	Tape and Reel
PowerSO-10™	VN920DSP	VN920DSP13TR

Note: (\*) See application schematic at page 9

Figure 2. Block Diagram

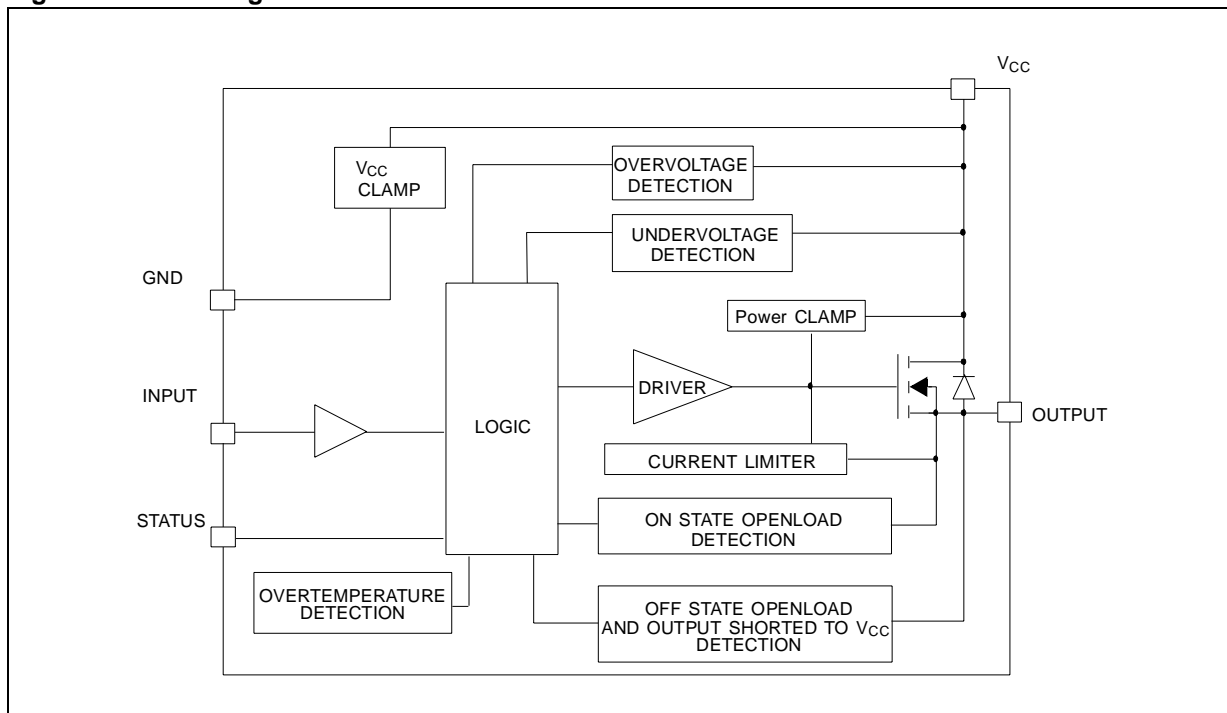


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	41	V
-V <sub>CC</sub>	Reverse DC Supply Voltage	- 0.3	V
-I <sub>GND</sub>	DC Reverse Ground Pin Current	- 200	mA
I <sub>OUT</sub>	DC Output Current	Internally Limited	A
-I <sub>OUT</sub>	Reverse DC Output Current	- 25	A
I <sub>IN</sub>	DC Input Current	+/- 10	mA
I <sub>STAT</sub>	DC Status Current	+/- 10	mA
V <sub>ESD</sub>	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
	- CURRENT SENSE	4000	V
	- OUTPUT	5000	V
	- V <sub>CC</sub>	5000	V
E <sub>MAX</sub>	Maximum Switching Energy (L=0.25mH; R <sub>L</sub> =0Ω; V <sub>bat</sub> =13.5V; T <sub>jstart</sub> =150°C; I <sub>L</sub> =45A)	362	mJ
P <sub>tot</sub>	Power Dissipation T <sub>C</sub> =25°C	96.1	W
T <sub>j</sub>	Junction Operating Temperature	Internally Limited	°C
T <sub>c</sub>	Case Operating Temperature	- 40 to 150	°C
T <sub>stg</sub>	Storage Temperature	- 55 to 150	°C

Figure 3. Configuration Diagram (Top View) & Suggested Connections for Unused and N.C. Pins

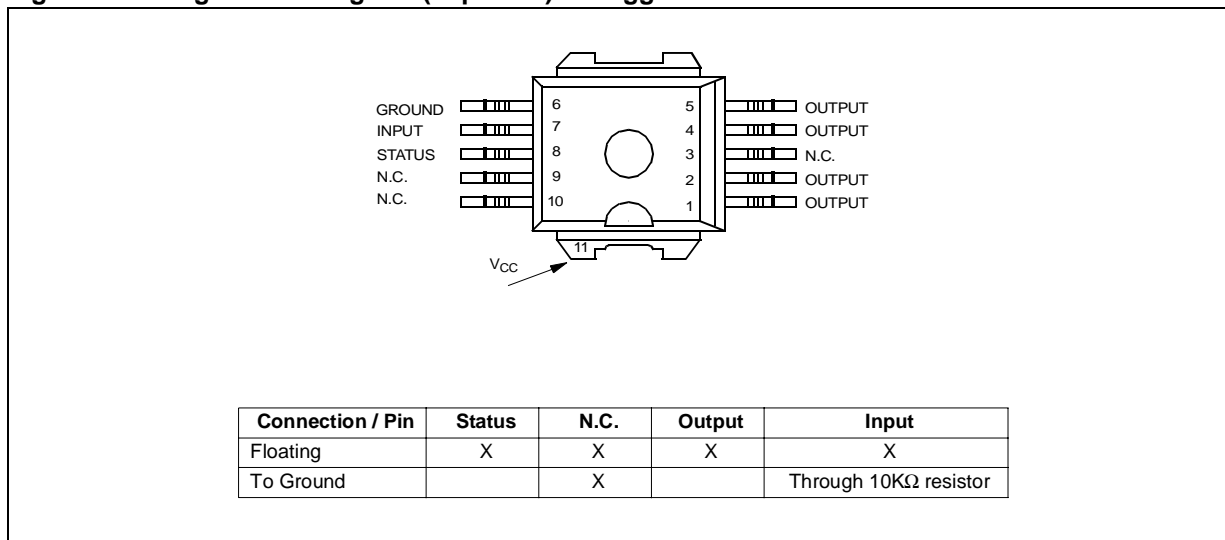


Figure 4. Current and Voltage Conventions

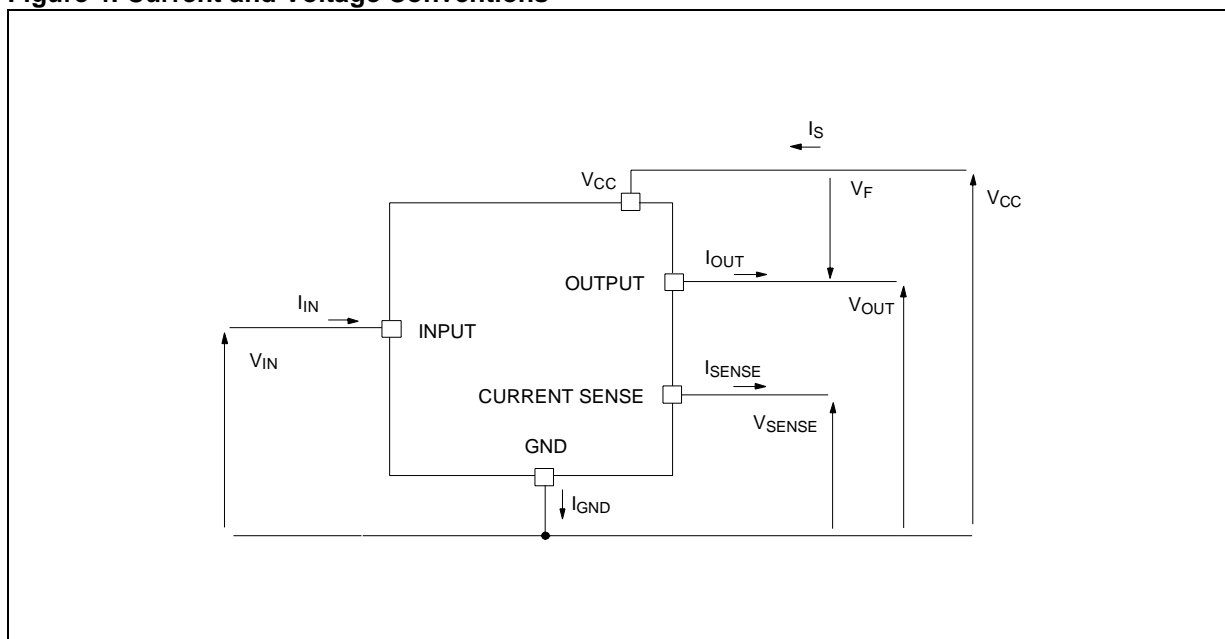


Table 4. Thermal Data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal Resistance Junction-case	Max 1.3	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient	Max 51.3 <sup>(1)</sup>   37 <sup>(2)</sup>	°C/W

Note: <sup>(1)</sup> When mounted on a standard single-sided FR-4 board with 0.5cm<sup>2</sup> of Cu (at least 35μm thick).

Note: <sup>(2)</sup> When mounted on a standard single-sided FR-4 board with 6 cm<sup>2</sup> of Cu (at least 35μm thick).

**ELECTRICAL CHARACTERISTICS**

 (8V < V<sub>CC</sub> < 36V; -40°C < T<sub>j</sub> < 150°C unless otherwise specified)

**Table 5. Power**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	Operating Supply Voltage		5.5	13	36	V
V <sub>USD</sub>	Undervoltage Shut-down		3	4	5.5	V
V <sub>USDhyst</sub>	Undervoltage Shut-down hysteresis			0.5		V
V <sub>OV</sub>	Overvoltage Shut-down		36			V
R <sub>ON</sub>	On State Resistance	I <sub>OUT</sub> =10A; T <sub>j</sub> =25°C			16	mΩ
		I <sub>OUT</sub> =10A			30	mΩ
		I <sub>OUT</sub> =3A; V <sub>CC</sub> =6V			50	mΩ
I <sub>S</sub>	Supply Current	Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V		10	25	μA
		Off State; V <sub>CC</sub> =13V; V <sub>IN</sub> =V <sub>OUT</sub> =0V; T <sub>j</sub> =25°C		10	20	μA
		On State; V <sub>CC</sub> =13V; V <sub>IN</sub> =5V; I <sub>OUT</sub> =0A			5	mA
I <sub>L(off1)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V	0		50	μA
I <sub>L(off2)</sub>	Off State Output Current	V <sub>IN</sub> =0V; V <sub>OUT</sub> =3.5V	-75		0	μA
I <sub>L(off3)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =125°C			5	μA
I <sub>L(off4)</sub>	Off State Output Current	V <sub>IN</sub> =V <sub>OUT</sub> =0V; V <sub>CC</sub> =13V; T <sub>j</sub> =25°C			3	μA

**Table 6. Switching (V<sub>CC</sub>=13V)**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	R <sub>L</sub> =1.3Ω		50		μs
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>L</sub> =1.3Ω		50		μs
dV <sub>OUT</sub> /dt <sub>(on)</sub>	Turn-on Voltage Slope	R <sub>L</sub> =1.3Ω		See relative diagram		V/μs
dV <sub>OUT</sub> /dt <sub>(off)</sub>	Turn-off Voltage Slope	R <sub>L</sub> =1.3Ω		See relative diagram		V/μs

**Table 7. Input Pin**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input Low Level				1.25	V
I <sub>IL</sub>	Low Level Input Current	V <sub>IN</sub> =1.25V	1			μA
V <sub>IH</sub>	Input High Level		3.25			V
I <sub>IH</sub>	High Level Input Current	V <sub>IN</sub> =3.25V			10	μA
V <sub>I(hyst)</sub>	Input Hysteresis Voltage		0.5			V
V <sub>ICL</sub>	Input Clamp Voltage	I <sub>IN</sub> =1mA	6	6.8	8	V
		I <sub>IN</sub> =-1mA		-0.7		V

## ELECTRICAL CHARACTERISTICS (continued)

Table 8. VCC - Output Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>F</sub>	Forward on Voltage	-I <sub>OUT</sub> =5A; T <sub>J</sub> =150°C			0.6	V

Table 9. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V <sub>STAT</sub>	Status Low Output Voltage	I <sub>STAT</sub> =1.6mA			0.5	V
I <sub>LSTAT</sub>	Status Leakage Current	Normal Operation V <sub>STAT</sub> =5V			10	μA
C <sub>STAT</sub>	Status Pin Input Capacitance	Normal Operation V <sub>STAT</sub> =5V			100	pF
V <sub>SCL</sub>	Status Clamp Voltage	I <sub>STAT</sub> =1mA	6	6.8	8	V
		I <sub>STAT</sub> =-1mA		-0.7		V

Table 10. Protections (see note 1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T <sub>TSD</sub>	Shut-down Temperature		150	175	200	°C
T <sub>R</sub>	Reset Temperature		135			°C
T <sub>hyst</sub>	Thermal Hysteresis		7	15		°C
t <sub>SDL</sub>	Status delay in overload condition	T <sub>J</sub> >T <sub>TSD</sub>			20	μs
I <sub>lim</sub>	Current limitation	5.5V<V <sub>CC</sub> <36V	30	45	75	A
					75	A
V <sub>demag</sub>	Turn-off Output Clamp Voltage	I <sub>OUT</sub> =2A; V <sub>IN</sub> =0V; L=6mH	V <sub>CC</sub> -41	V <sub>CC</sub> -48	V <sub>CC</sub> -55	V

Note: 1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 11. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I <sub>OL</sub>	Openload ON State Detection Threshold	V <sub>IN</sub> =5V	300	500	700	mA
t <sub>DOL(on)</sub>	Openload ON State Detection Delay	I <sub>OUT</sub> =0A			200	μs
V <sub>OL</sub>	Openload OFF State Voltage Detection Threshold	V <sub>IN</sub> =0V	1.5	2.5	3.5	V
t <sub>DOL(off)</sub>	Openload Detection Delay at Turn Off				1000	μs

Figure 5.

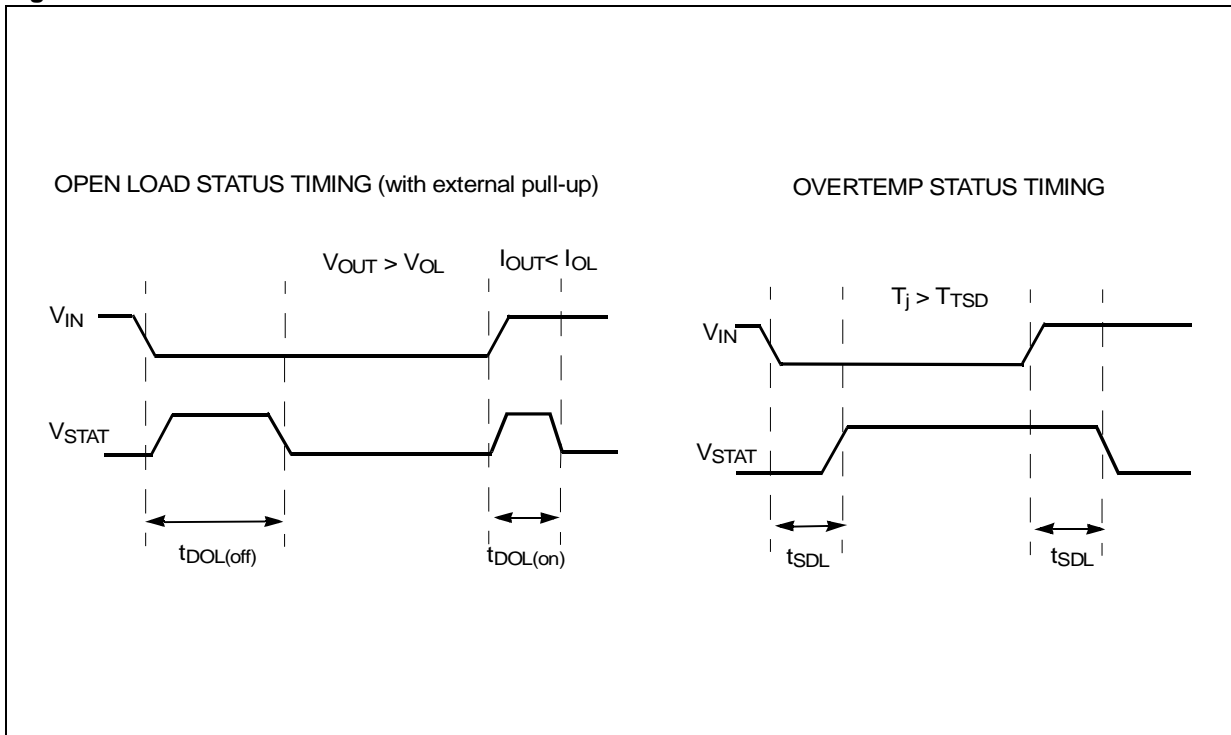


Figure 6. Switching time Waveforms

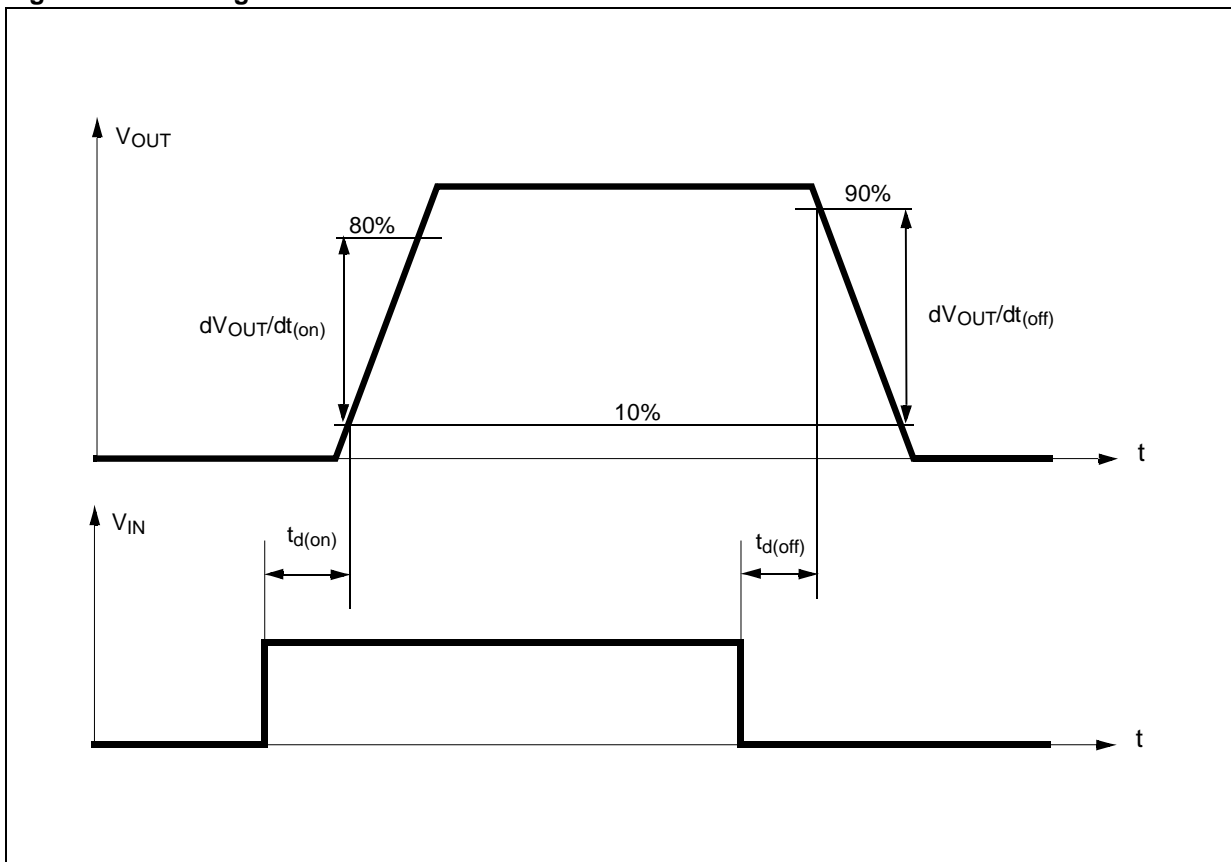


Table 12. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L	L	H
	H	H	H
Current Limitation	L	L	H
	H	X	( $T_j < T_{TSD}$ ) H
	H	X	( $T_j > T_{TSD}$ ) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output Voltage > $V_{OL}$	L	H	L
	H	H	H
Output Current < $I_{OL}$	L	L	H
	H	H	L

Table 13. Electrical Transient Requirements On  $V_{CC}$  Pin

ISO T/R 7637/1 Test Pulse	TEST LEVELS				Delays and Impedance
	I	II	III	IV	
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 $\Omega$
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 $\Omega$
3a	-25 V	-50 V	-100 V	-150 V	0.1 $\mu$ s 50 $\Omega$
3b	+25 V	+50 V	+75 V	+100 V	0.1 $\mu$ s 50 $\Omega$
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 $\Omega$
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 $\Omega$

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

Figure 7. Waveforms

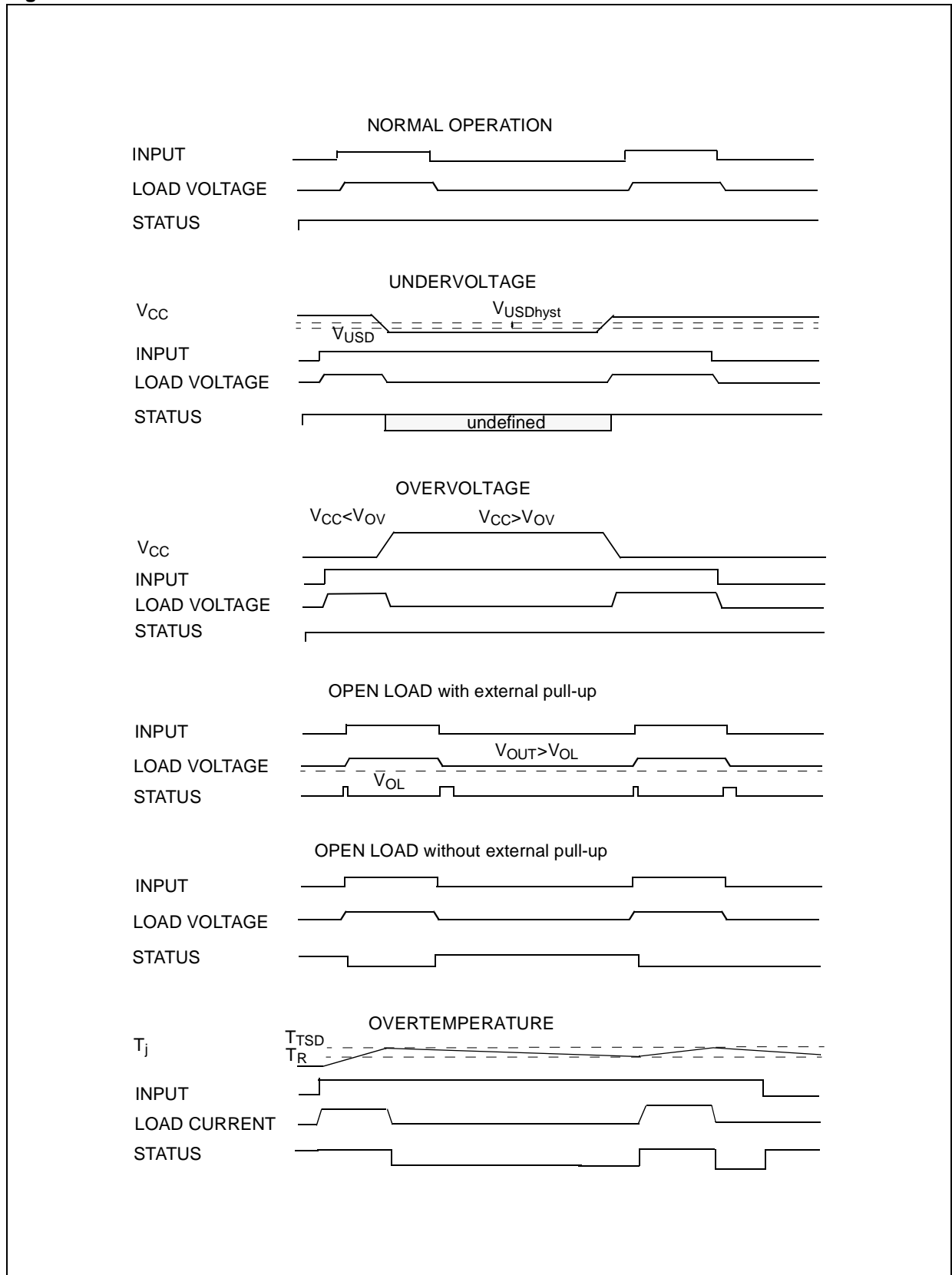
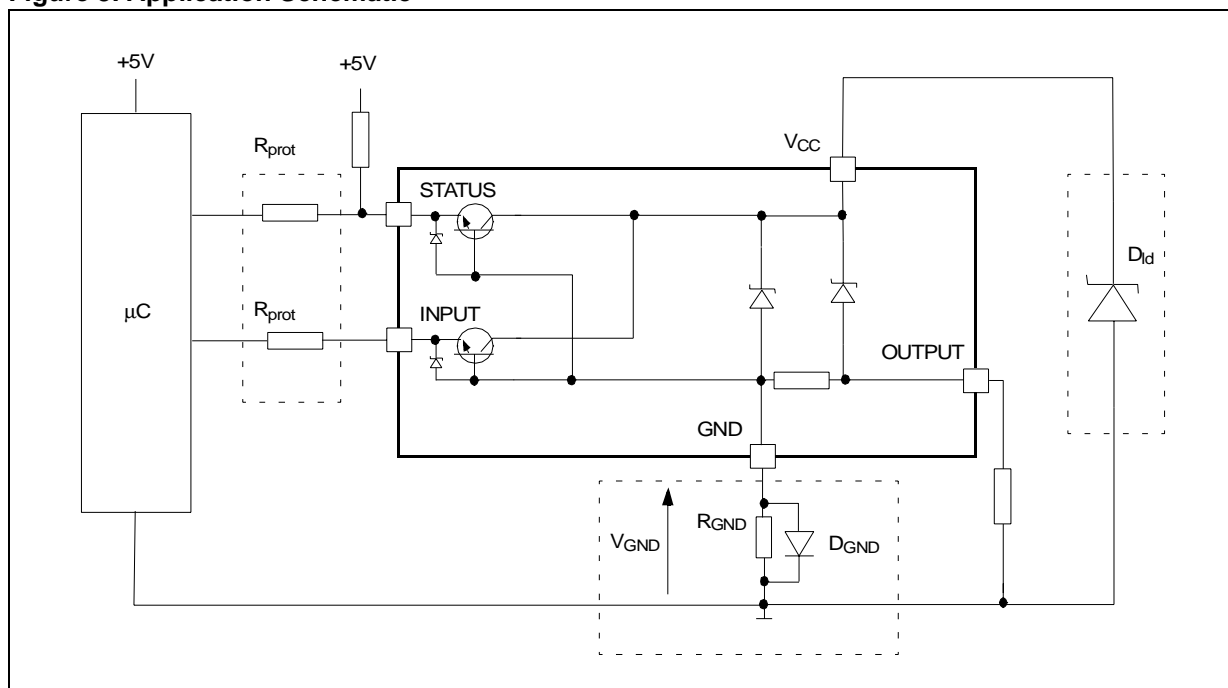




Figure 8. Application Schematic



### GND PROTECTION NETWORK AGAINST REVERSE BATTERY

**Solution 1:** Resistor in the ground line ( $R_{GND}$  only). This can be used with any type of load.

The following is an indication on how to dimension the  $R_{GND}$  resistor.

- 1)  $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$ .
- 2)  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in  $R_{GND}$  (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the  $R_{GND}$  will produce a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift will vary depending on many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

**Solution 2:** A diode ( $D_{GND}$ ) in the ground line.

A resistor ( $R_{GND} = 1\text{k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ( $\approx 600\text{mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in INPUT line is also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating.

Safest configuration for unused INPUT pin is to leave it unconnected, while unused SENSE pin has to be connected to Ground pin.

### LOAD DUMP PROTECTION

$D_{id}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds  $V_{CC}$  max DC rating. The same applies if the device will be subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO T/R 7637/1 table.

### µC I/Os PROTECTION:

If a ground protection network is used and negative transient are present on the  $V_{CC}$  line, the control pins will be pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu\text{C}$  I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of  $\mu\text{C}$  and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of  $\mu\text{C}$  I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For  $V_{CCpeak} = -100\text{V}$  and  $I_{latchup} \geq 20\text{mA}$ ;  $V_{OH\mu C} \geq 4.5\text{V}$   
 $5\text{k}\Omega \leq R_{prot} \leq 65\text{k}\Omega$ .

Recommended  $R_{prot}$  value is  $10\text{k}\Omega$ .

Figure 9. Off State Output Current

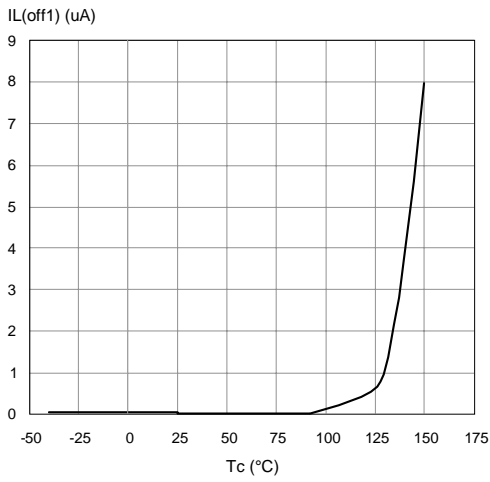


Figure 10. High Level Input Current

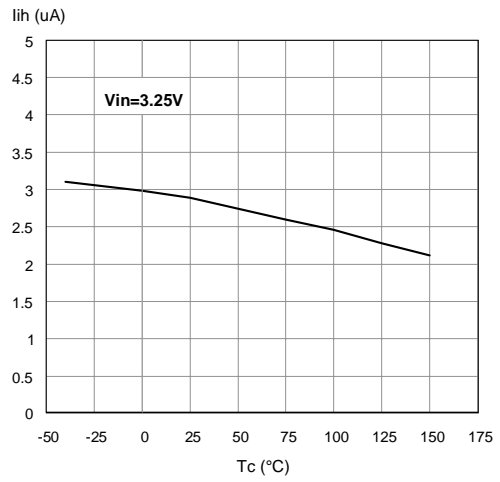


Figure 11. Input Low Level

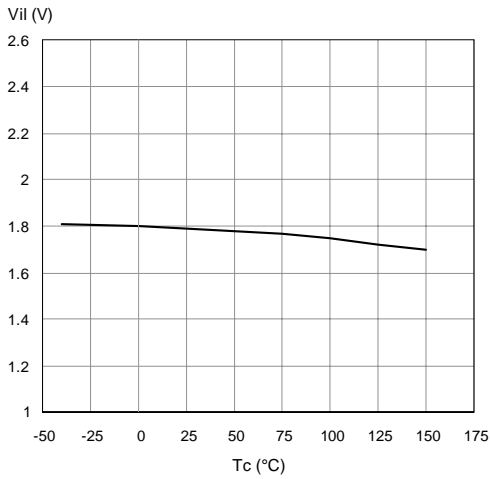


Figure 13. Input High Level

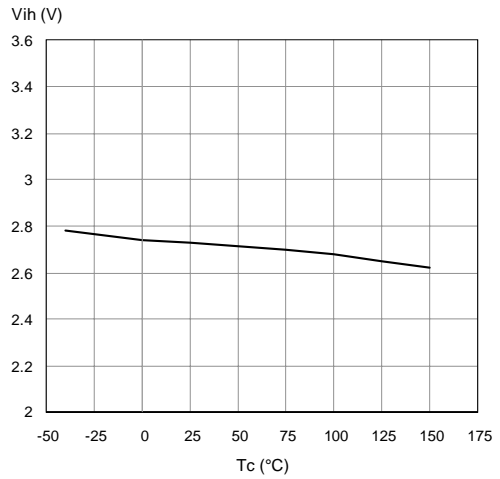


Figure 12. Input Clamp Voltage

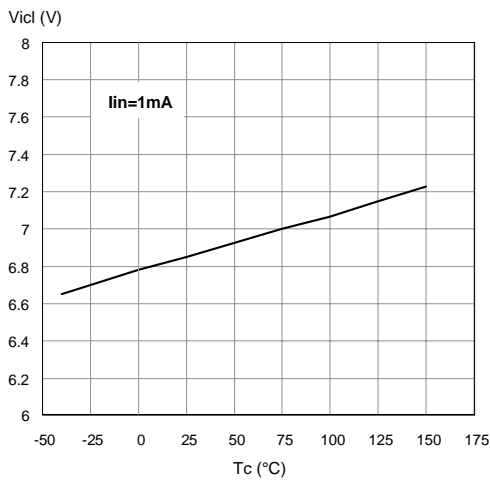


Figure 14. Input Hysteresis Voltage

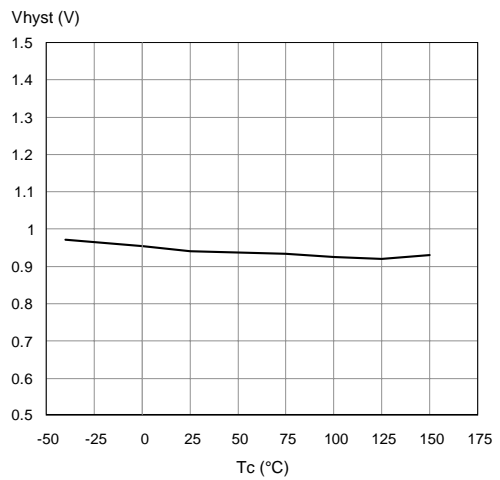


Figure 15. Overvoltage Shutdown

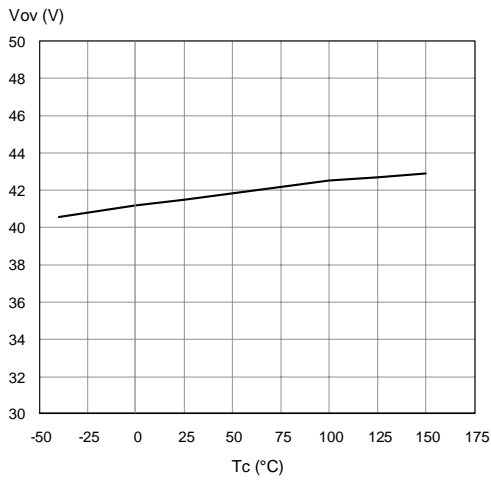


Figure 18. I<sub>LIM</sub> Vs T<sub>case</sub>

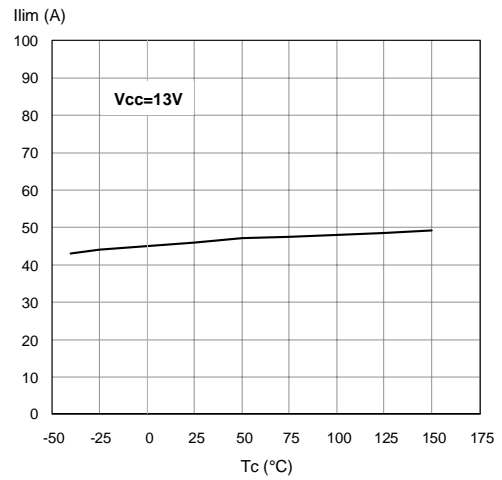


Figure 16. Turn-on Voltage Slope

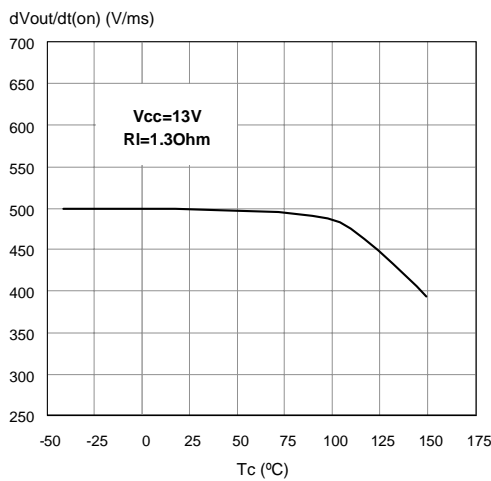


Figure 19. Turn-off Voltage Slope

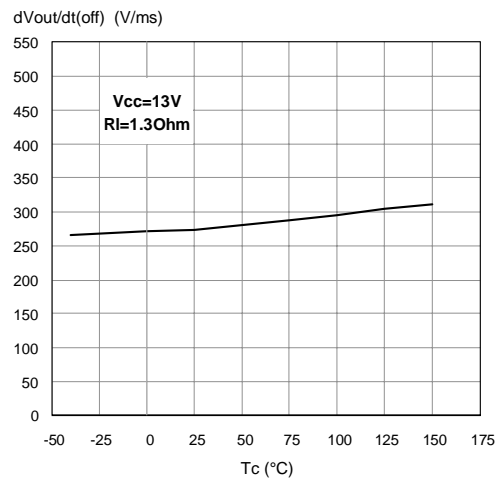


Figure 17. On State Resistance Vs T<sub>case</sub>

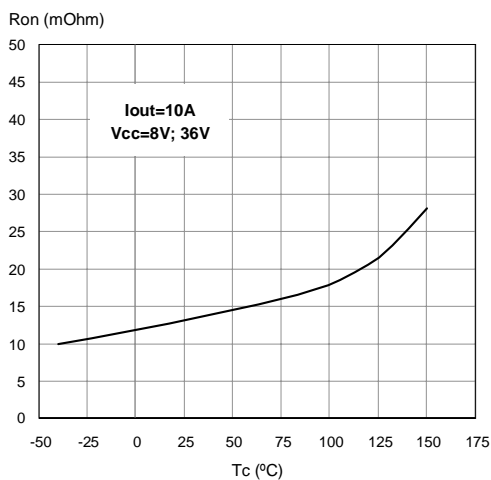


Figure 20. On State Resistance Vs V<sub>CC</sub>

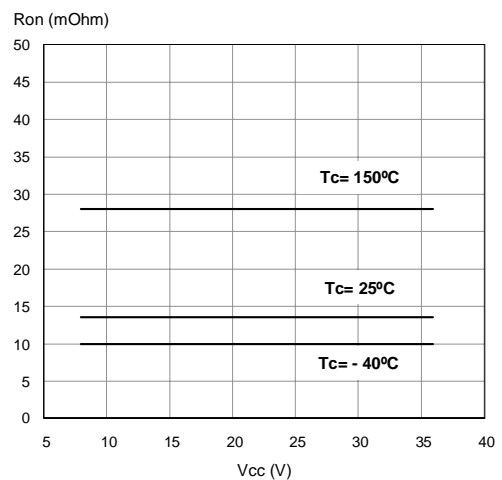


Figure 21. Status Leakage Current

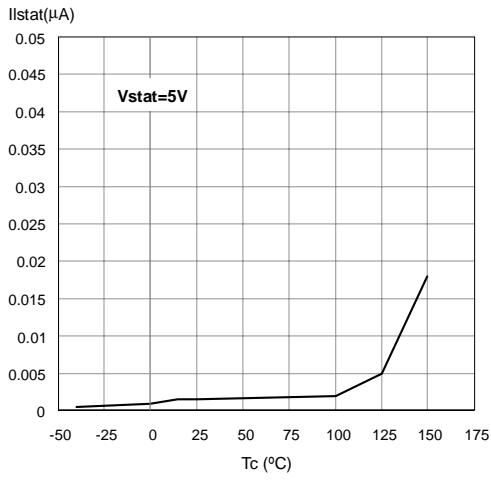


Figure 23. Status Low Output Voltage

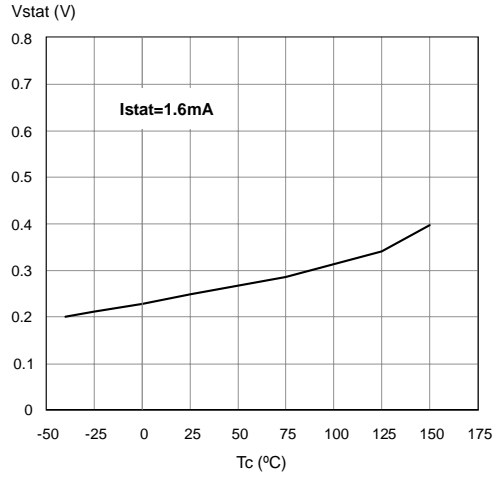


Figure 22. Status Clamp Voltage

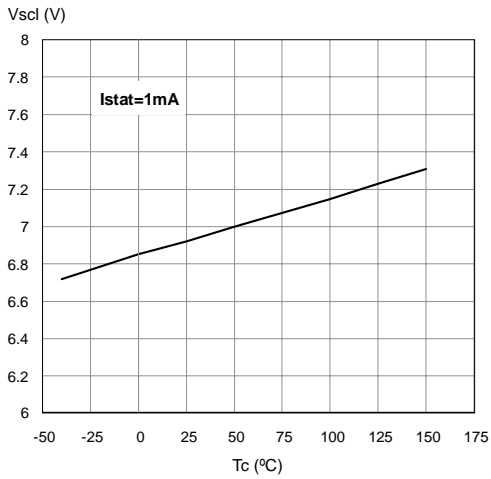
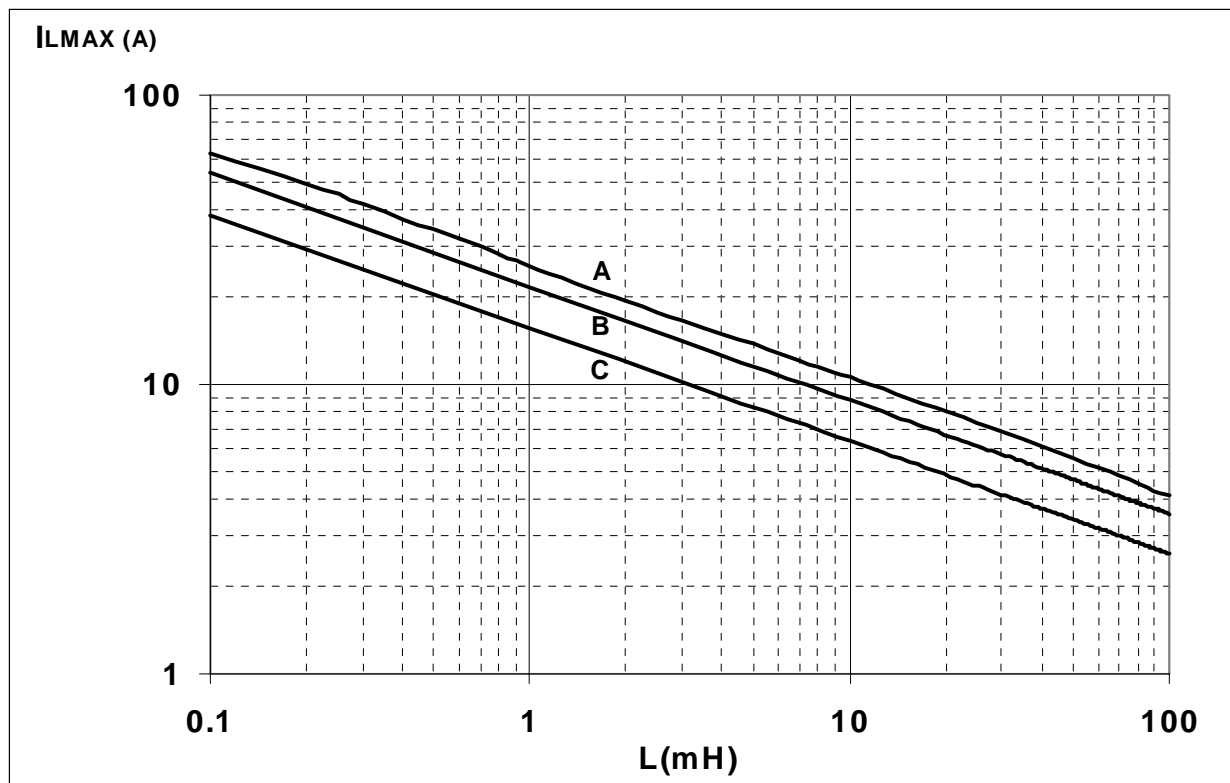


Figure 24. Maximum turn off current versus load inductance



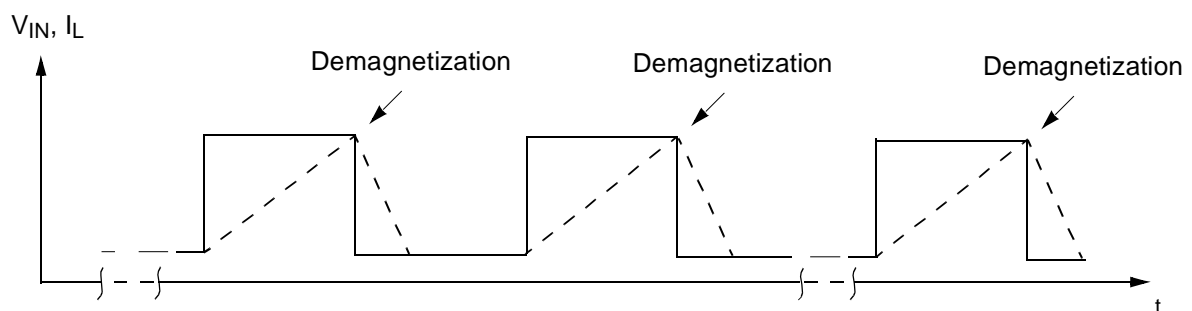
- A = Single Pulse at  $T_{Jstart}=150^{\circ}C$
- B= Repetitive pulse at  $T_{Jstart}=100^{\circ}C$
- C= Repetitive Pulse at  $T_{Jstart}=125^{\circ}C$

Conditions:

$V_{CC}=13.5V$

Values are generated with  $R_L=0\Omega$

In case of repetitive pulses,  $T_{Jstart}$  (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.



PowerSO-10™ Thermal Data

Figure 25. PowerSO-10™ PC Board

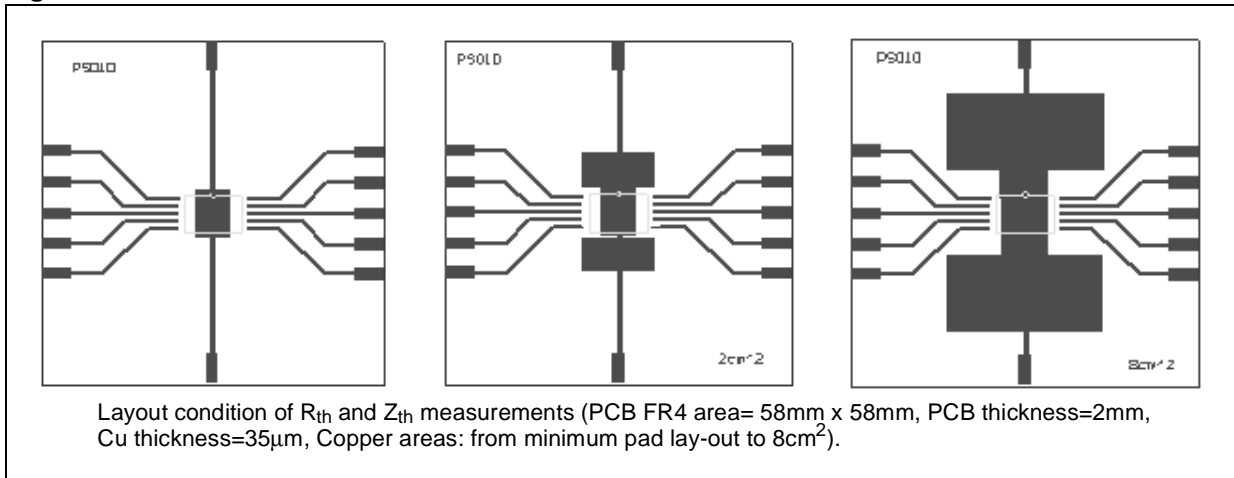


Figure 26.  $R_{thj-amb}$  Vs PCB copper area in open box free air condition

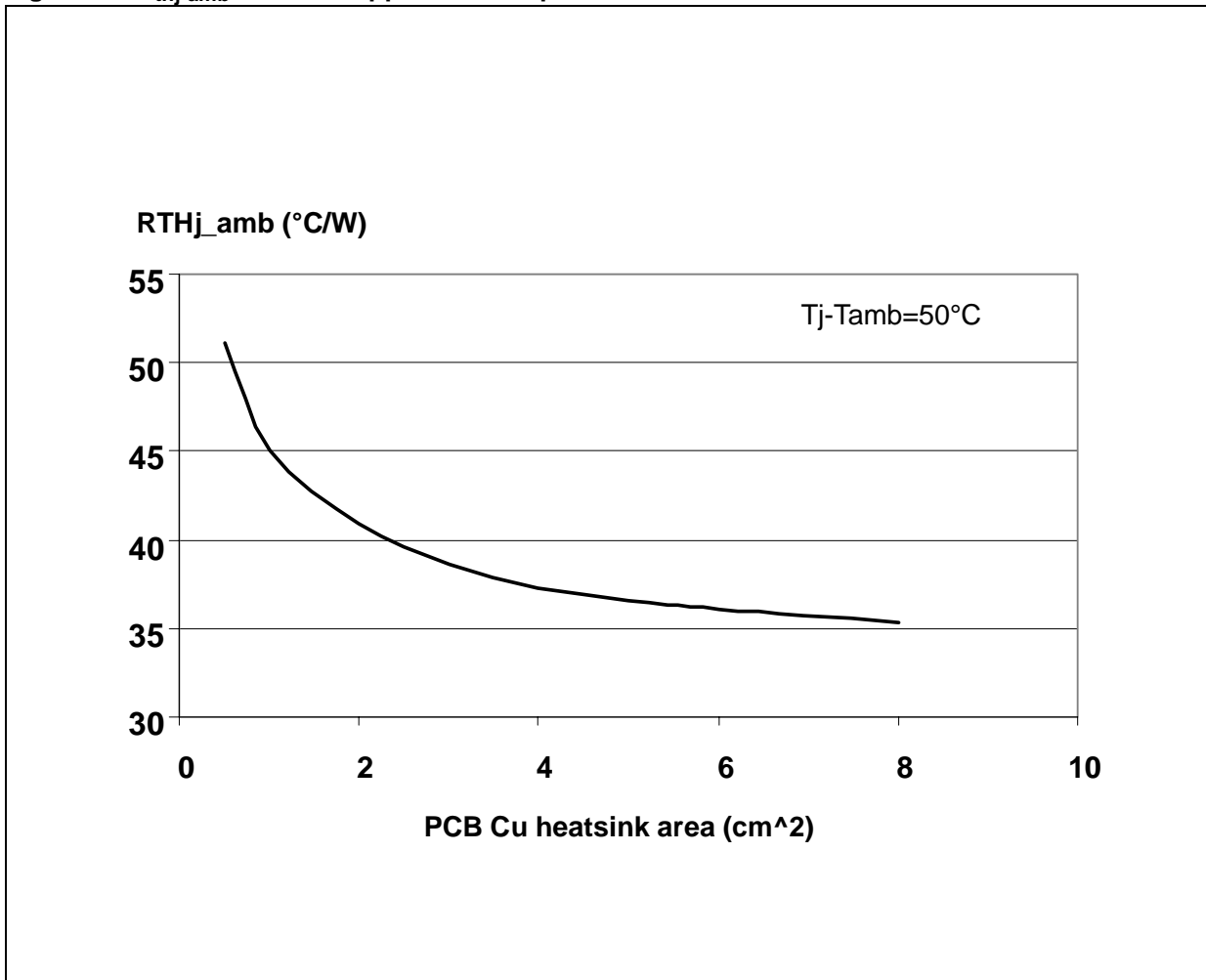


Figure 27. PowerSO-10 Thermal Impedance Junction Ambient Single Pulse

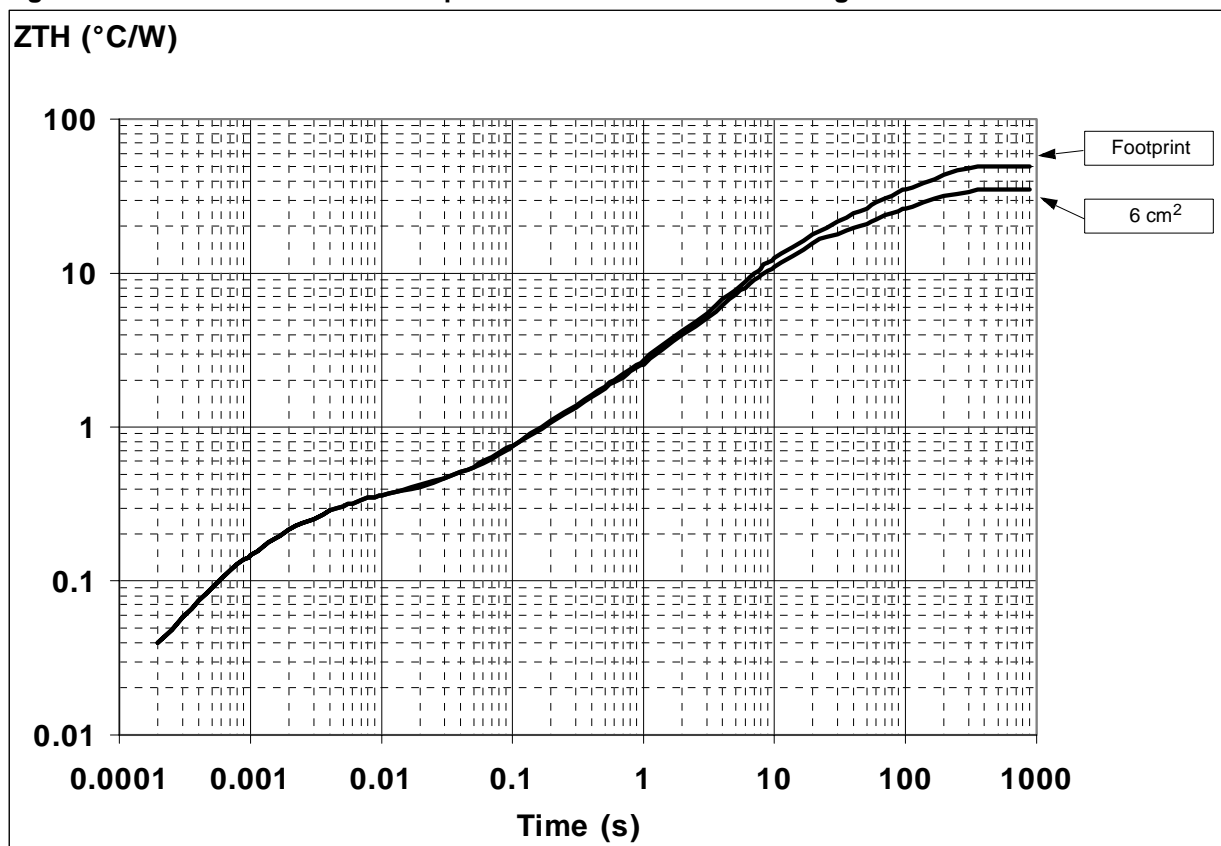
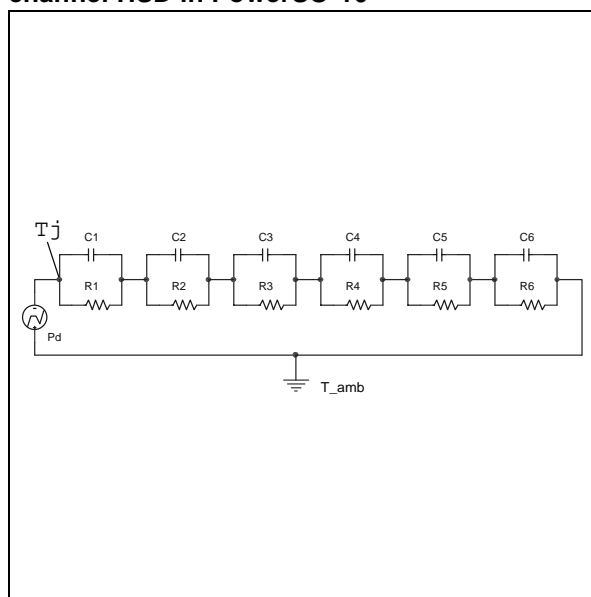


Figure 28. Thermal fitting model of a double channel HSD in PowerSO-10



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Table 14. Thermal Parameter

Area/island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.02	
R2 (°C/W)	0.1	
R3 (°C/W)	0.2	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0015	
C2 (W.s/°C)	7.00E-03	
C3 (W.s/°C)	0.015	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

PACKAGE MECHANICAL

Table 15. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0°		8°
α (*)	2°		8°

Note: (\*) Muar only POA P013P

Figure 29. PowerSO-10™ Package Dimensions

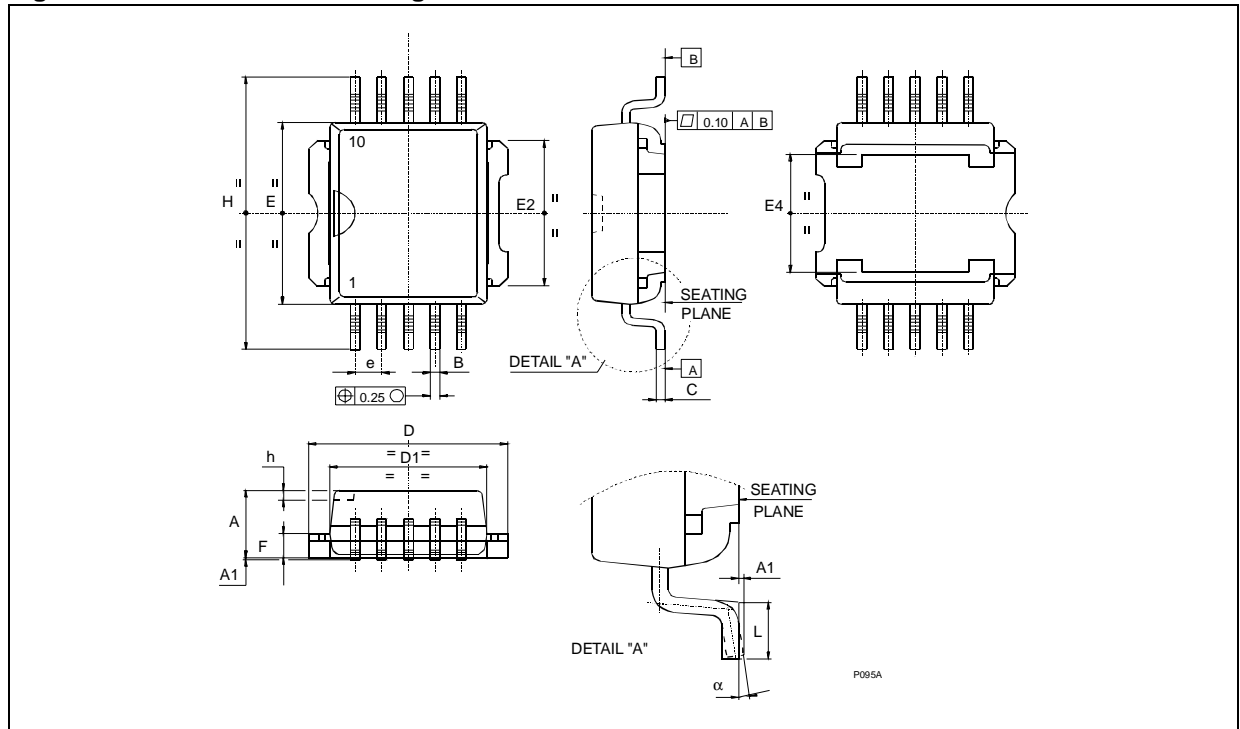




Figure 30. PowerSO-10™ Suggested Pad Layout And Tube Shipment (no suffix)

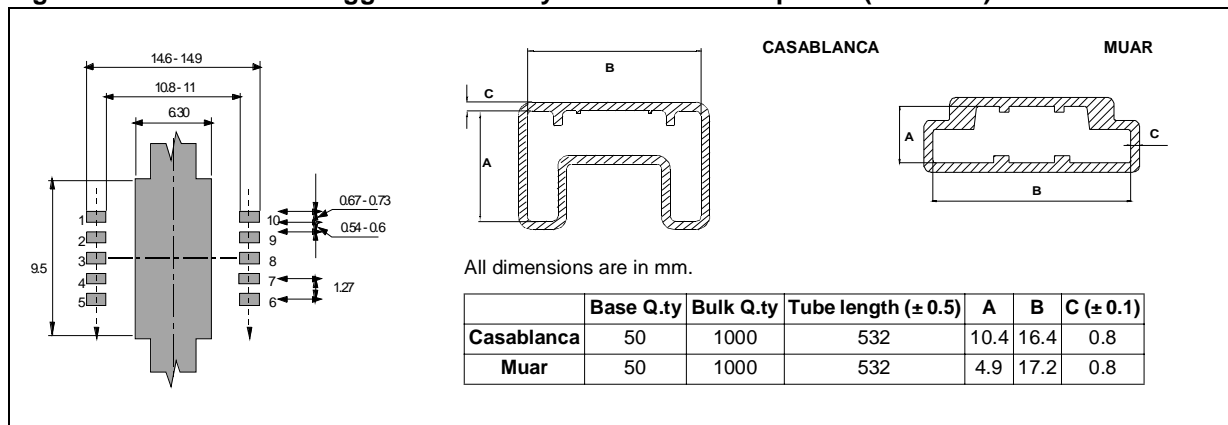
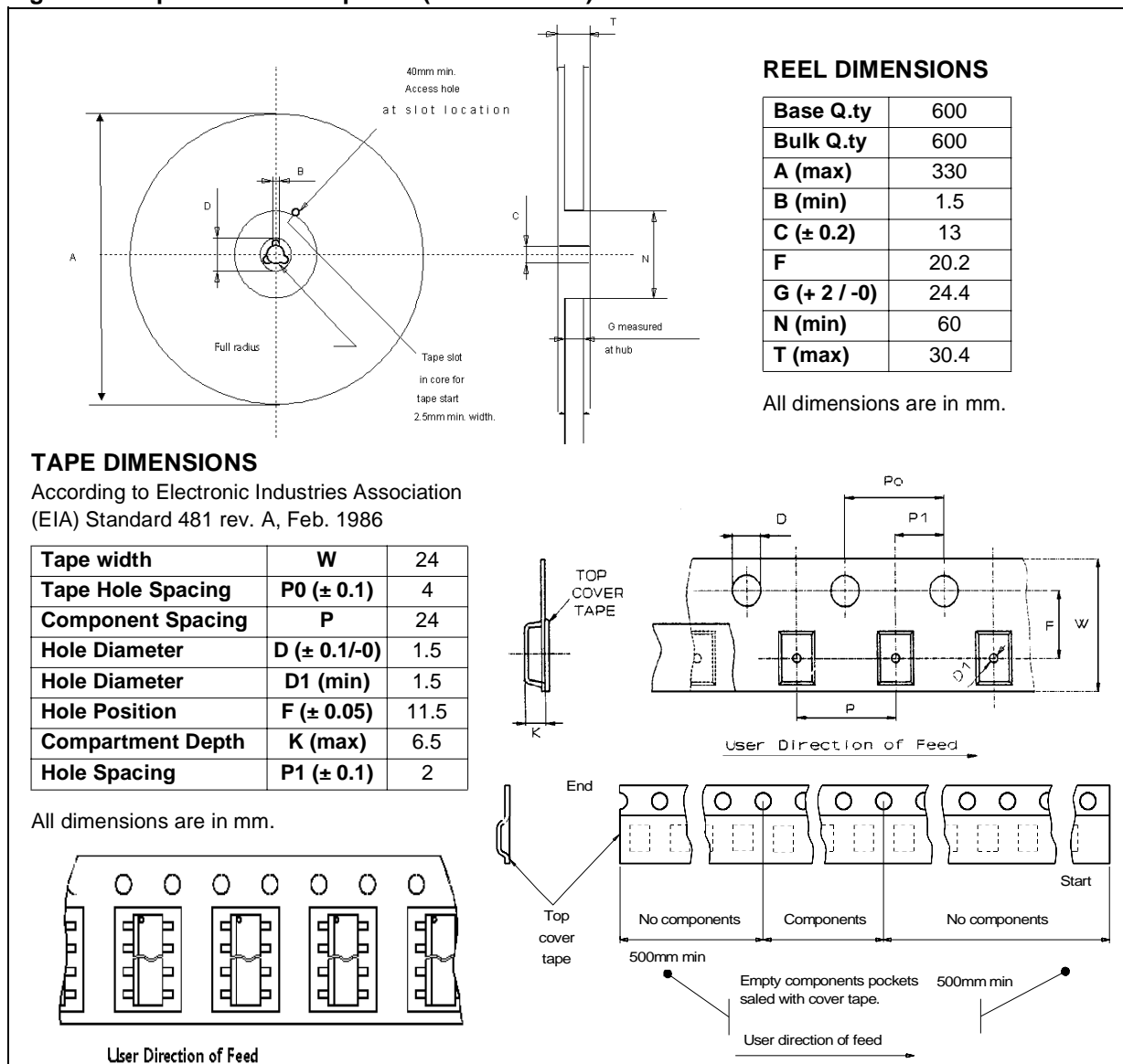


Figure 31. Tape And Reel Shipment (suffix “13TR”)



**REVISION HISTORY**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
Sep. 2004	1	- First Issue.
Oct. 2004	2	- Minor text change.
24-Sep-2013	3	- Updated Disclaimer

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