



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package
			TO-92
-500V	125Ω	-100mA	VP0550N3

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

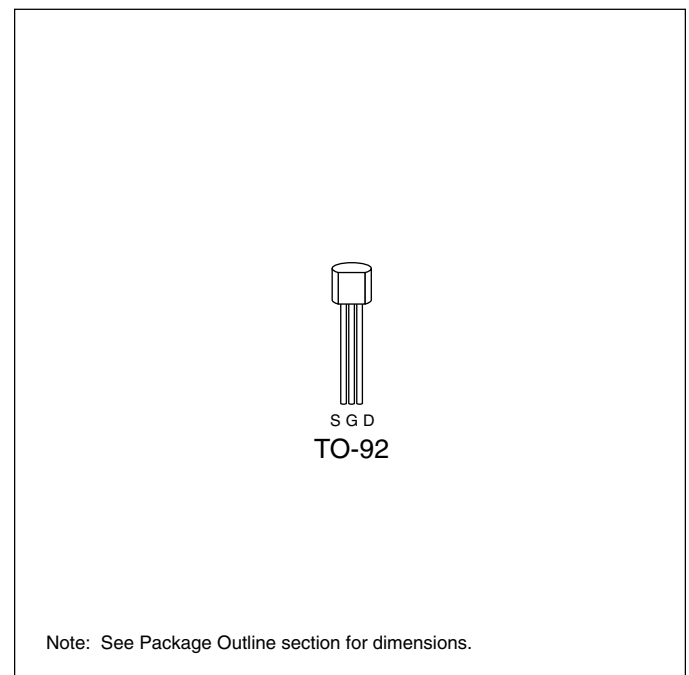
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Option



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{jc} $^\circ\text{C/W}$	θ_{ja} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-92	-54mA	-0.25A	1W	125	170	-54mA	-0.25A

* I_D (continuous) is limited by max rated T_j .

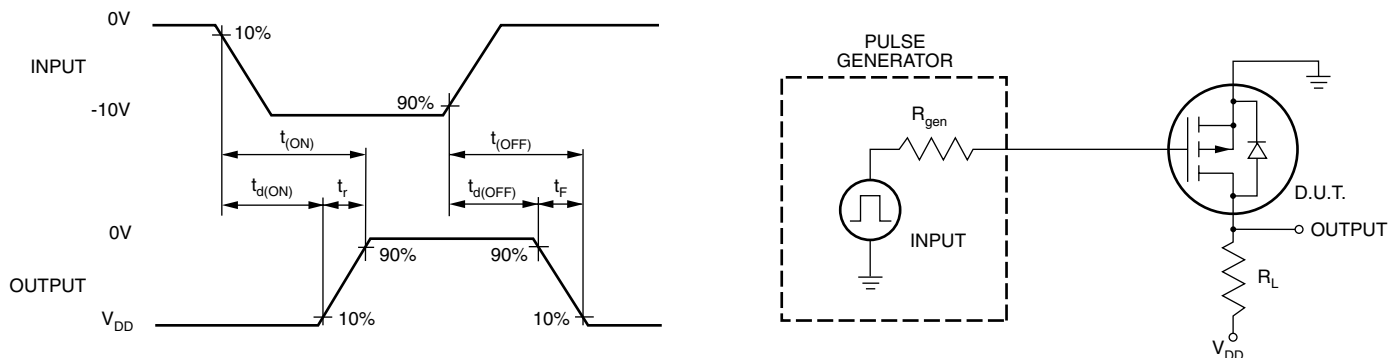
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-500			V	$V_{GS} = 0V, I_D = -1mA$
$V_{GS(th)}$	Gate Threshold Voltage	-2.0		-4.5	V	$V_{GS} = V_{DS}, I_D = -1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		3.5	6	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1mA$
I_{GSS}	Gate Body Leakage			-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current			-10	μA	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
				-1000		$V_{GS} = 0V, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		-90		mA	$V_{GS} = -5V, V_{DS} = -25V$
		-100	-240			$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		85		Ω	$V_{GS} = -5V, I_D = -5mA$
			80	125		$V_{GS} = -10V, I_D = -10mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.85		$\%/^\circ\text{C}$	$V_{GS} = -10V, I_D = -10mA$
G_{FS}	Forward Transconductance	25	40		m \bar{S}	$V_{DS} = -25V, I_D = -10mA$
C_{ISS}	Input Capacitance		40	70	pF	$V_{GS} = 0V, V_{DS} = -25V$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		10	20		
C_{RSS}	Reverse Transfer Capacitance		3	10		
$t_{d(ON)}$	Turn-ON Delay Time		5	10	ns	$V_{DD} = -25V$ $I_D = -100mA$ $R_{GEN} = 25\Omega$
t_r	Rise Time		8	10		
$t_{d(OFF)}$	Turn-OFF Delay Time		8	15		
t_f	Fall Time		5	16		
V_{SD}	Diode Forward Voltage Drop		-0.8	-1.5	V	$V_{GS} = 0V, I_{SD} = -0.1A$
t_{rr}	Reverse Recovery Time		200		ns	$V_{GS} = 0V, I_{SD} = -0.1A$

Notes:

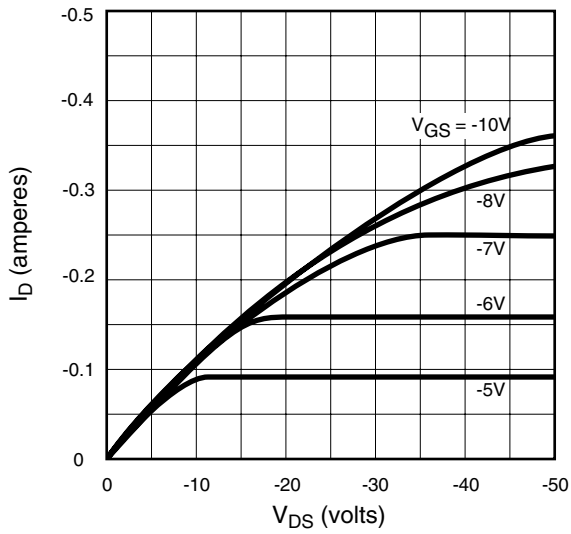
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

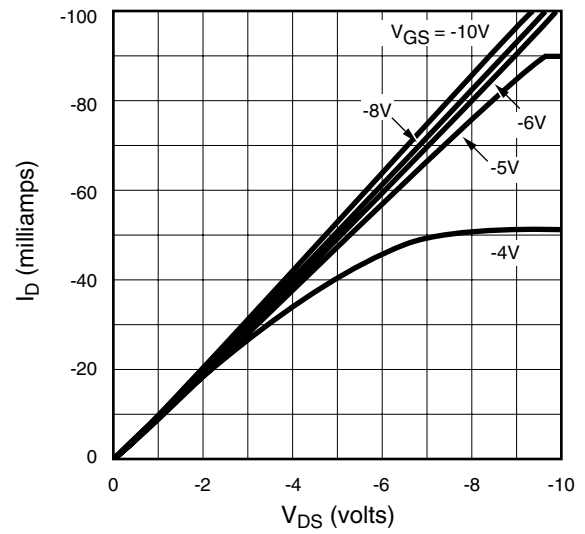


Typical Performance Curves

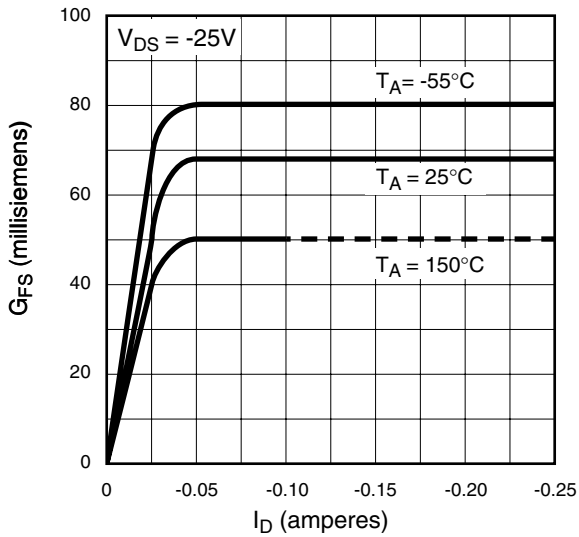
Output Characteristics



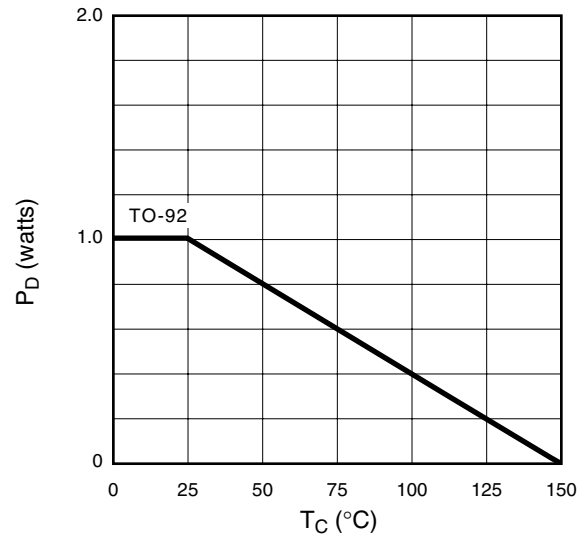
Saturation Characteristics



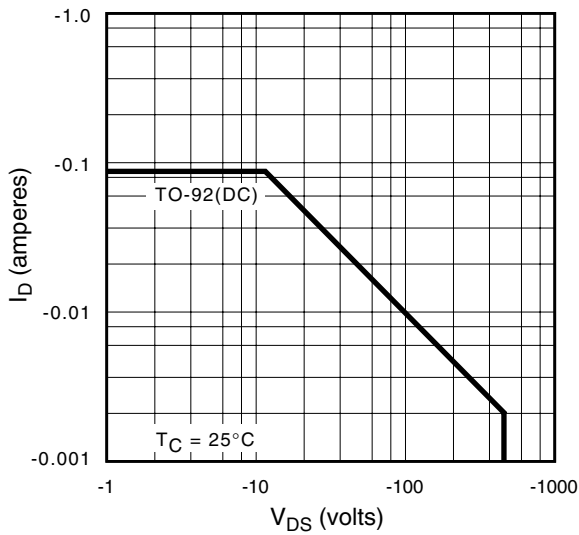
Transconductance vs. Drain Current



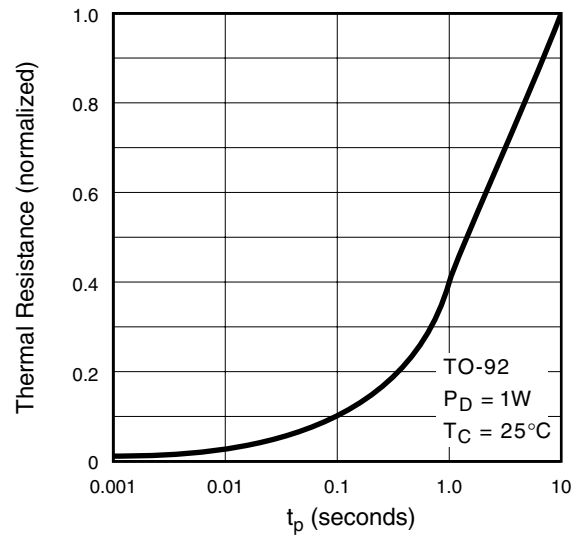
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



Typical Performance Curves

