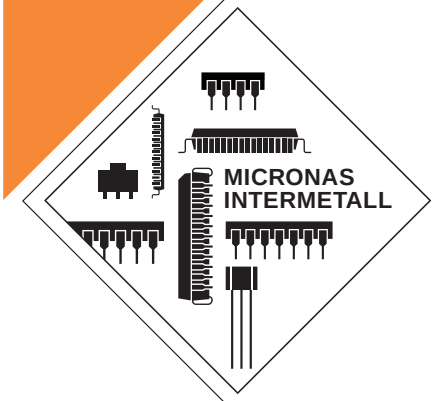


PRELIMINARY DATA SHEET

VPX 3220 A,
VPX 3216 B,
VPX 3214 C
Video Pixel Decoders

Edition July 1, 1996
6251-368-2PD

MICRONAS
INTERMETALL

Contents

Contents, continued

Contents, continued

Video Pixel Decoder Family

Release Notes: Revision bars indicate significant changes to the previous edition.

1. Introduction

The Video Pixel Decoder (VPX) is a full-feature video acquisition IC for consumer video and multimedia applications. All of the processing necessary to convert an analog video signal into a digital component stream has been integrated onto a single 44-pin IC. Its notable features include:

- single chip multistandard color decoding NTSC/PAL/SECAM/S-VHS, NTSC with chroma comb filter.
- two 8-bit video A/D converters with clamping and automatic gain control (AGC)
- four analog inputs with integrated selector for
  3 composite video sources (CVBS), or
  2 YC sources (SVHS), or
  2 composite video sources and one YC source.
- automatic standard detection
- horizontal and vertical sync detection for all standards
- hue, brightness, contrast, and saturation control
- horizontal resizing between 32 and 1056 pixel/line
- vertical resizing by line dropping
- high quality anti-aliasing filter (VPX 3220 A only)
- ITU-R601 level compatible
- YC_bC_r (4:4:4, 4:2:2, or 4:1:1) or
  γ-corrected RGB 4:4:4 (15, 16, or 24 bits)
  compressed Video (DPCM 8 bit)
  (VPX 3214 C supports only YCrCb 4:2:2)
- alpha key generation
  (only VPX 3220 A, and VPX 3216 B)
- 8-bit or 16-bit synchronous output mode
- asynchronous output mode via FIFO with status flags
- VBI bypass mode for Teletext, Closed Caption, and Intercast
- 44-pin plastic package (PLCC, TQFP)
- total power consumption under 1 W
- I^2C serial control, selectable power-up default state
- on-chip clock generation
- IEEE 1149.1 (JTAG) boundary scan interface

VPX 3220 A, VPX 3216 B, and VPX 3214 C are pin and software compatible, but differ slightly in the feature set.

1.1. Difference between VPX 3220 A and VPX 3216 B

VPX 3220 A performs low-pass filtering before resampling the data, whereas VPX 3216 B does not. For more info, see Fig. 1–1 and refer to section 2.3.

1.2. Difference between VPX 3216 B and VPX 3214 C

The VPX 3214 C is based on the VPX 3216 B but without color space conversion. VPX 3214 C supports only YC_bC_r 4:2:2.

1.3. System Architecture

The block diagram in Fig. 1–1 illustrates the signal flow through the VPX. A sampling stage performs 8-bit A/D conversion, clamping, and AGC. The color decoder separates the luma and chroma signals, demodulates the chroma, and filters the luminance. A sync slicer detects the sync edge and computes the skew relative to the sample clock. The component processing stage resizes the YCbCr samples, adjusts the contrast and brightness, and interpolates the chroma. The color space stage contains a dematrix, a γ^{-1} correction, a DPCM-like encoder, and an alpha key generator. The format stage arranges the samples into the selected byte format and (in the case of asynchronous output) buffers the data for output.

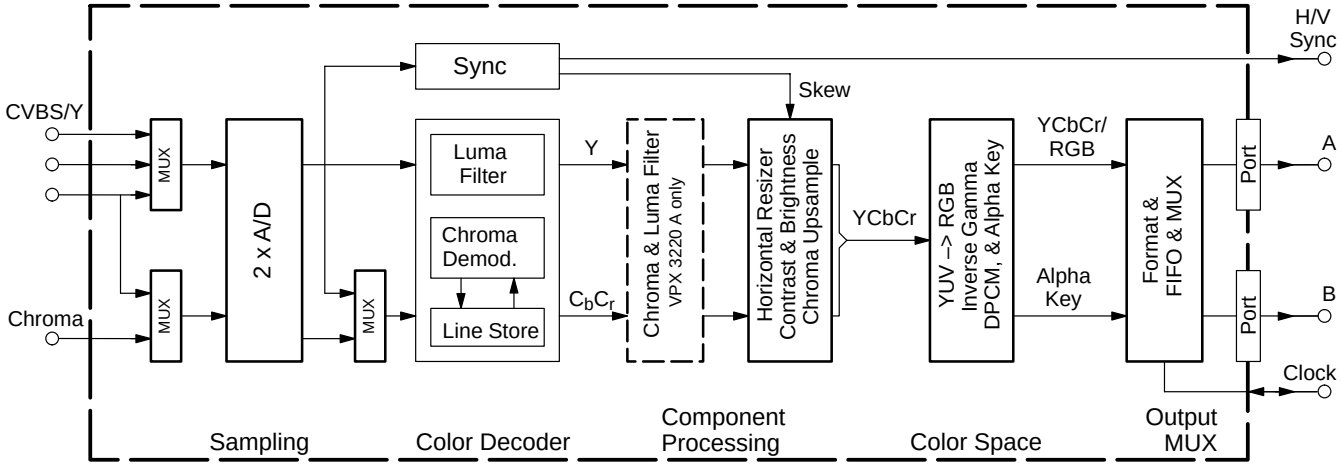


Fig. 1–1: Block diagram of the VPX

2. Functional Description

2.1. Analog Front-End

This block provides the analog interfaces to all video inputs and mainly carries out analog-to digital conversion for the following digital video processing. A block diagram is given in Fig. 2–2.

Most of the functional blocks in the front-end are digitally controlled (clamping, AGC, and clock-DCO). The control loops are closed by the Fast Processor ('FP') embedded in the decoder.

2.1.1. Input Selector

Up to four analog inputs can be connected. They all must be AC-coupled. Two of them (VIN2 and VIN3) are for input of composite video or S-VHS luma signal. These inputs are clamped to the sync back porch and are amplified by a variable gain amplifier. One input (CIN) is for connection of S-VHS carrier-chrominance signal. This input is internally biased and has a fixed gain amplifier. The fourth one (VIN1) can be used for both functions (see Fig. 2–2). For possible combinations and types of input signals, see Fig. 2–1.

CVBS	S-VHS
3	0
2	1
0	2

	CVBS	Luma	Chroma
VIN1	✓	✓	✓
VIN2	✓	✓	
VIN3	✓	✓	
CIN			✓

Fig. 2–1: Combinations and types of input signals

2.1.2. Clamping

The composite video input signals are AC-coupled to the IC. The clamping voltage is stored on the coupling capacitors and is generated by digitally controlled current sources. The clamping level is the back porch of the video signal. S-VHS chroma is also AC-coupled. The input pin is internally biased to the center of the ADC input range.

2.1.3. Automatic Gain Control

A digitally working automatic gain control adjusts the magnitude of the selected baseband by +6/–4.5 dB in 64 logarithmic steps to the optimal range of the ADC.

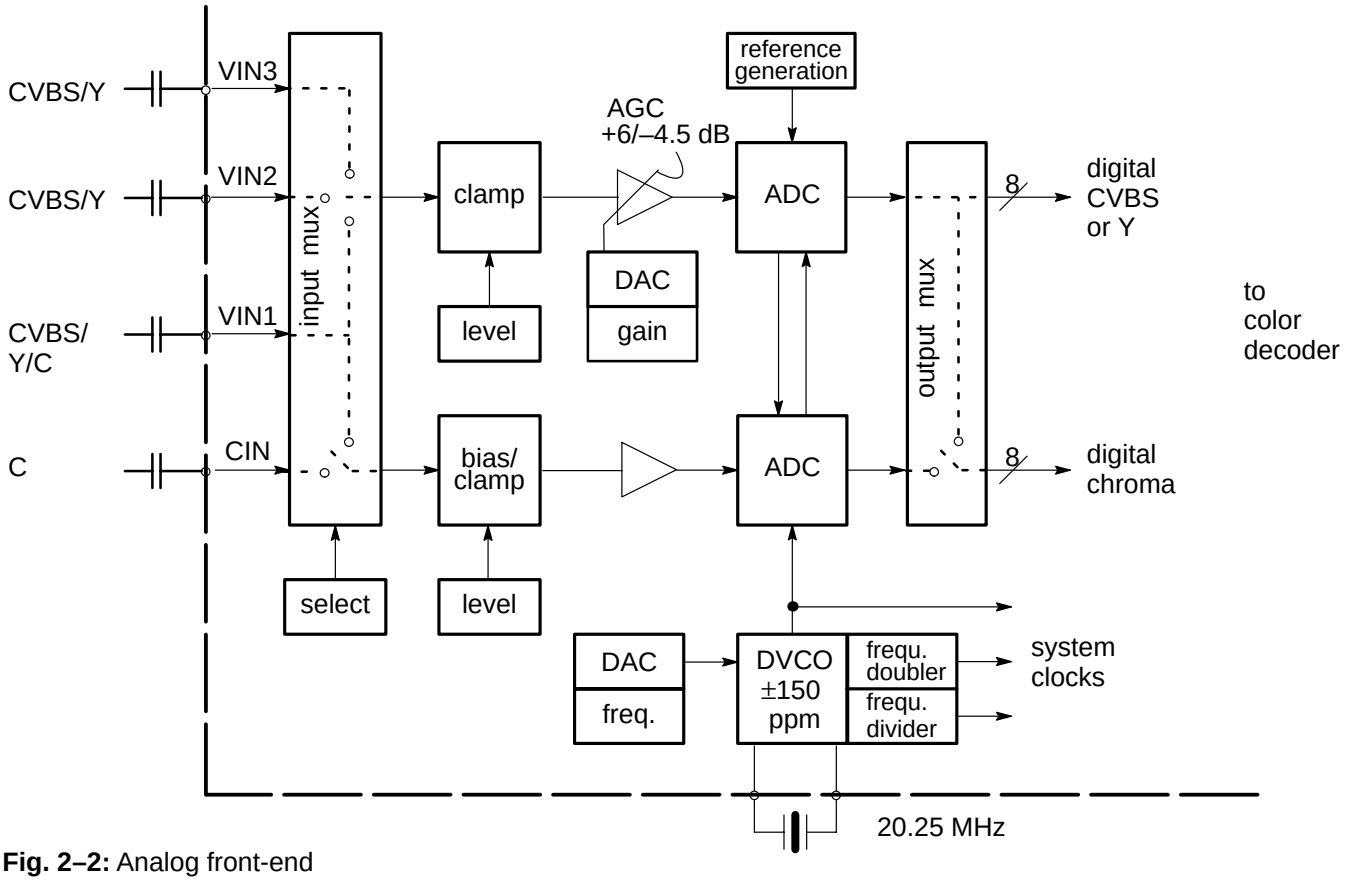


Fig. 2–2: Analog front-end

2.1.4. Digitally Controlled Clock Oscillator

The clock generation is also a part of the analog front-end. The crystal oscillator is controlled digitally by the control processor; the clock frequency can be adjusted within ±150 ppm if the recommended crystal is used.

2.1.5. Analog-to-Digital Converters

Two ADCs are provided to digitize the input signals. Each converter runs with 20.25 MHz and has 8-bit resolution. An integrated bandgap circuit generates the required reference voltages for the converters. The two ADCs are of a 2-stage subranging type.

2.2. Color Decoder

In this block, the entire luma/chroma separation and multistandard color demodulation is carried out. The color demodulation uses an asynchronous clock, thus allowing a unified architecture for all color standards.

Both luma and chroma are processed to an orthogonal sampling raster. Luma and chroma delays are matched. The total delay of the decoder is adjustable by a FIFO memory. Therefore, even when the display processing delay is included, a processing delay of exactly 64 µsec can be achieved.

The color decoder output is YC_rC_b in a 4:2:2 format.

2.2.1. IF-Compensation

With off-air or mistuned reception, any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Three different settings of the IF-compensation are possible:

– flat (no compensation)

– 6 dB/octave

– 12 dB/octave

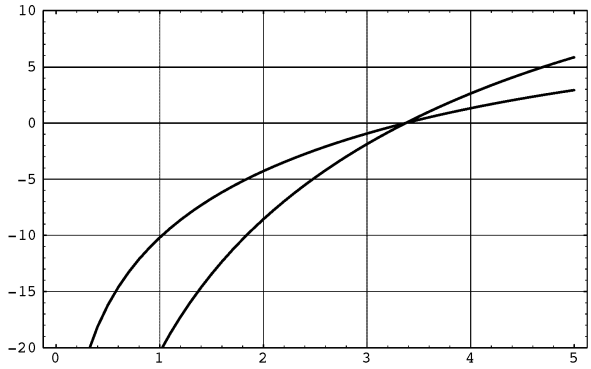


Fig. 2–3: Frequency response of chroma IF-compensation

2.2.2. Demodulator

The entire signal (which might still contain luma) is now quadrature-mixed to the baseband. The mixing frequency is equal to the subcarrier for PAL and NTSC, thus achieving the chroma demodulation. For SECAM, the mixing frequency is 4.286 MHz giving the quadrature baseband components of the FM modulated chroma. After the mixer, a lowpass filter selects the chroma components; a downsampling stage converts the color difference signals to a multiplexed half-rate data stream.

The subcarrier frequency in the demodulator is generated by direct digital synthesis; therefore, substandards such as PAL 3.58 or NTSC 4.43 can also be demodulated.

2.2.3. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with a bell-filter characteristic. At the output of the lowpass filter, all luma information is eliminated.

The lowpass filters are calculated in time multiplex for the two color signals. Three bandwidth settings (narrow, normal, broad) are available for each standard. The filter passband can be shaped with an extra peaking term at 1.25 MHz.

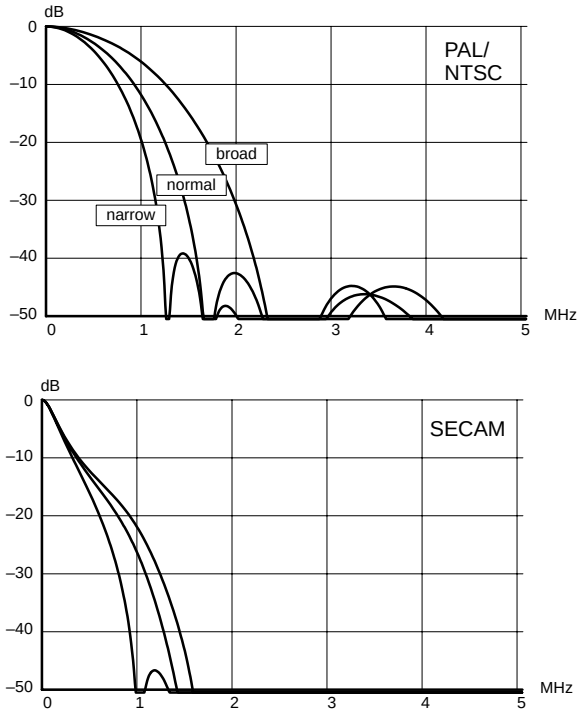


Fig. 2–4: Frequency response of chroma filters

2.2.4. Frequency Demodulator

The frequency demodulator for demodulating the SECAM signal is implemented as a CORDIC-structure. It calculates the phase and magnitude of the quadrature components by coordinate rotation.

The phase output of the CORDIC processor is differentiated to obtain the demodulated frequency. After a programmable deemphasis filter, the Dr and Db signals are scaled to standard C_rC_b amplitudes and fed to the cross-over-switch.

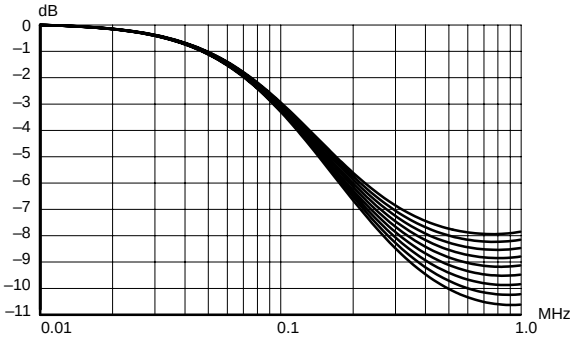


Fig. 2–5: Frequency response of SECAM deemphasis

2.2.5. Burst Detection

In the PAL/NTSC-system, the burst is the reference for the color signal. The phase and magnitude outputs of the CORDIC are gated with the color key and used for controlling the phase-lock-loop (APC) of the demodulator and the automatic color control (ACC) in PAL/NTSC.

The ACC has a control range of +30...–6 dB.

For SECAM decoding, the frequency of the burst is measured. Thus, the current chroma carrier frequency can be identified and is used to control the SECAM processing. The burst measurements also control the color killer operation.

2.2.6. Color Killer Operation

The color killer uses the burst-phase, -frequency measurement to identify a PAL/NTSC or SECAM color signal. For PAL/NTSC, the color is switched off (killed) as long as the color subcarrier PLL is not locked. For SECAM, the killer is controlled by the toggle of the burst frequency. The burst amplitude measurement is used to switch-off the color if the burst amplitude is below a programmable threshold. Thus, color will be killed for very noisy signals. The color amplitude killer has a programmable hysteresis.

2.2.7. Delay Line/Comb Filter

The color decoder uses one fully integrated delay line. Only active video is stored.

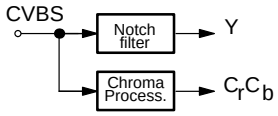
The delay line application depends on the color standard:

– NTSC: combfilter **or** color compensation

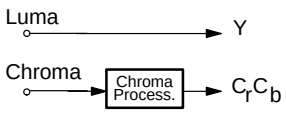
– PAL: color compensation

– SECAM: crossover-switch

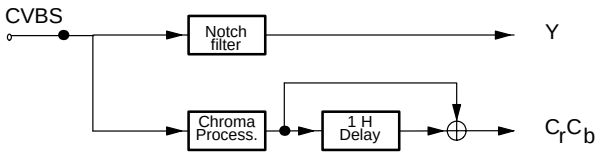
In the NTSC compensated mode, Fig. 2–6 c), the color signal is averaged for two adjacent lines. Therefore, cross-color distortion and chroma noise is reduced. In the NTSC combfilter mode, Fig. 2–6 d), the delay line is in the composite signal path, thus allowing reduction of cross-color components, as well as cross-luminance. The loss of vertical resolution in the luminance channel is compensated by adding the vertical detail signal with removed color information.



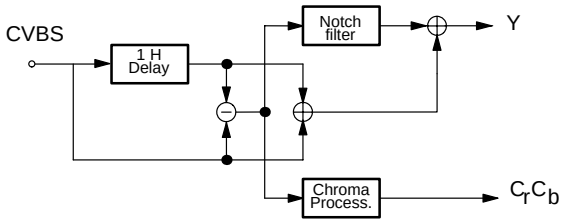
a) conventional



b) S-VHS

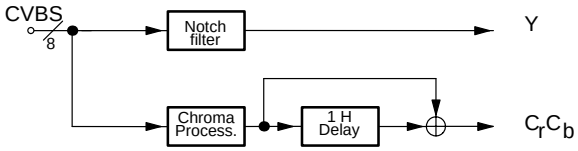


c) compensated

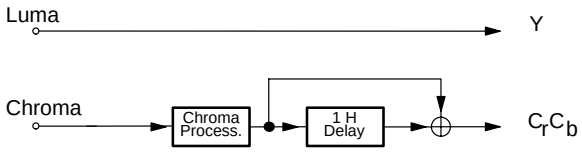


d) Comb Filter

Fig. 2–6: NTSC color decoding options



a) conventional



b) S-VHS

Fig. 2–7: PAL color decoding options

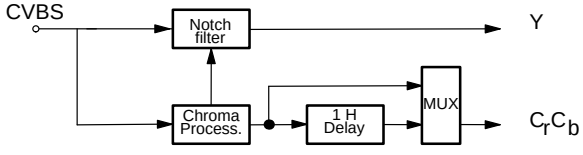
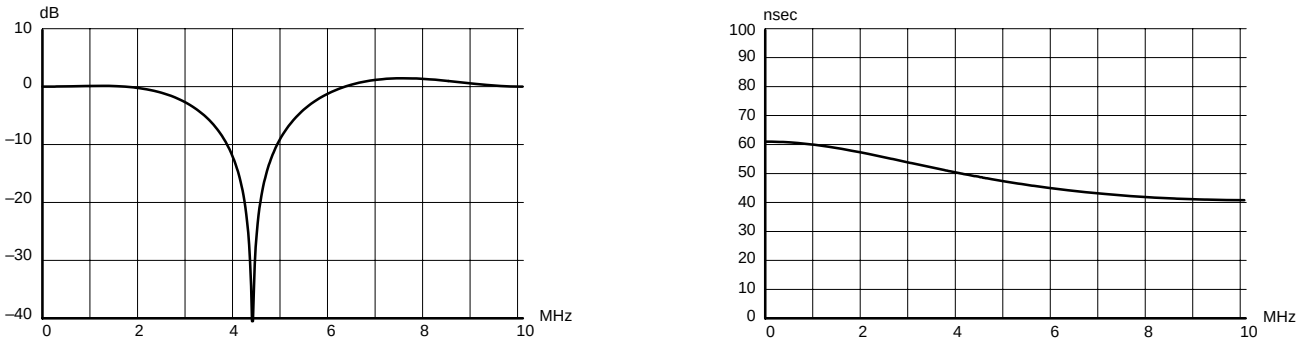


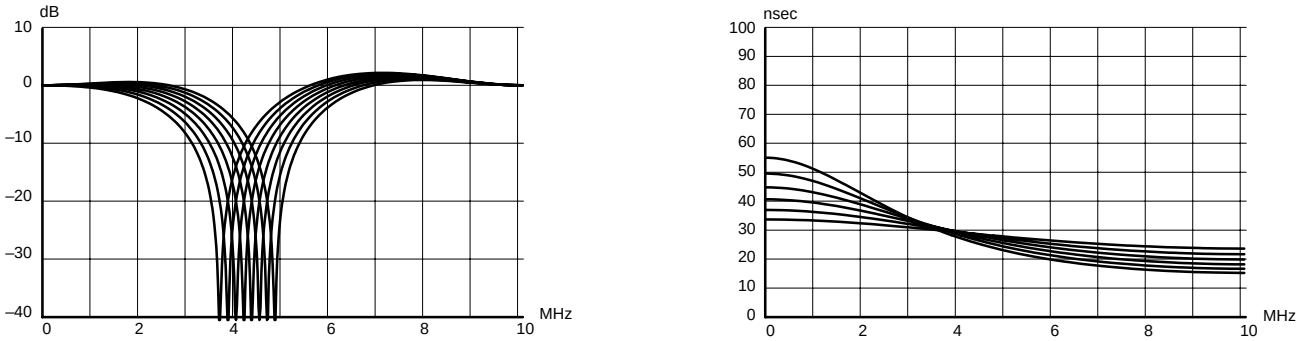
Fig. 2–8: SECAM color decoding

2.2.8. Luminance Notch Filter

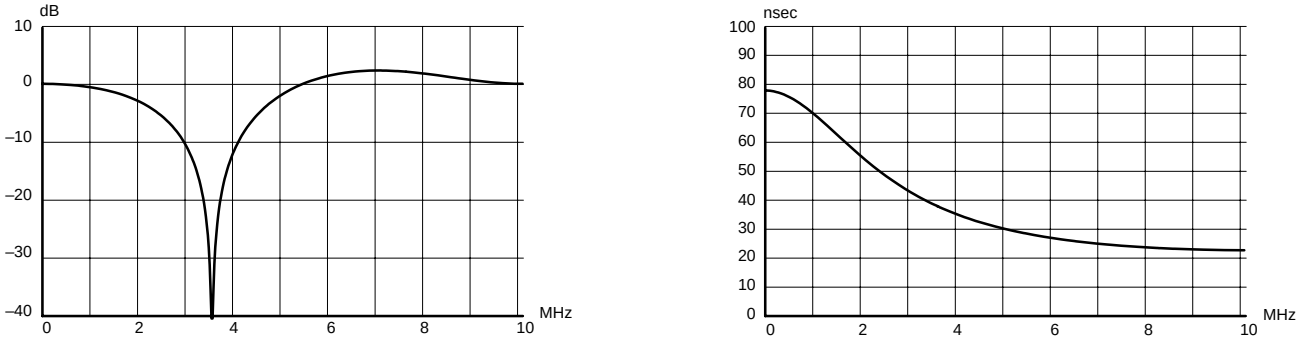
If a composite video signal is applied, the color information is suppressed by a programmable notch filter. The position of the filter center frequency depends on the subcarrier frequency for PAL/NTSC. For SECAM, the notch is directly controlled by the chroma carrier frequency. This considerably reduces the cross-luminance. The frequency responses and the delay characteristics of all three systems are shown below.



PAL notch filter



SECAM notch filter



NTSC notch filter

Fig. 2–9: Frequency responses and time delay characteristics for PAL, SECAM, and NTSC

2.2.9. YCbCr Color Space

The color decoder outputs luminance and two chrominance signals at a sample clock of 20.25 MHz. Active video samples are flagged by a separate reference signal. The number of active samples is 1056 for all standards (525 lines and 625 lines). The representation of the chroma signals is the ITUR-601 digital studio standard.

In the following equations, the RGB signals are already gamma-weighted.

– Y = 0.299*R + 0.587*G + 0.114*B

– (R–Y) = 0.701*R – 0.587*G – 0.114*B

– (B–Y) = –0.299*R – 0.587*G + 0.886*B

In the color decoder, the weighting for both color difference signals is adjusted individually. The default format will have the following specification:

– Y = 224*Y + 16 (pure binary),

– C_r = 224*(0.713*(R–Y)) + 128 (offset binary),

– C_b = 224*(0.564*(B–Y)) + 128 (offset binary).

2.3. Component Processing

Recovery of the YCbCr components by the decoder is followed by horizontal resizing and skew compensation. Contrast enhancement with noise shaping can also be applied to the luminance signal. The CbCr samples are interpolated to create a 4:4:4 format.

Fig. 2–10 illustrates the signal flow through the component processing stage. The YCbCr 4:2:2 samples are separated into a luminance path and a chrominance path. The **Luma Filtering** and **Chroma Filtering** blocks apply FIR lowpass filters with selectable cutoff frequencies. These filters are available only in VPX 3220 A. The **Resize** and **Skew** blocks alter the effective sampling rate and compensate for horizontal line skew. The YCbCr samples are buffered in a FIFO for continuous read out at a fixed clock rate. In the luminance path, the contrast and brightness can be varied and noise shaping applied. In the chrominance path, interpolation is used to generate a 24-bit/pixel output stream (4:4:4 format).

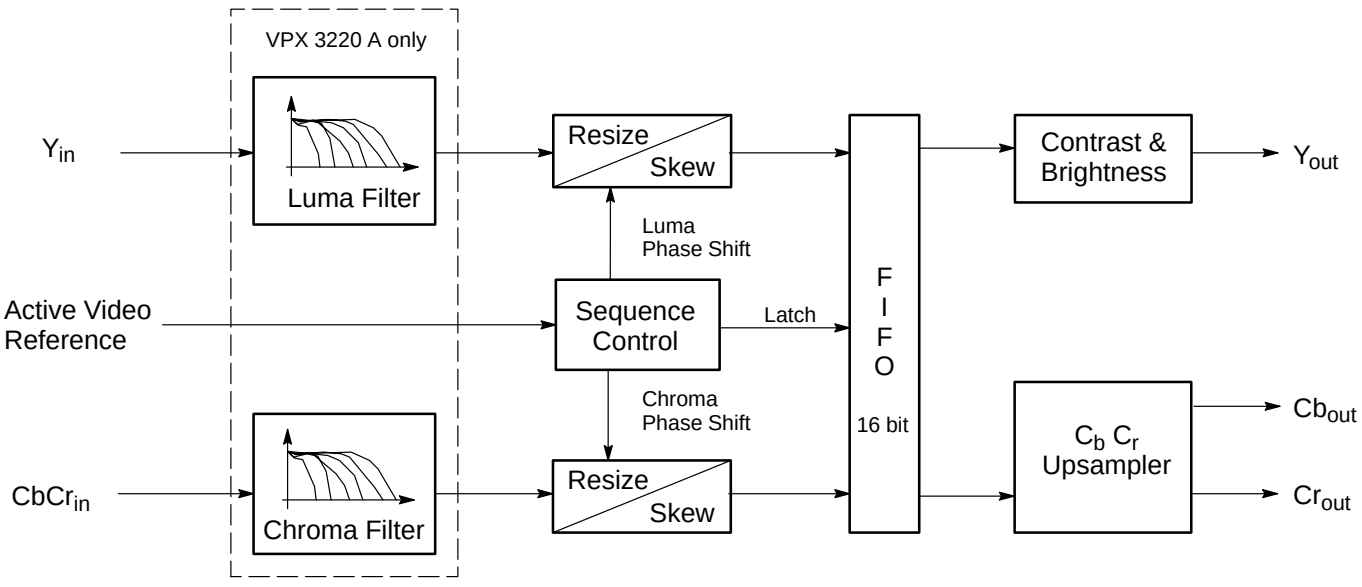


Fig. 2–10: Component processing stage

2.3.1. Horizontal Resizer

The horizontal resizer alters the sampling raster of the video signal, thereby varying the number of pixels in the active portion of the video line. The number of pixels per line is selectable within the range from 1056 to 32 in increments of 2 pixels. In the digital domain, this is done by lowpass filtering (VPX 3220 A only), followed by a programmable phase shift with an allpass filter.

The VPX 3220 A is equipped with a battery of 32 FIR filters to cover the four octave operating range of the resizer. Fig. 2–13 shows the magnitude response of the entire filter set. All filters exhibit a minimum stop band attenuation of at least 35 dB. Figures 2–11 and 2–12 illustrate the performance of the filters in detail.

Filter selection is performed by an internal processor based on the selected resizing factor. This automated selection is optimized for best visual performance but can be fine tuned to satisfy different needs. It is also possible to override the internal selection completely. In that case, filters are selected over I^2C bus.

The **Resize** and **Skew** block performs programmable phase shifting with subpixel accuracy. In the luminance path, a linear interpolation filter provides a phase shift between 0 and 31/32 in steps of 1/32. This corresponds to an accuracy of 1.6 ns. The chrominance signal can be shifted between 0 and 3/4 in steps of 1/4. Figs. 2–14 through 2–17 show the the transfer function of the two skew filters.

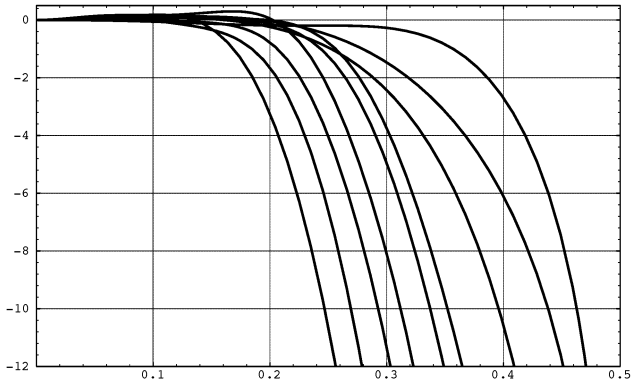


Fig. 2–11: Resizer filters for the upper octave

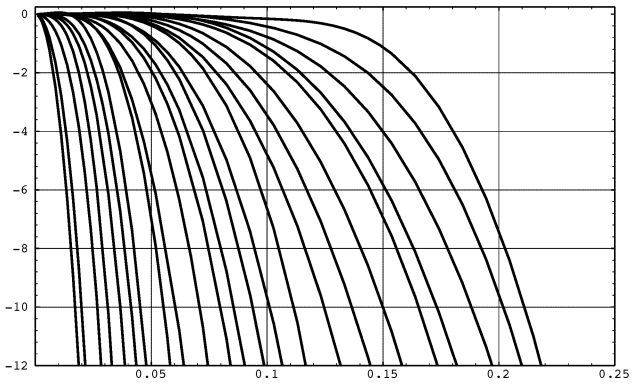


Fig. 2–12: Resizer filters for the lower three octaves

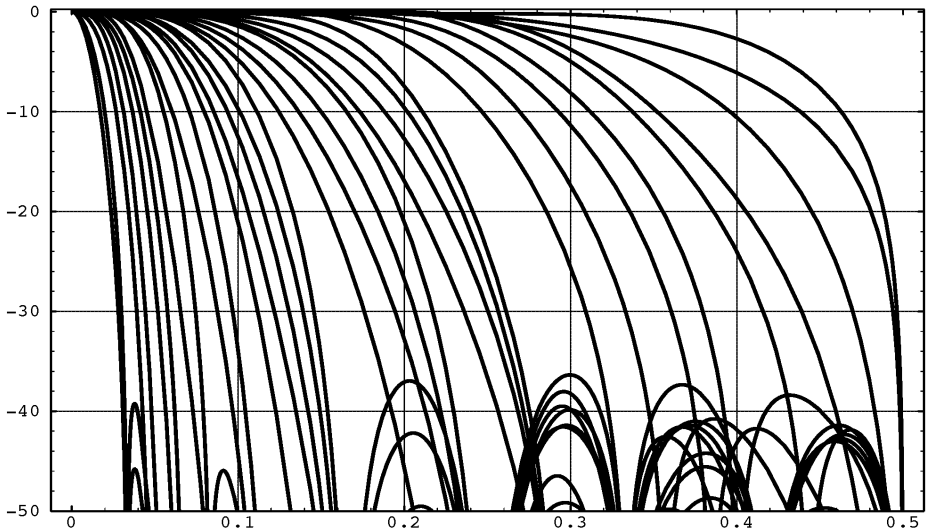


Fig. 2–13: Magnitude response of resizer filter bank (VPX 3220 A only)

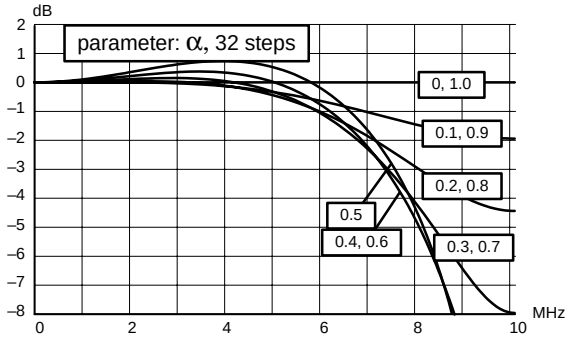


Fig. 2–14: Luminance skew filter magnitude frequency response

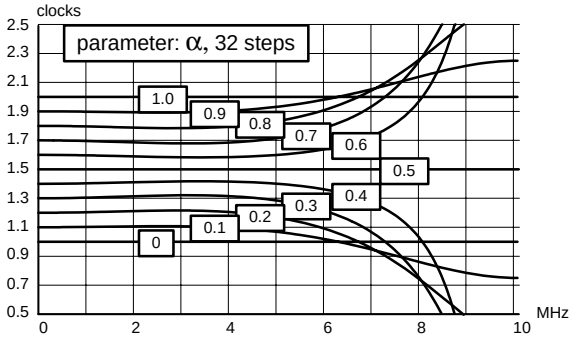


Fig. 2–15: Luminance skew filter group delay characteristics

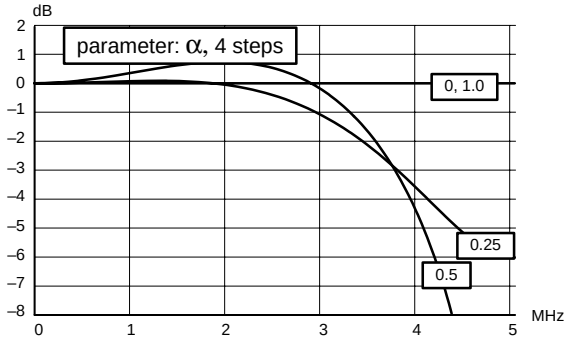


Fig. 2–16: Chrominance skew filter magnitude frequency response

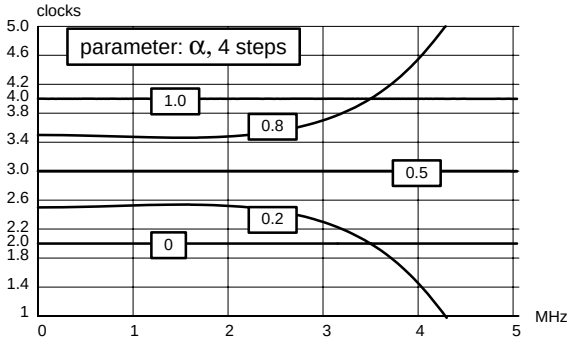


Fig. 2–17: Chrominance skew filter group delay characteristics

2.3.2. Skew Correction

The VPX delivers orthogonal pixels with a fixed clock even in the case of non-broadcast signals with substantial horizontal jitter (VCRs, laser disks, certain portions of the 6 o'clock news...).

This is achieved by highly accurate sync slicing combined with post correction. Immediately after the analog input is sampled, a horizontal sync slicer tracks the position of sync. This slicer evaluates, to within 1.6 ns., the skew between the sync edge and the edge of the pixel-clock. This value is passed as a skew on to the phase shift filter in the resizer. The skew is then treated as a fixed initial offset during the resizing operation.

2.3.3. Contrast, Brightness, and Noise Shaping

$$I_{out} = c * I_{in} + b \qquad \begin{array}{l} c = 0...63/32 \text{ in 64 steps} \\ b = -127...128 \text{ in 256 steps} \end{array}$$

A selectable gain and offset can be applied to the luminance samples. Both the gain and offset factors can be set externally via I^2C serial control. Fig. 2–18 gives a functional description of this circuit. First, a gain is applied, yielding a 10-bit luminance value. The conversion back to 8-bit is done using one of three selectable techniques: simple rounding, 1-bit error diffusion, or 2-bit error diffusion.

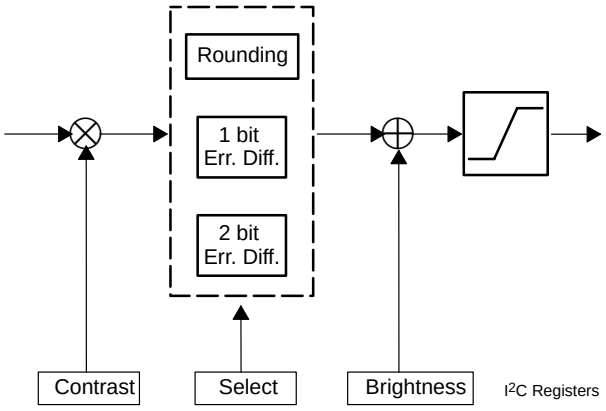


Fig. 2–18: Contrast and brightness adjustment

2.3.4. C_bC_r Upsampler

Simple interpolation is used to convert the 4:2:2 video samples up to the 4:4:4 format. The CbCr samples are upsampled and then band limited with the linear phase FIR kernel. The passband of this filter covers the entire chroma spectrum present in analog composite and S-VHS signals.

2.4. Color Space Stage

The color space stage (Fig. 2–19) of the VPX 3220 A and VPX 3216 B optionally performs a series of conversions in the color space and component format. Generation of an alpha key signal, compression using quantized differential coding, and inverse gamma correction are programmable options.

Beginning with the 24-bit/pixel YCbCr input signal, two other component formats (4:2:2 and 4:1:1) can be generated by simple downsampling of the chroma. Alternatively, the 24-bit YCbCr can be dematrixed to produce 24-bit RGB. The RGB components can either be output directly or further quantized to yield other quantization formats such as 16-bit (R:5 G:6 B:5) or 15-bit (R:5 G:5 B:5) The table below summarizes the supported output signal formats.

Components	Sampling Format	Quantization Format	Bits/ Pixel
YCbCr	4:4:4 4:2:2 4:1:1 4:4:4 (compressed)	8 8 8 8 8 8 8 8 8 8 8 8	24 16 12 8
RGB	4:4:4 4:4:4 4:4:4	8 8 8 5 6 5 5 5 5	24 16 15

2.4.1. Color Space Selection

$$\begin{bmatrix} 1 & 0 & 1.403 \\ 1 & -0.344 & -0.714 \\ 1 & 1.773 & 0 \end{bmatrix} \times \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

An optional dematrix stage converts the YCbCr 4:4:4 data into RGB using the matrix equations specified in the ITUR 601 recommendation (shown above). The saturation control in the color decoder is first selected to produce C_b and C_r, the ITUR studio chrominance norm. In the dematrix computation, the full 8-bit resolution is maintained.

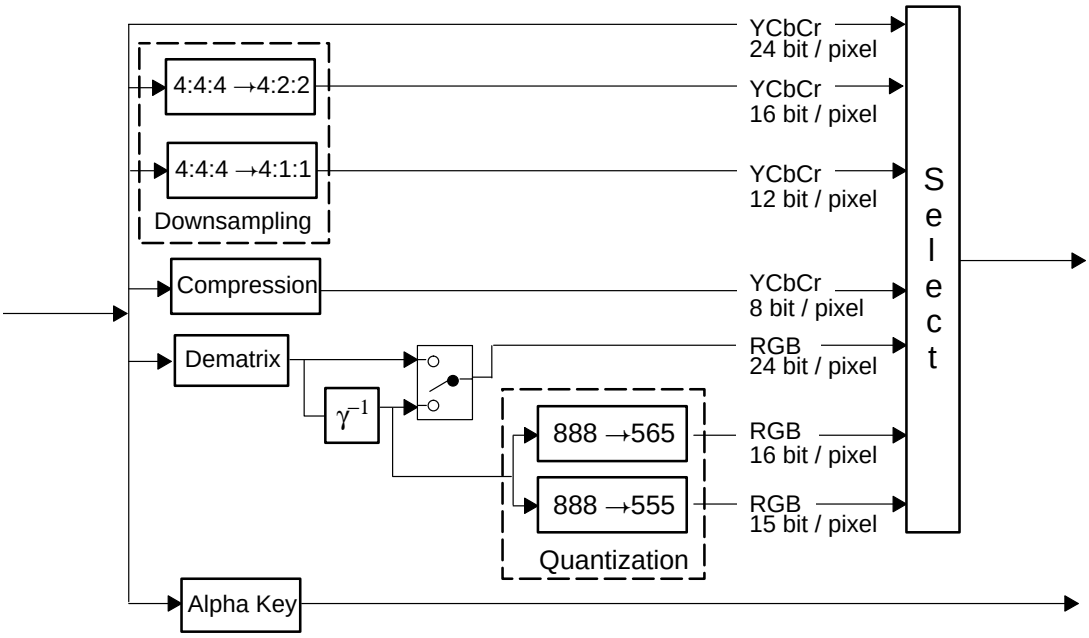


Fig. 2–19: The color space stage

2.4.2. Compression 24 → 8 bits

A variant of the time-honored DPCM coding technique is available to compress the 24-bit YCbCr 4:4:4 signal to an 8-bit per pixel signal. The technique combines differential coding, companding, and adaptive subsampling of the chrominance. For the most natural image material, the resulting bandwidth savings are purchased at a modest loss of amplitude resolution, which appears mostly as high frequency noise. Signals encoded in this form are readable by decoders, which are embedded in commercially available ICs (RAMDACs, back-end analog encoders, etc...).

Different techniques are used to code the luminance and the two chroma signals. For the luma, the difference between 8-bit luma value and a computed reference is companded to a 5-bit value for transmission. The computed reference is simply the 8-bit value of the nearest horizontal neighbor as it appears at the decoder. Each decoded luminance sample is therefore used as a prediction for the next pixel. This, in turn, requires that the encoder contains almost a complete decoder as a subset.

The chrominance samples are encoded in a similar fashion. The samples of each chrominance component are ordered into non-overlapping groups of four. For each group, one of the four samples is selected as a representative value. For each representative pixel, the relative position and companded differential amplitude are computed for transmission. The position data is relative to the beginning of the group and is encoded as a 2-bit word. The difference between the 8-bit value of the sample and the decoded reference value of the previous group is companded to a 5-bit word.

2.4.3. Inverse Gamma Correction

Today, most broadcast video sources anticipate the display on conventional CRTs by predistorting the RGB signals with a gamma function (shown below)

$$I' = cI^{\gamma} + I_0 \qquad \gamma \approx 2.2$$

c, I_0 = constants

$I \in \{R, G, B\}$...linear intensity

However, for video processing in a computer, linear space (no gamma distortion) is often the representation of choice. The VPX provides two options for gamma removal. Both conform to the basic formula:

$$I = I'^{(1/\gamma)}$$

These two γ–1 functions are realized as fixed entries in ROM. The first table compensates for a $\gamma = 1.4$. The second table compensates for a $\gamma = 2.2$.

2.4.4. Alpha Key

A 1-bit threshold select signal can be generated for every pixel in the YCbCr 4:4:4 signal. Using six registers, an upper and a lower threshold is separately defined for each of the Y, C_b, and C_r components. These six register values define a cube in YC_bC_r space. Equality is always included in comparison. For each pixel, an alpha bit is generated, which signals whether the pixel lies inside or outside this cube. A 3-point horizontal median filter is available to mitigate the effects of impulse noise.The alpha signal is fed out through the alpha pin, which is in turn multiplexed with JTAG TDO function (see chapter 5, sections 5.1. and 5.3.). When there is no JTAG activity, the TDO pin is used for the alpha signal. Polarity of this signal (high active or low active) can be programmed using I^2C.

2.4.4.1. Alpha Key as Static Control Signal

The alpha pin can also be used as a static control signal. When doing so, all comparators have to be set to their respective maximal or minimal values.

YMIN = 00 YMAX = FF	UMIN = 80 UMAX = 7F	VMIN = 80 VMAX = 7F

In this case, the alpha signal will always be correct and the output state (high or low) can be selected through the polarity bit (keyinv bit in FORMAT register).

2.5. Output Pixel Format

The output formatting stage (Fig. 2–20) receives the video samples from the color component stage, performs the necessary bit packing, buffers the data for transmission, and channels the output via one or both 8-bit ports. Data transfer can be either synchronous to an internally generated pixel clock or asynchronous with FIFO and status signals.

Format section controls:

– byte formats (bit order)

– number of ports (A only or both A and B)

– clock speed (single or double).

The video samples (and alpha key) arrive from the color component stage at one of two pixel transport rates: 13.5 MHz or 20.25 MHz. This clock rate is selectable via I^{2}C command. However, the use of the 13.5 MHz clock assumes that the resizer is reducing the number of active samples per line to a maximum of 768 pixels.

2.5.1. Output Ports

The two 8-bit ports produce TTL level signals coded in binary offset. The ports can be tristated either via the output enable pin ($\overline{OE}$) or via I^{2}C commands.

2.5.2. Output Port Formats

The format of output data depends on three parameters: the selected signal format, the number of active ports, and the output clock rate. For a given clock rate and number of active ports, a subset of these output formats is supported. Figures 2–21 and 2–22 illustrate this dependency. All single port transfers use port A only.

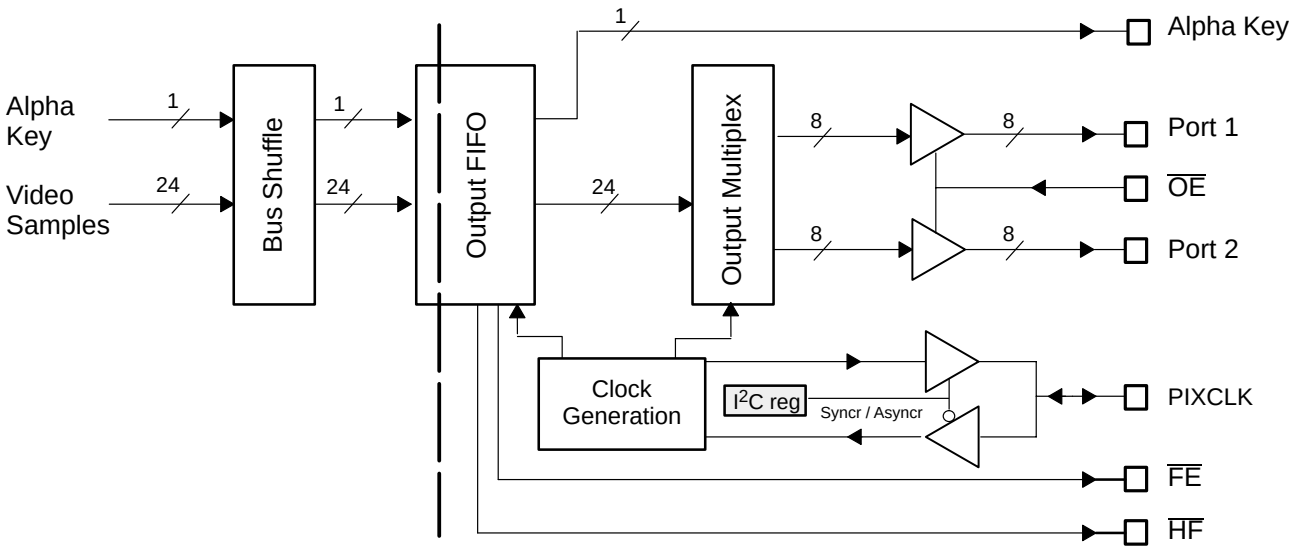
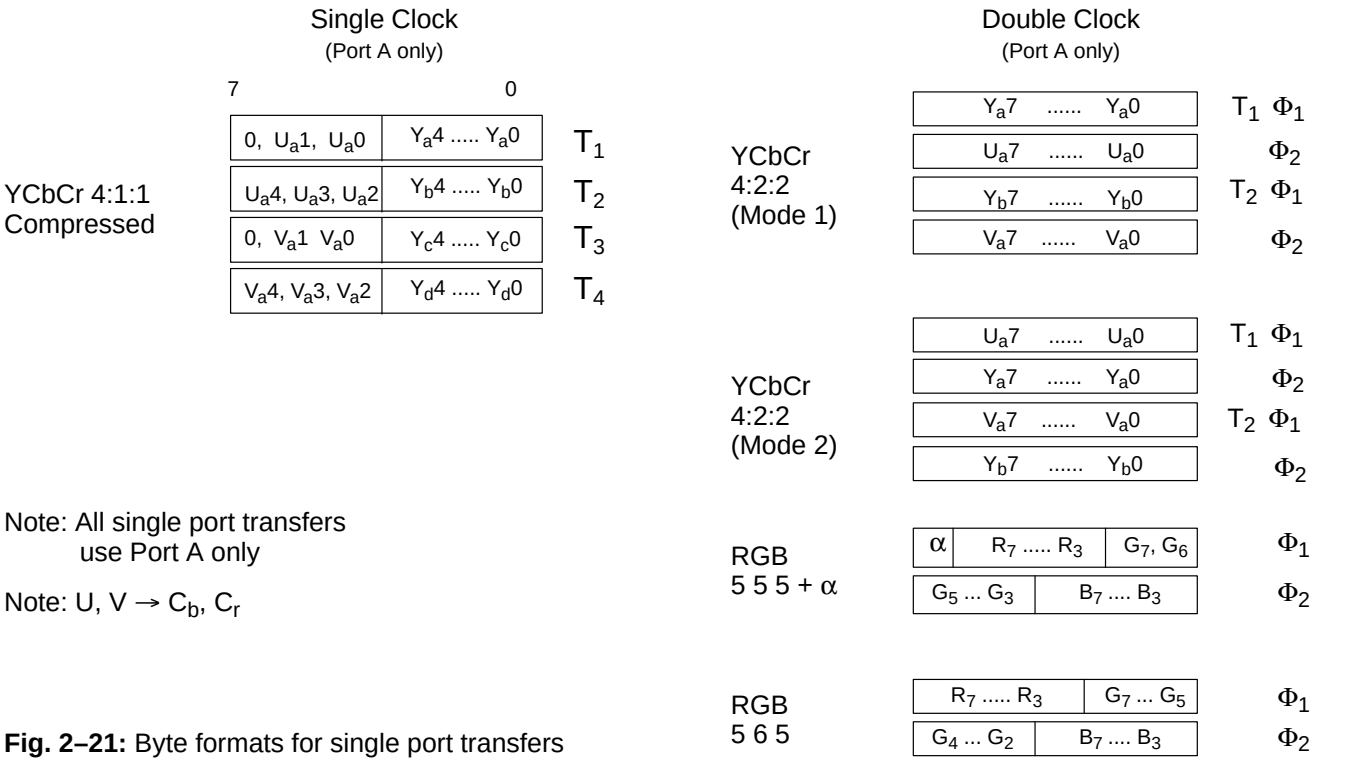


Fig. 2–20: Output formatting stage



Note: All single port transfers use Port A only

Note: U, V → C_b, C_r

Fig. 2–21: Byte formats for single port transfers

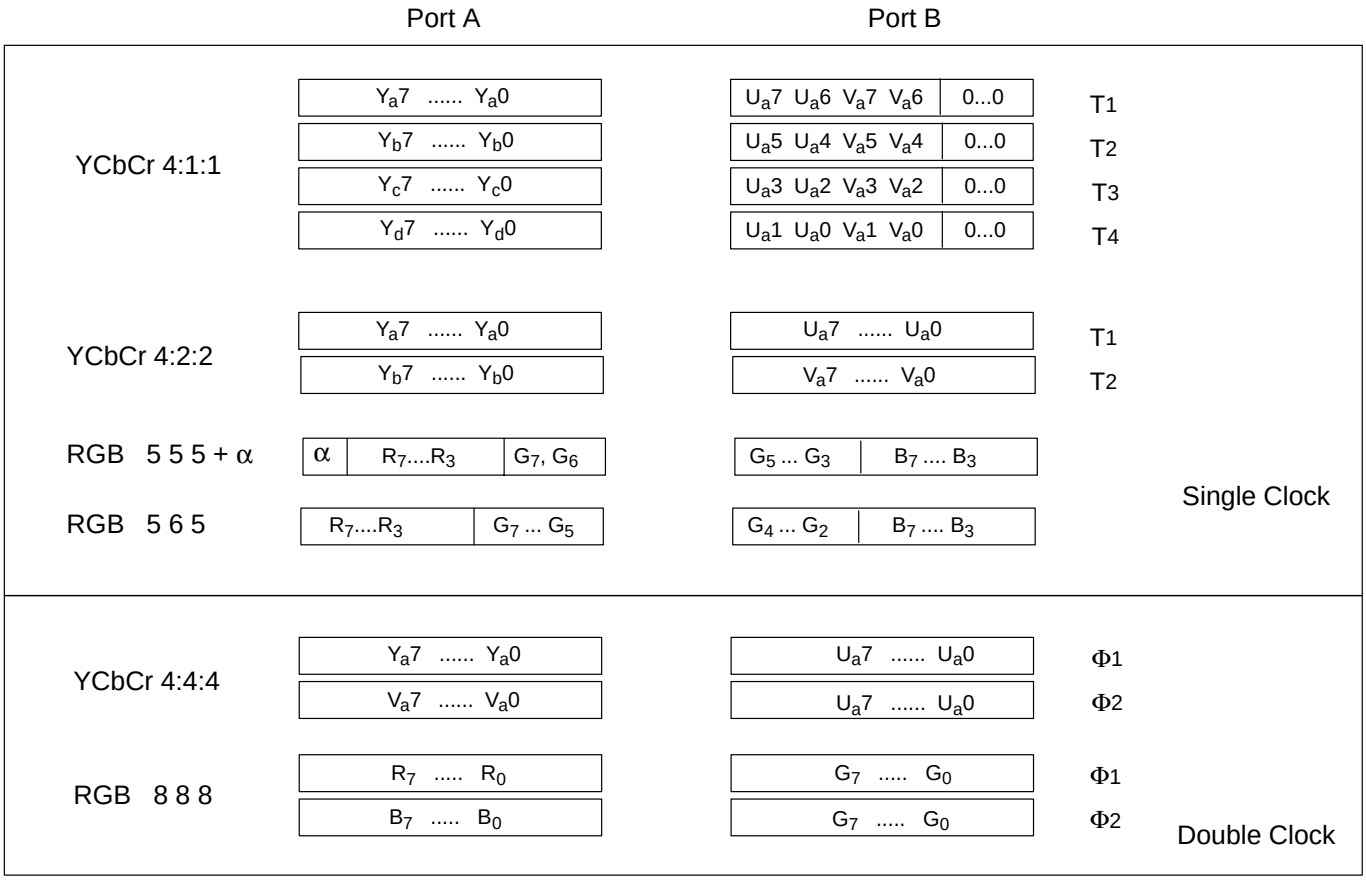


Fig. 2–22: Byte formats for double port transfers

3. Video Timing

3.1. Video Reference Signals HREF and VREF

The VPX generates two video reference signals; a horizontal reference (HREF) and a vertical reference (VREF). These two signals are generated by programmable hardware and can be either free running or synchronous to the analog input video. The video line standard (625/50 or 525/60) can be either inferred from the analog input video or forced via I^2C command from the external controller. The polarity of the two signals is individually selectable.

The circuitry which produces the VREF and HREF signals has been designed to provide a stable, robust set of timing signals, even in the presence of erratic behavior at the analog video input. Depending on the selected operating mode, the period of the HREF and VREF signals are guaranteed to remain within a fixed range. These video reference signals can therefore be used to synchronize the external components of a video subsystem (for example the neighboring ICs of a PC add-in card).

3.1.1. HREF

Fig. 3–1 illustrates the timing of the HREF signal relative to the analog input. The active period of HREF is fixed and is always equal to the length of the active portion of a video signal. Therefore, regardless of the video line standard, HREF is active for 1056 periods of the 20.25 MHz system clock. The total period of the HREF signal is expressed as $\Phi_{nominal}$ and depends on the video line standard.

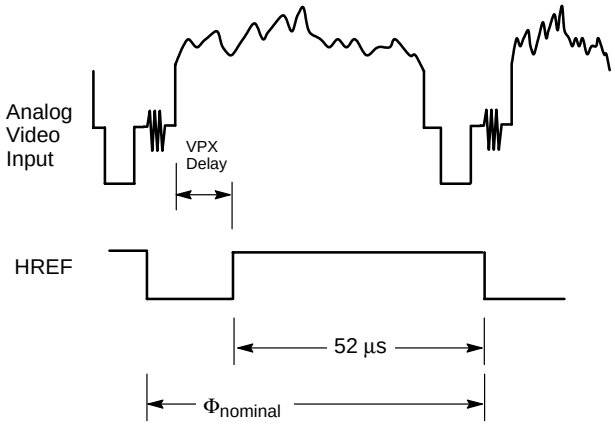


Fig. 3–1: HREF relative to Input Video

3.1.2. VREF

Figs. 3–2 and 3–3 illustrate the timing of the VREF signal relative to field boundaries of the two TV standards. The length of the VREF pulse is programmable in the range between 2 and 9 video lines.

3.1.3. Odd/Even

Information on whether the current field is odd or even, is supplied through the relationship between the edge (either leading or trailing) of VREF and level of HREF. This relationship is fixed and shown in Figs. 3–2 and 3–3. The same information can be supplied to the FIELD/PREF pin. The polarity of the signal is programmable.

3.2. Operational Modes

The relationship between the video timing signals (HREF and VREF) and the analog input video is determined by the selected operational mode. Three such modes are available: the **Open Mode**, the **Forced Mode**, and the **Scan Mode**. These modes are selected via I^2C commands from the external controller.

3.2.1. Open Mode

In the Open Mode, both the HREF and the VREF signal track the analog video input. In the case of a change in the line standard (i.e. switching between the video input ports), HREF and VREF automatically synchronize to the new input. When no video is present, both HREF and VREF float to the idling frequency of their respective PLLs. During changes in the video input (drop-out, switching between inputs), the performance of the HREF and VREF signals is not guaranteed.

3.2.2. Forced Mode

In the Forced Mode**,** VREF and HREF follow the input video signal within certain tolerances. Dedicated hardware is used to monitor the frequency of the analog timing. At the moment when the video signal exceeds the allowed timing tolerances, generation of the timing signals is taken over by free running hardware. If the input video is still present, the VPX continually attempts to resynchronize to it.

For each of the two video line standards (625/50 and 525/60), there exist normative values for the period of both the HREF and VREF signals. Many analog input signals deviate significantly from these norms (example, consumer VCRs in their shuttle modes). In the Forced Mode, monitoring hardware is used to impose an upper boundary on the deviation. The maximum allowed horizontal deviation is ± 24 µs. The upper boundary for vertical deviation is $\pm 11\%$ of the number of lines in the selected line standard (625/50: ± 35 lines, 525/60: ± 30 lines)

During the free-running operation, video output data is suppressed. If the VPX successfully resynchronizes, video output resumes. The specific method used to suppress the output video depends on the transfer mode (synchronous or asynchronous).

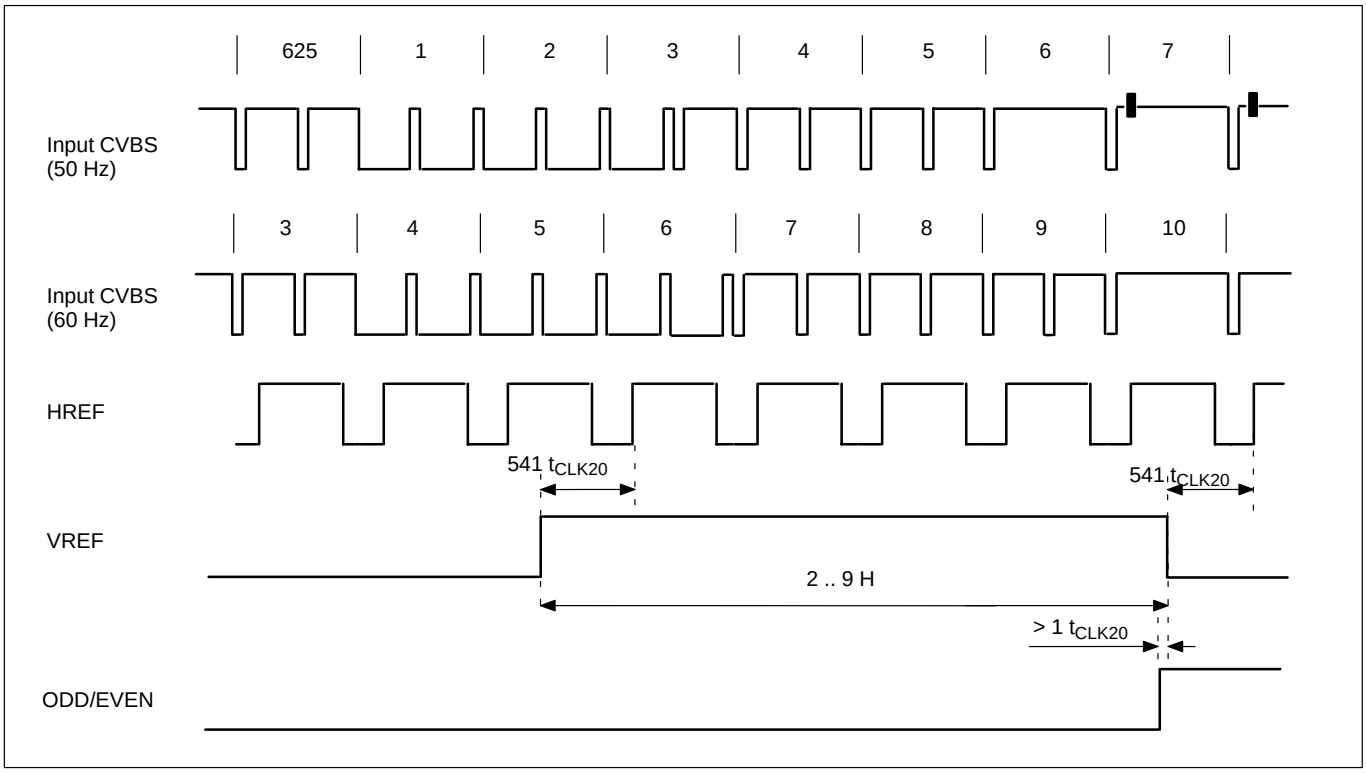


Fig. 3–2: VREF timing for ODD fields

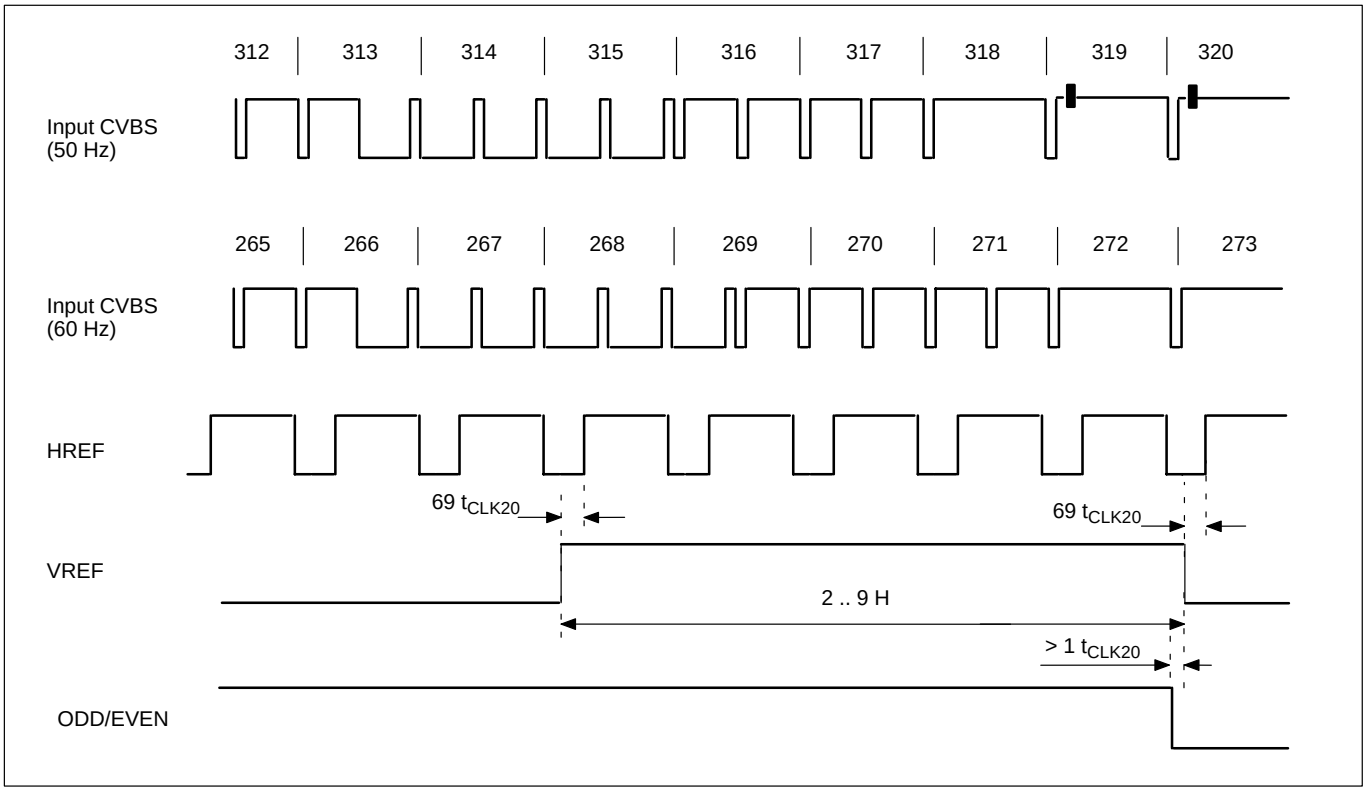


Fig. 3–3: VREF timing for EVEN fields

3.2.3. Scan Mode

In the Scan Mode, the HREF and VREF signals are always generated by free running hardware. They are therefore completely decoupled from the analog input. The output video data is always suppressed.

The purpose of the Scan Mode is to allow the external controller to freely switch between the analog inputs while searching for the presence of a video signal. Information regarding the video (standard, source, etc...) can be queried via I^2C read.

In the Scan Mode, the video line standard of the VREF and HREF signals can be changed via I^2C command. The transition always occurs at the first frame boundary after the I^2C command is received. Fig. 3–4, below, demonstrates the behavior of the VREF signal during the transition from the 525/60 system to the 625/50 system (the width of the vertical reference pulse is exaggerated for illustration).

3.2.4. Transition Behavior

During normal operation, the timing characteristics of the input video can change in response to a number of phenomena: power up/reset, unplugging of the video jack, switching between selected video inputs, etc... The effect of these changes on the video timing signals is dependent on the current operational mode. Table 3–1 summarizes this dependency.

In the Forced Mode, it can often occur that the VPX must resynchronize to an analog input signal after a period in free running sync generation. In such a case, it is likely that the internal sync generators are out of phase with the time base of the analog input. Maintaining a stable sync signal requires that the transition between time bases occur over several field periods.

Fig. 3–5 illustrates the transition between an internal free running vertical sync and a vertical sync of the analog input. The top two lines in this figure show the vertical time base of the analog input signal relative to that of the VREF generated from the free running clock. Both the analog input and free running syncs conform to the same line standard, but the field polarities are out of phase and the offset between field syncs (given by Φ_{error}) is greater than the allowed 20 lines.

In the Forced Mode, vertical resynchronization takes place on field boundaries (as opposed to frame boundaries) and begins immediately after the appearance of the analog input. In the first field after the appearance of this analog video, the period between VREF pulse is shortened by 20 lines ($\Phi_{rec-)}$ and the field polarity of the VREF is repeated. For each subsequent field, the phase error is reduced by Φ_{rec-} until the two signals are again in phase.

Because the resynchronization occurs on field boundaries and because the internally generated sync can be either lengthened or shortened, the maximum value of Φ_{error} is $313/2 \approx 157$ lines. With a maximum correction of 20 lines per field, field locking requires a maximum of 8 fields.

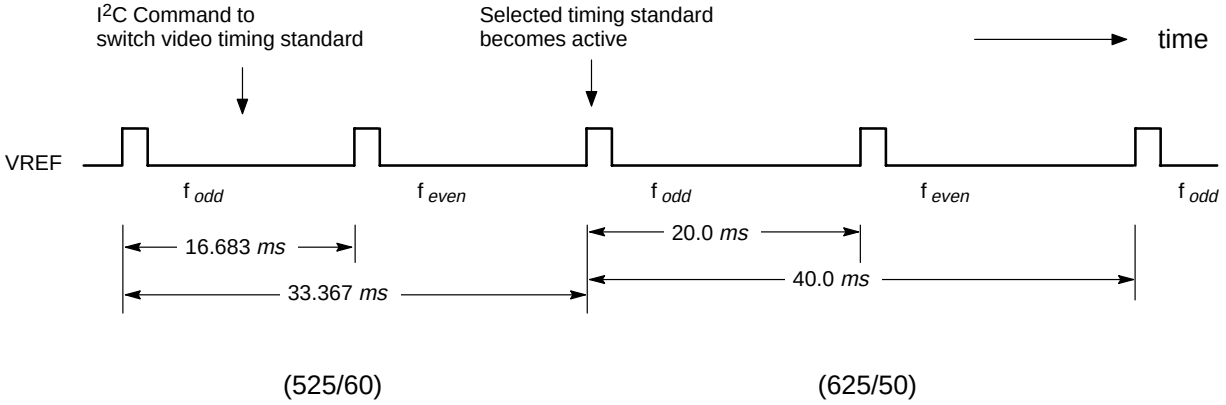


Fig. 3–4: Transition between timing standards

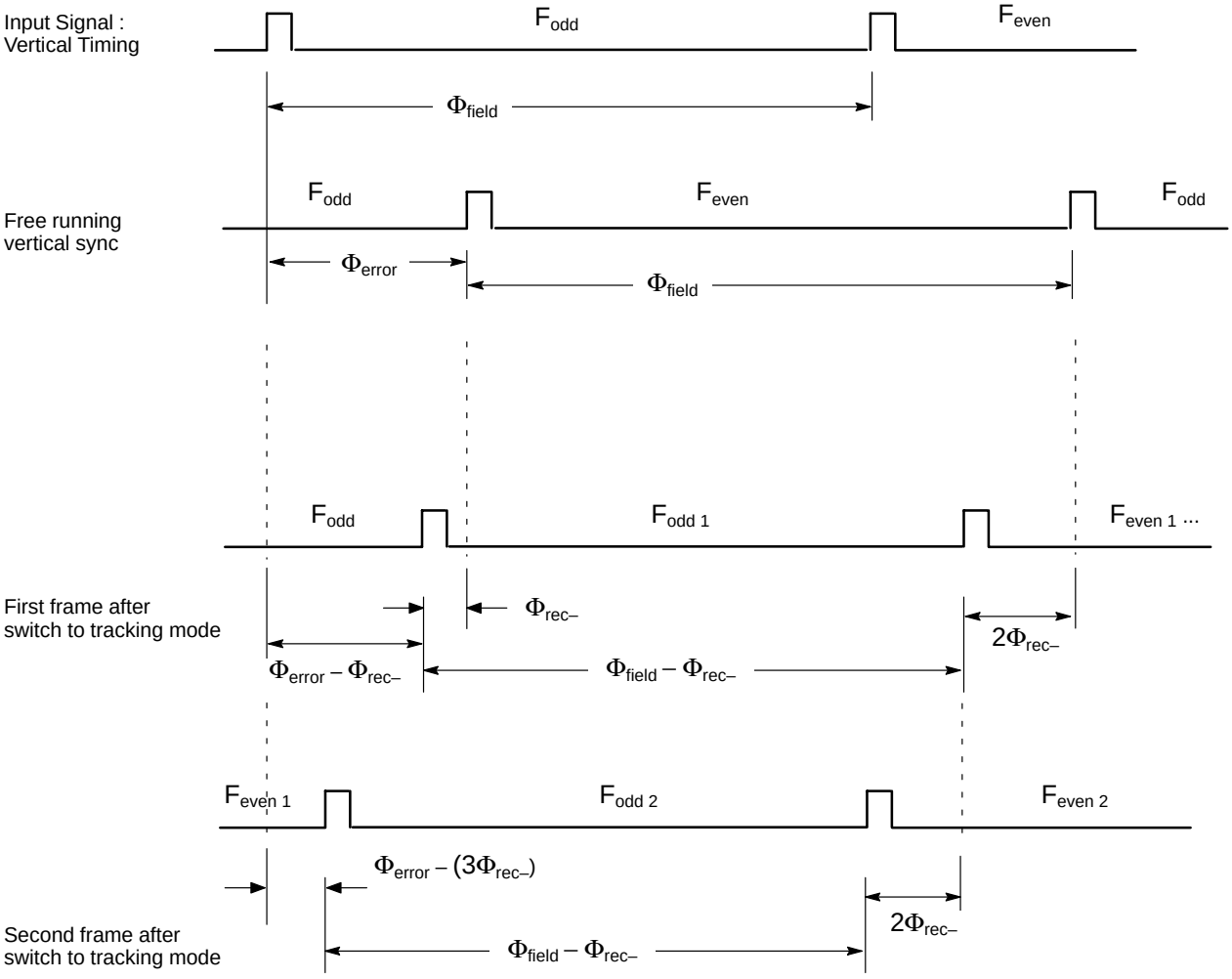


Fig. 3–5: Synchronization to analog input

Table 3–1: Transition Behavior as a Function of Operating Mode

Transition Behavior as a Function of Operating Mode		
Transition	**Mode**	**Behavior**
Power up / Reset	Forced	VREF, HREF: comes up free running (video timing standard read from internal initialization tables) Output ports: suppressed
	Open, Scan	not applicable
video → no video	Open	VREF, HREF: floats to steady state frequency of internal PLL Output ports: still enabled but with undefined data.
	Forced	VREF, HREF: switches immediately to free running Output ports: suppressed until video restored.
	Scan	no visible effect on any data or control signals – timing signals continue unchanged in free running mode, – data ports remain suppressed
no video → video	Open	VREF, HREF: track the input signal
	Forced	No change in timing standard: VREF, HREF: slowly resynchronize. When resynchronization is complete, the timing control switches back from free running to monitored tracking Output ports: re-enabled. Change in the timing standard: – no visible effect on any data or control signals
	Scan	VREF, HREF: no change, continues in free running mode Output ports: remain suppressed.
video → video (same timing standard)	Open	VREF, HREF: track the input video immediately Output Ports: Data available immediately after color decoder locks to input.
	Forced	VREF, HREF: brief period in free running mode while the timing is resynchronized Output Ports: suppressed during resynchronization.
	Scan	no outwardly visible effect on any data or control signals. – timing signals continue unchanged in free running mode, – data ports remain disabled.
video → video (different timing standard)	Open	same as above
	Forced	VREF, HREF: switches immediately to free running Output ports: suppressed
	Scan	same as the case no video → video

3.3. Windowing the Video Field

For each input video field, two non-overlapping windows can be defined. The dimensions of these two windows are supplied via I^2C commands. The presence of two windows allows separate processing parameters such as filter responses and the number of pixels per line to be selected.

External control over the dimensions of the windows is performed by I^2C writes to a window definition table (WinDefTab). For each window, a corresponding WinDefTab is defined in a table of I^2C registers. Data written to these tables does not become active until the the corresponding latch bit is set in a control register. A 2-bit flag specifies the field polarity over which the window is active.

Vertically, as can be seen in Fig. 3–6, each window is defined by a beginning line, a number of lines to be read-in, and a number of lines to be output. Each of these values is specified in units of video lines.

The option, to separately specify the number of input lines and the number of output lines, enables vertical compression. In the VPX, vertical compression is performed via simple line dropping. A nearest neighbor algorithm selects the subset of the lines for output. The presence of a valid line is signaled by a reference signal. The specific signal which is used for the blanking depends on the transfer mode (synchronous/asynchronous).

The numbering of the lines in a field of interlace video is dependent on the line standard. Figs. 3–7 and 3–8 illustrate the mapping of the window dimensions to the actual video lines. The indices on the left are the line numbers relative to the beginning of the frame. The indices on the right show the numbering used by the VPX. As seen here, the vertical boundaries of windows are defined relative to the field boundary. Spatially, the lines from field #1 are displayed above identically numbered from field #2. For example: On an interlace monitor, line #23 from field #1 is displayed directly above line #23 from field #2. There are a few restrictions to the vertical definition of the windows. Windows must not overlap vertically, but can be adjacent. Windows must begin after line #6 (i.e. line #7 is the first one allowed) of their respective fields. The number of lines out cannot be greater than the number of lines in (no vertical zooming). The combined height of the two windows cannot exceed the number of lines in the input field.

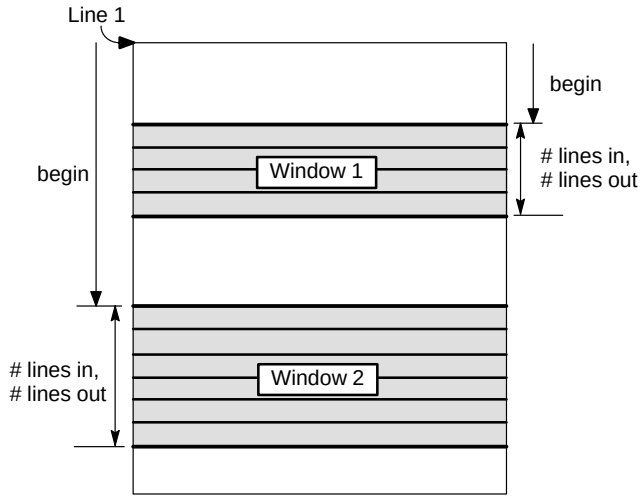


Fig. 3–6: Vertical dimensions of windows

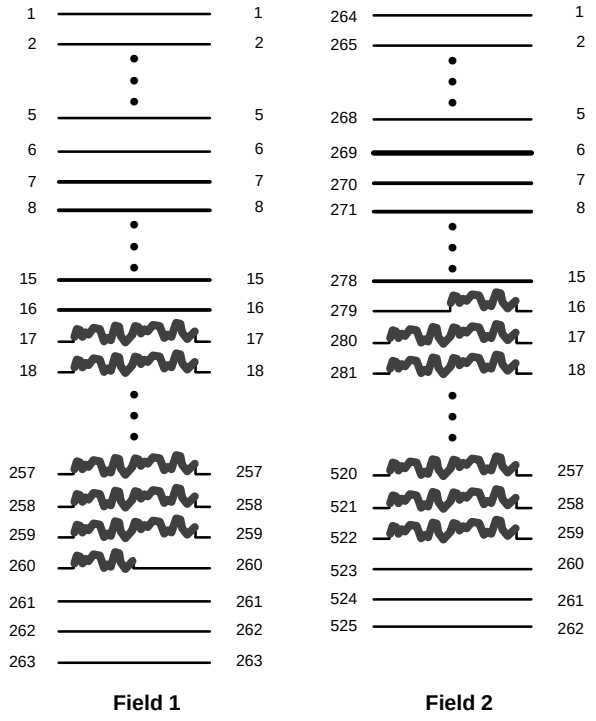


Fig. 3–7: Mapping for 525/60 line systems

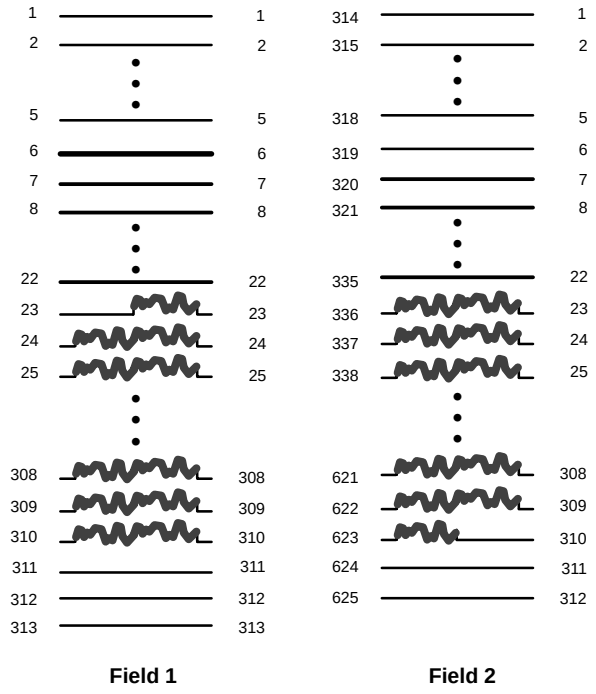


Fig. 3–8: Mapping for 625/50 line systems

Horizontally, the windows are defined by a starting point and a length. The starting point and the length are both given relative to the number of pixels in the active portion of the line (Fig. 3–9).

There are some restrictions in the horizontal window definition. The total number of active pixels (NPixel) must be an even number. The maximum value for NPixel depends on the selected transport clock. For a 20.25 MHz transport clock, the maximum value for NPixel is 1056. For a 13.5 MHz transport clock, the maximum value is 800. HLength should also be an even number. Obviously, the sum of HBegin and HLength may not be greater than NPixel.

Window boundaries are defined by writing the dimensions into the associated WinDefTab and then setting the corresponding latch bit in the control word. Window definition data is latched at the beginning of the next video frame. Once the WinDefTab data has been latched, the latch bit in the control word is reset. By polling the info-word, the external controller can know when the window boundary data has been read. Multiple window definitions within a single frame time are ignored and can lead to error.

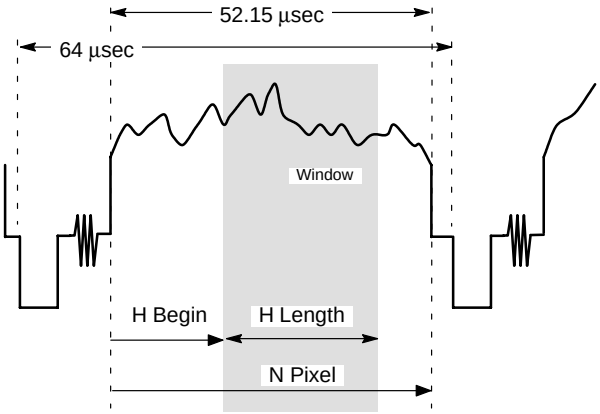


Fig. 3–9: Horizontal Dimensions of Sampling Window

3.4. Video Data Transfer

The VPX supports two methods of transfer for the sampled video data: a synchronous mode and an asynchronous mode. Both modes support all the byte formats shown in Figs. 2–21 and 2–22, as well as both alternative transport rates.

In both modes, data arrives at the output FIFO in an uninterrupted burst with a fixed transport rate. The transport rate is selected by the external controller to be either 13.5 MHz or 20.25 MHz. The duration of the burst is measured in clock periods of the transport clock and is equal to the number of pixels per output line.

The control signals on the three pins: PIXCLK, $\overline{FE}$/VACT, and $\overline{HF}$/FSY, LLC regulate the data transfer. Their function is dependent on the transfer mode (sync., or async.). For the synchronous mode, the signals at these pins are PIXCLK (internal), VACT, and LLC (respectively). For the asynchronous mode, the signals at these pins are PIXCLK (external), $\overline{FE}$, and $\overline{HF}$.

3.4.1. Synchronous Output

In the synchronous transfer mode, data is transferred synchronous to an internally generated PIXCLK. The frequency of the PIXCLK is equal to the selected transport rate. In the single clock mode, data can be latched onto the falling edge of PIXCLK. In double clock mode, output data must be latched onto both clock edges. The double clock mode is supported for the 13.5 MHz transport rate only. The available transfer bandwidths at the ports are therefore 13.5 MHz, 20.25 MHz (single clock), and 27.0 MHz (double clock).

The video data is output in a continuous stream. The PIXCLK is free running. The VACT signal flags the presence of valid output data. Fig. 3–10 illustrates the relationship between the video port data, VACT, and PIXCLK. Whenever a line of video data should be suppressed (line dropping, switching between analog inputs), it is done by suppression of the VACT signal.

Fig. 3–11 illustrates the temporal relationship between the VACT and the HREF signals as a function of the number of pixels per output line and the horizontal dimensions of the window. The duration of the active period of the HREF (Fig. 3–11**,** points B, D) is fixed. Table 3–2 lists the positions of the VACT edges (points A, C) relative to those of HREF.

The LLC signal is provided as an additional support for the 13.5 MHz single clock mode. The LLC provides a 2x PIXCLK signal (27 MHz) for interface to external components which rely on the Philips transfer protocols. In the single clock 13.5 MHz mode, the pixel data can be latched onto alternate rising edges of the LLC.

Table 3–2: Relationship of the HREF to the VACT in synchronous transfer mode

Resizing	Windowing	Timing of rising edges	Timing of falling edges
20.25 MHz Transport Rate			
npix/line = 1056	none	A = B	C = D
npix/line < 1056		A > B	C = D
npix/line ≤ 1056	Window begin > 0	A > B	
	Window end < 1055		C < D
13.5 MHz Transport Rate			
npix/line = 704	none	A = B	C = D
704 < npix/line ≤768		A = B	C > D
npix/line < 704		A > B	C = D
npix/line ≤ 704	Window begin > 0	A > B	
	Window end < 1055		C < D

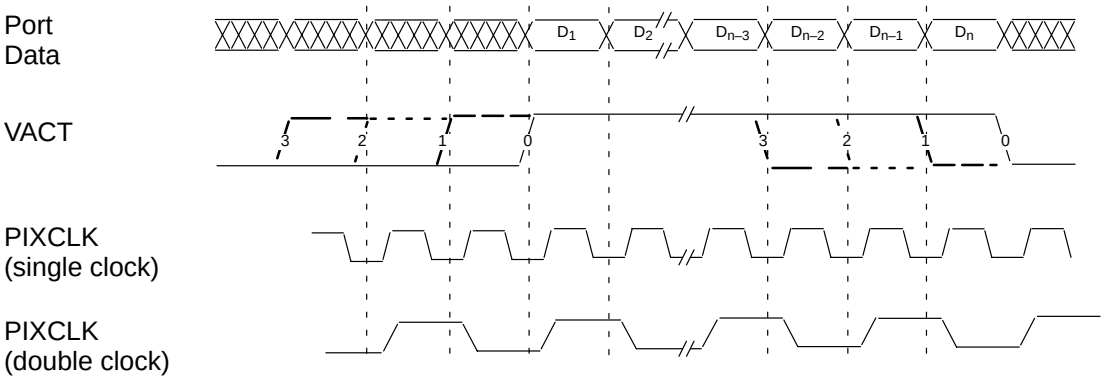


Fig. 3–10: Timing for synchronous output

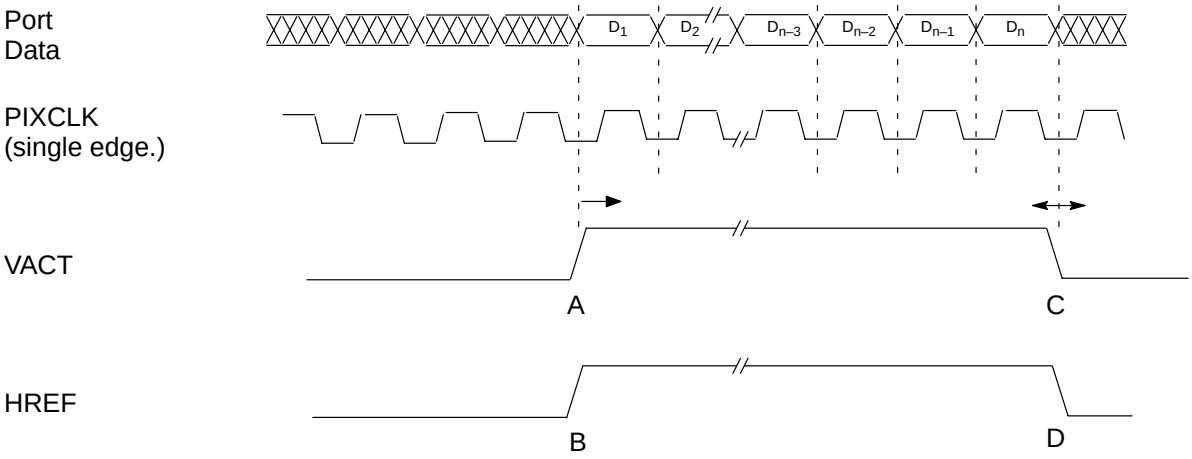


Fig. 3–11: Relation between HREF and VACT signals

3.4.2. Asynchronous Output

In the asynchronous mode, data is strobed from the VPX by an external clock supplied to the PIXCLK pin. A 32-pixel FIFO buffers the video samples for transfer. Two FIFO status signals ($\overline{HF}$ and $\overline{FE}$) arbitrate the transfer. The 'half full' signal ($\overline{HF}$) indicates that the number of samples present in the FIFO has exceeded some programmable threshold (defined over the range of 0→31). The $\overline{FE}$ signal indicates that the FIFO is empty.

Some implementations of the asynchronous mode require a more detailed understanding of the rates at which the data is written to and read from the 32 pixel output FIFO. On the input side of the FIFO, sampled video data from the VPX-core arrives as a continuous burst with a pixel rate equal to that of the transport clock (20 MHz or 13 MHz burst rate).

On the output side, the rate at which the FIFO is emptied is dependent on the speed of the PIXCLK and the selected clocking mode. In the asynchronous mode, the PIXCLK is always a single-edge clock.

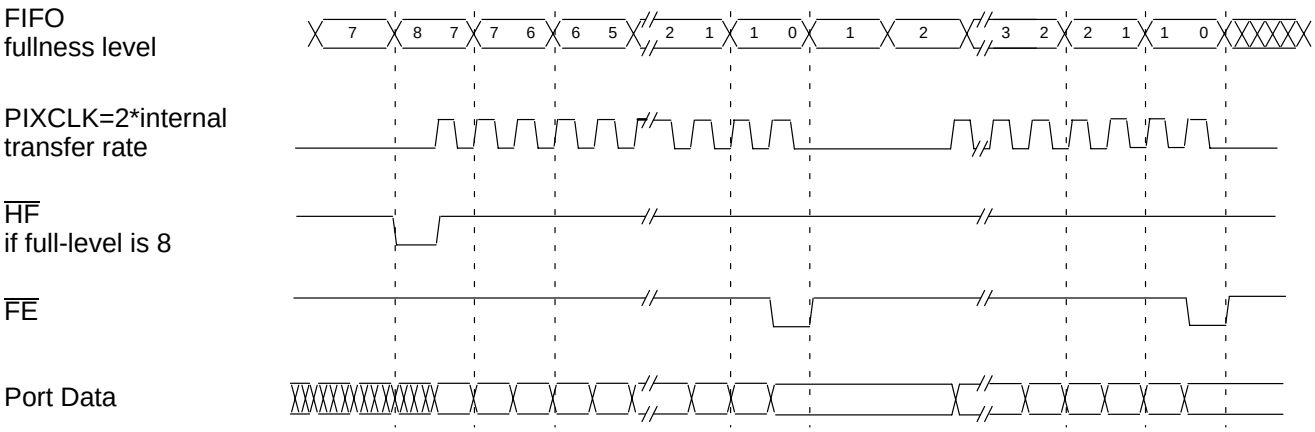


Fig. 3–12: Timing for Asynchronous Output

4. Serial Interface A

4.1. Overview

Communication between the VPX and the external controller is performed serially via the I²C-bus (pins SCL and SDA).

There are basically two classes of registers in the VPX. The first class of registers are the directly addressable I²C registers. These are registers embedded directly in the hardware. Data written to these registers is interpreted combinatorially directly by the hardware (as in any register driven state machine). These registers are all a maximum of 8 bits wide.

The second class of registers are the 'FP RAM registers': the RAM memory of the on-board microcontroller (INTERMETALL's Fast Processor). Data written into this class of registers is read and interpreted by the FP's micro-code. Internally, these registers are 12 bits wide. Communications with these registers requires I²C packets with 16-bit data payloads.

Communication with both classes of registers (I²C and FP RAM) is performed via I²C. But the format of the I²C telegram depends on which type of register is being addressed.

4.2. I²C-Bus Interface

The VPX has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required. The I²C-bus interface uses one level of subaddressing. First, the bus address selects the IC, then a subaddress selects one of the internal registers.

The I²C interface of the VPX conforms to the I²C-bus specification for the fast-mode. It incorporates slope control for the falling edges of the SDA and SCL signals. If the power supply of the VPX is switched off, both pins SCL and SDA float. External pull-up devices must be adapted to fulfill the required rise time for the fast-mode. For bus loads up to 200 pF, the pull-up device could be a resistor; for bus loads between 200 pF and 400 pF, the pull-up device can be a current source (3 mA max.) or a switched resistor circuit.

4.3. Reset and IC Address Selection

The VPX can respond to one of two possible chip addresses. The address selection is made at reset by an externally supplied level on the PREF pin. This level is latched onto the inactive going edge of $\overline{\text{RES}}$.

4.4. Protocol Description

Once the reset is complete, the IC is selected by asserting a the device address in the address part of a I²C transmission. A device address pair is defined as a write address (86 hex or 8e hex) and a read address (87 hex or 8f hex). Writing is done by sending the device write address first, followed by the subaddress byte and one or two data bytes. For reading, the read address has to be transmitted first by sending the device write address (86 hex or 8e hex), followed by the subaddress, a second start condition with the device read address (87 hex or 8f hex) and reading one or two bytes of data.

The I²C-bus device addresses are

A6	A5	A4	A3	A2	A1	A0	R/W	hex
1	0	0	0	0	1	1	1/0	86/87
1	0	0	0	1	1	1	1/0	8e/8f

The registers of the VPX have 8 or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data bytes with the high byte first. The order of the bits in a data/address/subaddress byte is always MSB first.

Write to Hardware Control Registers

S	10000110	ACK	sub-addr	ACK	send data-byte	ACK	P

Read from Hardware Control Registers

S	10000110	ACK	sub-addr	ACK	S	10000111	ACK	receive data-byte	NAK	P

Note: S = I²C-Bus Start Condition
P = I²C-Bus Stop Condition
ACK = Acknowledge-Bit (active low on SDA from receiving device)
NAK = No Acknowledge-Bit (inactive high on SDA from receiving device)

Before accessing the address or data registers for the FP interface (FPRD, FPWR, FPDAT), make sure that the busy bit of FP is cleared (FPSTA).

Figure 4–1 shows I²C bus protocols for read and write operations of the interface. The read operation requires an extra start condition after the subaddress and repetition of the read chip address, followed by the read data bytes. The following protocol examples use device address hex 86/87.

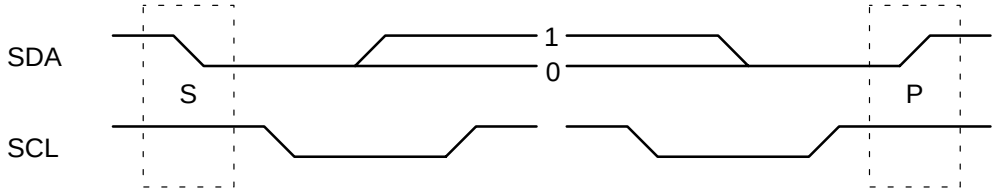


Fig. 4–1: I²C bus protocol (MSB first)

4.5. FP Control and Status Registers

In addition to the I²C subaddress space, a second class of address space is defined for direct communication with the on-board µ–controller. These registers are accessed via indirect addressing through I²C registers (see Fig. 4–2).

Due to the internal architecture of the VPX 3220 A, the IC cannot react immediately to all I²C requests which interact with the embedded processor (FP). The maximum response timing is approx. 20 ms (one TV field) for the FP processor if TV standard switching is active. If the addressed processor is not ready for further transmissions on the I²C bus, the clock line SCL is pulled low. This puts the current transmission into a wait state. After a certain period of time, the VPX releases the clock and the interrupted transmission is carried on.

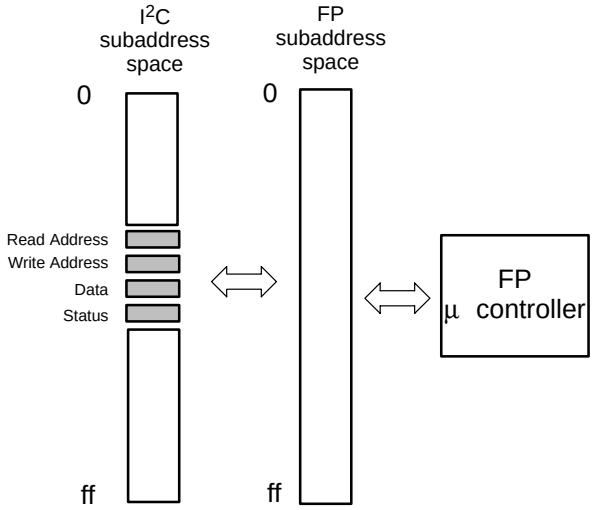


Fig. 4–2: FP register addressing

Write to FP

S	1 0 0 0 0 1 1 0	ACK	FPWR	ACK	send FP-address-byte high	ACK	send FP-address-byte low	ACK	P
S	1 0 0 0 0 1 1 0	ACK	FPDAT	ACK	send data-byte high	ACK	send data-byte low	ACK	P

Read from FP

S	1 0 0 0 0 1 1 0	ACK	FPRD	ACK	send FP-address-byte high	ACK	send FP-address-byte low	ACK	P

S	1 0 0 0 0 1 1 0	ACK	FPDAT	ACK	S	1 0 0 0 0 1 1 1	ACK	receive data-byte high	ACK	receive data-byte low	NAK	P

4.6. I²C Initialization

In order to completely specify the operational mode of the VPX, appropriate values must be loaded into both the I²C and FP registers. For both the I²C and FP registers, this data is loaded from internal ROM. The length of this set-up procedure is approximately 200 µsec after the leading edge of RES#.

Initialization is basically a two step procedure: first, the I²C registers are initialized, and afterwards, the FP runs its own initialization routine. There are two different set-ups for the I²C initialization available. The selection is made with the pin signal PIXCLK. On the active → inactive edge of the RES# signal, the state of the PIXCLK pin is latched and used as an index to the selected ROM table.

4.7. I²C Control and Status Registers

The following tables give definitions for the VPX control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in the hardware, i.e. a 9-bit register must always be accessed using two data bytes, but the 7 MSB will be don't care on write operations and 0 on read operations. Write registers that can be read back are indicated in the following table.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of values from one of four internal ROM tables.

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table

I²C Reg. Address	Number of Bits	Mode	Function	Name
Chip Identification				
00	8	r	Manufacture ID in accordance with JEDEC Solid State Products Engineering Council, Washington DC INTERMETALL Code EC_{hex}	I2C_ID0
01 / 02	8 / 8	r	16-bit Part number (01: LSBs, 02: MSBs) VPX 3220 A 4680_{hex} VPX 3216 B 4260_{hex} VPX 3214 C 4280_{hex}	I2C_ID1, I2C_ID2
Fast Processor (FP)				
26	12 / 16	wd	FP read address	FPRD
			bit [7:0] : address	addr
			bit [15:8] : reserved (must be set to zero)	
27	12 / 16	wd	FP write address	FPWR
			bit [7:0] : address	addr
			bit [15:8] : reserved (must be set to zero)	
Registers 26_{hex} and 27_{hex} use the same hardware by subaddressing.				
28	12 / 16	w	FP data	FPDAT
			bit [11:0] : data	data
			bit [15:12] : reserved (must be set to zero)	
29	3 / 8	r	FP status	FPSTA
			bit [0] : write request	
			bit [1] : read request	
			bit [2] : busy	
			bit [7:3] : reserved (return ones)	

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table				
I²C Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Analog Front-end				
33	8	w	Input Selector Luma ADC: bit [1:0] 00 VIN3 01 VIN2 10 VIN1 11 reserved (no luma input selected)	AFEND vis
			Input Selector Chroma ADC: bit [2] 0/1 select VIN1/CIN	cs
			Clamping Modes: bit [3] 0/1 clamp on/off for chroma ADC	dclc
			bit [5:4] reserved (must be set to zero)	
			bit [6] 1 stand-by luma ADC	
			bit [7] 1 stand-by chroma ADC	
Href, Vref				
D8	8	w	HREF and VREF control	REFSIG
			bit [0] : reserved (must be set to zero)	
			bit [1] : HREF Polarity 0 active high 1 active low	hpol
			bit [2] : VREF Polarity 0 active high 1 active low	vpol
			bit [5:3] : VREF Pulse width. binary value + 2 0 0 0 pulse width = 2 1 1 1 pulse width = 9	vlen
			bit [6] : PREF select 0 Odd/Even flag 1 PIntr (programmable interrupt signal)	prefsel
			bit [7] : PREF polarity 0 polarity unchanged 1 invert polarity	prefpol
Chroma Processing				
20	2 / 8	w	IF compensation:	IFC
			bit [1:0] 00 12 dB 01 reserved 10 6 dB/oct 11 0 dB/oct	
			bit [7:2] reserved (must be set to zero)	

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table				
I²C Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Color Space Converter				
E0	8	w	Alpha Keyer: Y_{max} (VPX 3220 A and VPX 3216 B)	YMAX
			bit [7:0] : Y_{max} (Integer)	ymax
E1	8	w	Alpha Keyer: Y_{min} (VPX 3220 A and VPX 3216 B)	YMIN
			bit [7:0] : Y_{min} (Integer)	ymin
E2	8	w	Alpha Keyer: $C_{b\ max}$ (VPX 3220 A and VPX 3216 B)	UMAX
			bit [7:0] : $C_{b\ max}$ (2's complement)	umax
E3	8	w	Alpha Keyer: $C_{b\ min}$ (VPX 3220 A and VPX 3216 B)	UMIN
			bit [7:0] : $C_{b\ min}$ (2's complement)	umin
E4	8	w	Alpha Keyer: $C_{r\ max}$ (VPX 3220 A and VPX 3216 B)	VMAX
			bit [7:0] : $C_{r\ max}$ (2's complement)	vmax
E5	8	w	Alpha Keyer: $C_{r\ min}$ (VPX 3220 A and VPX 3216 B)	VMIN
			bit [7:0] : $C_{r\ min}$ (2's complement)	vmin
E6	8	w	Contrast Brightness 1	CBM_BRI
			bit [7:0] : Brightness Level (binary offset)	brightness
E7	8	w	Contrast Brightness 2	CBM_CON
			bit [5:0] : Contrast Level .... linear scale factor for luminance [5] integer part [4:0] fractional part default = 1.0	contrast
			bit [7:6] : Noise Shaping .... Control for 10 bit to 8 bit conversion 0 0 : 9-bit to 8-bit via1-bit rounding 0 1 : 9-bit to 8-bit via truncation 1 0 : 9-bit to 8-bit via 1-bit error diffusion 1 1 : 10-bit to 8-bit via 2-bit error diffusion	noise

The control register modes are
– w: write/read register
– r: read-only register
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– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table				
I²C Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Color Space Converter				
E8	8	w	Format Selection, Alpha Keyer and Contrast Brightness	FORMAT
			bit [7, 5, 2:0] : unused in VPX 3214 C	
			bit [2:0] : Format Selector: 000 YUV 4:2:2, YUV 4:2:2 ITUR 001 YUV 4:4:4, 010 YUV 4:1:1 011 YUV 4:1:1 DPCM 100 RGB 888 – 24 bit 101 RGB 888 (Invers Gamma) – 24 bit 110 RGB 565 (Invers Gamma) – 16 bit 111 RGB 555 (Invers Gamma) + Alpha Key – 15+1 bit	format
			bit [3] : Select data format of C_b, C_r video output data stream 0 2's complement (–128 ... 127) 1 binary offset (0 ... 255)	twosq
			bit [4] : Contrast Brightness: Clamping Level 0 clamping level = 32, 1 clamping level = 16	clamp
			bit [5] : Gamma: Round Dither Enable (=1)	dither
			bit [6] : Alpha Key Polarity 0 active high 1 active low bit [6] : Programmable output pin in VPX 3214 C, connected to TDO	keyinv
			bit [7] : Alpha Key Median Filter 0 Median Filter is disable 1 Median Filter is enable	median
EA	8	w	Diverse settings	
			bit [2:0] : reserved (must be set to zero).	
			bit [3] : connect LLC2 to ALPHA/TDO pin	
			bit [4] : LLC2 polarity	
			bit [5] : 0 Output FIFO Pointer Reset with posedge of $VACT_{intern}$ 1 Output FIFO Pointer Reset with VRF=0.	FFRES
			bit [7:6] : reserved (must be set to zero)	

The control register modes are
– w: write/read register – r: read-only register
– d: register is double latched – v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table				
I²C Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Output Multiplexer				
F0	8	w	Output FIFO	OFIFO
			FIFO Control: (only available in Asynchronous Mode) bit [4:0] : FIFO Flag – Half Full Level (interface signal $\overline{HF}$)	hfull
			bit [7:5] : Bus Shuffler 000 Out[23:0] = In[23:0] 001, 010 Out[23:0] = In[7:0, 23:8] 011 Out[23:0] = In[15:0, 23:16] 100 Out[23:0] = In[15:8, 23:16, 7:0] 101, 110 Out[23:0] = In[7:0, 15:8, 23:16] 111 Out[23:0] = In[23:16, 7:0, 15:8] Meaning: In[23:0] : Data from Color Space Stage Out[23:0] : Data to Output FIFO	shuf
F1	8	w	Output Multiplexer	OMUX
		vact	bit [1:0]: Port Mode 00 parallel_out, 'single clock' Port A = FifoOut[23:16] Port B = FifoOut[15:8]; 01 'double clock' (only available with a transport rate of 13.5 MHz) Port A = FifoOut[23:16] / FifoOut[15:8], Port B = FifoOut[7:0]; 10,11 reserved	mode
		vact	bit [2] : ASYNCHRONOUS MODE: Clock Slope (if Clock Source = external) 1 negative edge triggered 0 positive edge triggered. SYNCHRONOUS MODE: Data Reset 1 set output ports to 0 during VACT(/FE#) = 0.	slope
		vact	bit [3] : Clock Source 1 Internal Source (Synchronous Mode) – PIXCLK is output 0 External Mode (Asynchronous Mode) – PIXCLK is input	clkio
		direct	bit [5:4] : delay signal 'active video' (signal $\overline{FE}$) with respect to video output data. Only available in Synchronous Mode. 00 no delay (default) 01 one clock cycle 10 two clock cycles 11 three clock cycles	delay
		direct	bit [6] : 1 disable FIFO-Empty $\overline{FE}$ low pass filter Only available in Asynchronous Mode.	
			bit [7] : 1 enable HLEN counter	hlen

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

I²C-Register Table				
I²C Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Output Multiplexer				
F2	8	w	Output Enable	OENA
		direct	bit [0] : 1 Enable Video Port A 0 Disable / High Impedance Mode	aen
		direct	bit [1] : 1 Enable Video Port B 0 Disable / High Impedance Mode	ben
		direct	bit [2] : reserved (must be set to zero)	
		direct	bit [3] : 1 Enable Controls (HREF, VREF, PREF, HF#, FE#, ALPHA) 0 Disable / High Impedance Mode	zen
		direct	bit [4] : 1 Enable LLC-Clock to $\overline{HF}$-Pad (if transport rate is 13 MHz and internal clock source is used)	llcen
		direct	bit [5] : 1 Enable FSY-Data to $\overline{HF}$-Pad (if transport rate is 20 MHz and internal clock source is used)	fsyen
		direct	bit [6] : 1 Synchronize HREF, VREF with PIXCLK	hvsynbyq
		direct	bit [7] : 1 disable OEQ pin function	
F8	6 / 8	w	Pad Driver Strength – TTL Output Pads Typ A	DRIVER_A
			bit [2:0] : Driver strength of Port A[7:0]	stra1
			bit [5:3] : Driver strength of PIXCLK, HF# and FE#	stra2
			bit [7:6] : additional PIXCLK driver strength strength = bit [5:3] | {bit [7:6], 0}	
F9	6 / 8	w	Pad Driver Strength – TTL Output Pads Typ B	DRIVER_B
			bit [2:0] : Driver strength of Port B[7:0] and C[7:0]	strb1
			bit [5:3] : Driver strength of HREF, VREF, PREF and ALPHA	strb2
			bit [7:6] : reserved (must be set to zero)	

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

4.8. FP Control and Status Registers

The tables below list the registers which are currently defined. Electrically, all of the registers in the FP subaddress space are both readable and writeable. Functionally, they are intended for either read or write (as shown in the 'mode' column)

Warning: The FP subaddress space accesses the RAM of the fast processor. It is therefore very sensitive to unintended access. In particular, the user must be sure not to overwrite reserved areas.

FP-Register Table

FP Reg. Address	Number of Bits	Mode	Function	Name
Load Table for Window #1				WinLoadTab1
88	12	w	Vertical Begin	
			bit [8:0] : Vertical Begin (field line number) minimum line number → 7 maximum line number → determined by current TV line standard	vbeg1
		A	bit [11:9] sharpness control .... regulates the subjective sharpness by selecting filters to admitting horizontal alias / blurring 1 1 1 maximum blurring 1 1 0 ..... 1 0 1 more blurring 0 0 0 default filter setting 0 0 1 more aliasing 0 1 0 ..... 0 1 1 maximum aliasing 1 0 0 set filters for pass-thru	
89	12	w	Vertical Lines In	
			bit [8:0] : Number of input lines	vlinei1
			bit [9] reserved (must be set to zero)	
			bit [11:10] : field flag 1 1 Window disabled 1 0 Window enabled in ODD fields only 0 1 Window enabled in EVEN fields only 0 0 Window enabled in both fields	
8A	12	w	Vertical Lines Out	
			bit [8:0] : Number of output lines	vlineo1
			bit [11:9] reserved (must be set to zero)	
8B	12	w	Horizontal Begin	
			bit [10:0] : Horizontal start of window	hbeg1
			bit [11] reserved (must be set to zero)	
8C	12	w	Horizontal Length	
			bit [10:0] : Horizontal length of window	hlen1
			bit [11] reserved (must be set to zero)	
8D	12	w	Number of Pixels	
			bit [10:0] : Number of active pixels per line	npix1
			bit [11] reserved (must be set to zero)	

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

FP-Register Table				
FP Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Load Table for Window #2				WinLoadTab2
8E	12	w	Vertical Begin	
			bit [8:0] : Vertical Begin (field line number) minimum line number → 7 maximum line number → determined by current TV line standard	vbeg2
		A	bit [11:9] sharpness control ...regulates the subjective sharpness by selecting filters to admitting horizontal alias / blurring 1 1 1 maximum blurring 1 1 0 ..... 1 0 1 more blurring 0 0 0 default filter setting 0 0 1 more aliasing 0 1 0 ..... 0 1 1 maximum aliasing 1 0 0 set filters for pass-thru	
8F	12	w	Vertical Lines In	
			bit [8:0] : Number of input lines	vlinei2
			bit [9] reserved (must be set to zero)	
			bit [11:10] : field flag 1 1 Window disabled 1 0 Window enabled in ODD fields only 0 1 Window enabled in EVEN fields only 0 0 Window enabled in both fields	
90	12	w	Vertical Lines Out	
			bit [8:0] : Number of output lines	vlineo2
			bit [11:9] reserved (must be set to zero)	
91	12	w	Horizontal Begin	
			bit [10:0] : Horizontal start of window	hbeg2
			bit [11] reserved (must be set to zero)	
92	12	w	Horizontal Length	
			bit [10:0] : Horizontal length of window	hlen2
			bit [11] reserved (must be set to zero)	
93	12	w	Number of Pixels	
			bit [10:0] : Number of active pixels per line	npix2
			bit [11] reserved (must be set to zero)	

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

FP-Register Table				
FP Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Control Word				
F0	12	w r	Register for control and latching	CMDWD
		w	bit [0] : Transport Rate 0 20.25 MHz. 1 13.5 MHz.	settr
		w	bit [1] : Latch Transport Rate 1 latch (reset automatically)	lattr
		w	bit [3:2] : Sync timing mode 0 0 Open 0 1 Forced 1 x Scan	settm
		w	bit [4] : Latch Timing Mode 1 latch (reset automatically)	lattm
		w	bit [5] : Latch Window #1 1 latch (reset automatically)	latwin1
		w	bit [6] : Latch Window #2 1 latch (reset automatically)	latwin2
		wr	bit[8] : Odd/Even mode 0 toggles always 1 follows odd/even property of input video signal	disoef
			bit [11:9] reserved (must be set to zero)	
Info Word				InfoWord
F1	12	r	Internal status register do not overwrite	
			bit [2:0] : reserved	
			bit [5:3] : Current active TV standard x x x see table of 3-bit code of TV standards	acttv
			bit [6] : Line Standard of currently active TV standard 0 525 / 60 1 625 / 50	actls
			bit [11:7] reserved	

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

The FP RAM locations which manage the TV coding standard (selection/recognition) all use a 3-bit code for the eight supported standards. This code (shown below) is assumed in the register descriptions which follow.

0 0 0	PAL B,G,H,I	(625/50)
0 0 1	NTSC M	(525/60)
0 1 0	SECAM	(625/50)
0 1 1	NTSC 44	(525/60)
1 0 0	PAL M	(525/60)
1 0 1	PAL N	(625/50)
1 1 0	PAL 60	(525/60)
1 1 1	NTSC Comb	(525/60)

FP-Register Table

FP Reg. Address	Number of Bits	Mode	Function	Name
TV Standard – Write				TVstndWr
F2	12	w	writeable control register for managing the TV coding standard	
			bit [0] : Manual / Automatic Select 0 Automatic 1 Manual	mansel
			bit [3:1] : TV standard for manual selection x x x see table above	settv
			bit [4] : Latch the TV standard manually 1 latch (reset automatically)	lattv
			bit [5] : Composite / S-VHS select 0 Composite 1 S-VHS	svhssel
			bit [9:6] : Threshold for standard search results 1 1 1 1 perfect score (maximum score) 0 0 0 0 'no video' (minimum score) 1 1 1 1 default	score
			bit [11:10] reserved (must be set to zero)	

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

FP-Register Table				
FP Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
TV Standard – Read				TVstndRd
F3	12	r	Readable control register for managing the TV coding standard	
			bit [0] : VACT suppress 0 enabled 1 suppressed	
			bit [1] : Status of recognition routine 0 idle 1 running	
			bit [4:2] : TV standard detected (by recognition routines) x x x see table above	
			bit [5] : 'No video' flag 0 TV standard shown in bit [4:2] present 1 no video at selected input	
			bit [9:6] : High score from video recognition routine (confidence level) 1 1 1 1 maximum confidence 0 0 0 0 minimum confidence	
			bit [10] : TV line standard (for TV standard from bit [4:2] above) 0 525/60 1 625/50	
			bit [11] : reserved	
Vertical Standard				
E7	12	w	Writeable control register for vertical locking	vsdt
			bit [0]: vertical standard lock enable 0 disabled 1 enabled	
			bit [11:1] expected number of lines per field	
Color Processing				
1C			NTSC tint angle, $\pm 512 = \pm \pi/4$	tint
A0			ACC reference; also used to control color saturation ACCref = 0: ACC turned off ACCref = 1: minimal color saturation ie. color switched off	ACCref
A3			ACC multiplier value for SECAM Dr chroma component to adjust C_r level	ACCr
A4			ACC multiplier value for SECAM Db chroma component to adjust C_b level	ACCb
A8			amplitude color killer level kilvl = 0: killer disabled	kilvl

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

FP-Register Table				
FP Reg. Address	**Number of Bits**	**Mode**	**Function**	**Name**
Automatic Gain Control				
B2	12	w	sync amplitude reference AGCref = 0: AGC disabled Write 0 to FP register B5 after writing 0 to AGCref to disable the AGC	AGCref
BE	12	w	start value for AGC gain while vertical lock or AGC is inactive	sgain
20	12	r	AGC gain value	gain
DVCO				
58	12	w	crystal oscillator center frequency adjust, –2048..2047	dvco
59	12	r	crystal oscillator center frequency adjustment value for line lock mode. true adjust value is DVCO – ADJUST. For factory crystal alignment: set DVCO=0, set lock mode, read crystal offset from ADJUST register and use negative value for initial center frequency adjustment via DVCO.	adjust
26	12	w	line locked mode lock command/status	xlg
			write: 100 enable lock 0 disable lock	
			read: 4095/0 locked / unlocked	
Horizontal PLL				
4B	12	w	gain of the horizontal PLL	
			bit [4:0] gain for the integrating part of PLL control	if1
			bit [9:5] gain for the proportional part of PLL control	if2
			bit [11:10] reserved	

The control register modes are
– w: write/read register
– r: read-only register
– A: register or register field has function only in VPX 3220 A

The mnemonics used in the Intermetall VPX demo software are given in the last column.

4.9. Initial Values on Reset

PIXCLK LOW on Reset		Table of Initial Values		
Type	**Name**	**Address**	**Data**	**Description**
I^2C	OFIFO	F0	0A	Half full level to $0A_{hex}$ (10_{dec}), bus shuffler off
I^2C	AFEND	33	0D	Video input 2, chroma ADC from Chroma input, clamp off for chroma ADC
I^2C	IFC	20	03	IF compensation 0 dB/oct
I^2C	YMAX	E0	FF	Open up all comparators, so that Alpha Key is always true (set)
I^2C	YMIN	E1	00	
I^2C	UMAX	E2	7F	
I^2C	UMIN	E3	80	
I^2C	VMAX	E4	7F	
I^2C	VMIN	E5	80	
I^2C	CBM_BRI	E6	00	Brightness to 0
I^2C	CBM_CON	E7	20	Contrast to 1.0, noise shaping 9 to 8 bit via 1 bit rounding
I^2C	FORMAT	E8	F8	YUV 422, C_r,C_b in binary offset, con/bri clamp to 16_{dec}, Gamma dither enabled, Alpha active low, Alpha median filter enabled
I^2C	OMUX	F1	00	single clock, PIXCLK input, posedge triggered, **HLEN counter disabled**
I^2C	DRIVER_A	F8	12	Port A, PIXCLK, HF# and FE# strength to 2
I^2C	DRIVER_B	F9	24	Port B, HREF, VREF, PREF and ALPHA strength to 4
I^2C	OENA	F2	00	All outputs disabled
PIXCLK HIGH on Reset				
I^2C	OFIFO	F0	0B	Half full level to $0B_{hex}$ (11_{dec}), bus shuffler off
I^2C	AFEND	33	0D	Video input 2, chroma ADC from Chroma input, clamp off for chroma ADC
I^2C	IFC	20	03	IF compensation 0 dB/oct
I^2C	YMAX	E0	FF	Open up all comparators, so that Alpha Key is always true (set)
I^2C	YMIN	E1	00	
I^2C	UMAX	E2	7F	
I^2C	UMIN	E3	80	
I^2C	VMAX	E4	7F	
I^2C	VMIN	E5	80	
I^2C	CBM_BRI	E6	00	Brightness to 0
I^2C	CBM_CON	E7	20	Contrast to 1.0, noise shaping 9- to 8-bit via 1-bit rounding
I^2C	FORMAT	E8	F8	YUV 422, C_r,C_b in binary offset, con/bri clamp to 16_{dec}, Gamma dither enabled, Alpha active low, Alpha median filter enabled
I^2C	OMUX	F1	08	single clock, PIXCLK output, **HLEN counter disabled**
I^2C	DRIVER_A	F8	12	Port A, PIXCLK, HF# and FE# strength to 2
I^2C	DRIVER_B	F9	24	Port B, HREF, VREF, PREF and ALPHA strength to 4
I^2C	OENA	F2	5F	All outputs enabled: synchronize HREF, VREF with PIXCLK

PIXCLK LOW or HIGH on Reset		Table of Initial Values		
Type	**Name**	**Address hex**	**Data dec**	**Description**
FP	TINT	1C	0	Neutral tint
FP		4B	664	HPLL: if1 = 24 if2 = 20
FP	DVCO	58	0	
FP	ADJUST	59	0	
FP	WinLoadTab1	88	12	
FP		89	1	
FP		8A	1	
FP		8B	0	
FP		8C	704	
FP		8D	704	
FP	WinLoadTab2	8E	17	
FP		8F	500	
FP		90	500	
FP		91	0	
FP		92	704	
FP		93	704	
FP	ACCREF	A0	2070	
FP	KILVL	A8	30	
FP	AGCREF	B2	768	
FP	SGAIN	BE	27	
FP	VSDT	E7	523	
FP	CMDWD	F0	114	Transport rate 20.25 MHz, sync timing mode Open, both windows latched, VACT enabled
FP	TVstndWr	F2	979	Manual TV standard select, composite signal

5. JTAG Boundary-Scan, Test Access Port (TAP)

The design of the Test Access Port, which is used for Boundary-Scan Test conforms to standard IEEE 1149.1-1990, with one exception. Also included is a list of the mandatory instructions supported, as well as the optional instructions. This is only a brief overview of some of the basics, as well as any optional features which are incorporated. The IEEE 1149.1 document may be necessary for a more concise description. Finally, an adherence section goes through a checklist of topics and describes how the design conforms to the standard.

The implementation of the instructions HIGHZ and CLAMP conforms to the supplement P1149.1/D11 (October 1992) to the standard 1149.1-1990.

5.1. General Description

The TAP in the VPX is incorporated using the four signal interface. The interface includes TCK, TMS, TDI, and TDO. The optional TRESET signal is not used. This is not needed because the chip has an internal power-on-reset which will automatically steer the chip into the TEST-LOGIC-RESET state. The goal of the interface is to provide a means to test the boundary of the chip. There is no support for internal or BIST(built-in self test). The one exception to IEEE 1149.1 is that the TDO output is shared with the ALPHA signal. This was done because of I/O restrictions on the chip (see section 5.3. “Exceptions to IEEE 1149.1” for more information).

5.2. TAP Architecture

The TAP function consists of the following blocks: TAP-controller, instruction register, boundary-scan register, bypass register, optional device identification register, and master mode register.

5.2.1. TAP Controller

The TAP Controller is responsible for responding to the TCK and TMS signals. It controls the transition between states of this machine. These states control selection of the data or instruction registers and the actions which occur in these registers. These include capture, shifting, and update. See Fig. 5–1 of IEEE 1149.1 for TAP state diagram.

5.2.2. Instruction Register

The instruction register chooses which one of the data registers is placed between the TDI and TDO pins when the select data register state is entered in the TAP controller. When the select instruction register state is active, the instruction register is placed between the TDI and TDO.

Instructions

The following instructions are incorporated:

– bypass

– sample/preload

– extest

– master mode

– ID code

– HIGHZ

– CLAMP

5.2.3. Boundary Scan Register

The boundary-scan register (BSR) consists of boundary-scan cells (BSCs) which are distributed throughout the chip. These cells are located at or near the I/O pad. It allows sampling of inputs, controlling of outputs, and shifting between each cell in a serial fashion to form the BSR. This register is used to verify board interconnect.

Input Cell

The input cell is constructed to achieve capture only. This is the minimal cell necessary since Internal Test (INTEST) is not supported. The cell captures either the system input in the CAPTURE-DR State or the previous cells output in the SHIFT-DR State. The captured data is then available to the next cell. No action is taken in the UPDATE-DR State. See Figure 10–11 of IEEE 1149.1 for reference.

Output Cell

The output cell will allow both capture and update. The capture flop will obtain system information in the CAPTURE-DR State or previous cells information in the SHIFT-DR state. The captured data is available to the next cell. The captured or shifted data is downloaded to the update flop during the UPDATE-DR state. The data from the update flop is then multiplexed to the system output pin when the EXTEST instruction is active. Otherwise, the normal system path exists where the signal from the system logic flows to the system output pin. See Fig. 10–12 of IEEE 1149.1 for reference.

Tristate Cell

Each group of output signals which are tristatable is controlled by a boundary scan cell (output cell type). This allows either the normal system signal or the scanned signal to control the tristate control. In the VPX, there are four such tristate control cells which control groups of output signals (see section “Output Driver Tristate Control” for further information).

Bidirect Cell

The bidirect cell is comprised of an input cell and a tristate cell as described in the IEEE standard. The signal PIXCLK is a bidirectional signal.

5.2.4. Bypass Register

This register provides a minimal path between TDI and TDO. This is required for complicated boards where many chips may be connected in serial.

5.2.5. Device Identification Register

This is an optional 32-bit register which contains the-INTERMETALL identification code (JEDEC controlled), part and revision number. This is useful in providing the tester with assurance that the correct part and revision are inserted into a PCB.

5.2.6. Master Mode Data Register

This is an optional register used to control an 8-bit test register in the chip. This register supports shift and update. No capture is supported. This was done so the last word can be shifted out for verification.

5.3. Exception to IEEE 1149.1

There is one exception to IEEE 1149.1. The exception is to paragraphs 3.1.1.c., 3.5.1.b, and 5.2.1.d (TEST-LOGIC-RESET state). Because of pin limitations on the chip, a pin is shared for two functions. When the circuit is in the TEST-LOGIC-RESET state, the ALPHA signal is driven out the TDO/ALPHA pin. When the circuit leaves the TEST-LOGIC-RESET state, the TDO signal is driven on this line. As long as the circuit is not in the TEST-LOGIC-RESET state, all the rules for application of the TDO signal adhere to the IEEE1149.1 spec.

Since the VPX uses the JTAG function as a boundary-scan tool, the VPX does not sacrifice test of this pin since it is verified by exercising JTAG function. The designer of the PCB must make careful note of this fact, since he will not be able to scan into chips receiving the ALPHA signal via the VPX. The PCB designer may want to put this chip at the end of the chain or bring the VPX TDO out separately and not have it feed another chip in a chain.

5.4. IEEE 1149.1-1990 Spec Adherence

This section defines the details of the IEEE1149.1 design for the VPX. It describes the function as outlined by IEEE1149.1, section 12.3.1. The section of that document is referenced in the description of each function.

5.4.1. Instruction Register

(section 12.3.1.b.i of IEEE 1149.1-1990)

The instruction register is three bits long. No parity bit is included. The pattern loaded in the instruction register during CAPTURE-IR is binary “101” (MSB to LSB). The two LSBs are defined by the spec to be “01” (bit 1 and bit 0) while the MSB (bit 2) is set to “1”.

5.4.2. Public Instructions

(Section 12.3.1.b.ii of IEEE 1149.1-1990)

A list of the public instructions is as follows:

Instruction	Code (MSB to LSB)
EXTEST	000
SAMPLE/PRELOAD	001
ID CODE	010
MASTER MODE	011
HIGHZ	100
CLAMP	110
BYPASS	100 – 111

The EXTEST and SAMPLE/PRELOAD instructions both apply the boundary scan chain to the serial path. The ID CODE instruction applies the ID register to the serial chain. The BYPASS, the HIGHZ, and the CLAMP instructions apply the bypass register to the serial chain.

The MASTER MODE instruction is a test data instruction for public use. It provides the ability to control an 8-bit test register in the chip.

5.4.3. Self-test Operation

(Section 12.3.1.b.iii of IEEE 1149.1-1990). There is no self-test operation included in the VPX design which is accessible via the TAP.

5.4.4. Test Data Registers

(Section 12.3.1.b.iv of IEEE 1149.1-1990).

The VPX includes the use of four test data registers. They are the required bypass and boundary scan registers, the optional ID code register and the master mode register.

The bypass register is, as defined, a 1-bit register accessed by codes 100 through 111, inclusive. Since the design includes the ID code register, the bypass register is not placed in the serial path upon power-up or Test-Logic-Reset.

The master mode is an 8-bit test register which is used to force the VPX into special test modes. This is reset upon power-on-reset. This register supports shift and update only. It is not recommended to access this register. The loading of that register can drive the IC into an undefined state.

5.4.5. Boundary-Scan Register

(Section 12.3.1.b.v of IEEE 1149.1-1990)

The boundary-scan chain has a length of 38 shift registers. The scan chain order is specified in the section “Pin Connections”.

5.4.6. Device Identification Register

(Section 12.3.1.b.vi of IEEE 1149.1-1990)

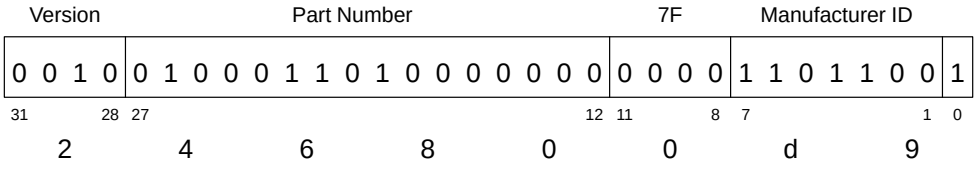
The manufacturer’s identification code for-INTER-METALL is “6C”$_{(hex)}$. The general implementation scheme uses only the 7 LSBs and excludes the MSB, which is the parity bit. The part number is “4680”$_{(hex)}$. The version code starts from “1”$_{(hex)}$ and changes with every revision. The version number relates to changes of the chip interface only.

5.4.7. Performance

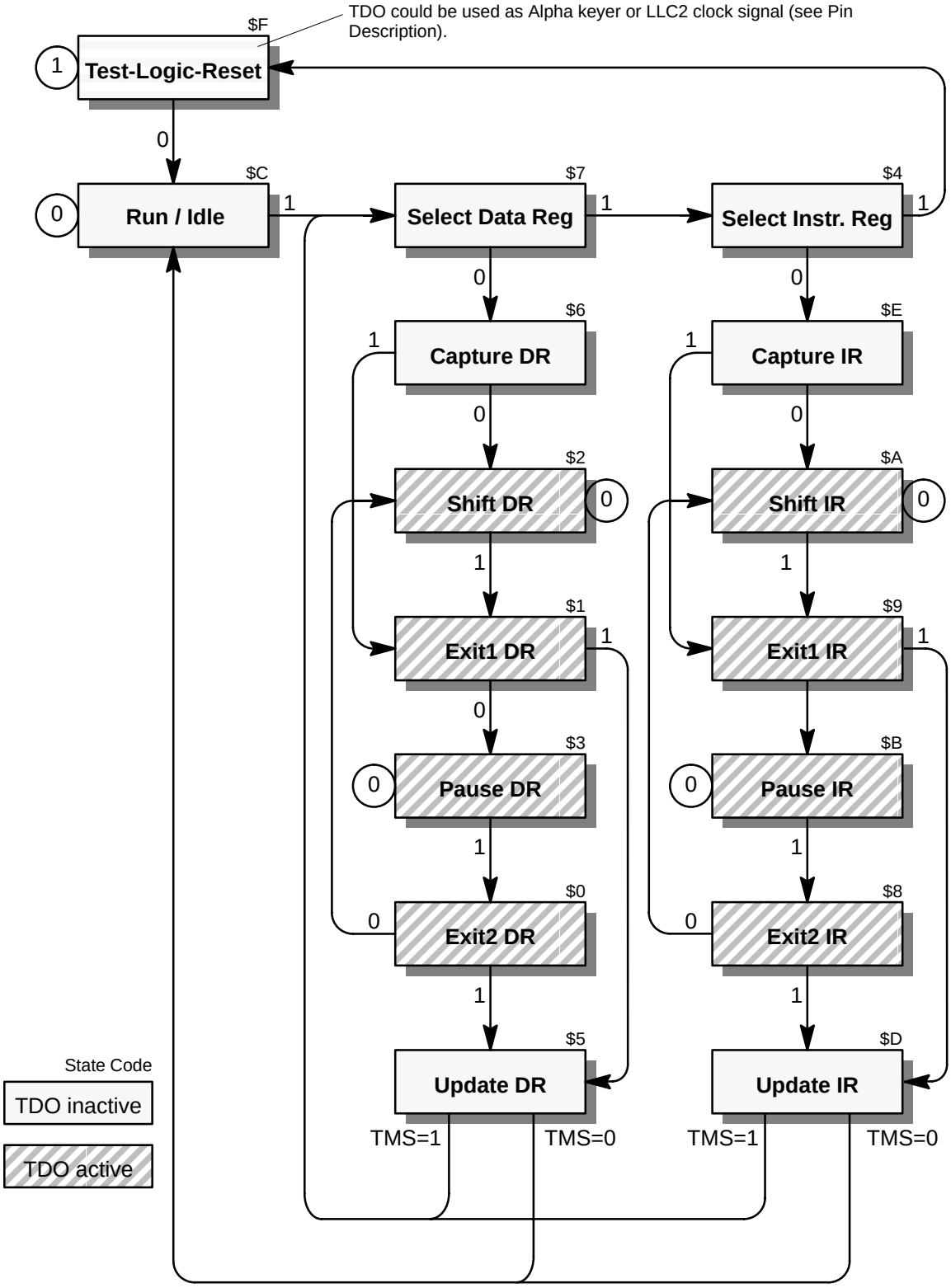
(Section 12.3.1.b.vii of IEEE 1149.1-1990)

See section “Specification” for further information.

The Device Identification Register



TAP State Transitions



State transitions are dependend on the value of TMS, synchronized by TCK.

```
--************************************************************
--
-- This is the BSDL for the 44-Pin Version of the VPXA design.
--
--************************************************************
Library IEEE;
Use work.STD_1149_1_1990.ALL;

Entity VPXA_44 is
Generic (Physical_Pin_Map:string := "UNDEFINED");

Port(                                                          --define ports
        TDI,TCK,TMS:            in bit;
        TDO,HREF,VREF,PREF:     out bit;
        A:                      out bit_vector(7 downto 0);
        PVDD,PVSS:              linkage bit;
        PIXCLK:                 inout bit;
        OEQ:                    in bit;
        HFQ,FEQ:                out bit;
        B:                      out bit_vector(7 downto 0);
        SDA,SCL:                inout bit;
        VSS,XTAL2,XTAL1,VDD:    linkage bit;
        RESQ:                   in bit;
        AVDD,AVSS,VRT,ISGND:    linkage bit;
        CIN,VIN1,VIN2,VIN3:     in bit
   );

Attribute Pin_Map of VPXA_44 : Entity is Physical_Pin_Map;

constant Package_44 : Pin_Map_String :=                        --map pins to signals
        "TDI    :  1 " &
        "TCK    :  2 " &
        "TDO    :  3 " &
        "HREF   :  4 " &
        "VREF   :  5 " &
        "PREF   :  6 " &
        "A      : (7,8,9,10,14,15,16,17)" &
        "PVDD   : 11 " &
        "PIXCLK : 12 " &
        "PVSS   : 13 " &
        "OEQ    : 18 " &
        "HFQ    : 19 " &
        "FEQ    : 20 " &
        "B      : (21,22,23,24,25,26,27,28)," &
        "SDA    : 29 " &
        "SCL    : 30 " &
        "VSS    : 31 " &
        "XTAL2  : 32 " &
        "XTAL1  : 33 " &
        "VDD    : 34 " &
        "RESQ   : 35 " &
        "AVDD   : 36 " &
        "CIN    : 37 " &
        "AVSS   : 38 " &
        "VIN1   : 39 " &
        "VIN2   : 40 " &
        "VRT    : 41 " &
        "VIN3   : 42 " &
        "ISGND  : 43 " &
        "TMS    : 44 " ;

Attribute  Tap_Scan_In      of TDI      : signal is true;      --define JTAG Controls
Attribute  Tap_Scan_Mode    of TMS      : signal is true;
Attribute  Tap_Scan_Out     of TDO      : signal is true;
Attribute  Tap_Scan_Clock   of TCK      : signal is (10.0e6,Both);  --max frequency and levels TCK can be stopped at.

Attribute Instruction_Length        of VPXA_44: entity is 3;   --define instr. length

Attribute Instruction_Opcode        of VPXA_44: entity is
        "EXTEST                     (000)," &                  --External Test
```

```
        ”SAMPLE         (001),”  &                          —Sample/Preload
        ”IDCODE         (010),”  &                          —ID Code
        ”MASTERMODE     (011),”  &                          —Master Mode (internal Test)
        ”HIGHZ          (100),”  &                          — Highz
        ”CLAMP”         (110),”  &                          — Clamp
        ”BYPASS         (100,101,110,111),”;                —Bypass

Attribute Register_Access       of VPXA_44: entity is       —instr. vs register
        ”BOUNDARY       (EXTEST,SAMPLE),” &                 —control
         ”BYPASS        (BYPASS, HIGHZ, CLAMP),” &
        ”IDCODE[32]     (IDCODE),” &
        ”MASTERMODE[8]  (MASTERMODE) ”;

Attribute INSTRUCTION_Capture of VPXA_44: entity is ”101”;  —captured instr.

Attribute IDCODE_Register       of VPXA_44: entity is
                                ”0001” &                    —initial rev
                                ”0100011010000000” &        —part numb. 4680
                                ”0000” &                    —7F Count
                                ”1101100” &                 —INTERMETALL Code–Parity
                                ”1”;                        —Mandatory LSB

Attribute Boundary_Cells        of VPXA_44: entity is ”BC_1,BC_4”;  –-BC_1 for output cell
                                                                    —BC_4 for input cell

Attribute Boundary_Length       of VPXA_44: entity is 38;   —Boundary scan length

Attribute Boundary_Register     of VPXA_44: entity is       —Boundary scan defin.
—       num     cell    port    function safe    ccel    disval  rslt
        ”  37   (BC_4, VIN3,    input,    X                       ),” &
        ”  36   (BC_4, VIN2,    input,    X                       ),” &
        ”  35   (BC_4, VIN1,    input,    X                       ),” &
        ”  34   (BC_4, CIN,     input,    X                       ),” &
        ”  33   (BC_4, RESQ,    input,    X                       ),” &
        ”  32   (BC_1, *,       internal, X                       ),” &   —clock health
        ”  31   (BC_4, SCL,     input,    X                       ),” &
        ”  30   (BC_1, SCL,     output3, X,       30,     1,      Z       ),” &   —open collector
        ”  29   (BC_4, SDA,     input,    X                       ),” &
        ”  28   (BC_1, SDA,     output3, X,       28,     1,      Z       ),” &   —open collector
        ”  27   (BC_1, B(0),    output3, X,       19,     1,      Z       ),” &
        ”  26   (BC_1, B(1),    output3, X,       19,     1,      Z       ),” &
        ”  25   (BC_1, B(2),    output3, X,       19,     1,      Z       ),” &
        ”  24   (BC_1, B(3),    output3, X,       19,     1,      Z       ),” &
        ”  23   (BC_1, B(4),    output3, X,       19,     1,      Z       ),” &
        ”  22   (BC_1, B(5),    output3, X,       19,     1,      Z       ),” &
        ”  21   (BC_1, B(6),    output3, X,       19,     1,      Z       ),” &
        ”  20   (BC_1, B(7),    output3, X,       19,     1,      Z       ),” &
        ”  19   (BC_1, *,       control,  X                       ),” &   —control
        ”  18   (BC_1, FEQ,     output3, X,       16,     1,      Z       ),” &
        ”  17   (BC_1, HFQ,     output3, X,       16,     1,      Z       ),” &
        ”  16   (BC_1, *,       control,  X                       ),” &   —control
        ”  15   (BC_4, OEQ,     input,    X                       ),” &
        ”  14   (BC_1, A(0),    output3, X,       7,      1,      Z       ),” &
        ”  13   (BC_1, A(1),    output3, X,       7,      1,      Z       ),” &
        ”  12   (BC_1, A(2),    output3, X,       7,      1,      Z       ),” &
        ”  11   (BC_1, A(3),    output3, X,       7,      1,      Z       ),” &
        ”  10   (BC_1, CLKIO,   control,  X                       ),” &
        ”  9    (BC_4, PIXCLK,input,    X                       ),” &
        ”  8    (BC_1, PIXCLK,output3, X,       10,     1,      Z       ),” &   —bidirect
        ”  7    (BC_1, *,       control,  X                       ),” &   —control
        ”  6    (BC_1, A(4),    output3, X,       7,      1,      Z       ),” &
        ”  5    (BC_1, A(5),    output3, X,       7,      1,      Z       ),” &
        ”  4    (BC_1, A(6),    output3, X,       7,      1,      Z       ),” &
        ”  3    (BC_1, A(7),    output3, X,       7,      1,      Z       ),” &
        ”  2    (BC_1, PREF,    output3, X,       16,     1,      Z       ),” &
        ”  1    (BC_1, VREF,    output3, X,       16,     1,      Z       ),” &
        ”  0    (BC_1, HREF,    output3, X,       16,     1,      Z       ),”;

End VPXA_44;
```

6. Specification

6.1. Outline Dimensions

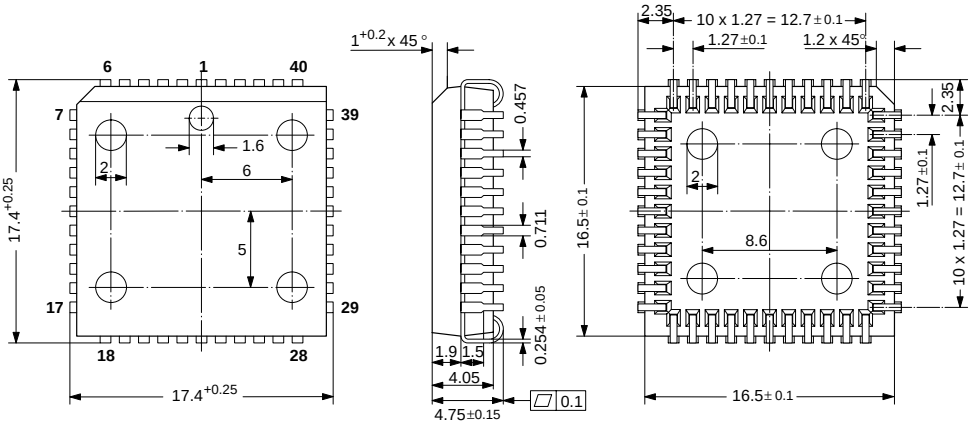


Fig. 6–1:
44-Pin Plastic Leaded Chip Carrier Package
(PLCC44)
Weight approximately 2.5 g
Dimensions in mm

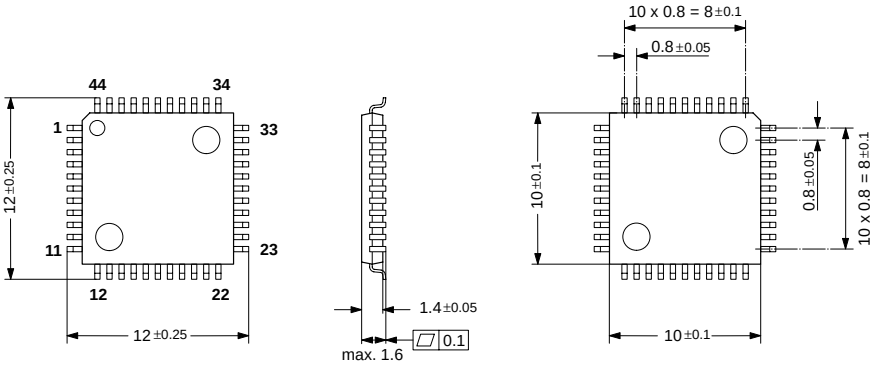


Fig. 6–2: 44-Pin Plastic Thin-Quad-Flat-Pack
(PTQFP44F)
SPGS1234/1
Weight approximately 0.35 g
Dimensions in mm

6.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
S.T.B. = shorted to BAGNDI if not used

DVSS = if not used, connect to DVSS
X = obligatory; connect as described in circuit diagram
AHVSS = connect to AHVSS

Pin No. PLCC 44-pin	Pin No. PTQFP 44-pin	Connection (if not used)	Pin Name	Type	Short Description
1	39	NC	TDI	IN	Boundary-Scan-Test Data Input
2	40	NC	TCK	IN (+Pull-up)	Boundary-Scan-Test Clock Input
3	41	NC	TDO	OUT	Boundary-Scan-Test Data Output if TAP is active (see remarks on Boundary-Scan Test)
			ALPHA	OUT	If Test Access Port (TAP) is in Test-Logic-Reset State: Alpha Key Signal (I^2C Reg. EA_{hex} bit[3] = 0)
			LLC2	OUT	If Test Access Port (TAP) is in Test-Logic-Reset State: LLC/2 = 13 MHz clock signal (I^2C Reg. EA_{hex} bit[3] = 1)
4	42	NC	HREF	OUT	Horizontal Reference
5	43	NC	VREF	OUT	Vertical Reference
6	44	NC	PREF	OUT	Programmable Interrupt
			ODD/EVEN	OUT	ODD/EVEN Frame Identifier
			I^2C-ADDR	IN	I^2C-Initialization Control by positive edge of $\overline{RES}$: PREF = 0 : I^2C device address 0 PREF = 1 : I^2C device address 1 (for more information see I^2C description)
7	1	NC	A7	OUT	Port 1 – Video Data Output
8	2	NC	A6	OUT	Port 1 – Video Data Output
9	3	NC	A5	OUT	Port 1 – Video Data Output
10	4	NC	A4	OUT	Port 1 – Video Data Output
11	5		PVDD	SUPPLY	Supply Voltage Pad Circuits
12	6	NC	PIXCLK	OUT IN	Pixel Clock I/O Synchronous mode Asynchronous mode
			I^2C-INIT	IN	I^2C-Initialization Control by positive edge of $\overline{RES}$: PIXCLK = 0 : I^2C ROM table 0 PIXCLK = 1 : I^2C ROM table 1 (for more information see I^2C description)
13	7		PVSS	SUPPLY	Supply Voltage Pad Circuits

Pin Connections and Short Descriptions, continued

Pin No. PLCC 44-pin	Pin No. PTQFP 44-pin	Connection (if not used)	Pin Name	Type	Short Description
14	8	NC	A3	OUT	Port 1 – Video Data Output
15	9	NC	A2	OUT	Port 1 – Video Data Output
16	10	NC	A1	OUT	Port 1 – Video Data Output
17	11	NC	A0	OUT	Port 1 – Video Data Output
18	12	VSS	$\overline{OE}$	IN	Output Ports Enable
19	13	NC	$\overline{HF}$ FSY LLC	OUT OUT OUT	Asynchronous Mode: FIFO half full, active low Synchronous Mode (20.25 MHz): Front Sync Synchronous Mode (13.5 MHz): 2 x PIXCLK = 27 MHz
20	14	NC	$\overline{FE}$ VACT	OUT OUT	Asynchronous Mode: FIFO empty, active low Synchronous Mode: active video
21	15	NC	B7	OUT	Port 2 – Video Data Output
22	16	NC	B6	OUT	Port 2 – Video Data Output
23	17	NC	B5	OUT	Port 2 – Video Data Output
24	18	NC	B4	OUT	Port 2 – Video Data Output
25	19	NC	B3	OUT	Port 2 – Video Data Output
26	20	NC	B2	OUT	Port 2 – Video Data Output
27	21	NC	B1	OUT	Port 2 – Video Data Output
28	22	NC	B0	OUT	Port 2 – Video Data Output
29	23	NC	SDA	OUT (Pull-down/IN)	I^2C Data
30	24	NC	SCL	OUT (Pull-down/IN)	I^2C Clock
31	25		$\overline{RES}$	IN	Reset input
32	26		VSS	SUPPLY	Supply Voltage for digital circuitry
33	27		VDD	SUPPLY	Supply Voltage for digital circuitry
34	28		XTAL2	OSC OUT	Crystal
35	29		XTAL1	OSC IN	Crystal
36	30		AVDD	SUPPLY	Supply Voltage for analog circuitry
37	31	NC	CIN	AIN	Chroma Input (SVHS)
38	32		AVSS	SUPPLY	Supply Voltage for analog circuitry

Pin No. PLCC 44-pin	Pin No. PTQFP 44-pin	Connection (if not used)	Pin Name	Type	Short Description
39	33	NC	VIN1	AIN	Video 1 or Luminance (SVHS) Input
40	34	NC	VIN2	AIN	Video 2 Input
41	35		VRT	Reference	Reference Voltage Top (ADC)
42	36	NC	VIN3	AIN	Video 3 Input
43	37		ISGND	SUPPLY	Signal Ground
44	38	NC	TMS	IN (Pull-up)	Boundary-Scan-Test Mode Select

6.3. Pin Descriptions (Pin Numbers for PLCC44)

Pins 44, 1 – JTAG Input Pins TMS, TDI (Fig. 6–6)
Mode Select and Data Input signal for the JTAG Test Access Port (TAP). These inputs have small pull-ups and input stages with Schmitt trigger characteristics.

Pin 2 – JTAG Input Pin TCK (Fig. 6–5)
Clock input pin for JTAG Test Access Port (TAP). This input has an input stage with Schmitt trigger characteristics and no pull-up.

Pin 3 – JTAG Output Pin TDO (Fig. 6–8)
Data output for JTAG Test Access Port (TAP), and output pin for the ALPHA key signal, if the TAP is in Test-Logic-Reset state. The output circuit belongs to the characteristics of TTL output driver type B.

Pins 4 to 6 – Reference Signals HREF, VREF, and PREF (Fig. 6–8)
These signals are internally generated sync signals. Their output characteristics belong to the output driver type B.

Pins 7 to 10, 14 to 17 – Video Port A (Fig. 6–8)
The output characteristics of these pins belong to the characteristics of output driver type A.

Pin 11 – Supply Voltage, Pad Circuitry PVDD

Pin 12 – Pixel Clock PIXCLK (Fig. 6–9)
This signal is either input or output depending on the selected mode. In synchronous mode it has the characteristics of TTL output driver type A. In asynchronous mode it has TTL Schmitt trigger input characteristics. PIXCLK is the reference clock for the video data transmission ports A[7:0] and B[7:0]. Moreover, the state of the PIXCLK signal at the inactive going edge of $\overline{\text{RES}}$ determines which I^{2}C_INIT table will be loaded (see section 4.9.)

Pin 13 – Ground, Pad Circuitry PVSS

Pin 18 – Output Enable Input Signal (Fig. 6–5)
The output enable input signal has TTL Schmitt trigger input characteristics. It controls the tristate condition of both video ports.

Pins 19, 20 – $\overline{\text{HF}}$, $\overline{\text{FE}}$, (Fig. 6–8)
These pins have different functionality depending on which video data output mode is selected. The output circuits belong to the characteristics of TTL output driver type A.

Pins 21 to 28 – Video Port B (Fig. 6–8)
The output characteristics of these pins belong to the characteristics of TTL output driver type B.

Pin 29 – I^{2}C Data SDA (Fig. 6–7)
This pin connects to the I^{2}C-bus data line.

Pin 30 – I^{2}C Clock SCL (Fig. 6–7)
This pin connects to the I^{2}C-bus clock line.

Pin 31 – Reset Input $\overline{\text{RES}}$ (Fig. 6–5)
A low level on this pin resets the circuit.

Pin 32 – Ground, Digital Circuitry VSS

Pin 33 – Supply Voltage, Digital Circuitry VDD

Pins 34, 35 – XTAL1 Crystal Input and XTAL2 Crystal Output (Fig. 6–11)
These pins are connected to a 20.25 MHz crystal oscillator which is digitally tuned by integrated shunt capacitances. An external clock can be fed into XTAL1. In this case clock frequency adjustment must be switched off.

Pin 36 – Supply Voltage, Analog Circuitry AVDD

Pin 37 – Chroma Input CIN (Fig. 6–10, Fig. 6–14)
This pin is connected to the S-VHS chroma signal. A resistive divider is used to bias the input signal to the middle of the converter input range. CIN can only be connected to the chroma (Video 2) AD converter. The signal must be AC-coupled.

Pin 38 – Ground, Analog Front-end AVSS

Pins 39, 40, 42 – Video Input 1–3 VIN1,VIN2,VIN3 (Fig. 6–12)
These are the analog video inputs. A CVBS, S-VHS luma signal is converted using the luma (Video 1) AD converter. The VIN1 input can also be switched to the chroma (Video 2) ADC. The input signal must be AC-coupled.

Pin 41 – Reference Voltage Top VRT (Fig. 6–13)
Via this pin, the reference voltage for the AD converters is decoupled. The pin is connected with 10 µF/47 nF to the Signal Ground Pin.

Pin 43 – Signal Ground for Analog Input ISGND
This is the high-quality ground reference for the video input signals.

6.4. Pin Configuration

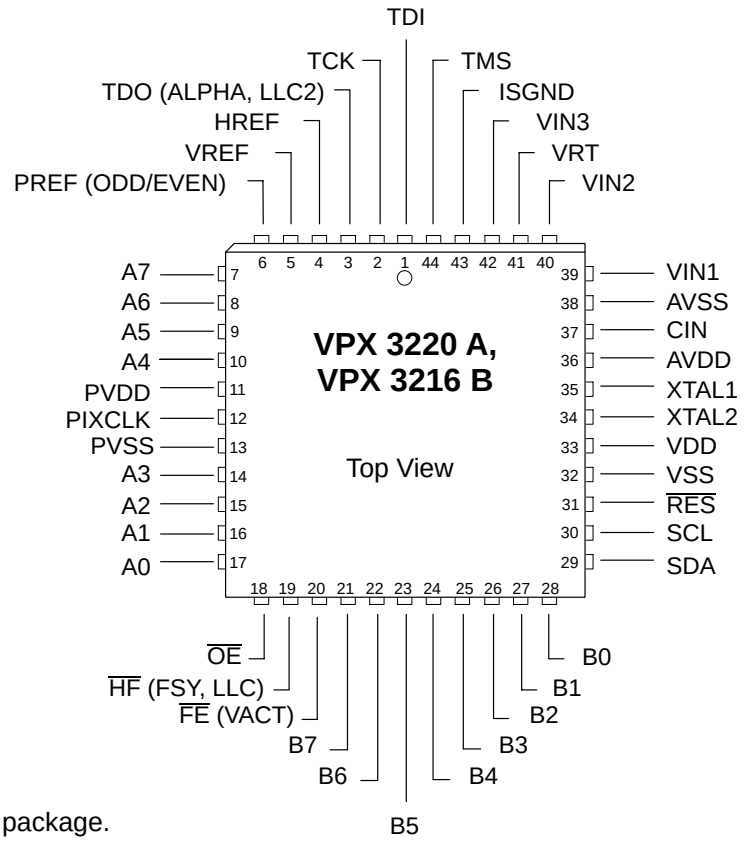


Fig. 6–3: 44-pin PLCC package.

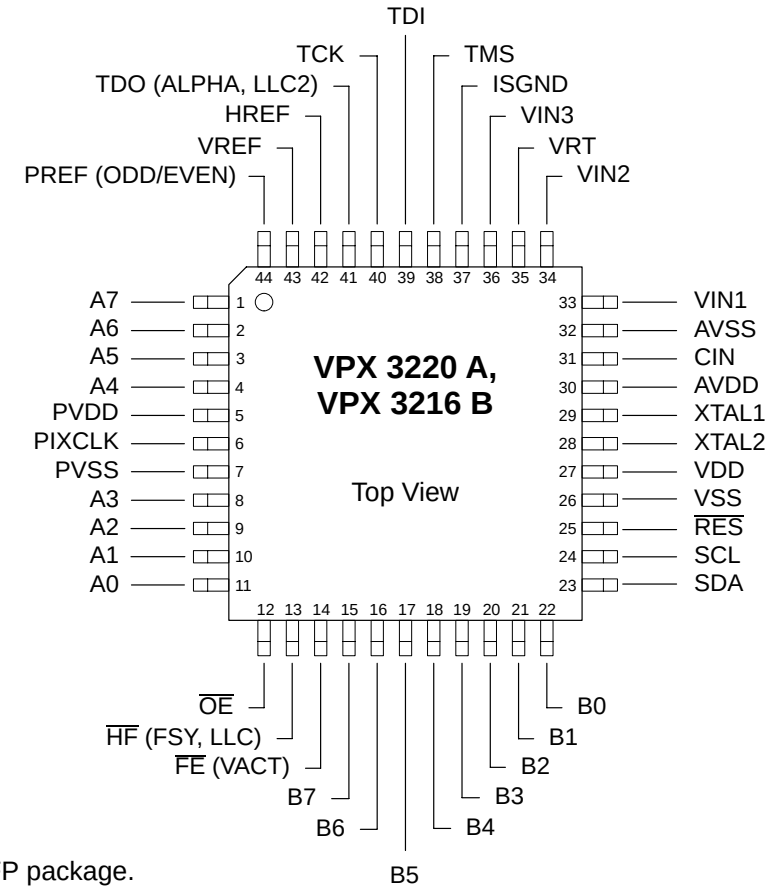


Fig. 6–4: 44-pin PTQFP package.

6.5. Pin Circuits

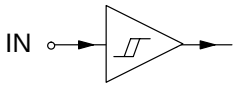


Fig. 6–5: TCK, $\overline{OE}$, $\overline{RES}$

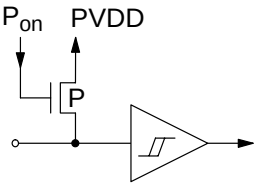


Fig. 6–6: JTAG Inputs TMS, TDI

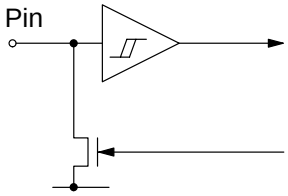


Fig. 6–7: I^2C Interface SDA, SCL

The characteristics of the Schmitt Triggers are dependent of the supply of VDD/VSS.

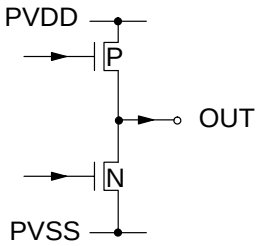


Fig. 6–8: A[7:0], B[7:0], HREF, VREF, PREF, $\overline{HF}$, $\overline{FE}$, TDO

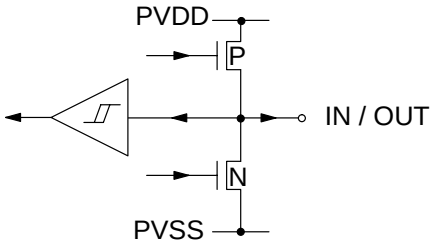


Fig. 6–9: Input/Output PIXCLK

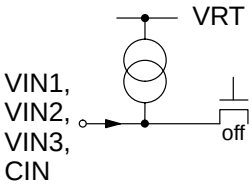


Fig. 6–10: Unselected Video Inputs

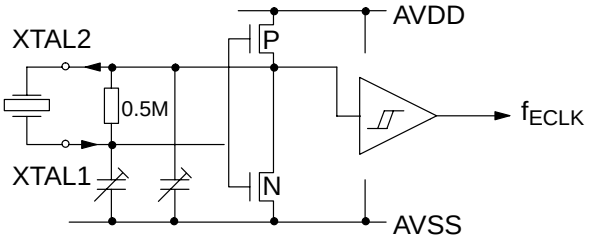


Fig. 6–11: Crystal Oscillator

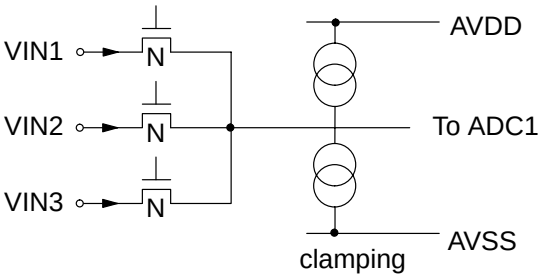


Fig. 6–12: Video Inputs ADC1

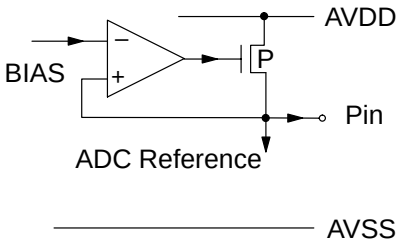
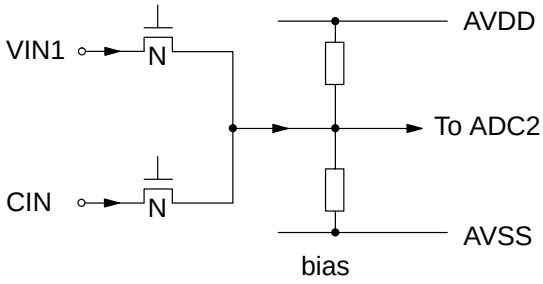
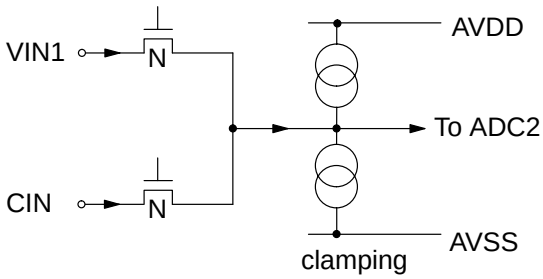


Fig. 6–13: Reference Voltage VRT





clamping or bias is selectable via I^2C reg. 33_{hex} bit[3]

Fig. 6–14: Video Inputs ADC2

6.6. Electrical Characteristics

6.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Temperature		0	65	°C
T_S	Storage Temperature		–40	125	°C
T_J	Junction Temperature		0	125	°C
V_{SUB}	Supply Voltage, all Supply Inputs		–0.3	6	V
	Input Voltage of PIXCLK, TMS, TDI		PVSS – 0.5	PVDD + 0.5 [1)]	V
	Input Voltage	TCK	PVSS – 0.5	6	V
	Input Voltage	SDA, SCL	VSS – 0.5	6	V
	Signal Swing	A[7:0], B[7:0], PIXCLK, HREF, VREF, PREF, $\overline{HF}$, $\overline{FE}$, TDO	PVSS – 0.5	PVDD + 0.5 [1)]	V
	Maximum Δ | VDD – AVDD |			0.5	V
	Maximum Δ | VSS – PVSS | Maximum Δ | VSS – AVSS | Maximum Δ | PVSS – AVSS |			0.1	V

[1)] **Note:** external voltage exceeding PVDD+0.5V should not be applied to these pins even when they are three-stated.

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Limitations due to Package Characteristics (test conditions at T_A = 65 °C and T_j = 125 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{thJC}	Thermal Resistance Junction-Case of PTQFP44		5		K/W	
R_{thA}	Thermal Resistance Ambient of PTQFP44		68		K/W	still air
P_{max}	Maximum Power Radiation of PTQFP44 due to the thermal resistance of the package			890	mW	still air, no cooling
R_{thJC}	Thermal Resistance Junction-Case of PLCC44 without internal heat sink		11		K/W	
R_{thA}	Thermal Resistance Ambient (still air) of PLCC44 without internal heat sink		55		K/W	
P_{max}	Maximum Power Radiation of PLCC44 without internal heat sink due to the thermal resistance of the package			1089	mW	still air, no cooling
R_{thJC}	Thermal Resistance Junction-Case of PLCC44 with internal heat sink		8		K/W	
R_{thA}	Thermal Resistance Ambient (still air) of PLCC44 with internal heat sink		44		K/W	
P_{max}	Maximum Power Radiation of PLCC44 with internal heat sink due to the thermal resistance of the package			1370	mW	still air, no cooling

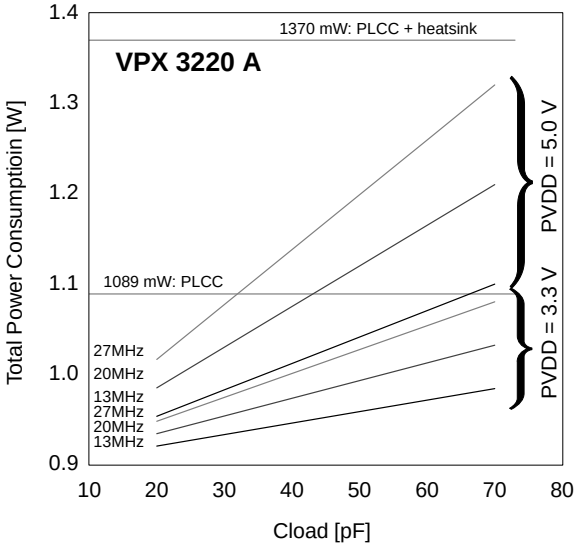
6.6.2. Recommended Operating Conditions

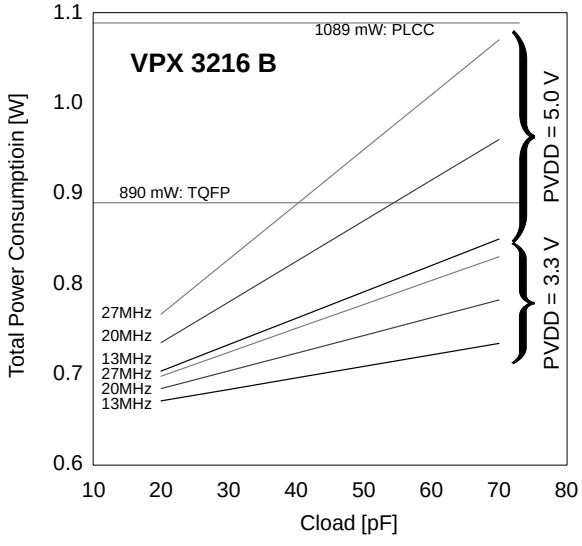
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
ASUP	Analog Supply Voltage	AVDD	4.75	5.0	5.25	V
DSUP	Digital Supply Voltage	VDD	4.75	5.0	5.25	V
PSUP	Pad Supply Voltage	PVDD	3.0	3.3	3.6	V
f_{OSC}	Clock Frequency	XTAL1, XTAL2		20.25		MHz

6.6.3. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	supply current VPX 3220 A					
	between VDD and VSS	115	135	155	mA	
	between AVDD and AVSS	35	44	53	mA	
	between PVDD and PVSS	application dependent			mA	
I_{DD}	supply current VPX 3216 B					
	between VDD and VSS		86		mA	
	between AVDD and AVSS	35	44	53	mA	
	between PVDD and PVSS	application dependent			mA	

The diagrams below illustrate some of the possible output modes and their impact on the power consumption. These values are worst case numbers in terms of number of active output drivers. Only the video data interface A[7:0] and B[7:0], and the clock signals PIXCLK have to be considered. As a first order approximation, the remaining signals have no impact on the power consumption.





Based on a worst case scenario of 18 active output pins, no static loads, and a typical power consumption.

6.6.4. Characteristics, Reset

at T_A = 0 to 65 °C, V_{SUP} = 4.75 to 5.25 V, f = 20.25 MHz for min./max. values
at T_C = 60 °C, V_{SUP} = 5 V, f = 20.25 MHz for typical values

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{RES\ EXT}$	External Reset Hold Time	50			ns	
$t_{RES\ INT}$	Internal Reset Hold Time	3.2			µs	xtal osc. is working
$t_{RES\ INT2}$	Internal Register Setup after Reset (I^2C Initialization)		200		µs	

6.6.5. Input Characteristics of $\overline{RES}$ and $\overline{OE}$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Voltage LOW	–0.5		0.8	V	
V_{IH}	Input Voltage HIGH	2.0	–	6	V	
V_{TRHL}	Trigger Level at Transition High to Low		1.2		V	
V_{TRLH}	Trigger Level at Transition Low to High		1.6		V	

6.6.6. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_A	Operating Ambient Temperature	0	–	65	°C	
f_P	Resonance Frequency	–	20.250	–	MHz	C_L = 13 pF, T_A = 25 °C
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	±20	ppm	T_A = 25 °C
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	±30	ppm	over operating temperature range with respect to frequency at 25 °C
C_0	Shunt Capacitance	3	–	7	pF	
C_1	Motional Capacitance	18	–	–	fF	
R_r	Series Resistance			30	Ω	

6.6.7. XTAL Input Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_I	Clock Input Voltage, XTAL1	1.3			V_{PP}	capacitive coupling of XTAL1, XTAL2 open

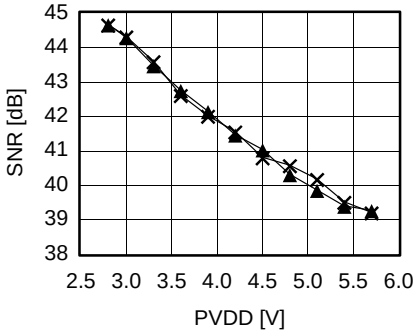
6.6.8. Characteristics, Analog Video Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Analog Input Voltage	VIN1 VIN2 VIN3 CIN	0		2.5	V	
C_{IN}	Input Capacitance				13	pF	V_{IN} = 1.5 V
C_{CP}	Input Coupling Capacitor Video Inputs	VIN1–3		680		nF	
C_{CP}	Input Coupling Capacitor Chroma Input	CIN		1		nF	

6.6.9. Characteristics, Analog Front-End and ADCs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Full Scale Input Voltage, Video 1	VIN1, VIN2, VIN3	1.8	2.0	2.2	V_{PP}	min. AGC Gain
V_{VIN}	Full Scale Input Voltage, Video 1		0.5	0.6	0.7	V_{PP}	max. AGC Gain
V_{VINCL}	Video 1 Input Clamping Level, CVBS			1.0		V	Binary Level = 68 LSB min. AGC Gain
V_{CIN}	Full Scale Input Voltage, Chroma	CIN, VIN1	1.08	1.2	1.32	V_{PP}	
V_{VINCL}	Video 2 Input Clamping Level, CVBS			1.2		V	Binary Level = 68 LSB
V_{CINB}	Video 2 Input Bias Level, SVHS Chroma		–	1.5	–	V	
R_{CIN}	Video 2 Input Resistance SVHS Chroma		1.4	2	2.6	kΩ	
	Binary Code for Open Chroma Input	VIN1 CIN		128			
Q_{CL}	Input Clamping Current Resolution	VIN1–3, CIN	–16		15	steps	
I_{CL}	Input Clamping Current per step		0.7	1	1.3	µA	
V_{VRT}	Reference Voltage Top	VRT	2.5	2.6	2.8	V	10 µF/10 nF, 1 GΩ Probe
BW	Video 1 Bandwidth			10		MHz	–3 dB for full-scale signal
BW	Video 2 Bandwidth			10		MHz	–3 dB for full-scale signal
XTALK	Crosstalk, any Two Video Inputs			–56		dB	at 1 MHz
THD	Distortion			–50	–42	dB	at 1 MHz, 5th harmonics
SNDR	Video Signal to Noise and Distortion Ratio	VIN1–3, CIN	41	45		dB	at 1 MHz, only one output
INL	Video Integral Non-Linearity, static				±1	LSB	Code Density
DNL	Video Differential Non-Linearity			±0.5	±0.8	LSB	Code Density
DG	Video Differential Gain				±3	%	300 mV_{PP}, 4.4 MHz on ramp
DP	Video Differential Phase				3	deg	300 mV_{PP}, 4.4 MHz on ramp

Dependency between SNR and Power Supply



Both ADCs are working and routed to A[7:0], and B[7:0].
All Interfaces are working with maximum driver strength
Bandwidth measurement is performed up to 5 MHz.

6.6.10. Characteristics of the JTAG Interface

TCK
Clock signal of the Test-Access Port. It is used to synchronize all JTAG functions. When JTAG operations are not being performed, this pin should be driven to VSS. The input stage of the TCK uses a TTL Schmitt Trigger.

TMS, TDI
Test Mode Selection and Test Data Input. Both signals are inputs with a TTL compatible input specification. To comply with JTAG specification they use pull-ups at their input stage. The input stage of the TMS and TDI uses a TTL Schmitt Trigger.

TDO
Test Data Output. This signal is multiplexed with the function ALPHA. The output specification conforms to the specification of the TTL output driver type B.

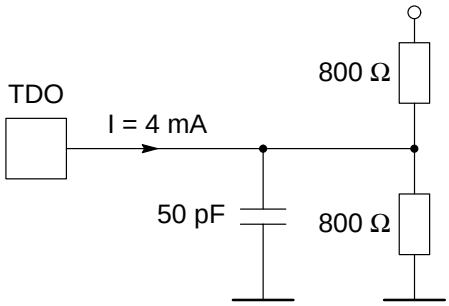


Fig. 6–15: TDO Test Circuit

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Voltage LOW			0.6	V	
V_{OH}	Output Voltage HIGH	2.4	–	PVDD	V	
A special VDD, VSS supply is used only to support the digital output pins. This means inherently that in case of tristate conditions, external sources should not drive these signals above the voltage PVDD which supplies the output pins.						
V_{IL}	Input Voltage LOW	–0.5		0.8	V	
V_{IH}	Input Voltage HIGH for input pin TCK	2.0	–	6	V	
V_{IH}	Input Voltage HIGH for input pin TDI, TMS	2.0	–	PVDD + 0.3	V	
Φ_{CYCL}	JTAG Cycle Time	100	–	–	ns	
Φ_H	TCK High Time	50	–	–	ns	
Φ_L	TCK Low Time	50	–	–	ns	
C_I	Input Capacitance of Pins TCK of Pins TDI and TMS				 pF pF	
C_O	Output Capacitance (Pin TDO)				pF	
I_{IH}	Input Pull-up Current (Pins TDI and TMS)				mA	$V_I = V_{SS}$
I_I	Input Leakage Current (Pin TCK)				µA	$V_{SS} \le V_I \le V_{DD}$
I_O	Output Leakage Current (Pin TDO)				µA	TAP controller is in TEST-RESET state
Schmitt Trigger Hysteresis This specification defines the Schmitt Trigger Hysteresis of the inputs TCK, TMS, and TDI.						
V_{TRHL}	Trigger Level at Transition High to Low		1.2		V	
V_{TRLH}	Trigger Level at Transition Low to High		1.6		V	

6.6.10.1. Timing of the Test Access Port TAP

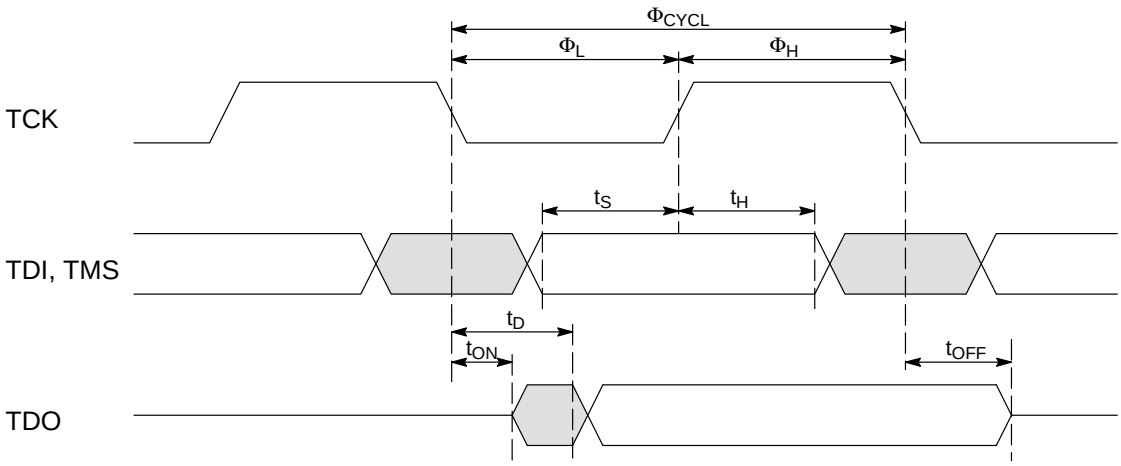


Fig. 6–16: Timing of Test Access Port TAP

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_S	TMS, TDI Setup Time		3		ns	
t_H	TMS, TDI Hold Time	3	4	4	ns	
t_D	TCK to TDO Propagation Delay for Valid Data	35	40	45	ns	
t_{ON}	TDO Turn-on Delay	35	40	45	ns	
t_{OFF}	TDO Turn-off Delay	35	40	45	ns	

6.6.11. Characteristics, I²C Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{ITF}	Input Trigger Level High to Low	SDA, SCL	1.5	0.3*VDD	2.0	V	
V_{ITR}	Input Trigger Level Low to High		2.5	0.6*VDD	3.0	V	
V_{ITH}	Input Trigger Hysteresis		0.5	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3 mA I_I = 6 mA
V_{IH}	Input Capacitance		–	–	20	pF	
I_I	Input Leakage Current		–1	–	1	µA	$V_{ss} \le V_i \le V_{dd}$
t_F	Signal Fall Time		–	–	300	ns	C_L=400 pF
t_R	Signal Rise Time		–	–	1000	ns	
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_s	Setup Time PREF to $\overline{RES}$	PREF	10			ns	
t_h	Hold Time PREF to $\overline{RES}$		10			ns	

The state of PREF and PIXCLK pins are sampled at the high (inactive) going edge of $\overline{RES}$ in order to determine two power-on parameters (see Fig. 6–17).

PREF determines the I²C address:

PREF=0: Address →1000 011_{bin}
PREF=1: Address →1000 111_{bin}

PIXLCK determines the internal ROM table which is used to initialize some of I²C and FP registers (see section 4.9.)

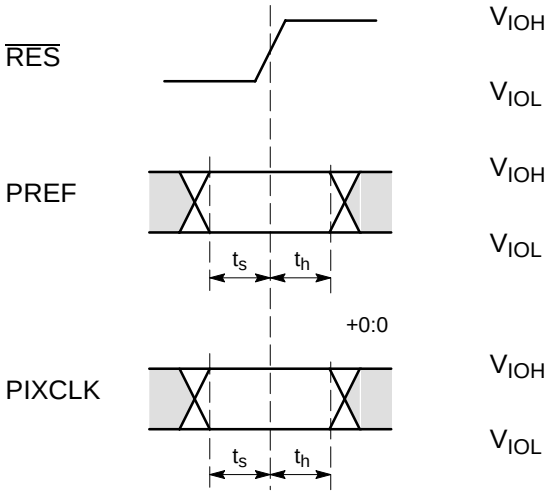


Fig. 6–17: I²C Selection: Slave Address (PREF) and Init Table (PIXCLK)

6.6.12. Digital Video Interface

The following timing specifications refer to the timing diagrams of sections 6.6.12.1., 6.6.12.2., 6.6.12.3., and 6.6.12.4. For pin driver specific values (driver types A and B) see 6.6.13.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$\overline{OE}$: see 6.6.5.						
PIXCLK: Synchronous Mode						
t_{CLK13}	Cycle Time at 13.5 MHz internal Data Rate		74		ns	
t_{CLK20}	Cycle Time at 20.25 MHz internal Data Rate		49.4		ns	
k_{PIXCLK}	Duty Cycle Φ_H / (Φ_L + Φ_H)		50		%	
t_{H2}	Output Signal Hold Time for					
	A [7:0]	15	16	18	ns	
	B [7:0]	16	17	19	ns	
	ALPHA	16	17	19	ns	
t_{H3}	Output Signal Hold Time of VACT	3	4	6	ns	
LLC (is only available in synchronous output mode at a transport rate of 13.5 MHz.)						
t_{LLC}	Cycle Time		37		ns	
Φ_H	Pulse width 'HIGH'	12	18	24	ns	
t_{H1}	Output Signal Hold Time for PIXCLK	7	10	12	ns	

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
PIXCLK: Asynchronous Mode						
V_{IL}	Input Voltage LOW	–0.5		0.8	V	
V_{IH}	Input Voltage HIGH for input pin PIXCLK	2.0	–	PVDD + 0.3	V	
V_{TRHL}	Trigger Level at Transition High to Low		1.2		V	
V_{TRLH}	Trigger Level at Transition Low to High		1.6		V	
Φ_{CYCL}	Cycle Time	35			ns	
Φ_H	Minimum Pulse width 'HIGH'		–	–	ns	
Φ_L	Minimum Pulse width 'LOW'		–	–	ns	
t_D	Delay PIXCLK(input) to					
	A [7:0]		11		ns	
	B [7:0]		20		ns	
	neg. edge of $\overline{FE}$		20		ns	
	pos. edge of $\overline{HF}$		tbd		ns	
	ALPHA		20		ns	

A special PVDD, PVSS supply is used only to support the digital output pins. This means, inherently, that in case of tristate conditions, external sources should not drive these signals above the voltage PVDD which supplies the output pins.

All timing specifications are based on the following assumptions:

– the load capacitance of the fast pins (output driver type A) is C_A = 30 pF,

– the load capacitance of the remaining pins (output driver type B) is C_B = 50 pF;

– no static currents are assumed;

– the driving capability of the pads is STR = 4, which means that 5 of 8 output drivers are enabled.

The typical case specification relates to:

– the ambient temperature is T_A = 25 °C, which relates to a junction temperature of T_J = 70 °C;

– the power supply of the pad circuits is PVDD = 3.3 V, and the power supply of the digital parts is VDD = 5.0 V.

The best case specification relates to:

– a junction temperature of T_J = 0 °C;

– the power supply of the pad circuits is PVDD = 3.6 V, and the power supply of the digital parts is VDD = 5.25 V.

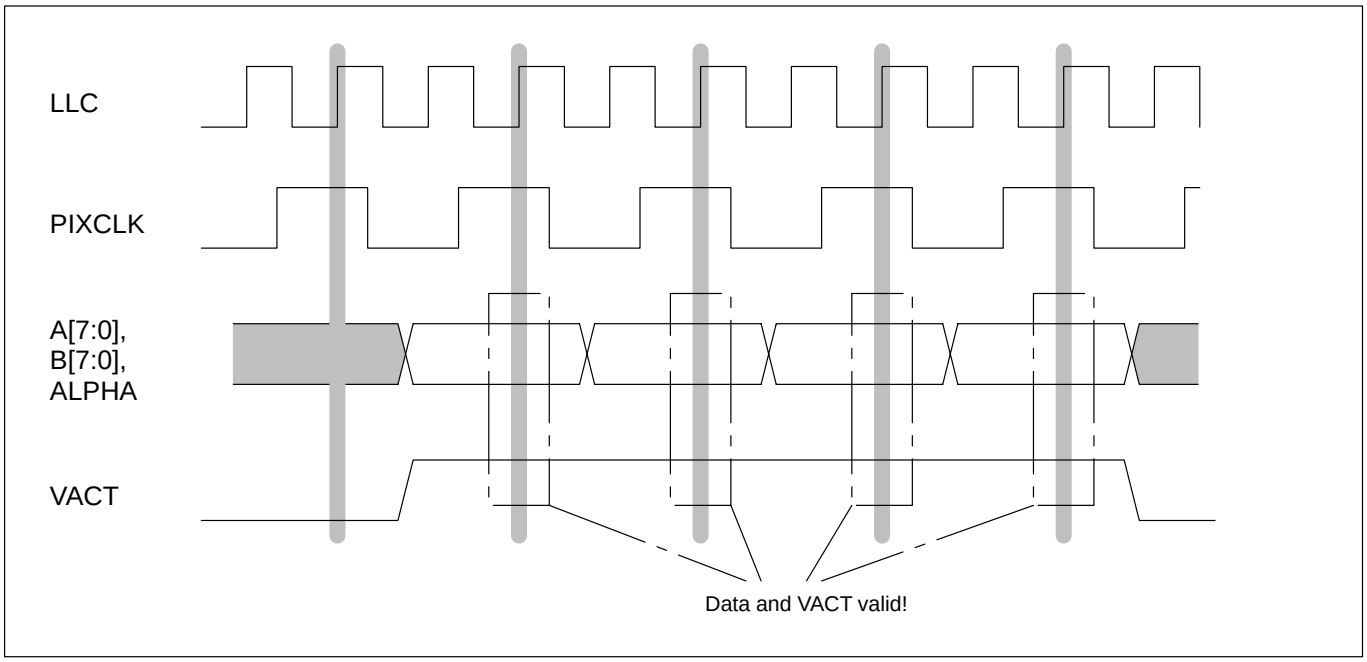
The worst case specification relates to:

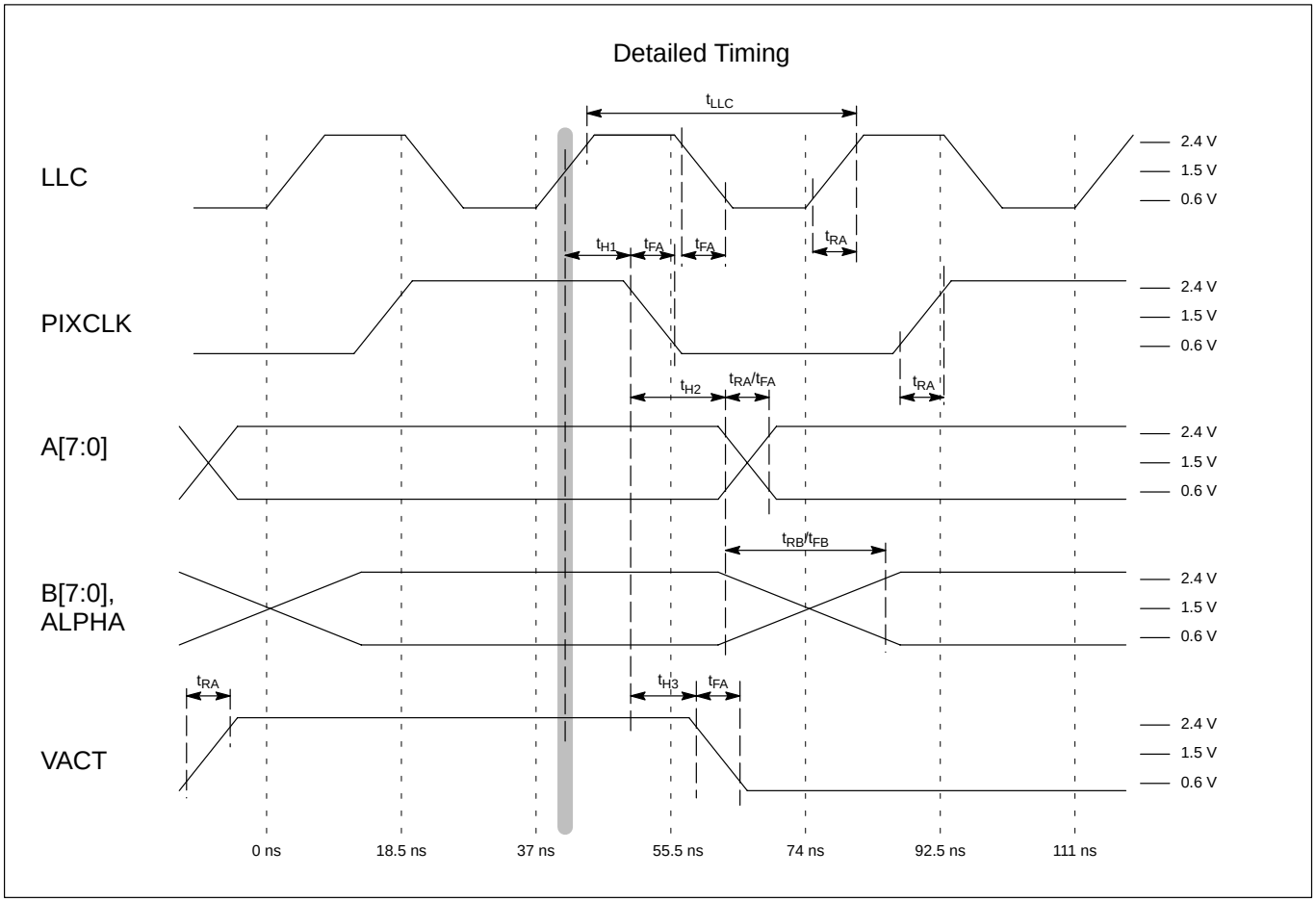
– a junction temperature of T_J = 125 °C;

– the power supply of the pad circuits is PVDD = 3.0 V, and the power supply of the digital parts is VDD = 4.75 V.

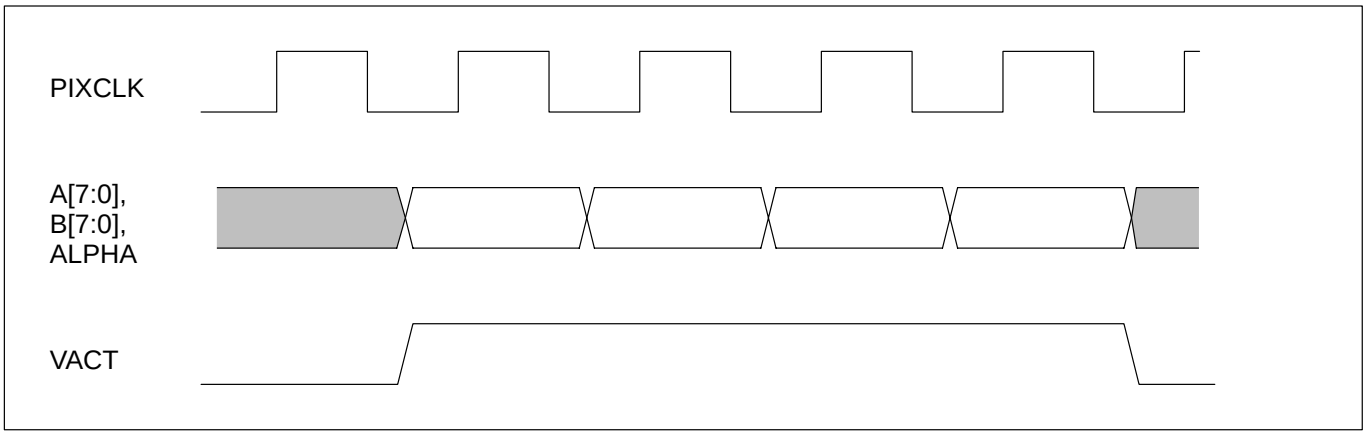
Rise times are specified as a transition between 0.6 V to 2.4 V. Fall times are defined as a transition between 2.4 V to 0.6 V.

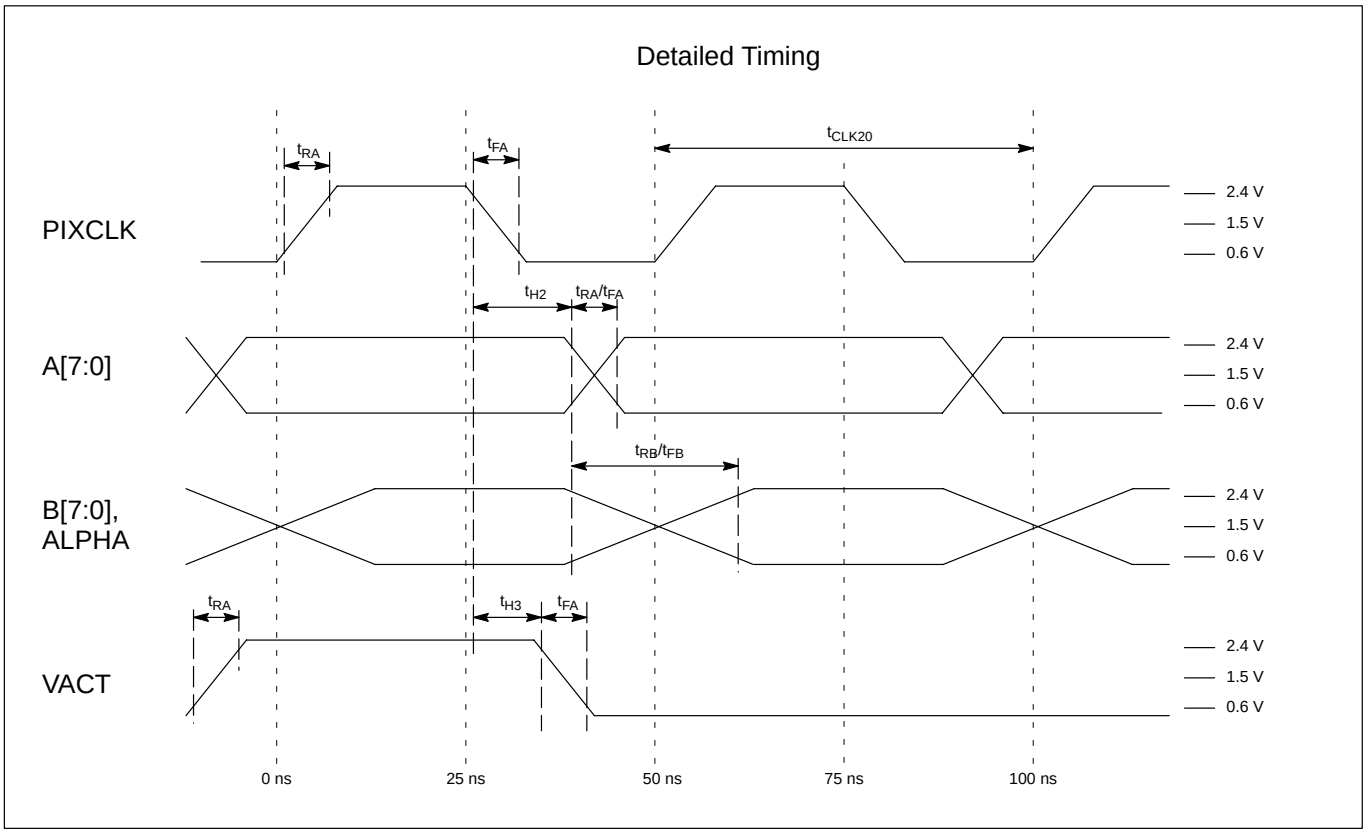
6.6.12.1. Characteristics, Synchronous Mode, 13.5 MHz Data Rate, “Single Clock”



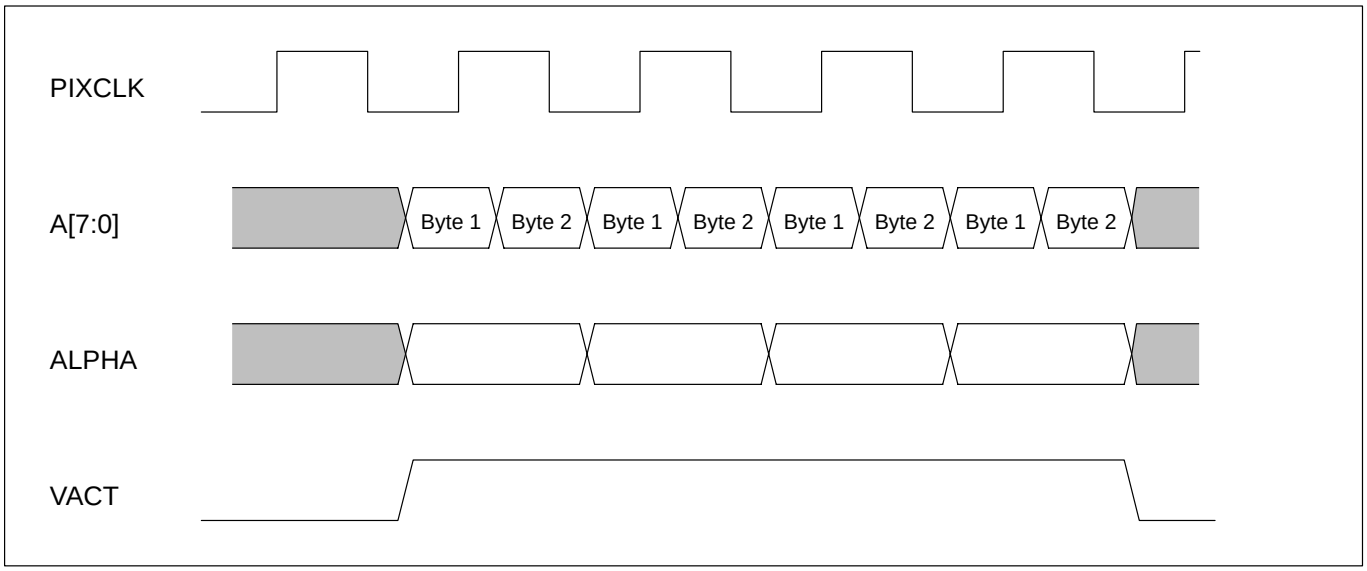


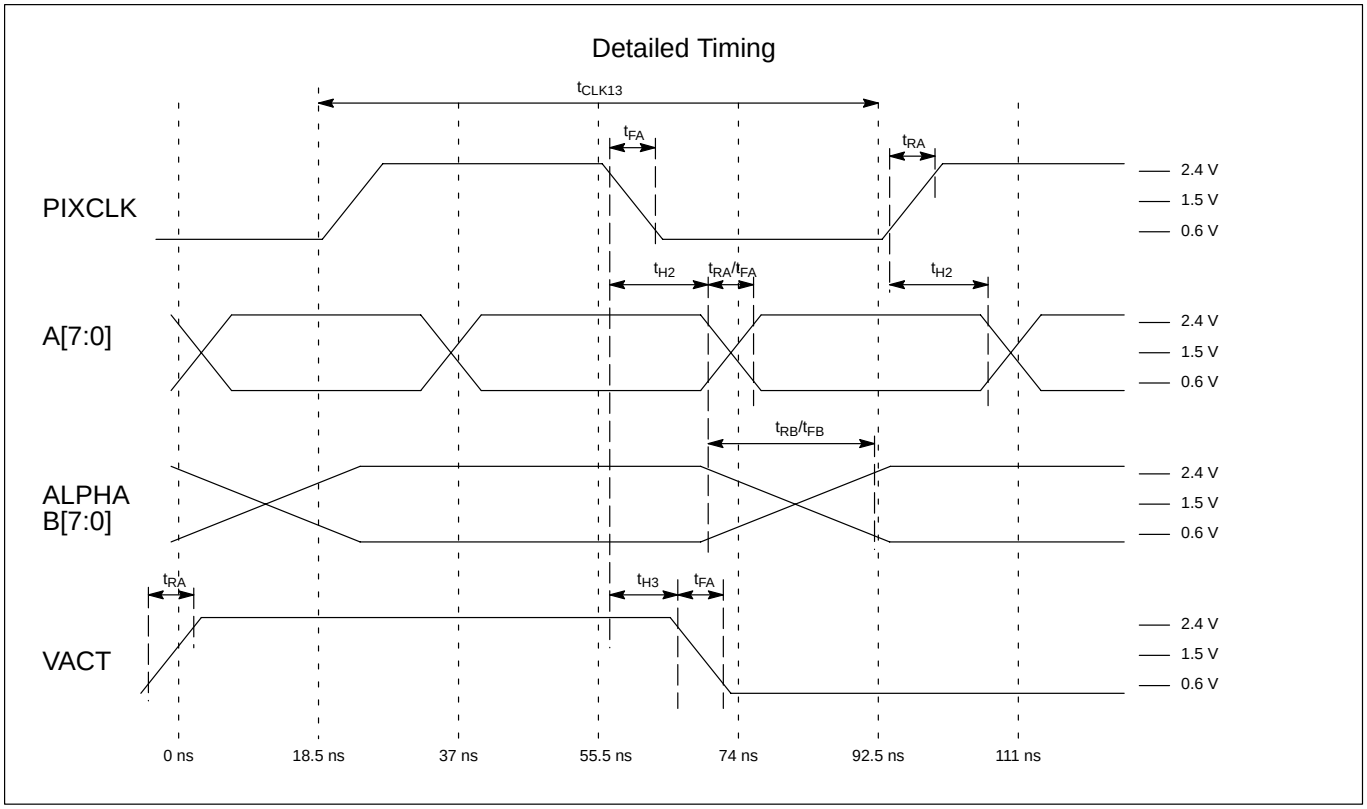
6.6.12.2. Characteristics, Synchronous Mode, 20.25 MHz Data Rate, “Single Clock”





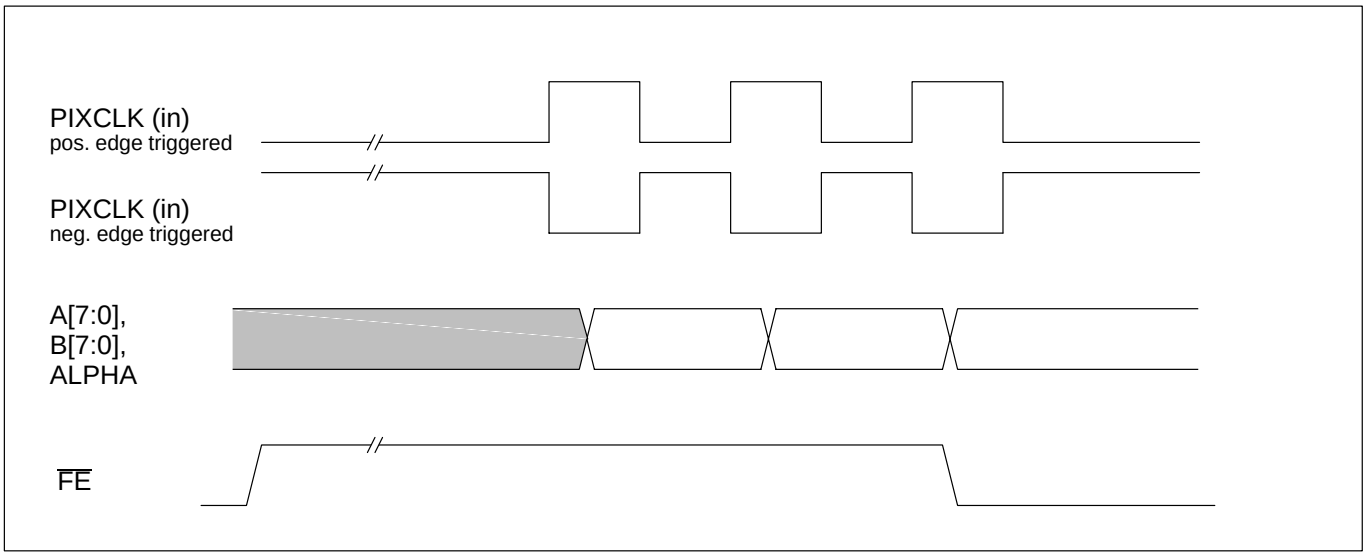
6.6.12.3. Characteristics, Synchronous Mode, 13.5 MHz Data Rate, “Double Clock”

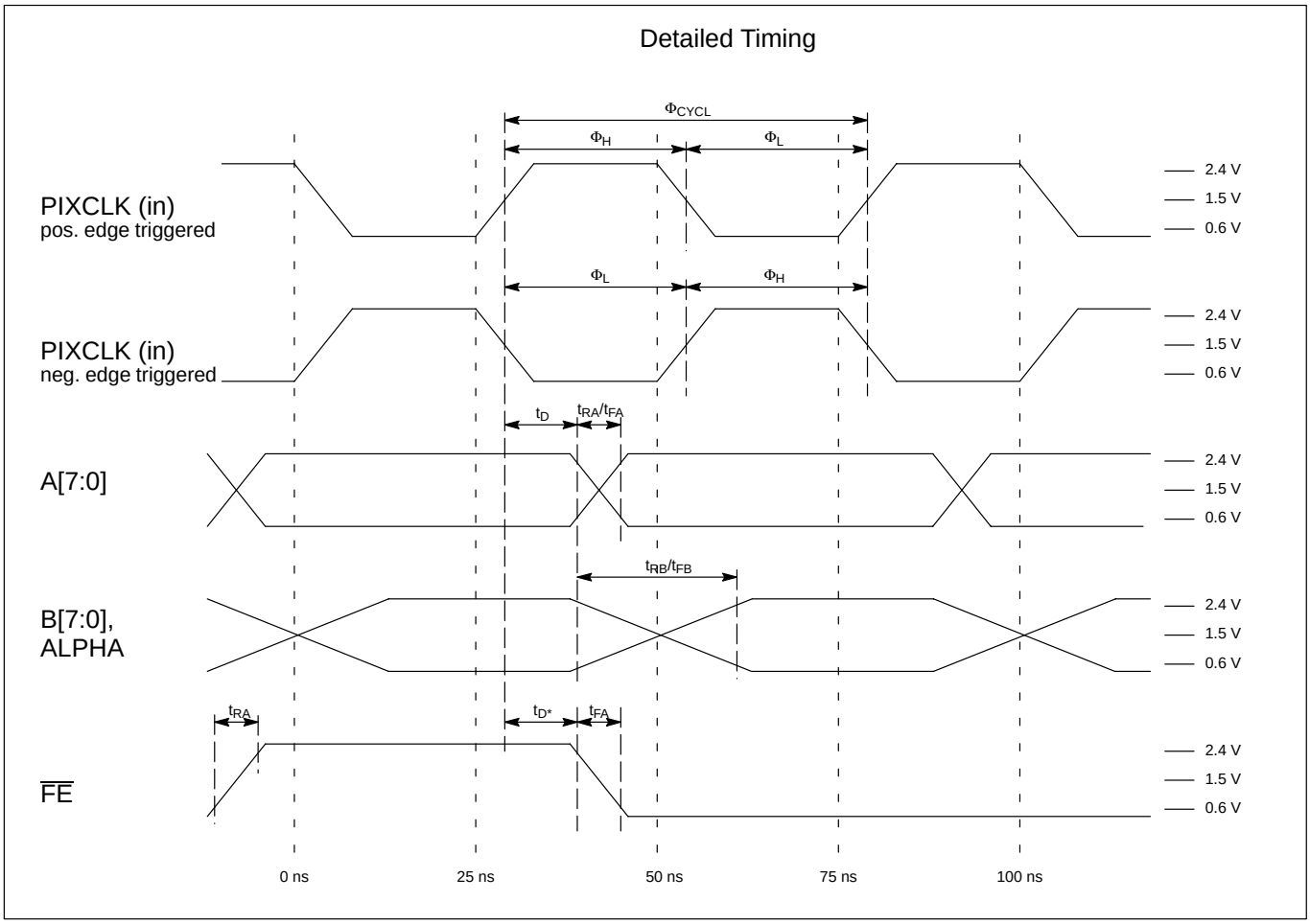




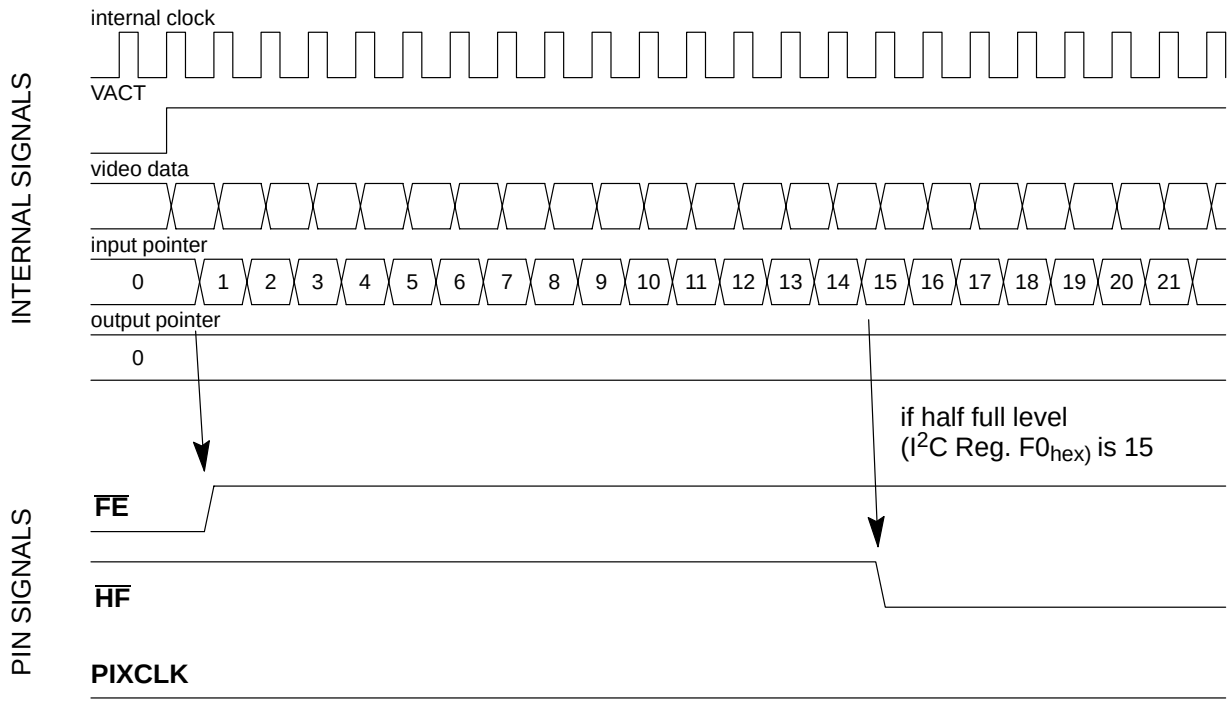
6.6.12.4. Characteristics, Asynchronous Mode

If the digital video interface is in asynchronous mode, then the data transfer is controlled by an external clock signal. Therefore, the interface signal PIXCLK is used as an input signal. The video data refers to the positive or negative slope of PIXCLK, depending on the setting of the I^2C reg. $F1_{hex}$ bit[2]. In asynchronous mode, the PIXCLK is always a single edge clock. If luma and chroma data should be transferred via A-port (double clock mode), then each data requires a complete clock cycle of PIXCLK. A complete pixel (luma and chroma) needs two complete clock cycles.

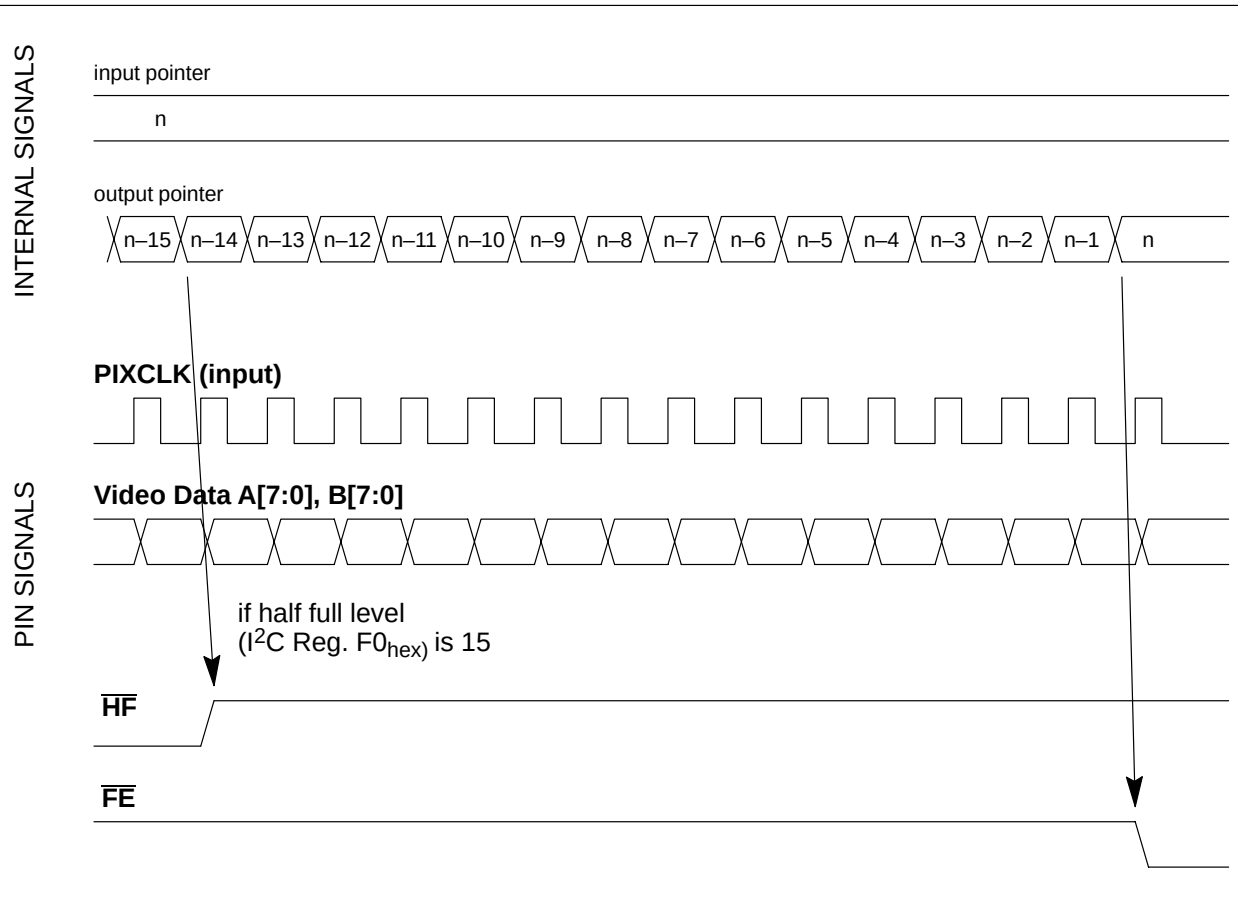




Start and End of an Asynchronous Transfer Mode



Note: The positive slope of $\overline{FE}$ and the negative slope of $\overline{HF}$ is determined by internal timing! There is no relation to any pin signal.



6.6.13. Characteristics, TTL Output Driver

The drivers of the output pads are implemented as a parallel connection of 8 tristate buffers of the same size. The buffers are enabled depending on the desired driver strength. This opportunity offers the advantage of adapting the driver strength to on-chip and off-chip constraints, e.g. to minimize the noise resulting from steep signal transitions.

The driving capability/strength is controlled by the state of the two I^2C registers $F8_{hex}$ and $F9_{hex}$.

F8	Pad Driver Strength – TTL Output Pads Type A
	bit [2:0] : Driver strength of Port A[7:0]
	bit [5:3] : Driver strength of PIXCLK, $\overline{HF}$ and $\overline{FE}$
	bit [7:6] : additional PIXCLK driver strength strength = bit [5:3] | {bit[7:6], 0}
F9	Pad Driver Strength – TTL Output Pads Type B
	bit [2:0] : Driver strength of Port B[7:0]
	bit [5:3] : Driver strength of HREF, VREF, PREF and ALPHA/TDO

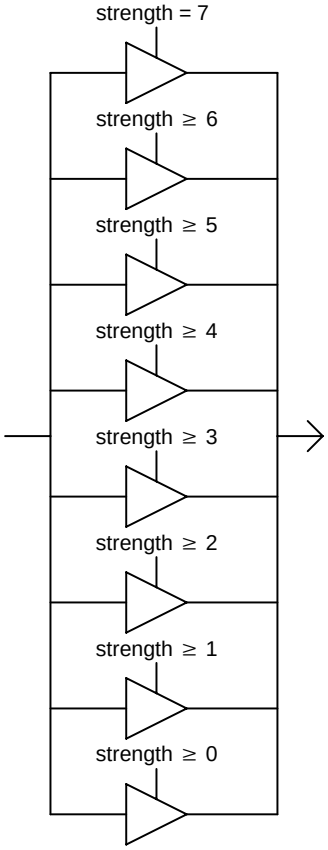


Fig. 6–18: Block diagram of the output stages

6.6.13.1. TTL Output Driver Type A

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_A		65	RT	0	°C	Ambient Temperature
VDD, AVDD		4.75	5.0	5.25	V	Supply
PVDD		3.0	3.3	3.6	V	Pad Supply
t_{RA}	Rise time	2	5	10	ns	C_l = 30 pF, strength = 5
t_{FA}	Fall time	2	5	10	ns	C_l = 30 pF, strength = 5
$I_{OH}(0)$	Output High Current (strength = 0)	–1.37	–2.25	–2.87	mA	V_{OH} = 0.6 V
$I_{OL}(0)$	Output Low Current (strength = 0)	1.75	3.5	4.5	mA	V_{OH} = 2.4 V
$I_{OH}(7)$	Output High Current (strength = 7)	–11	–18	–25	mA	V_{OH} = 0.6 V
$I_{OL}(7)$	Output Low Current (strength = 7)	14	28	36	mA	V_{OH} = 2.4 V
C_O	High-Impedance Output Capacitance		5	8	pF	

6.6.13.2. TTL Output Driver Type B

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_A		65	RT	0	°C	Ambient Temperature
VDD, AVDD		4.75	5.0	5.25	V	Supply
PVDD		3.0	3.3	3.6	V	Pad Supply
t_{RB}	Rise time	6	12	25	ns	C_l = 50 pF, strength = 5
t_{FB}	Fall time	6	12	25	ns	C_l=50 pF, strength = 5
$I_{OH}(0)$	Output High Current (strength = 0)	–0.63	–1.13	–1.38	mA	V_{OH} = 2.4 V
$I_{OL}(0)$	Output Low Current (strength = 0)	0.81	1.81	2.38	mA	V_{OH} = 0.6 V
$I_{OH}(7)$	Output High Current (strength = 7)	–5	–9	–12	mA	V_{OH} = 2.4 V
$I_{OL}(7)$	Output Low Current (strength = 7)	6.5	14.5	19	mA	V_{OH} = 0.6 V
C_O	High-Impedance Output Capacitance		5	8	pF	

6.6.14. Characteristics, Enable/Disable of Output Signals

In order to enable the output pins of the VPX to achieve the high impedance/tristate mode, various controls have been implemented. The following paragraphs give an overview of the different tristate modes of the output signals. It is valid for all output pins, except the XTAL2 (which is the oscillator output) and the VRT pin (which is an analog reference voltage).

BS (Boundary-Scan) Mode:

The tristate control by the test access port TAP for boundary-scan has the highest priority. Even if the TAP-controller is in the EXTEST or CLAMP mode, the tristate behavior is only defined by the state of the different boundary scan registers for enable control. If the TAP controller is in HIGHZ mode, then all output pins are in tristate mode independently of the state of the different boundary scan registers for enable control.

RESET State:

If the TAP-controller is not in the EXTEST mode, then the RESET-state defines the state of all digital outputs. The only exception is made for the data output of the boundary scan interface TDO. If the circuit is in reset condition ($\overline{RES}$ = 0), then all output interfaces are in tristate mode.

I^2C Control:

The tristate condition of groups of signals can also be controlled by setting the I^2C-Register $F2_{hex}$. If the circuit is neither in EXTEST mode nor RESET state, then the I^2C-Register $F2_{hex}$ defines whether the output is in tristate condition or not. The I^2C-Register #F1 uses different bits for different groups of outputs (see "I^2C-Register Table").

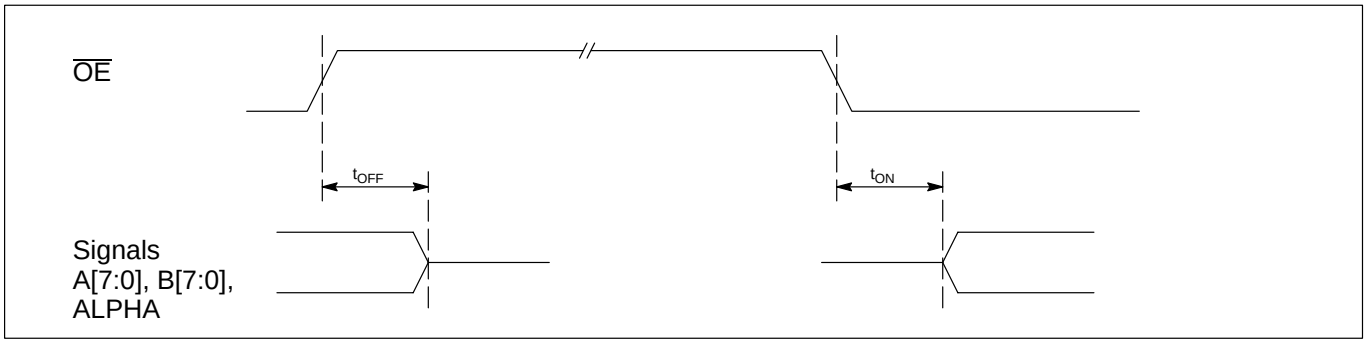
Output Enable Input $\overline{OE}$:

The output enable signal $\overline{OE}$ only effects the video output ports. If the previous three conditions do not cause the output drivers to go into high impedance mode, then the $\overline{OE}$ signal defines the driving conditions of the video data ports.

EXTEST	RESET	I^2C	OE#	Driver Stages
active	–	–	–	Output driver stages are defined by the state of the different boundary-scan enable registers.
inactive	active	–	–	Output drivers are in high impedance mode.
inactive	inactive	= 0	–	Output drivers are in high impedance mode. PIXCLK is working.
inactive	inactive	= 1	–	Output drivers HREF, VREF, PREF, $\overline{FE}$, $\overline{HF}$ are working.
inactive	inactive	= 1	= 1	Output drivers of ALPHA, A[7:0], B[7:0], and C[7:0] are in high impedance mode.
inactive	inactive	= 1	= 0	Outputs ALPHA, A[7:0], B[7:0], and C[7:0] are working

Remark: EXTEST mode is an instruction conforming to the standard for Boundary-Scan Test IEEE 1149.1 – 1990

Output Enable by Pin $\overline{OE}$



Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Voltage LOW	–0.5		0.8	V	
V_{IH}	Input Voltage HIGH for Input pins $\overline{OE}$, $\overline{RES}$	2.0	–	6	V	
V_{TRHL}	Trigger Level at Transition High to Low		1.2		V	
V_{TRLH}	Trigger Level at Transition Low to High		1.6		V	
t_{ON}	Output Enable $\overline{OE}$ of A[7:0], B[7:0], ALPHA		6		ns	
t_{OFF}	Output Disable $\overline{OE}$ of A[7:0], B[7:0], ALPHA		8		ns	

Video Pixel Decoder Family Addendum

1. Introduction for Addendum

VPX 3214C has two additional features compared to the VPX 3220A and VPX 3216B:

– another output timing mode called NewVACT and

– low power mode.

2. New Output Timing – NewVACT

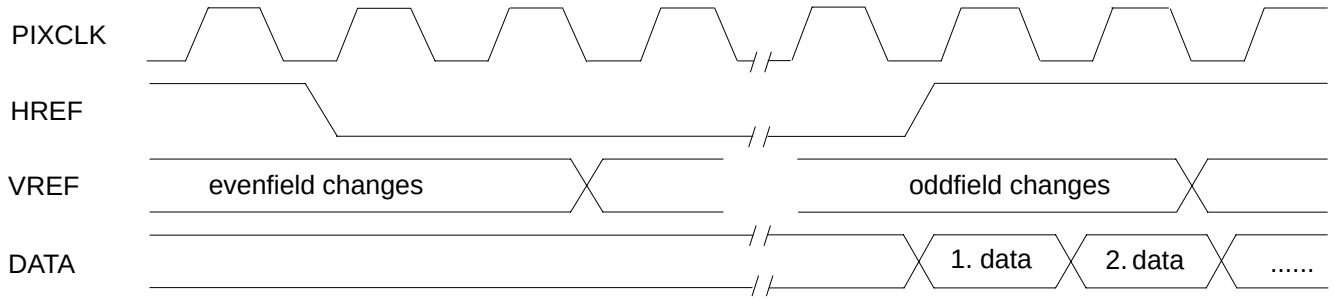
The VPX family operates with a system and sampling clock of 20.25 MHz. When the oscillator is not locked to the line frequency of the processed video signal, the number of samples per video scan line can vary from line to line. The HREF signal marks the active video line and has a fixed width of 1056 clocks. The inactive part of the HREF can therefore vary in length. The same principle applies to the VACT signal, the difference being that the active length of VACT equals the number of output pixels times transport rate of either 20.25 or 13.5 MHz. This behavior of HREF and VACT signals is well suited for the systems using state machines to handle these signals and data delivered from VPX. On the other hand this behavior causes problems in case the system uses plain counters to decide when to strobe the data. These systems require that the inactive period of HREF also has a fixed length: they use the inactive going edge of HREF to reset their counters, count afterwards a certain amount of clocks and then strobe the preprogrammed number of data almost regardless of the state of VACT signal. That's why this new timing mode was introduced.

In this mode signal at VACT pin has an unpredictable behavior and NewVACT signal is available at the HREF pin carrying all the information. It goes inactive, stays inactive for the programmable number of transport rate clocks. This inactive phase is at least 8 clocks long and can be extended in clock units to the maximum length of 23 by writing the field [3:0] of the OFIFO register (I^2C address 0xF0). After that NewVACT goes active exactly before the first valid video data, so it still can be used as qualifier for the start of data. It stays active for the rest of the line regardless of the number of valid video data, so it can not be used as the end-qualifier. The system using the data has to count properly and strobe only the valid data.

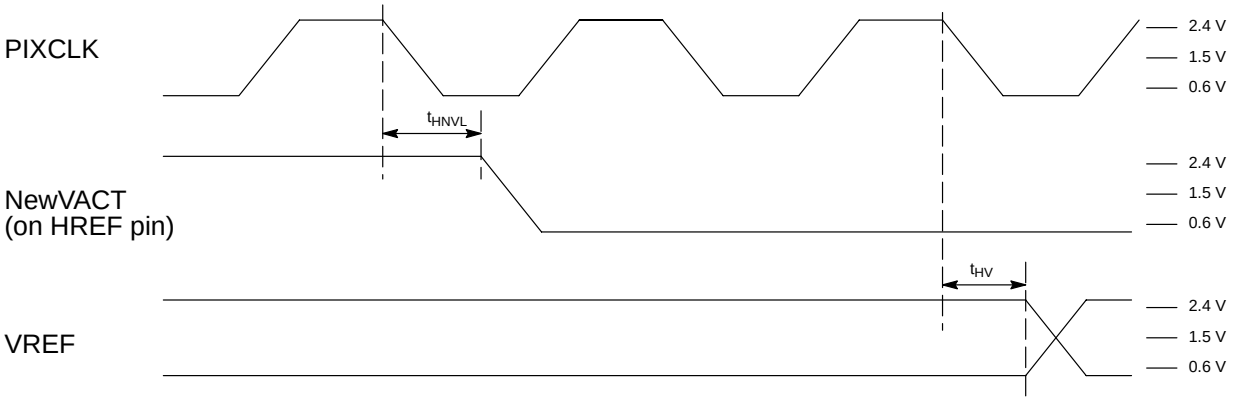
After reset, the VPX operates in its usual output timing mode. There are two registers controlling the new mode. The FP register is used to switch it on and off and I^2C register is used to control the length of the HREF inactive period.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{HNVL}	Hold Time of inactive going NewVACT after PIXCLK		20		ns	
t_{HNVH}	Hold Time of active going NewVACT after PIXCLK		15		ns	
t_{HV}	Hold Time of VREF change after PIXCLK		10		ns	

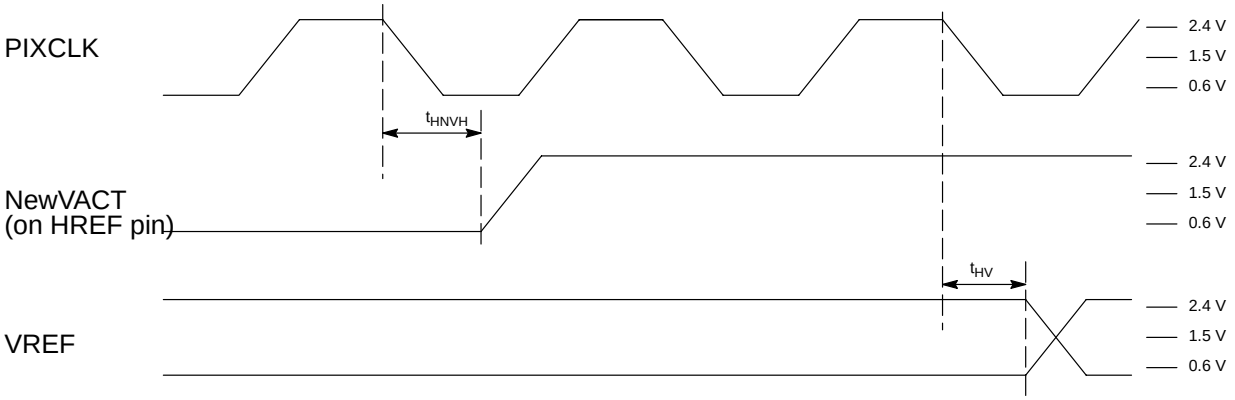
NewVACT–Timing (13.5/20.25MHz)



Detailed Timing – inactive going NewVACT and both VREF edges in Even Field



Detailed Timing – active going NewVACT and both VREF edges in Odd Field



I²C Reg. Address	Number of Bits	Mode	Function	Name
F0	8	w	Output FIFO	OFIFO
			FIFO Control: (only available in Asynchronous Mode) bit [4:0] : FIFO Flag – Half Full Level (interface signal $\overline{HF}$)	hfull
			NewVACT Control: (only available in Synchronous Mode) **bit [3:0] : Additional length of NewVACT inactive period.** **Total length in clocks equals 8 + bit[3:0]** **bit [4] : reserved (must be set to zero)**	
			bit [7:5] : Bus Shuffler 000 Out[23:0] = In[23:0] 001, 010 Out[23:0] = In[7:0, 23:8] 011 Out[23:0] = In[15:0, 23:16] 100 Out[23:0] = In[15:8, 23:16, 7:0] 101, 110 Out[23:0] = In[7:0, 15:8, 23:16] 111 Out[23:0] = In[23:16, 7:0, 15:8] Meaning: In[23:0] : Data from Color Space Stage Out[23:0] : Data to Output FIFO	shuf

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

3. Low power mode

In order to accommodate power consumption critical applications, low power mode is introduced. It can be turned on and off through the I²C register 0xAA. There are three levels of low power. When any of them is turned on, VPX waits for at least one complete video scan line in order to complete all internal tasks and then goes into three-state mode. The exact moment is not precisely defined, so care should be taken to deactivate the system using VPX data before the end of the video scan line in which VPX is switched into low power mode. During the low power mode all the I²C and FP registers are preserved, so that VPX restores its normal operation as soon as low power mode is turned off without need for any reinitialization. On the other hand all the I²C and FP registers can be read / written as usual. The only exception is the third level (value of 3 in I²C register 0xAA) of low power. In that mode, I²C speeds above 100 kbit/sec are not allowed. In modes 1 and 2, I²C can be used up to the full speed of 400 kbit/sec.

I²C Reg. Address	Number of Bits	Mode	Function	Name
AA	8	w	Low power	
			bit [1:0] : Low power 00 active mode 01 outputs three–stated; clock divided by 2; I²C full speed 10 outputs three–stated; clock divided by 4; I²C full speed 11 outputs three–stated; clock divided by 8; I²C only up to 100 kbit/sec	lowpow

The control register modes are
– w: write/read register
– r: read-only register
– d: register is double latched
– v: register is latched with vsync
– A: register is available only in VPX 3220 A; VPX 3216 B returns valid ACK, although no internal action is performed

The mnemonics used in the Intermetall VPX demo software are given in the last column.

4. Data Sheet History

1. Data sheet “VPX 3220 A, VPX 3216 B Video Pixel Decoder”, Aug. 25, 1995, 6251-368-1PD: First preliminary release of the data sheet.

2. Data sheet “VPX 3220 A, VPX 3216 B, VPX 3214 C Video Pixel Decoders”, July 1, 1996, 6251-368-2PD: Second preliminary release of the data sheet. Major changes:

– VPX 3214 C has been included

– Fig. 6–1: package dimensions changed

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