Advance Product Information

VSC6501

SMPTE-292M Reclocker and Cable Driver at 1.485 Gb/s

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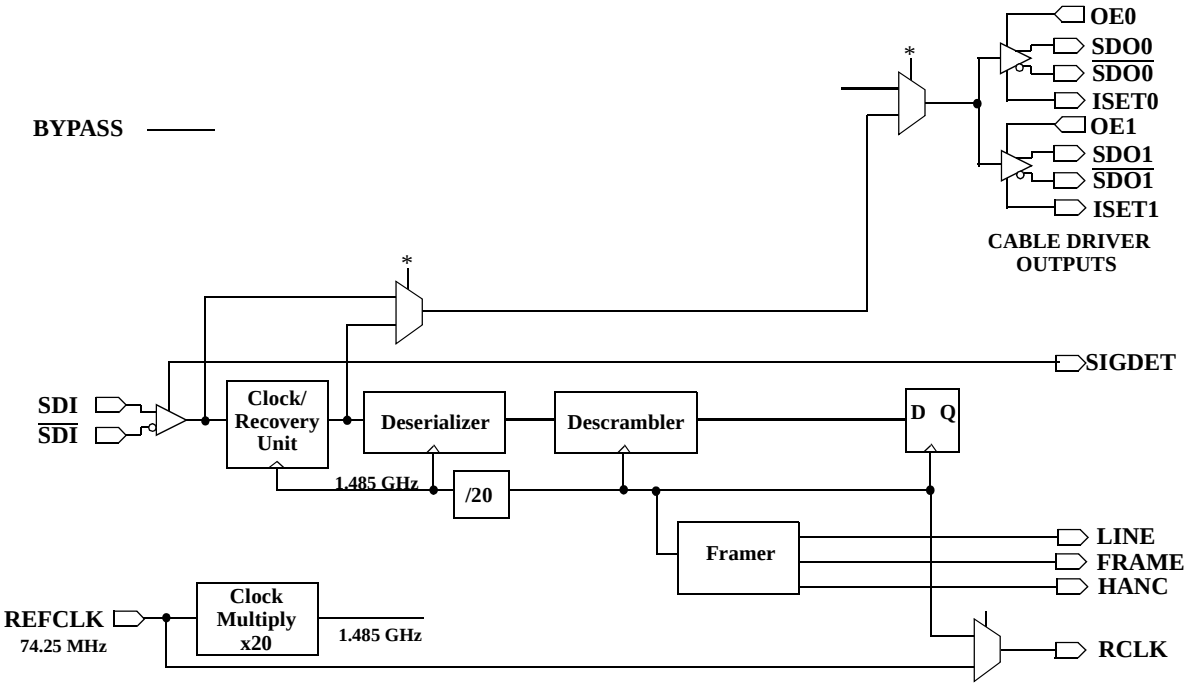
Features

- Compliant with SMPTE-292M @ 1.485Gb/s
- Clock and Data Recovery
- 2 or 4 user Configurable 75 ohm cable driver outputs
- CRU BYPASS mode for SMPTE 259M or other data rates
- Buffered REFCLK output for distribution to additional devices
- 3.3V, Low Power -- 800 mW typical
- 64-pin, 10x10x1.0mm Exposed Pad TQFP

General Description

The VSC6501 is a SMPTE-292M compatible Reclocker with 2 or 4 user configurablable 75 ohm Cable Driver outputs which operate at 1.485Gb/s. HDTV serial data on the SDI/$\overline{\text{SDI}}$ inputs is recovered and retransmitted on the SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$ outputs. The CRU portion of the reclocker may be bypassed for operation with non-HDTV data rates. The VSC6501 can be used to build routing switchers and video distribution amplifiers.

VSC6501 Reclocker Block Diagram



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Reclocker Functional Description

Clock Multiplier Unit (CMU)

The CMU generates the internal 1.485 GHz baud rate clock from the 74.25 MHz TTL REFCLK input. The rising edges of the REFCLK are used by a PLL which multiplies the frequency by a factor of 20. An off-chip 0.1uF capacitor sets the loop bandwidth of the CMU. REFCLK should be a high quality, low jitter signal with sharp rise times in order to minimize the amount of jitter transferred from the REFCLK through the CMU to the serializer. Although not shown on the block diagram, the digital CRU requires the baud rate clock of the CMU for proper operation.

REFCLK is also buffered onto the RCLK output allowing multiple devices to be daisy-chained in order to simplify REFCLK distribution to an array of devices.

Serial Input

The differential PECL-style input, SDI/$\overline{\text{SDI}}$, is the input source for 1.485 Gb/s SMPTE 292M data. An analog signal detector monitors the input signal for valid amplitude and outputs status on the SIGDET pin. If SIGDET is HIGH, the differential input swing is greater than 400 mV. If SIGDET is LOW, the differential swing is below 200 mV. If the input swing is between 200 and 400 mV, the SIGDET output is indeterminate. The SIGDET function is disabled in Serializer mode and will output a LOW.

Clock Recovery Unit

The serial data on the SDI/$\overline{\text{SDI}}$ input is sent to the digital Clock Recovery Unit (CRU) which extracts the clock and retimes the data. This digital CRU is completely monolithic and requires no external components. Furthermore, it automatically locks onto data when present and locks to REFCLK when data is not present. This eliminates the need for the system to control the CRU.

Descrambler and NRZI Decoder

The VSC6501 contains a descrambler which processes the recovered serial data and outputs unscrambled serial data from the deserializer. The serial scrambled data is descrambled/NRZI decoded assuming data has NRZI encoded with the following combined generator polynomial: $G(x)=(x^9+x^4+1)(x+1)$. Descrambling is enabled with the SCREN input is HIGH and disabled when LOW.

Pattern Detector

The VSC6501 monitors the serial data stream for SAV/EAV characters. These characters should be located within each line of video data. If SAV/EAV is not detected within the period of one line, the Framer sends a signal to the Deserializer to shift the data one bit. The Frame then looks for SAV/EAV and the process repeats until properly detected. Without these patterns, serial data is not aligned in any way with the parallel outputs. The Framer outputs a once-per-line (LINE) and a once-per-frame (FRAME) signal indicating the detection of the proper synchronization pulse in the data.

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Table 1: Reclocker Logic Signals

SIGNAL	*FUNCTION*
292M	292M Output: When HIGH, indicates that the output of the CRU is a SMPTE-292M style signal. This output combines the analog signal detect with a state machine which monitors SAV/EAV events. If 4000 words occur without an SAV/EAV, then this output goes LOW to indicate invalid data. This output goes HIGH if the analog signal detection is asserted and an SAV/EAV is located within the last 4000 words.
BYPASS	BYPASS Input: When HIGH, SDI/$\overline{\text{SDI}}$ are routed around the CRU directly to the SDO0/SDO1 outputs. When LOW, the output of the CRU is sent to SDO0/SD)1 outputs.

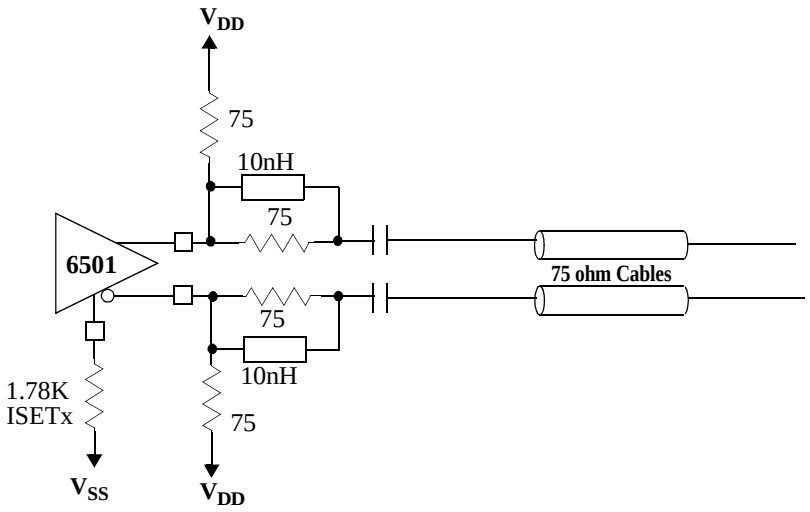
Table 2: Reclocker Operation

SIGNAL	*RECLOCKER Operation*
292M BYPASS	Active Active
O0/O1 Serial Outputs	SOURCE IS CRU SDI/$\overline{\text{SDI}}$
RCLK Output	BUFFERED REFCLK
CRU Bypass Mux	SDI/$\overline{\text{SDI}}$ GOES TO SDO0/SDO1
SDI/$\overline{\text{SDI}}$ Serial Input	ACTIVE
SIGDET Output	ACTIVE
FRAME Output	ACTIVE
1.001 Output	ACTIVE
LINE Output	ACTIVE
HANC Output	ACTIVE

Application Information

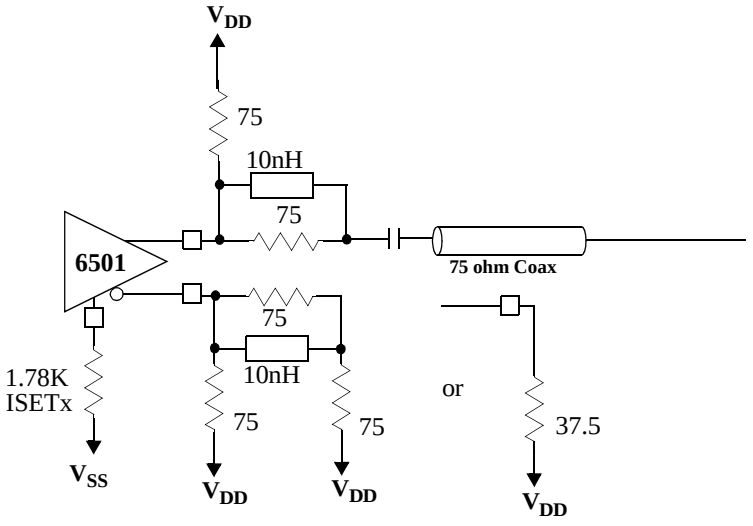
The VSC6501 cable driver output is intended to fully comply with the SMPTE 292M cable driver specifications. This includes an 800mV swing and a return loss of less than -15dB. The circuit shown below shows how to connect the output of the VSC6501to the 75 ohm cable and downstream device. The output of the VSC6501 is actually 1200mV. The output termination circuit shown below attenuates the output signal to 800mV and ensures a return loss better than -15dB. The ISET resistor is 1.78K

Figure 1: High Speed Interconnect Example (Differential)



NOTE: All resistors are 1%
WARNING: SUBJECT TO CHANGE

Figure 2: High Speed Interconnect Example (Single Ended)



NOTE: All resistors are 1%
Optional use of external Voltage Reference provides tighter swing tolerance

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The output swing of the VSC6501 is controlled through the ISETx pins and a VREF input. By connecting an 1.78K ohm resistor, 1%, between VSS and ISETx the output swing will be controlled to within 800mV +/- 7%. An optional bandpass voltage reference may be used to further tighten the output swings by accurately driving the VREF input.

Figure 3: REFCLK Timing Waveforms

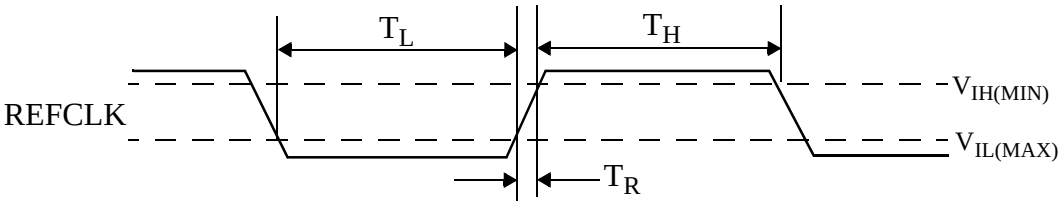
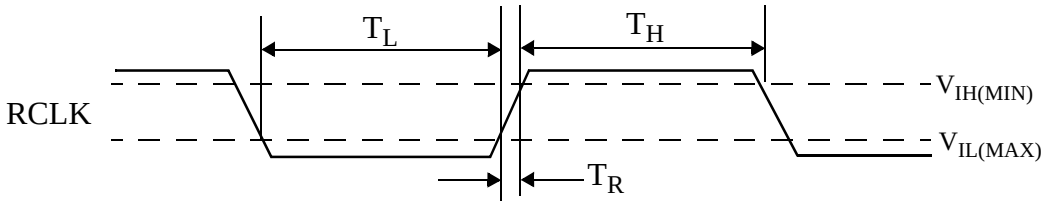


Table 3: Reference Clock Requirements *

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	73.75	74.50	MHz	Will accept both 74.176/74.25MHz
FO	Frequency Offset	-1000	1000	ppm.	Difference in REFCLK frequencies between the transmitting and receiving VSC6501s.
DC	REFCLK duty cycle	-15	+15	%	Measured at 1.5V
T_H, T_L	REFCLK high/low times	3.0	—	ns.	Measured between $V_{IL(MAX)}$ to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ to $V_{IH(MIN)}$
T_R	REFCLK rise	—	2.0	ns.	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$

Note: The PLL locks to the rising edge of REFCLK.

Figure 4: RCLK Timing Waveforms*



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Absolute Maximum Ratings (1)

Power Supply Voltage (V_{DD}) .....-0.5V to +4V
PECL DC Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage..... -0.5V to 5.5V
DC Voltage Applied to TTL Outputs ..... -0.5V to V_{DD} + 0.5V
TTL Output Current .....+/-50mA
PECL Output Current .....+/-50mA
Case Temperature Under Bias .....-55° to +125°C
Storage Temperature.....-65° to + 150°C
Maximum Input ESD (Human Body Model)..... 1500 V

Recommended Operating Conditions

Power Supply Voltage..... ....3.3V +/- 5%
Ambient Operating Temperature Range.....0 °C Ambient to +95°C Case

Notes:

1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	500	µA	V_{IN} = 2.4 V, 6.8Kohm Pull-up resistor on all inputs.
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V, 6.8Kohm Pull-up resistor on all inputs.
V_{OH}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL}= +1.0mA
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.3V $\pm$ 5%
P_D	Power Dissipation: (Estimated)	—	800	—	mW	Outputs open, V_{DD} = V_{DD} max (These are estimates)
ΔV_{IN}	PECL input swing:	200	—	1200	mVp-p	AC Coupled. Internally biased at V_{DD}/2
ΔV_{OUT75}	PECL output swing:	750	—	850	mVp-p	Using appropriate termination network

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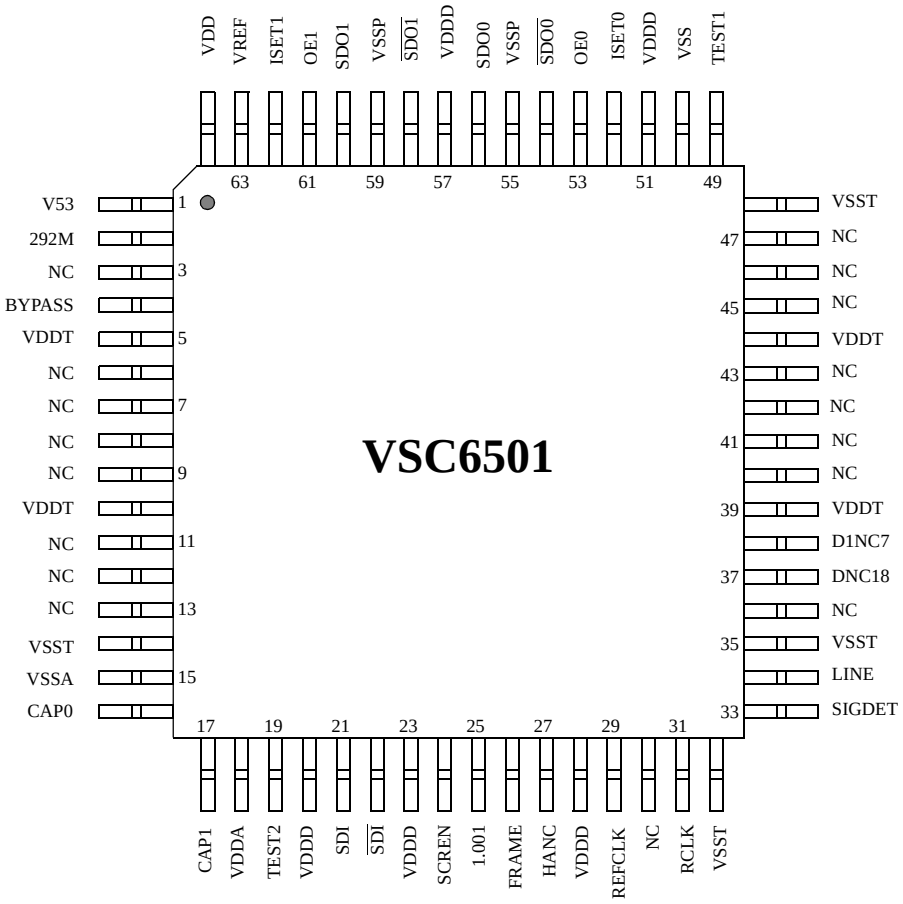
Package Pin Descriptions

Figure 5: Pin Diagram



(Top View)

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Table 3: Pin Identification

Pin #	*Name*	*Description*
2	292M	Status Output
4	BYPASS	Control Input to BYPASS CRU.
50 64	VSS VDD	Connect with 10k resistor to appropriate signal.
24	SCREN	INPUT - TTL: When HIGH, enables scrambling in Serializer/Deserializer modes
3,7,8,9,11 12,13,47,46 45,43,42,41 40,38,37,36,30	NC	No Connect: Leave these pins floating
26	FRAME	OUTPUT - TTL: In Deserializer and Deserializer/Reclocker modes, this is an output which, when HIGH, indicates that a FRAME synchronization event is on D[0:19].
34	LINE	OUTPUT - TTL: In Deserializer and Deserializer/Reclocker modes, this is an output which, when HIGH, indicates that a LINE synchronization event is on D[0:19].
27	HANC	OUTPUT- TTL: Output which is HIGH during the Horizontal Blanking period between EAV and SAV.
25	1.001	OUTPUT - TTL: When HIGH, indicates that a valid receive signal is present on IP/IN and that the SMPTE-292M incoming data is greater than 500ppm from 20xREFCLK.
21,22	SDI, $\overline{\text{SDI}}$	INPUT - Differential. Serial input to CRU.
56,54 60,58	SDO0, $\overline{\text{SDO0}}$ SDO1, $\overline{\text{SDO1}}$	OUTPUT - Differential. High Speed Cable Driver output. Serial output from the Reclocker or SDI, $\overline{\text{SDI}}$ input buffer.
52,62	ISET0, ISET1	Connect resistor to ground to set the output swing of SDO0, SDO1
53,61	OE0, OE1	INPUT - TTL. Output enable pins for SDO0 and SDO1. Enabled when high for each output.
29	REFCLK	INPUT - TTL. REFerence CLocK at 74.25 MHz. This is the input to the CMU and times D[19:0] in Serializer Mode.
31	RCLK	OUTPUT - TTL: Output clock. In Serializer and Reclocker Mode, this is a buffered version of REFCLK. In Deserializer Mode, this is the recovered clock used to time D[19:0]
33	SIGDET	OUTPUT - TTL. An analog signal detect output which, when HIGH, indicates that the SDI input contains a valid SMPTE-292M amplitude signal.
16,17	CAP0, CAP1	Analog I/O: Loop Filter Capacitor, 0.1uF nominal, 3V swing maximum
49,19	TEST1, TEST2	INPUT - TTL. LOW for factory test, HIGH for normal operation.
1	V53	INPUT - POWER: This power supply would normally be 3.3V. If 5V tolerance is required, this pin should be connected to 5V supply.
20,23,28,57,51	VDDD	Power Supply. 3.3V Supply for digital logic.
5,10,39,44	VDDT	TTL I/O Power Supply.
63	VREF	Voltage Reference Input. If used, this is biased to 1.25V.
18	VDDA	Analog Power Supply. 3.3V for Clock Multiplier PLL. Bypass to pin 15.
55,59	VSSP	Ground for High Speed Outputs
14,32,35,48	VSST	TTL I/O Ground
15	VSSA	Analog Ground Bypass to pin 18.

Package Thermal Characteristics

The VSC6501 is packaged in an exposed pad, thin quad flat pack (TQFP) which adheres to industry standard EIAJ footprints for a 10x10x1.0mm body, 64 lead TQFP. The package construction is shown below. The bottom of the lead frame is exposed so that it can be soldered to the printed circuit board and connected to the ground plane. This provides excellent thermal characteristics and reduces electrical parasitics as well.

Figure 6: Package Cross Section

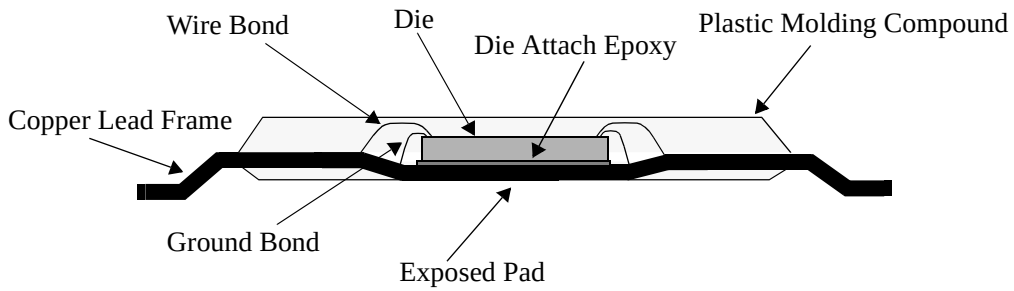

Table 4: 64-pin, Exposed Pad TQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
$\theta_{ca\text{-}0}$	Thermal resistance from case to ambient, still air	30	^{o}C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient, 100 LFPM air	25	^{o}C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient, 200 LFPM air	23	^{o}C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient, 400 LFPM air	21	^{o}C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient, 600 LFPM air	20	^{o}C/W

The VSC6501 is designed to operate with a case temperature up to 95^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown above, the VS6501 can operate in still air ambient temperatures of 70^{o}C [~70^{o}C = 95^{o}C - 0.8W * 30]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided. Additional heat can be transferred to the printed circuit board by not using thermal reliefs on the power and ground plane vias as well as using multiple vias to the power and ground planes.

If the exposed pad is not soldered to the printed circuit board and grounded, both thermal and electrical performance will be degraded significantly.

Moisture Sensitivity Level

This device is rated with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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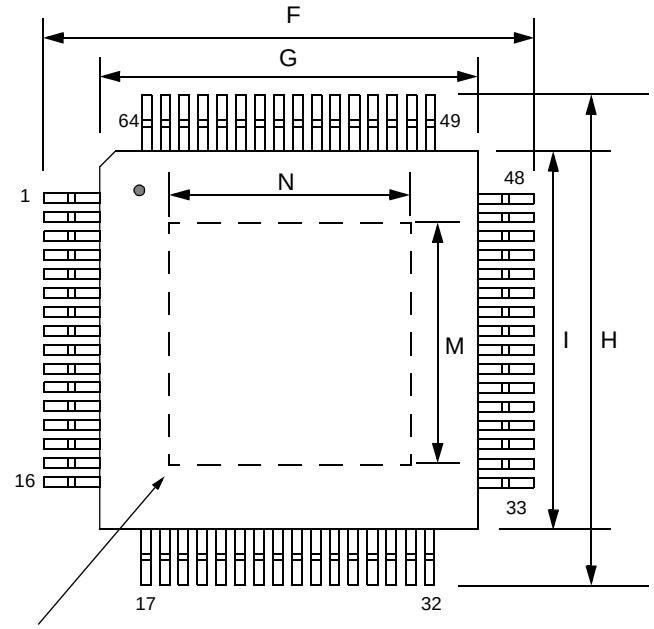
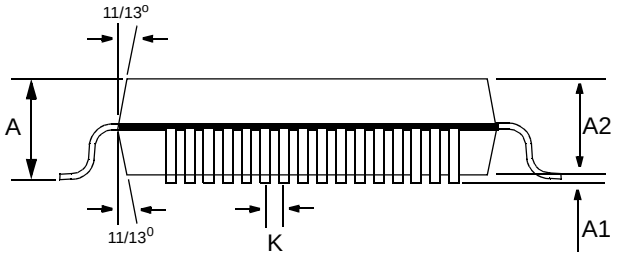
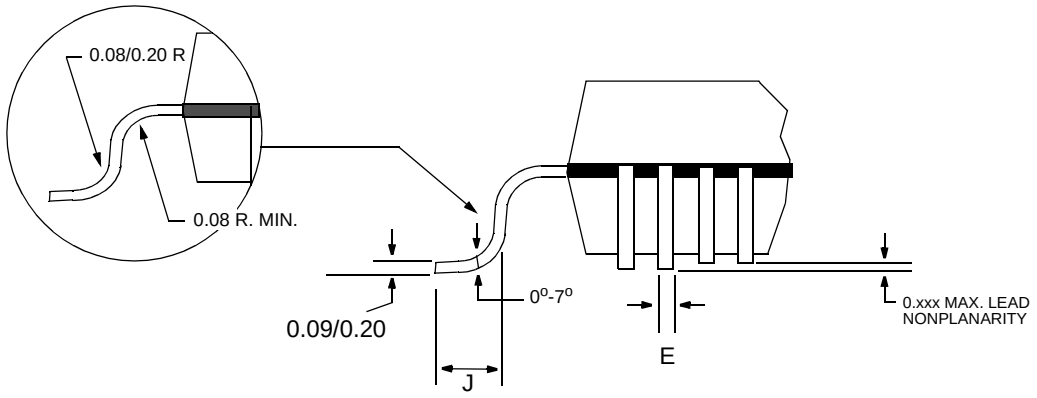
Package Information: 64-pin Exposed Pad TQFP



Item	*mm*	*Tolerance*
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	12.00	±0.40
G	10.00	±0.10
H	12.00	±0.40
I	10.00	±0.10
J	0.60	±0.15
K	0.50	BSC
M	x.xx	±0.xx
N	x.xx	±0.xx





NOTES:
Drawing not to scale.
Exposed Pad Electrically Grounded
All dimensions in millimeters

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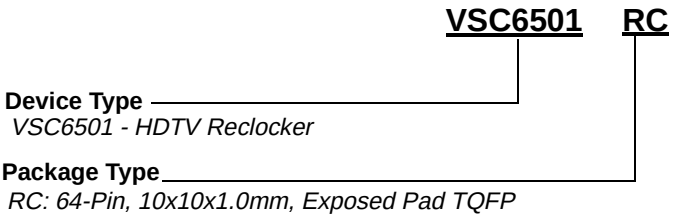
Ordering Information

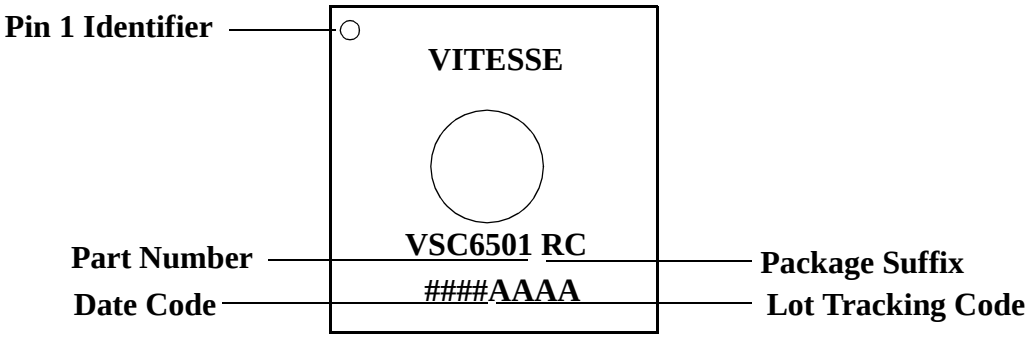
The order number for this product is formed by a combination of the device number, and package type.



Marking Information

The package is marked with three lines of text as shown below.

Figure 7: Package Marking Information



Notice

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Warning

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Revision History

2.0 - New Document

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