Advance Product Information

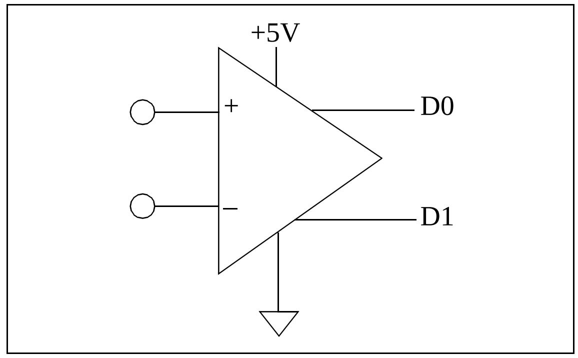
VSC7711

Transimpedance Amplifier
Family for Optical Communication

Features

- Transimpedance Amplifier optimized for high speed optical communications applications
- Integrated AGC
- Fibre Channel and Gigabit Ethernet
- Low Input Noise Current
- Differential Output
- Single 5V Supply with On-chip biasing for photodetectors

Block Diagram:
Photodetector/Transimpedance Amplifier



Part Number	*Data Rate (Gb/s)*	*Bandwidth (MHz)*	*Transimpedance (kΩ)*	*Input Noise (nA RMS)*
VSC7711	1.25	800	3.5	180

General Description

The VSC7711 Transimpedance Amplifiers provide a high performance solution for amplifying high speed photodetector output signals from a fiber optic communications channel into a differential output voltage. The benefits of Vitesse Semiconductor’s Gallium Arsenide H-GaAs III process are fully utilized to provide a very high bandwidth and low noise amplifier. The detector bias is supplied on-chip eliminating the need for a separate bias connection. The sensitivity, duty cycle distortion and jitter meet or exceed all Fibre Channel and Gigabit Ethernet requirements.

In conjunction with suitable photodetectors, these parts can be easily used in developing a wide range of Fibre Channel and Gigabit Ethernet optoelectronic receivers for both short wavelength (850nm) as well as long wavelength (1300nm) applications.

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Table 1: Electrical Characteristics of Transimpedance Amplifiers *(V_S = 5V & T = 25°C unless otherwise noted)*

Symbol	*Parameter*	*Min.*	*Max.*	*Units*	*Conditions*
V_{DD}	Supply Voltage	4.5	5.5	V	—
I_s	Supply Current	—	62	mA	I_{in} 4µA_{pp} to 1.5mA_{pp}
BW	Optical Modulation Bandwidth	800		MHz	I_{in} = 20µA_{pp}, detector capacitance = 0.6pf
F_c	Low Frequency Cutoff		1.5	MHz	I_{in} = 20µA_{pp}
T_r, T_f	Output Rise & Fall Time	—	250	ps	20% to 80% I_{in}-1.0mA_{pp}
R_d	Differential Transresistance	3.5	—	kΩ	R_L = 100Ω, differential I_{in}= 20µA
I_{max}	Output Drive Current	1.5	—	mA_{pp}	10% Duty Cycle Distortion
I_n	Input Noise Equivalent Current	—	180	nA RMS	BW = 800 MHz
I_n	Input Noise Equivalent Current Spectral Density	—	6.4	pA/ √Hz	BW = 800 MHz
PDJ	Pattern Dependent Jitter	—	60	ps	
R_o	Single Ended Output Impedance	25	75	Ω	—
V_{max}	Maximum Differential Output Voltage	—	700	MV_{pp}	I_{in} = 1.0mA_{pp} R_L = 100Ω, differential
V_B	Output Bias Voltage	0.5	1.7	V	—
V_{off}	Output Offset Voltage		0.15	V	—
PSRR	Power Supply Rejection Ratio	35	—	dB	f = 0.3MHz - 40MHz, with external filter

Table 2: Absolute Maximum Ratings

Symbol	*Parameter*	*Limits*
V_{DD}	Power Supply	6V
T_{stg}	Storage Temperature	-55°C to 125°C (die temperature under bias)

Table 3: Recommended Operating Conditions

Symbol	*Parameter*	*Limits*
V_{DD}	Power Supply	4.5-5.5V (5.0V nominal)
T_{op}	Operating Temperature	0°C (ambient) to 80°C (die)

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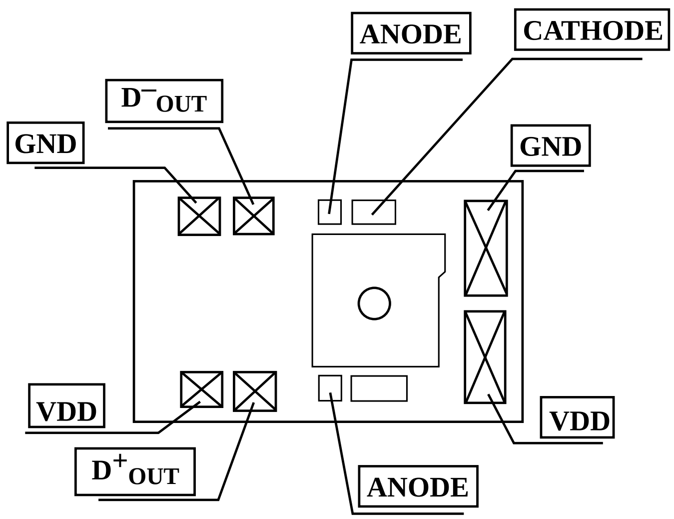
Table 4: Pin Table Specifications for Bare Die

Symbol	*Description*
D^{+}_{OUT}	Data output normal (with reference to incident light)
D^{-}_{OUT}	Data output complement (inverting) (with reference to incident light)
VDD	Power supply
GND	Ground (package case)

Figure 1: Schematic View of Bare Die Pad Assignments

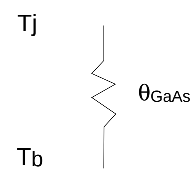


Note: Refer to Figure 4 for die layout detail.

Thermal Resistance Calculation For Bare Die

In order to relate the junction temperature to the temperature of the back side of the bare die, the following thermal characteristics of the package are provided

Table 5: Thermal Resistance Calculation for Bare Die.

Chip Size	0.168cm x 0.104cm	Thermal Path
Chip Area A	0.015 cm^2	
Die height (T_{die})	0.066 cm	
Thermal Conductivities		
K GaAs	0.55W / cm °C	

$$\theta_{GaAs} = \frac{T_{die}}{K_{GaAs}A} = \frac{0.066}{0.55 \times 0.015} = 8°C/W$$

θ_{JB} = Thermal Resistance from Junction to back = 8°C/W

Example:

For VSC7711 at nominal supply current of 25mA and V_{DD} = 5V
Temperature rise from junction to back = 0.025A x 5V x 8°C/W = 1°C

Figure 2: Mechanical Specifications

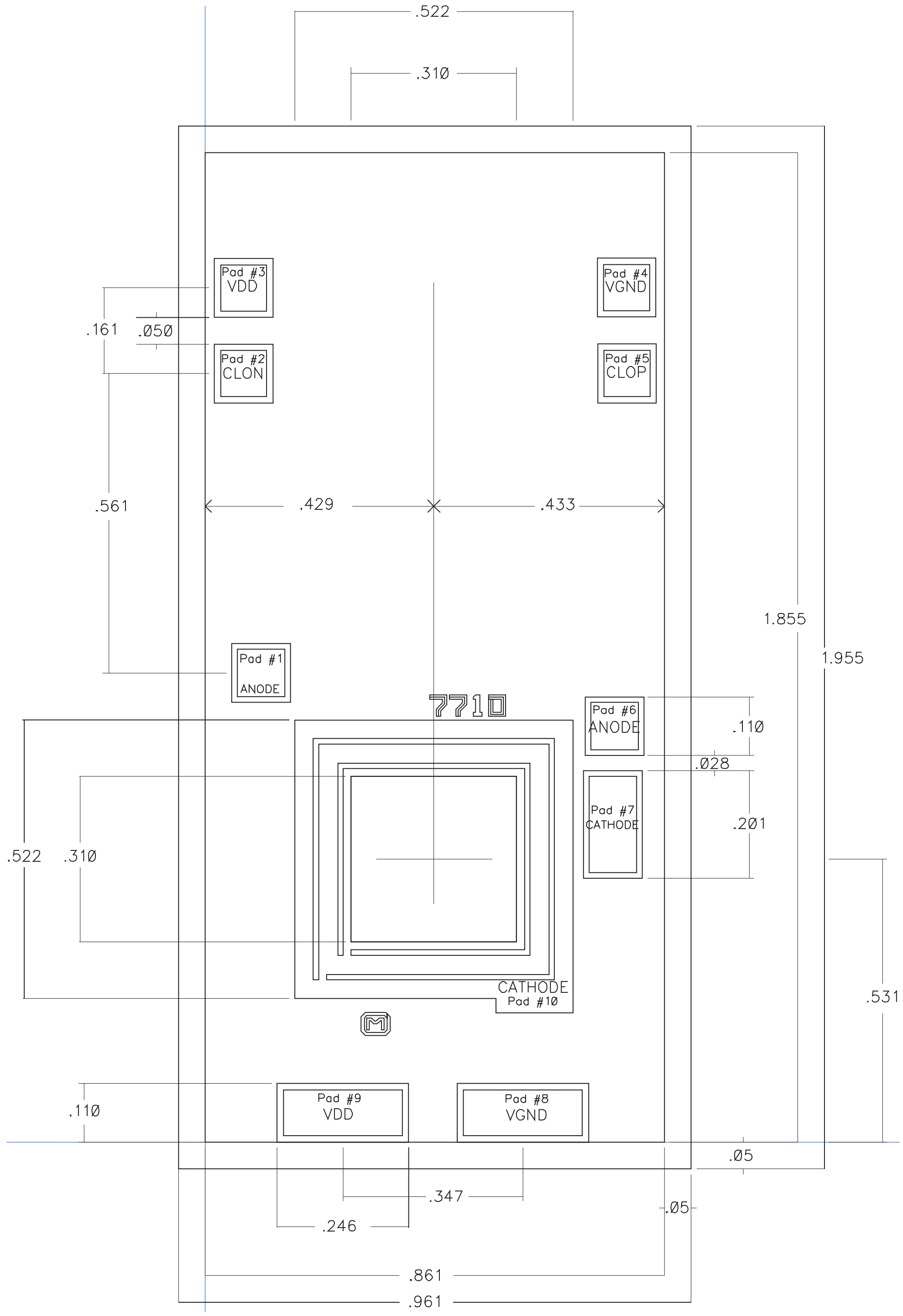


Table 6: Die Pad Descriptions

Pad Number	*Pad Name*	*Pad Locations*		*Pad Size*	*Pass Opening*	*Pad Finish*	*Finish Thickness*
		X	*Y*				
1	ANODE	104.5	880	110 x 110	89 x 89	Gold	1500 Å
2	CLON	71.7	1440.6	110 x 110	89 x 89	Gold	1500 Å
3	VDD	71.7	1601.2	110 x 110	89 x 89	Gold	1500 Å
4	VGND	790	1602.1	110 x 110	89 x 89	Gold	1500 Å
5	CLOP	790	1441.1	110 x 110	89 x 89	Gold	1500 Å
6	ANODE	765.9	781.2	110 x 110	89 x 89	Gold	1500 Å
7	CATHODE	764.3	595.8	110 x 201	89 x 180	Gold	1500 Å
8	VGND	595.4	55	246 x 110	223 x 86	Gold	1500 Å
9	VDD	258	55	246 x 110	223 x 86	Gold	1500 Å
10	CATHODE	428.5	530.5	522 x 522	310 x 310	Gold	1500 Å

Ordering Information

Part Numbering Scheme:

VSC7711X

X   Individual Die

Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

Warning

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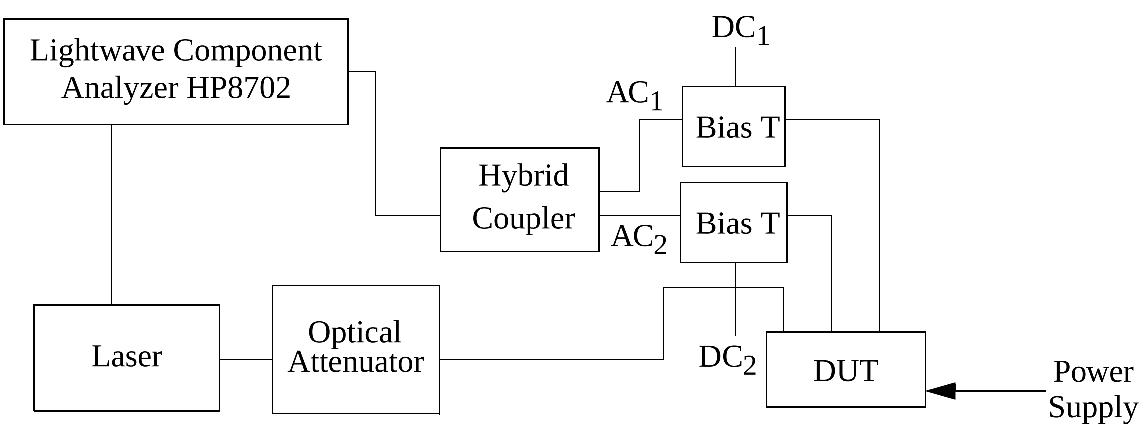
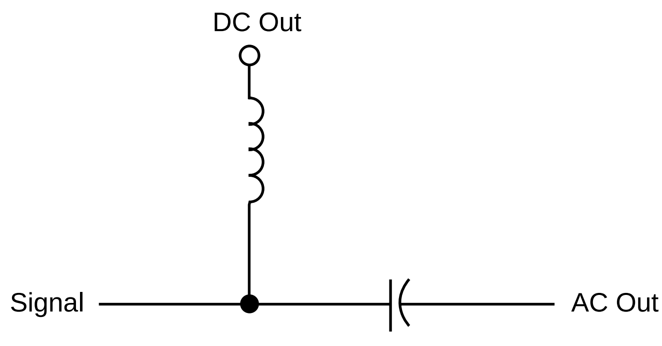
Notes on Measurement Conditions & Applications

Note 1:Measurement Setup for Frequency Response



Note 2:Bias T Schematic



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