Preliminary Data Sheet

VSC7938

SONET/SDH 3.125Gb/s Laser Diode Driver with Automatic Power Control

Features

- Power Supply: 3.3V or 5V ±5%
- AC-Coupled to Laser Diode
- Programmable Modulation Current: 5mA to 60mA
- Programmable Bias Current: 1mA to 100mA
- Enable/Disable Control
- Typical Rise/Fall Times of 60ps
- Automatic Optical Average Power Control
- Supply Current of 33mA at 3.3V

Applications

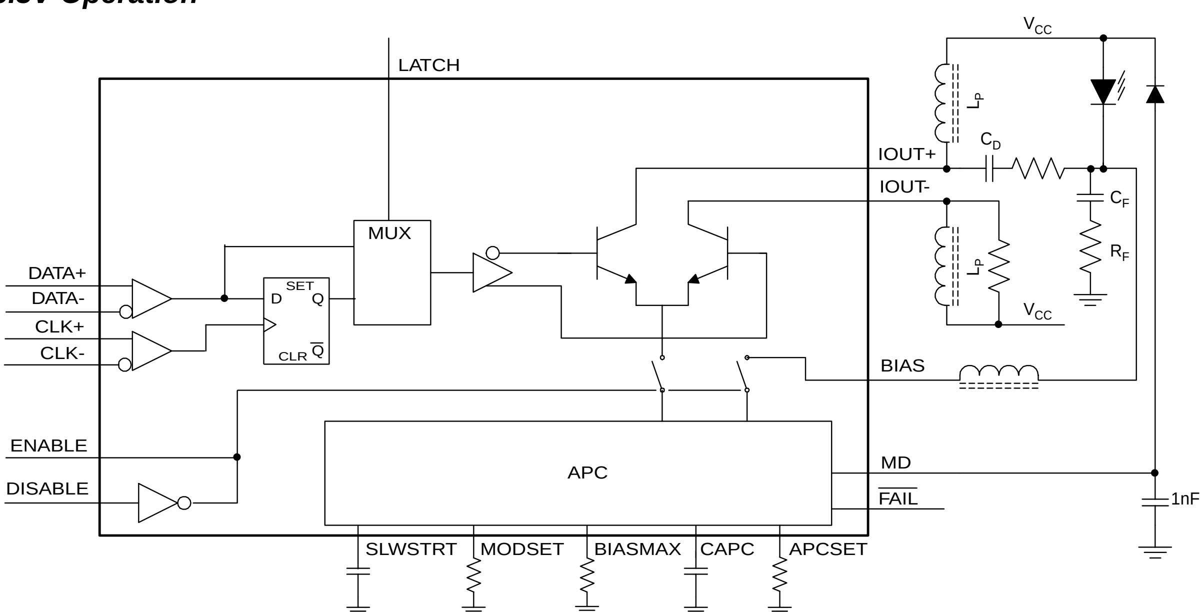
- SDH/SONET at 622Mb/s, 1.244Gb/s, 2.488Gb/s, 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)

General Description

The VSC7938 is a single 3.3V or 5V supply laser diode driver specially designed for SDH/SONET applications up to 3.125Gb/s. External resistors set a wide range of bias and modulation currents for driving the laser. Data and clock inputs accept differential PECL signals. The automatic power control (APC) loop maintains a constant average optical power over temperature and lifetime. The dominant pole of the APC loop can be controlled with an external capacitor. Other features include enable/disable control, short-circuit protection for the modulation and bias inputs, short rise and fall times, programmable slow-start circuit to set laser turn-on delay, and failure-monitor output to indicate when the APC loop is unable to maintain the average optical power. The VSC7938 is available in die form or in a 48-pin TQFP package.

Block Diagram

3.3V Operation



Electrical Characteristics

Table 1: AC Specifications

AC specifications are guaranteed by design and characterization. Typical values are for 3.3V.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{SU}	Input Latch Setup Time	100			ps	LATCH=high
t_H	Input Latch Hold Time	100			ps	LATCH=high
	Enable/Start-up Delay		250		ns	
t_R	Output Rise Time		60	80	ps	20% to 80%
t_F	Output Fall Time		60	80	ps	20% to 80%
PWD	Pulse Width Distortion		10	50	ps	See Notes 1, 2
CID_{MAX}	Maximum Consecutive Identical Digits	80			bits	
t_J	Jitter Generation		7	20	ps_{p-p}	Jitter BW=12kHz to 20MHz, 0-1 pattern.

NOTES:(1) Measured with 622Mb/s 0-1 pattern, LATCH=high. (2) PWD = (wider pulse - narrower pulse) / 2).

Table 2: DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{CC}	Supply Current		TBD	45	mA	R_{MODSET}=7.3kΩ $R_{BIASMAX}$=4.8kΩ I_{BIAS} and I_{MOD} excluded V_{CC}=5V
I_{BIAS}	Bias Current Range	1		100	mA	Voltage at BIAS pin=(V_{CC}-1.6)
$I_{BIAS-OFF}$	Bias Off Current			100	µA	ENABLE=low or DISABLE=high$^{(1)}$
S_{BIAS}	Bias Current Stability		230		ppm/°C	APC Open loop. I_{BIAS}=100mA
			900			APC Open loop. I_{BIAS}=1mA
	Bias Current Absolute Accuracy		±15		%	Refers to part-to-part variation
VR_{MD}	Monitor Diode Reverse Bias Voltage	1.5			V	
I_{MD}	Monitor Diode Reverse Current Range	18		1000	µA	
	Monitor Diode Bias Setpoint Stability	-480	-50	480	ppm/°C	I_{MD}=1mA$^{(2)}$
			90			I_{MD}=18µA$^{(2)}$
	Monitor Diode Bias Absolute Accuracy	-15		15	%	Refers to part-to-part variation
I_{MOD}	Modulation Current Range	5		60	mA	
$I_{MOD-OFF}$	Modulation Off Current			200	µA	ENABLE=low or DISABLE=high$^{(1)}$
	Modulation Current Absolute Accuracy		±15		%	See Note 2
	Modulation Current Stability	-480	-50	480	ppm/°C	I_{MOD}=60mA
			250			I_{MOD}=5mA

NOTES: (1) Both I_{BIAS} and I_{MOD} will turn off if any of the current set pins are grounded. (2) Assumes laser diode to monitor diode transfer function does not change with temperature.

Table 3: PECL and TTL/CMOS Inputs and Outputs Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{ID}	Differential Input Voltage	100		1600	mV_{p-p}	(DATA+)-(DATA-)
V_{ICM}	Common-Mode Input Voltage	V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - $V_{ID}/4$	V	PECL Compatible
I_{IN}	Clock and Data Input Current	-1		10	µA	
V_{IH}	TTL Input High Voltage (ENABLE, LATCH)	2.0			V	
V_{IL}	TTL Input Low Voltage (ENABLE, LATCH)			0.8	V	
	TTL Output High Voltage ($\overline{FAIL}$)	2.4	V_{CC} - 0.3	V_{CC}	V	Sourcing 50µA
	TTL Output Low Voltage ($\overline{FAIL}$)	0.1		0.44	V	Sinking 100µA

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC})........ -0.5V to 6V
Current into BIAS........ -20mA to +150mA
Current into OUT+, OUT-........ TBD
Current into MD........ -5mA to +5mA
Current into $\overline{FAIL}$........ -10mA to 30mA
Voltage at DATA+, DATA-, CLK+, CLK-, ENABLE, LATCH........ -0.5V to (V_{CC} + 0.5V)
Voltage at APCFILT, MODSET, BIASMAX, APCSET, MD, $\overline{FAIL}$, SLWSTRT........ -0.5V to +3.0V
Voltage at OUT+, OUT-........ -0.5V to (V_{CC} + 1.5V)
Voltage at BIAS........ -0.5V to (V_{CC} + 0.5V)
Continouous Power Dissipation (T_A = +85°C, TQFP derate 20.8mW/°C above +85°C)........ 1350mW
Operating Junction Temperature Range........ -55°C to +150°C
Storage Temperature Range........ -65°C to +165°C

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

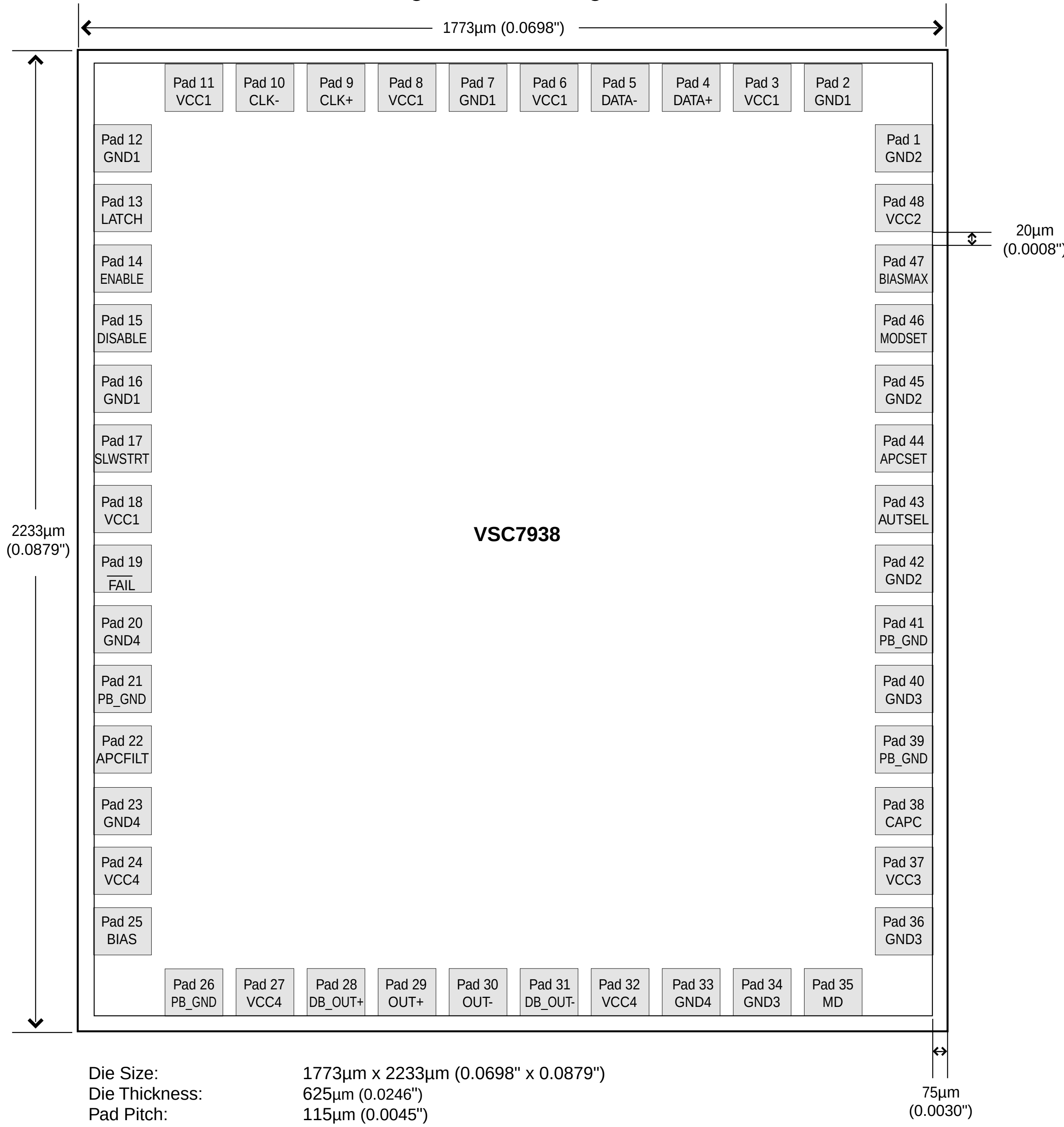
Recommended Operating Conditions

Positive Voltage Rail (V_{CC})........ +3.135V to +5.25V
Negative Voltage Rail (GND)........ 0V
Modulation Current (I_{MOD})(1)........ 30mA
Ambient Temperature Range (T_A)........ -40°C to +85°C

NOTE: (1) V_{CC} = 3.3V, I_{BIAS} = 60mA.

Bare Die Descriptions

Figure 1: Pad Assignments



Die Size:	1773µm x 2233µm (0.0698" x 0.0879")
Die Thickness:	625µm (0.0246")
Pad Pitch:	115µm (0.0045")
Pad Size:	95µm x 95µm (0.0037" x 0.0037")
Pad to Pad Clearance:	20µm (0.0008")
Pad Passivation Opening:	95µm x 95µm (0.0037" x 0.0037")
Scribe Size:	75µm (0.0030")

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Table 4: Pad Coordinates

Signal Name	Pad Number	Coordinates (µm)		Signal Name	Pad Number	Coordinates (µm)	
		X	Y			X	Y
GND2	1	1613.55	1863.475	BIAS	25	159.45	368.475
GND1	2	1414.525	2073.55	PB_GND	26	369.525	159.45
VCC1	3	1289.525	2073.55	VCC4	27	484.525	159.45
DATA+	4	1174.525	2073.55	DB_OUT+	28	599.525	159.45
DATA-	5	1059.525	2073.55	OUT+	29	714.525	159.45
VCC1	6	944.525	2073.55	OUT-	30	829.525	159.45
GND1	7	829.525	2073.55	DB_OUT-	31	944.525	159.45
VCC1	8	714.525	2073.55	VCC4	32	1059.525	159.45
CLK+	9	599.525	2073.55	GND4	33	1174.525	159.45
CLK-	10	484.525	2073.55	GND3	34	1289.525	159.45
VCC1	11	369.525	2073.55	MD	35	1404.525	159.45
GND1	12	159.45	1863.475	GND3	36	1613.55	368.475
LATCH	13	159.45	1748.475	VCC3	37	1613.55	483.475
ENABLE	14	159.45	1633.475	CAPC	38	1613.55	598.475
DISABLE	15	159.45	1518.475	PB_GND	39	1613.55	713.475
GND1	16	159.45	1403.475	GND3	40	1613.55	828.475
SLWSTRT	17	159.45	1288.475	PB_GND	41	1613.55	943.475
VCC1	18	159.45	1058.475	GND2	42	1613.55	1058.475
$\overline{\text{FAIL}}$	19	159.45	1058.475	AUTSEL	43	1613.55	1173.475
GND4	20	159.45	828.475	APCSET	44	1613.55	1288.475
PB_GND	21	159.45	828.475	GND2	45	1613.55	1403.475
APCFILT	22	159.45	598.475	MODSET	46	1613.55	1518.475
GND4	23	159.45	598.475	BIASMAX	47	1613.55	1633.475
VCC4	24	159.45	483.475	VCC2	48	1613.55	1748.475

Package Pin Descriptions

Figure 2: Pin Diagram

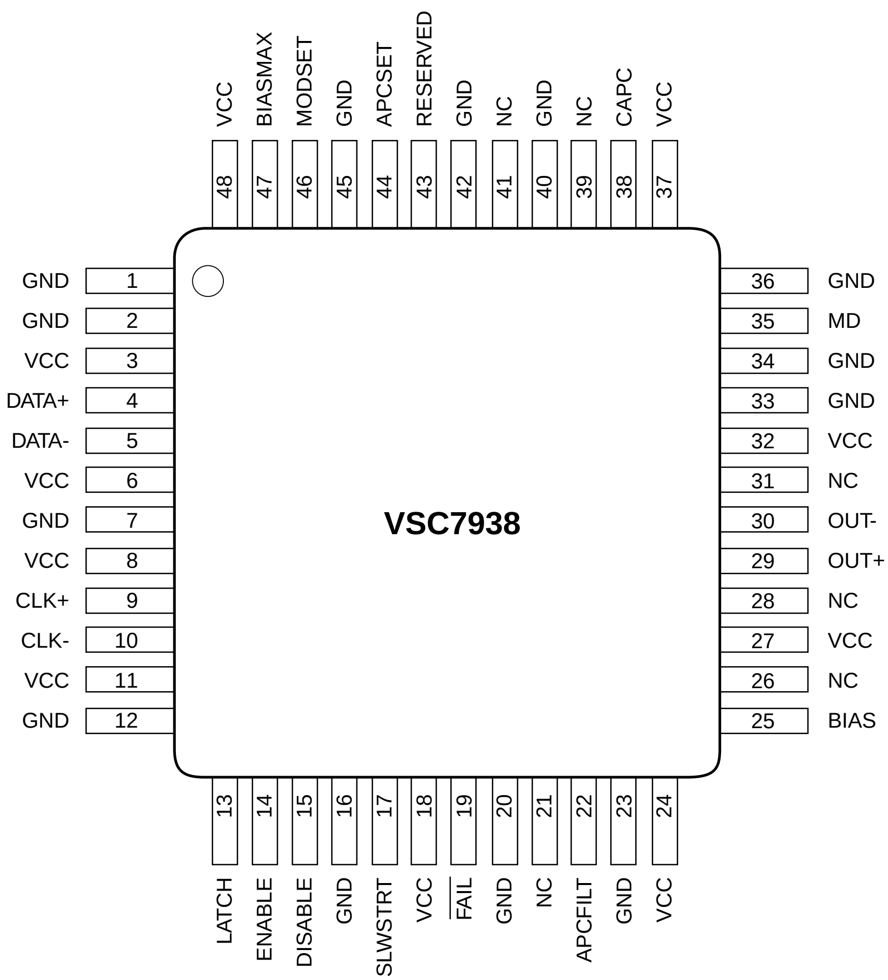

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Table 5: Pin Identifications

Pin Name	*Pin Number*	*Description*
GND	1, 2, 7, 12, 16, 20, 23, 33, 34 36, 40, 42, 45	Ground
V_{CC}	3, 6, 8, 11, 18, 24, 27, 32, 37, 48	Power Supply
DATA+	4	Positive Data Input (PECL)
DATA-	5	Negative Data Input (PECL)
CLK+	9	Positive Clock Input (PECL). Connect to V_{CC} if data retiming is not used.
CLK-	10	Negative Clock Input (PECL). Leave unconnected if data retiming is not used.
LATCH	13	Latch Input (TTL/CMOS). Connect to V_{CC} for data retiming and GND for direct data.
ENABLE	14	Enable Input (TTL/CMOS). If used, connect DISABLE to GND. Connect to V_{CC} for normal operation and GND to disable laser bias and modulation currents.
DISABLE	15	Disable Input (TTL/CMOS). If used, leave ENABLE pin floating. Connect to GND for normal operation and V_{CC} to disable laser bias and modulation currents.
SLWSTRT	17	Connect capacitor to GND to delay turn on time of bias and modulation currents.
$\overline{\text{FAIL}}$	19	Output (TTL/CMOS). When low, it indicates APC failure.
NC	21, 26, 28, 31, 39, 41	No Connection. Leave these pins unconnected.
APCFILT	22	No effect on device operation.
BIAS	25	Laser Bias Current Output
OUT+	29	Positive Modulation-Current Output. I_{MOD} flows when input data is high.
OUT-	30	Negative Modulation-Current Output. I_{MOD} flows when input data is low.
MD	35	Monitor Diode Input. Connect to monitor photodiode anode. Connect capacitor to GND to filter high-speed AC monitor photocurrent.
CAPC	38	Capacitor to GND sets dominant pole of the APC feedback loop.
RESERVED	43	Do not connect.
APCSET	44	Resistor to GND sets desired average optical power. If APC is not used connect 100kΩ resistor to GND.
MODSET	46	Connect resistor to GND to set desired modulation current.
BIASMAX	47	Connect resistor to GND to set maximum bias current. The APC function can subtract from this value, but it cannot add to it.

Detailed Description

The VSC7938 is a high-speed laser driver with Automatic Power Control. The device is designed to operate up to 3.125Gb/s with a 3.3V or 5V supply. The data and clock inputs support PECL inputs as well as other inputs that meet the common-mode voltage and differential voltage swing specifications. The differential pair output stage is capable of sinking up to 60mA from the laser with typical rise and fall times of 60ps. This output may be DC-coupled for 5V operation. To allow for larger output swings during 3.3V operation, the VSC7938 was designed to be AC-coupled to the laser cathode with a pull-up inductor for DC-biasing. This configuration will isolate laser forward voltage from the output circuitry and will allow the output at OUT+ to swing above and below the supply voltage V_{CC}. The key features of the VSC7938 are Automatic Power Control, low power supply current, and fast rise and fall times. The VSC7939 and VSC7940 are other Vitesse laser drivers with similar features in a 32-pin TQFP package. These devices also have pins for monitoring modulation and bias currents. The VSC7940 is a special version of the VSC7939 designed to drive 100mA into a DC-coupled load with a 5V supply.

Automatic Power Control

To ensure constant average optical power, the device utilizes an Automatic Power Control loop. A photodiode mounted in the laser package provides optical feedback to compensate for changes in average laser output power due to changes that affect laser performance such as temperature and laser lifetime. The laser bias current is adjusted by the APC loop according to the reference current set at APCSET by an external resistor. An external capacitor at CAPC controls the time constant for the APC feedback loop. The recommended value for CAPC is 0.1µF. This value reduces pattern-dependent jitter associated with the APC feedback loop and guarantees stability. Because the APC loop noise is internally filtered, APCFILT is not internally connected and does not need to be connected to any external components. The device’s performance will not be affected if a capacitor is connected to APCFILT. If the APC loop cannot adjust the bias current to track the desired monitor current, $\overline{\text{FAIL}}$ is set low.

The device may be operated with or without APC. To utilize APC, a capacitor must be connected at CAPC (0.1µF) and a resistor must be connected at APCSET to set the average optical power. For open-loop operation (no APC), a 100kΩ resistor should be connected between APCSET and GND. CAPC has no effect on open-loop operation. In both modes of operation, resistors to ground should be placed at BIASMAX and MODSET to set the bias and modulation currents.

Data Retiming

The VSC7938 provides inputs for differential PECL clock signals for data retiming to minimize jitter at high speeds. To incorporate this function, LATCH should be connected to V_{CC}. If this function is unused, CLK+ should be connected to V_{CC}, CLK- should be left unconnected, and LATCH should be connected to GND.

Short-Circuit Protection

If BIASMAX or MODSET are shorted to ground, the output modulation and bias currents will be turned off.

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Enable/Disable

Two pins are provided to allow either ENABLE or DISABLE control. If ENABLE is used, connect DISABLE to ground. Is DISABLE is used, leave ENABLE floating. Both modulation and bias currents are turned off when ENABLE is low or DISABLE is high. Typically, ENABLE or DISABLE responds within approximately 250ns.

Slow-Start

For laser safety, the VSC7938 offers a slow-start mechanism via the SLWSTRT pin which provides delay for enabling the laser diode. To disable Slow-Start, leave SLWSTRT open. An external capacitor to ground sets the delay by the following equation:

$$\tau_{ENABLE}(ns) = C_{SLWSTRT}(pF) * 20 + 250ns$$

Controlling the Modulation Current

The output modulation current may be determined from the following equation where $P_{p\text{-}p}$ is the peak-to-peak optical power, P_{AVE} is the average power, r_e is the extinction ratio, and η is the laser slope efficiency:

$$I_{MOD} = P_{p\text{-}p} / \eta = 2 * P_{AVE} * (r_e\text{-}1) / (r_e\text{+}1) / \eta$$

A resistor at MODSET controls the output bias current. Graphs of I_{MODSET} vs. R_{MODSET} in *Typical Operating Characteristics* for both 3.3V and 5V operation describe the relationship between the resistor at MODSET and the output modulation current at 25°C. After determining the desired output modulation current, use the graph to determine the appropriate resistor value at MODSET.

Controlling the Bias Current

A resistor at BIASMAX should be used to control the output bias current. Graphs of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* for both 3.3V and 5V operation describe the relationship between the resistor at BIASMAX and the output bias current at 25°C. If the APC is not used, the appropriate resistor value at BIASMAX is determined by first selecting the desired output bias current, and then using the graph to determine the appropriate resistor value at BIASMAX. When using APC, BIASMAX sets the maximum allowed bias current. After determining the maximum end-of-life bias current at 85°C for the laser, refer to the graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* to select the appropriate resistor value.

Controlling the APC Loop

To select the resistor at APCSET, use the graph of I_{MD} vs. R_{APCSET} in *Typical Operating Characteristics.* The graph relates the desired monitor current to the appropriate resistance value at APCSET. I_{MD} may be calculate from the desired optical average power, $P_{AVE,}$, and the laser-to-monitor transfer, ρ_{MON}, for a specific laser using the following equation:

$$I_{MD} = P_{AVE} * \rho_{MON}$$

Laser Diode Interface

An RC shunt network should be placed at the laser output interface. The sum of the resistor placed at the output and the laser diode resistance should be 25Ω. For example, if the laser diode has a resistance of 5Ω, a 20Ω resistor should be placed in series with the laser. For optimal performance, a bypass capacitor should be placed close to the laser anode.

A "snubber network" consisting of a capacitor C_F and resistor R_F should be placed at the laser output to minimize reflections from the laser (see Block Diagram). Suggested values for these components are 80Ω and 2pF, respectively. However, these values should be adjusted until an optical output waveform is obtained.

Reducing Pattern-Dependent Jitter

Three design values significantly affect pattern-dependent jitter; the capacitor at CAPC, the pull-up inductor at the output (L_P), and the AC-coupling capacitor at the output (C_D). As previously stated, the recommended value for the capacitor at CAPC is 0.1μF. This results in a 10kHz loop bandwidth which makes the pattern-dependent jitter from the APC loop negligible.

For 2.5Gb/s data rates, the recommended value for C_D is 0.056μF. The time constant at the output is dominated by L_P. The variation in the peak voltage should be less that 12% of the average voltage over the maximum consecutive identical digit (CID) period. The following equation approximates this time constant for a CID period, t, of 100UI = 40ns:

$$\tau_{LP} = -t / \ln(1-12\%) = 7.8t = L_P / 25\Omega$$

Therefore, the inductor L_P should be a 7.8μH SMD ferrite bead inductor for this case.

Input/Output Considerations

Although the VSC7938 is PECL compatible, this is not required to drive the device. The inputs must only meet the common-mode voltage and differential voltage swing specifications.

Power Consumption

The following equation provides the device supply current (I_S) in terms of quiescent current (I_Q), modulation current (I_{MOD}), and bias current (I_{BIAS}):

$$I_S = I_Q + 0.47 * I_{MOD} + 0.15 * I_{BIAS}$$

For 3.3V operation, I_Q is 15mA. For 5V operation, I_Q is 20mA.

This equation may be used to determine the estimated power dissipation:

$$P_{DIS} = V_{CC} * I_S$$

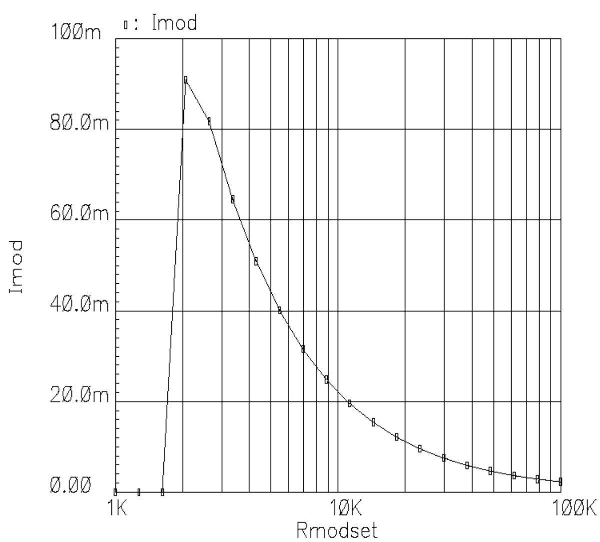
For example, if the device were operated at 3.3V with a 30mA modulation current and a 10mA bias current, the supply current would be:

$$I_S = 15mA + 0.47 * 30mA + 0.15 * 10mA = 31$$

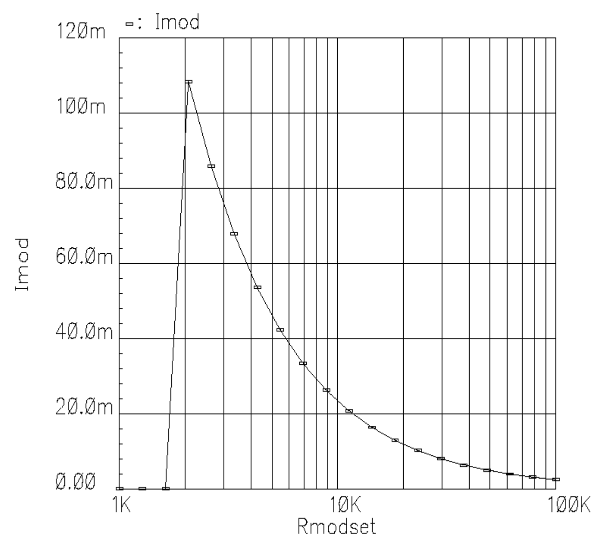
This corresponds to a power dissipation of 3.3V * 31mA = 102mW.

Typical Operating Characteristics

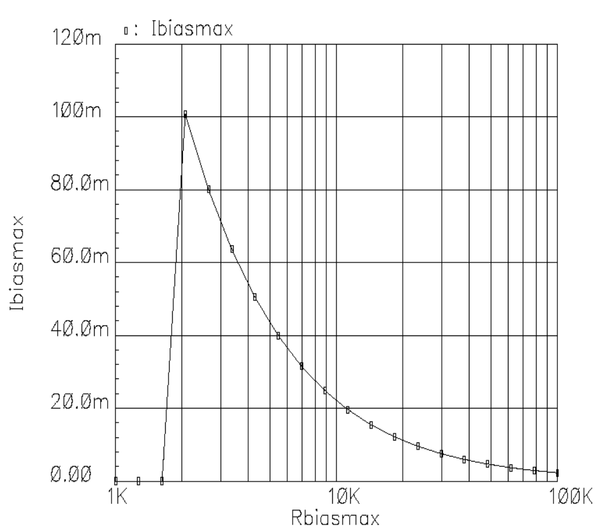
I_{MODSET} vs. R_{MODSET}
$T=25°C$ $V_{CC} = 3.3V$



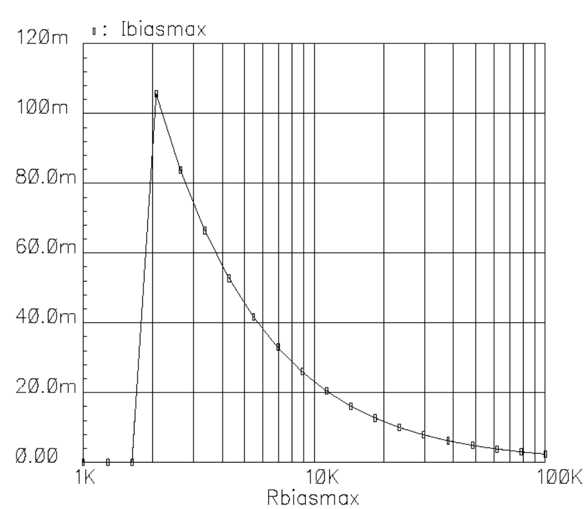
I_{MODSET} vs. R_{MODSET}
$T=25°C$ $V_{CC} = 5V$

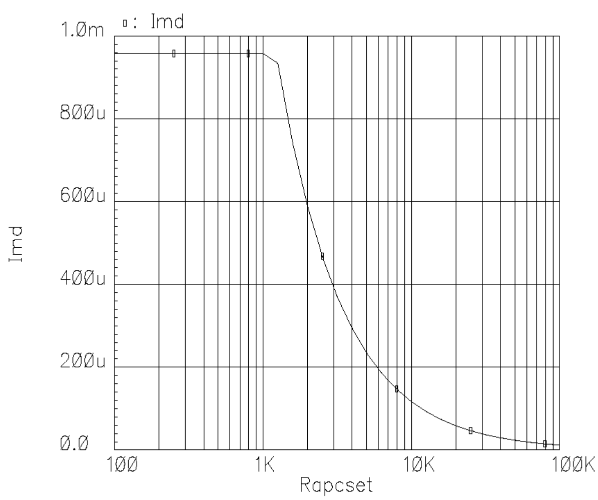
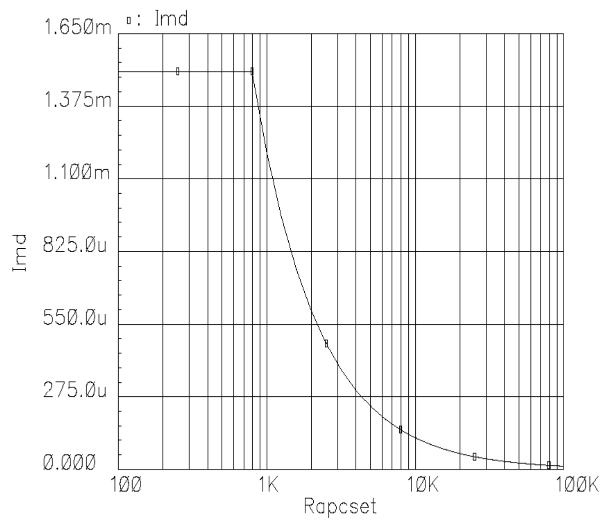


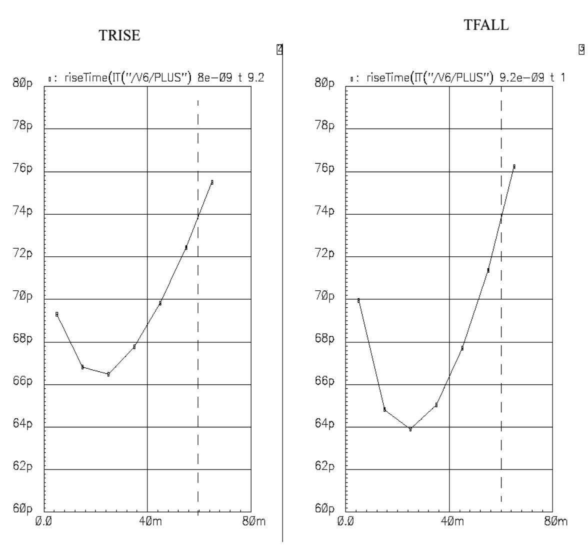
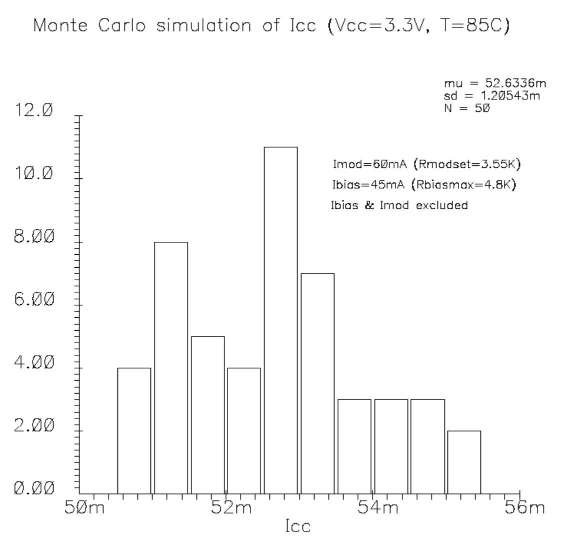
$I_{BIASMAX}$ vs. $R_{BIASMAX}$
$T=25°C$, $V_{CC} = 3.3V$



$I_{BIASMAX}$ vs. $R_{BIASMAX}$
$T=25°C$, $V_{CC} = 5V$



I_{MD} vs. R_{APCSET}, T=25°C, V_{CC} = 3.3V	***I_{MD} vs. R_{APCSET}, T=25°C, V_{CC} = 5V***
	

Rise and Fall Times T=85°C, V=3.3V	***Monte Carlo Simulation of I_{CC}***
	

Applications Information

The following is a typical design example for the VSC7938 assuming 3.3V operation with APC.

Select a Laser

The Table 5 provides specifications for a typical communication-grade laser capable of operating at 2.5Gb/s.

Table 6: Typical Laser Characteristics

Symbol	*Parameter*	*Value*	*Units*
λ	Wavelength	1310	nm
P_{AVE}	Average Optical Output Power	6	mW
I_{th}	Threshold Current	6	mA
ρ_{MON}	Laser to Monitor Transfer	0.04	mA/mW
η	Laser Slope Efficiency	0.4	mW/mA
T_C	Operating Temperature Range	-40 to +85	°C

Select Resistor for APCSET

The monitor diode current is estimated by $I_{MD} = P_{AVE} * \rho_{MON}$ = 6mW * 0.04mA/mW = 0.24mA. The I_{MD} vs. R_{APCSET} in *Typical Operating Characteristics* shows the resistor at APCSET should be 5kΩ.

Select Resistor for MODSET

To ensure some minimum extinction ratio over temperature and lifetime, assume an optimal extinction ratio of 20 (13dB) at 25°C. The modulation current may be calculated from the following equation:

$$I_{MOD} = P_{p\text{-}p} / \eta = 2 * P_{AVE} * (r_e-1) / (r_e+1) / \eta = 2 * 6\text{mA} * (20-1) / (20 + 1) / 0.4 = 27.1\text{mA}$$

The graph of I_{MODSET} vs. R_{MODSET} in *Typical Operating Characteristics* shows the resistor for MODSET should be 8.5kΩ.

Select Resistor for BIASMAX

The maximum threshold current at +85°C and end of life must be determined. A graph of a typical laser's I_{th} versus T_C reveals a maximum threshold current of 30mA at 85°C. Therefore, the maximum bias can be approximated by:

$$I_{BIASMAX} = I_{TH\text{-}MAX} + I_{MOD} / 2 = 30\text{mA} + 27.1\text{mA} / 2 = 43.6\text{mA}$$

The graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* shows the resistor for BIASMAX should be 5kΩ.

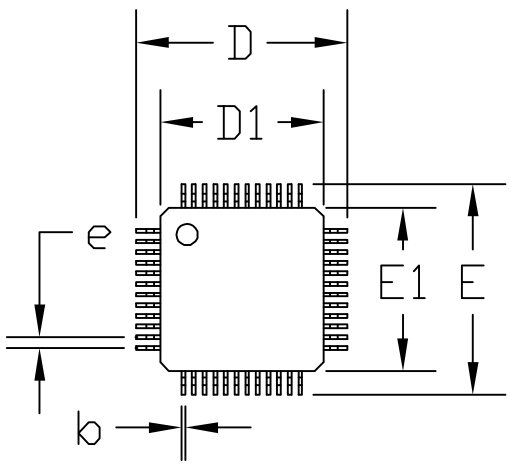
Wire Bonding

For best performance, gold ball-bonding techniques are recommended. Wedge bonding is not recommended. For best performance and to minimize inductance keep wire bond lengths short.

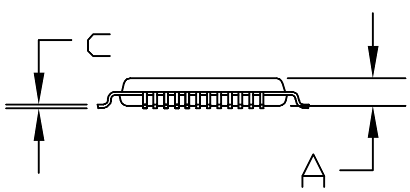
PCB Layout Guidelines

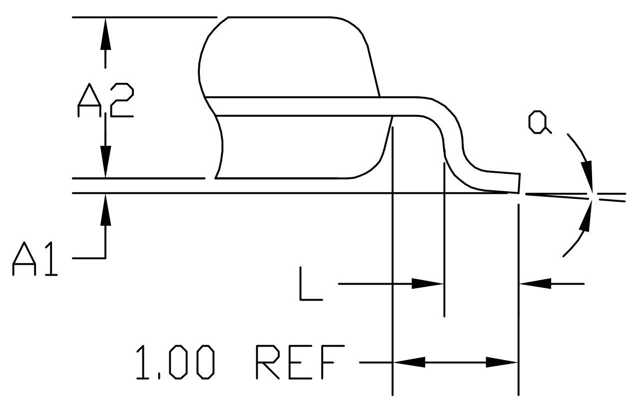
Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. The output traces to the laser diode must be short to minimize inductance. Short output traces will provide best performance.

Package Information - 48 Pin TQFP



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
	TQPF			
	MIN.	NOM.	MAX.	
A	~	~	1.60	
A_1	0.05	~	0.15	
A_2	1.35	1.40	1.45	
D	9.00 BSC.			
D_1	7.00 BSC.			
E	9.00 BSC.			
E_1	7.00 BSC.			
L	0.45	0.60	0.75	
N	48			
e	0.5 BSC.			
b	0.17	0.22	0.27	
c	0.09	~	0.20	
α	0	~	7	





1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Controlling dimension: millimeter.
3. This outline conforms to JEDEC Publication 95 Registration MS-026.

Ordering Information

The order number for this product is formed by a combination of the device type and package type.

VSC7938 xx

Device Type
SONET/SDH 3.125Gb/s
Laser Diode Driverwith Automatic Power Control

Package
RO: 48-Pin TQFP, 7x7x1.4mm
W: Dice Waffle Pack

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