Data Sheet

VSC8021/VSC8022

2.5Gb/s SONET-Compatible 8-Bit MUX/DEMUX Chipset

Features

- Serial Data Rates up to 2.5Gb/s
- Parallel Data Rates up to 312.5Mb/s
- ECL 100K Compatible Parallel Data I/Os
- Divide-by-8 Clock for Synchronization of Parallel Data to Interfacing Chips
- SONET Frame Recovery Circuitry (VSC8022)
- Compatible with STS-3 to STS-48 SONET Applications
- Differential or Single-Ended Inputs and Outputs
- Low Power Dissipation: 2.3W (Typ Per Chip)
- Standard ECL Power Supplies: V_{EE} = -5.2V, V_{TT} = -2.0V
- Available in Commercial (0°C to +70°C) or Industrial (-40°C to +85°C) Temperature Ranges
- Proven E/D Mode GaAs Technology
- 52-Pin Leaded Ceramic Chip Carrier

Functional Description

The VSC8021 and VSC8022 are high-speed SONET interface devices capable of handling serial data at rates up to 2.5Gb/s. These devices can be used for STS-3 through STS-48 SONET applications.

These products are fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high-speed and low power dissipation. These products are packaged in a ceramic 52-pin leaded ceramic chip carrier.

VSC8021

The VSC8021 contains an 8:1 multiplexer and a self-positioning timer. The 8:1 multiplexer accepts 8 parallel differential ECL data inputs (D1-D8, D1N-D8N) at rates up to 312.5Mb/s and multiplexes them into a serial differential bit stream output (DO, DON) at rates up to 2.5Gb/s.

The internal timing of the VSC8021 is built around the high-speed clock (up to 2.5GHz) delivered onto the chip through a differential input (CLKI, CLKIN). This signal is subsequently echoed at the high-speed differential output (CO, CON).

The parallel data inputs are clocked to on-chip input registers with an externally supplied differential ECL input (BYCLK, BYCLKN) operating at the same rate as the data inputs. An internal byte clock, which is a divide-by-8 version of the high-speed clock, is used to transfer the data to a set of buffer registers. This internal byte clock is brought off chip at the ECL output CLK8, CLK8N.

Internal circuitry monitors the internal and external byte clocks and generates an ERR signal if a timing violation is detected. This signal can be gated to the SYNC input which is edge sensitive high. An active SYNC input allows the VSC8021 timing to shift, positioning it properly against the external byte clock, CLK8, CLK8N. When a CLK8 timing switch is made, normal data flow will be invalid for 1 byte.

There are two clock inputs, CLKI and BYCLK, going into the VSC8021. These two clocks serve as timing references for different parts of the VSC8021. The BYCLK is used to trigger the input registers for the parallel data inputs, while the CLKI is used to trigger the high-speed serial output register as well as some of the timing circuitry for the parallel to serial conversion. Furthermore, in order to make this part easy to use, the user is not required to assume a known phase relationship between CLKI and the BYCLK.

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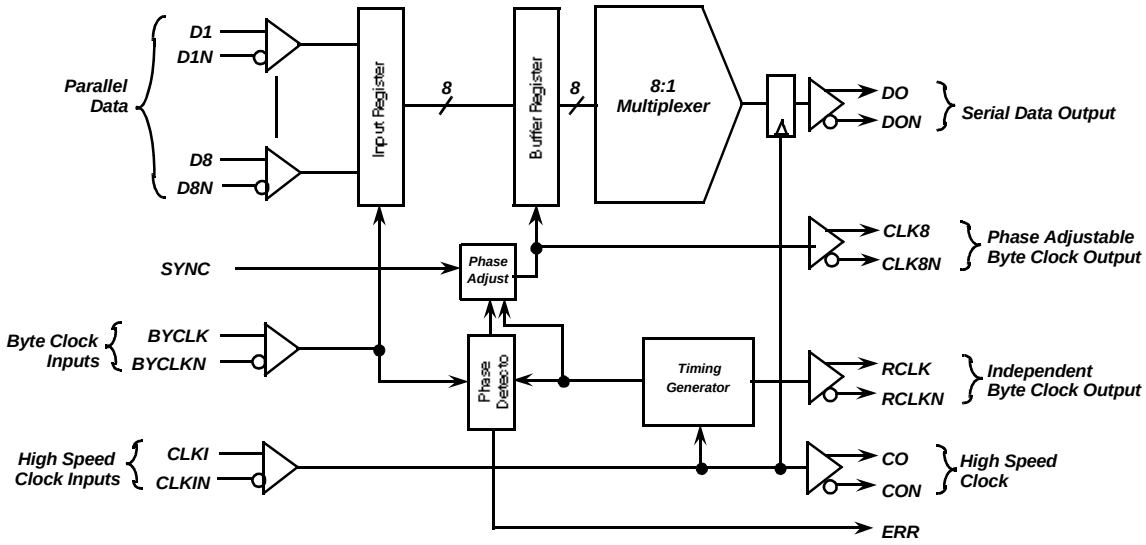
An internal Phase Detector and Phase Adjust Circuit are used to facilitate the two asynchronous circuits to work with each other. The Phase Detector and the Phase Adjust Circuit work together to adjust the internal clock CLK8 to make sure the set up and hold conditions are met for the internal registers. CLK8 is derived from CLKI and the RCLK is a non-phase varying byte clock output. The edge sensitive SYNC signal is simply the control signal that enables the Phase Detector circuitry.

As a summary, the CLKI is the high-speed clock input. The BYCLK is the external byte clock. The CLK8 is the internal byte clock derived from CLKI, phase-adjusted if SYNC is enabled. The RCLK is a non-phase-adjusted divided-by-8 clock generated from CLKI. The phase of RCLK, RCLKN is not affected by the self-adjusting circuitry, therefore it can be used as a system reference clock. RCLK, RCLKN can be used by the system designer to generate BYCLK, BYCLKN. The self-positioning timer and RCLK, RCLKN allow for the creation of very tight parallel data timing for the VSC8021.

Figure 1: VSC8021 Block Diagram



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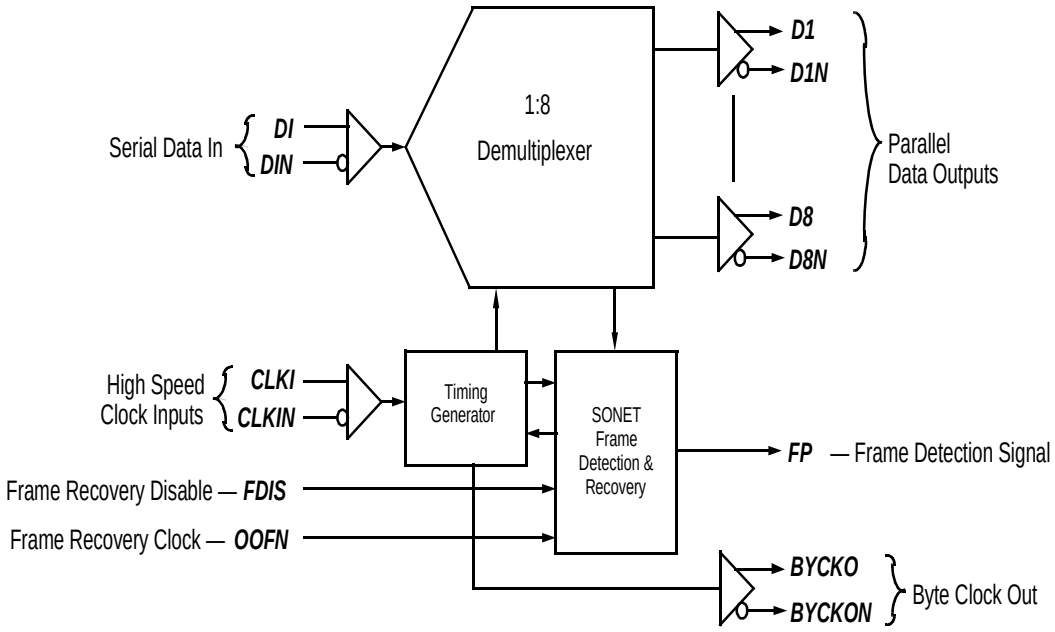
VSC8022

The VSC8022 contains both a 1:8 demultiplexer and SONET frame recovery circuitry. The 1:8 demultiplexer accepts a serial data input (DI, DIN) at rates up to 2.5Gb/s and converts it into 8 parallel differential ECL data outputs (D1-D8, D1N-D8N) at rates up to 312.5Mb/s. Valid parallel data outputs are indicated by the divide by 8 differential clock outputs BYCKO, BYCKON.

The VSC8022 also contains a SONET frame recovery circuit. The frame recovery circuits are enabled by a falling edge on the OOFN ECL input when the FDIS input is low. Once enabled, the frame recovery circuit starts looking for the SONET framing sequence. Once the frame is detected, the word boundary is realigned, a confirmation signal is sent off-chip through the FP ECL output and the frame recovery circuits are disabled. While the frame aligner is hunting for the frame, BYCKO, BYCKON and parallel data are invalid.

Figure 2: VSC8022 Block Diagram



Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

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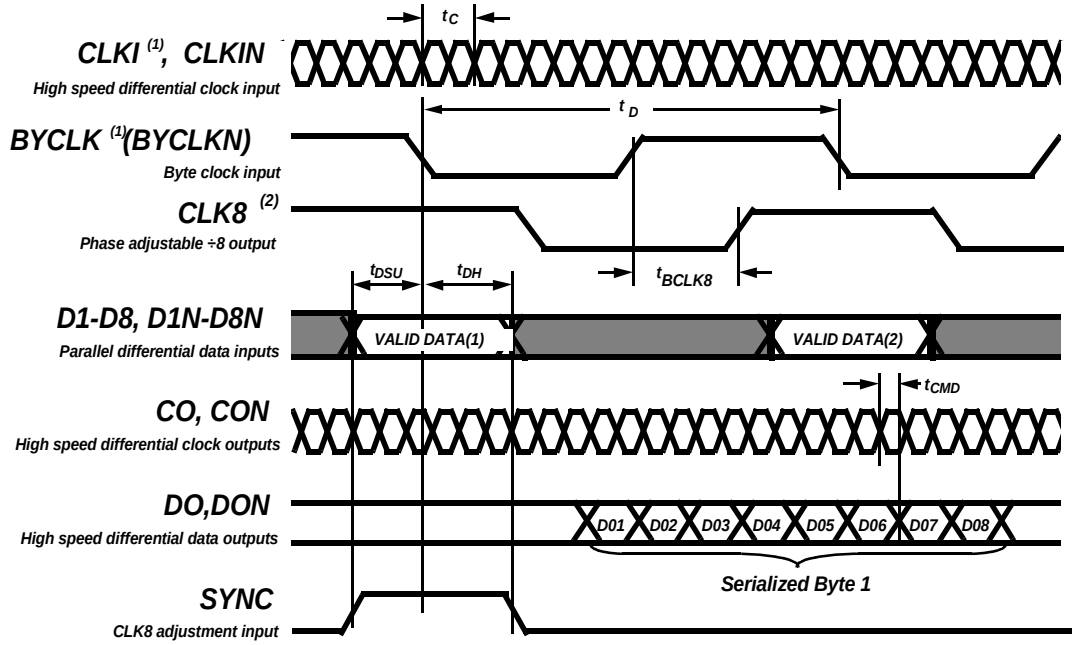
VSC8021 Multiplexer AC Characteristics *(Over recommended operating conditions)*

Figure 3: VSC8021 Multiplexer Waveforms



NOTES: (1) Negative edge is active edge.
(2) BYCLK/CLK8 timing required when SYNC not connected to ERR.
CLKI (CLKIN) period x 8 = BYCLK (BYCLKN) period.
= Don't care.

Table 1: VSC8021 Multiplexer AC Characteristics (over recommended operating conditions)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_C	Clock period(1)	400			ps	
t_D	BYTE clock period ($t_D = t_C$ x 8)	3.2			ns	
t_{DSU}	Parallel data set-up time	0.6			ns	
t_{DH}	Data hold time	1.4			ns	
t_{CMD}	High-speed clock output (CO, CON) timing, falling edge of CO to muxed data output, (DO, DON) timing	220		350	ps	
t_{BCLK8}	Byte clock to CLK8 timing(2)	0.5	1.0	1.5	ns	
Jitter (p-p)	CLKI, CLKIN to DO, DON (max-min), (HI to LO), same part, same pin at constant conditions		<50		ps	

NOTES: (1) The parts are guaranteed by design to operate from DC to a maximum frequency of 2.5GHz.
(2) Required when SYNC not connected to ERR.

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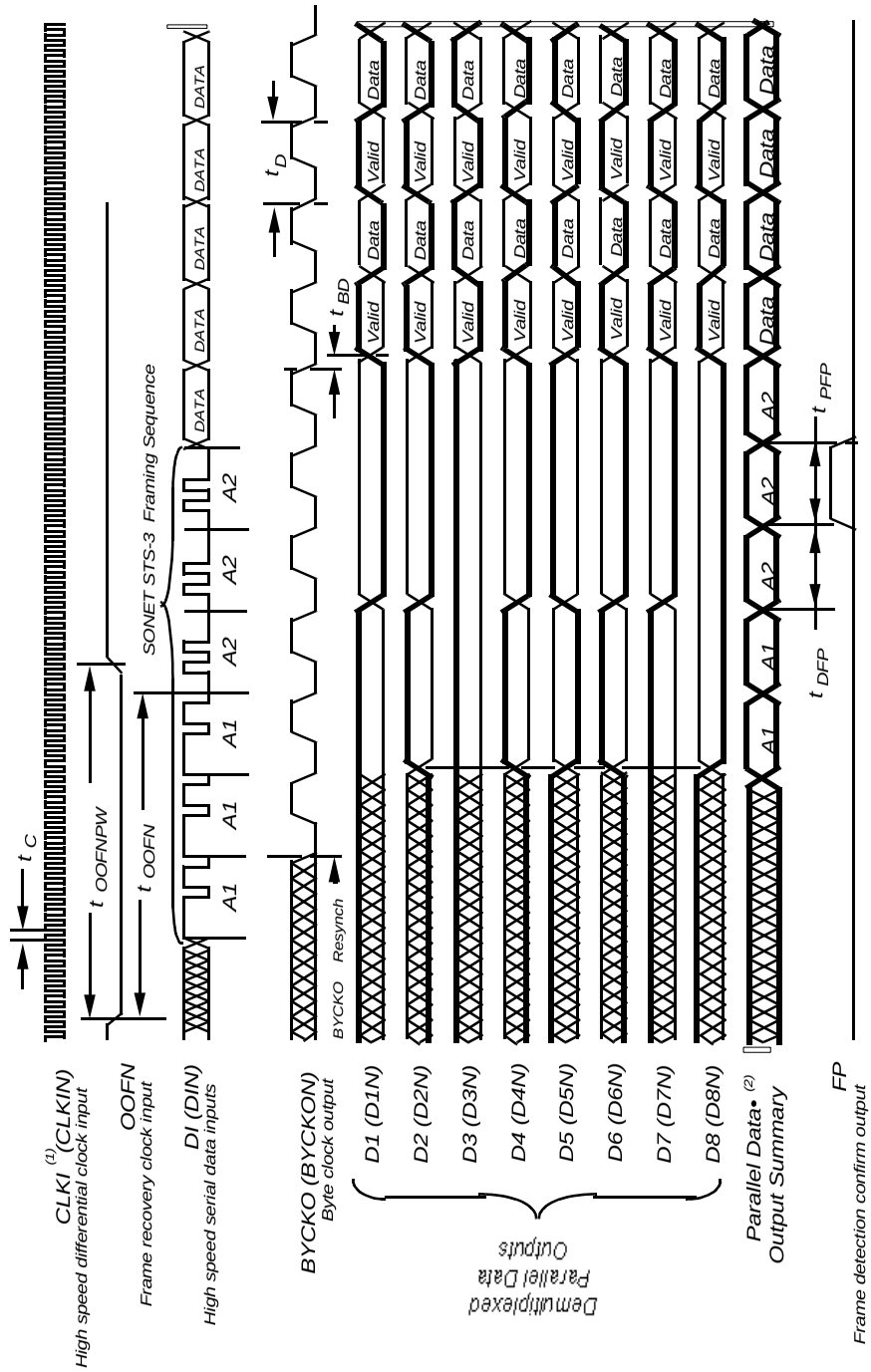
VSC8022 AC Characteristics *(Over recommended operating conditions)*

Figure 4: VSC8022 Demultiplexer Waveforms



NOTES:
1) Negative edge is active edge.
2) The parallel data outputs only begin showing valid data after the last A2 of the SONET framing sequence. The example waveforms shown above use an STS-3 framing sequence for convenience, thus valid data is output after the third A2 in the sequence.

= Don't care.

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Table 2: VSC8022 Demultiplexer AC Characteristics

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_C	Clock period(1)	400			ps	
t_D	BYTE clock period ($t_D = t_C$ x 8) (framed)	3.2			ns	
t_{BD}	BYTE clock output to valid data	0.5	1.0	2.0	ns	
t_{DFP}	FP rising edge from parallel data output change from A1 to A2 ($t_{DFP} = t_D$)		3.2		ns	
t_{PFP}	FP pulse width ($t_{PFP} = t_D$)	3.2			ns	
t_{OOFN}	OOFN falling edge before A1 chan ges to A2 ($t_{OOFN} = t_D$ x 4)	12.8			ns	
t_{OOFNPW}	OOFN pulse width ($t_{OOFNPW} = t_D$)	3.2			ns	
Phase Margin	Serial data phase timing margin with respect to high-speed clock: $Phase\ Margin = \left(1 - \frac{t_{SU} + t_H}{t_C}\right)360°$	135	180		degrees	

NOTE: (1) If t_C changes, all the remaining parameters change as indicated by the equations.

DC Characteristics

Table 3: Low Speed ECL Inputs and Outputs

(Over recommended operating range with internal V_{REF}, V_{CC} = GND, output load = 50Ω to -2.0V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage	-1020		-700	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{OL}	Output LOW voltage	V_{TT}		-1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
V_{IH}	Input HIGH voltage	-1150		-600	mV	Guaranteed HIGH signal for all inputs
V_{IL}	Input LOW voltage	V_{TT}		-1500	mV	Guaranteed LOW signal for all inputs
ΔV_{OUT}	Output voltage swing	0.8	1.0	1.4	V	Output load 50Ω to V_{TT}

Note: Differential ECL output pins must be terminated identically.

Table 4: High-Speed Inputs and Outputs

(Over recommended operating conditions, V_{CC} = GND, Output load = 50Ω to -2.0V)

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔV_{IN}	Input voltage swing	0.8	1.0	1.2	V	AC-coupled
V_{OH}	Output HIGH voltage		-0.9		V	Output load, 50Ω to -2.0V
V_{OL}	Output LOW voltage		-1.8		V	Output load, 50Ω to -2.0V
$\Delta V_{OUT(DATA)}$	Output voltage swing for data	0.6	0.8	1.2	V	Output load, 50Ω to -2.0V
$\Delta V_{OUT(clk)}$	Output voltage swing for clock	0.6	0.7	1.2	V	Output load, 50Ω to -2.0V

NOTES: (1) A reference generator is built in to each high-speed input, and these inputs are designed to be AC-coupled.
(2) If a high-speed input is used single-ended, a 150pF capacitor must be connected between the unused high-speed or complement input and the power supply (V_{TT}).
(3) Differential high-speed outputs must be terminated identically.

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Table 5: Power Dissipation

(Over recommended operating conditions, V_{CC} = GND, outputs open circuit)

Parameter	*Description*	*VSC8021*			*VSC8022*			*Units*	*Conditions*
		Min	*Typ*	*Max*	*Min*	*Typ*	*Max*		
I_{EE}	Power supply current from V_{EE}		400	600		450	600	mA	
I_{TT}	Power supply current from V_{TT}		110	200		120	200	mA	
P_D	Power dissipation		2.3	3.75		2.6	3.75	W	

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{TT}) ..... -3.0V to + 0.5V
Power Supply Voltage (V_{EE}) ..... V_{TT} + 0.7V to -6.0V
ECL Input Voltage Applied(2) (V_{ECLIN}) ..... -2.5V to + 0.5V
High-Speed Input Voltage Applied(2) (V_{HSIN}) ..... V_{EE} -0.7V to V_{CC} + 0.7V
Output Current (DC, output HIGH) (I_{OUT}) ..... -50 mA
Case Temperature Under Bias (T_C) ..... -55ºC to +125ºC
Storage Temperature(3) (T_{STG}) ..... -65ºC to +150ºC

Recommended Operating Conditions

ECL Power Supply Voltage(4) (V_{TT}) ..... -2.0V ± 0.1V
Power Supply Voltage (V_{EE}) ..... -5.2V ± 0.26V
Operating Temperature Range(3) (T) ..... (Commercial) 0ºC to +70ºC, (Industrial) -40ºC to +85ºC

Notes: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) V_{TT} must be applied before any input signal voltage magnitude ($|V_{ECLIN}|$ and $|V_{HSIN}|$) can be greater than $|V_{TT}$ -0.5V.|

(3) Lower limit of specification is ambient temperature and upper limit is case temperature.

(4) When using internal ECL 100K reference level.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8021/VSC8022 is rated to the following ESD voltages based on the human body model:

1. All ECL pins are rated at or above 1000V.
2. All high-speed clock and data pins at rated at or above 500V.

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VSC8022 SONET Frame Recovery and Detection

The SONET framing sequence is a string of A1 bytes followed by a string of A2 bytes. (A1 = 11110110 and A2 = 00101000). The first serial bit starts at the left of the byte. Table 6 shows the number of A1 and A2 bytes in each SONET frame for different line rates. The VSC8022 contains a frame recovery circuit and a frame detection circuit.

Table 6: A1/A2 Byte Count

STS Level	*Line Rate (Mb/s)*	*# of A1 Bytes*	*# of A2 Bytes*
STS-3	155.520	3	3
STS-12	622.080	12	12
STS-48	2488.32	48	48

Frame Recovery Circuit

The frame recovery circuit is designed to scan the serial data stream, looking for the A1 byte. When it finds the A1 pattern, it adjusts internal timing so that the serial data is properly demultiplexed onto the eight parallel outputs. Subsequently, the MSB of the A1 byte will appear in the D1 position and LSB of the A1 byte will appear in the D8 position. This word boundary alignment causes the BYCKO, BYCKON output to be resynchronized. While the frame aligner is hunting for the frame, BYCKO and parallel data are invalid. Frame recovery circuits are disabled by frame detection (resulting in FP) or by a falling edge on the OOFN input while FDIS is high.

Frame Detection Circuit

The frame detection circuit monitors the demultiplexed data, and senses the boundary between A1 and A2 bytes. This pulse on the FP output will reset the frame recovery circuit, so that no further resynchronization will occur until permission is given through OOFN.

Circuit Operation

The frame recovery circuits are initialized and enabled on the falling edge of the OOFN ECL input with FDIS held low. The OOFN must be at least one byte clock period wide. It must occur at least four byte clock periods before the A1/A2 boundary. The circuit requires at least three A1 bytes followed by 3 A2 bytes for successful alignment. The first A1 byte is used by the frame recovery circuit to obtain initial word boundary alignment, while the following two A1 and three A2 bytes are used to reset the frame recovery circuit and maintain alignment for the subsequent bit stream. Frame recognition will occur for each word boundary aligned A1A1A2A2A2 sequence in the data stream. Frame recognition is signaled by a one byte clock period high pulse on the FP ECL output pin. This FP pulse will appear one byte period after the first A2 byte appears on the parallel data output pins.

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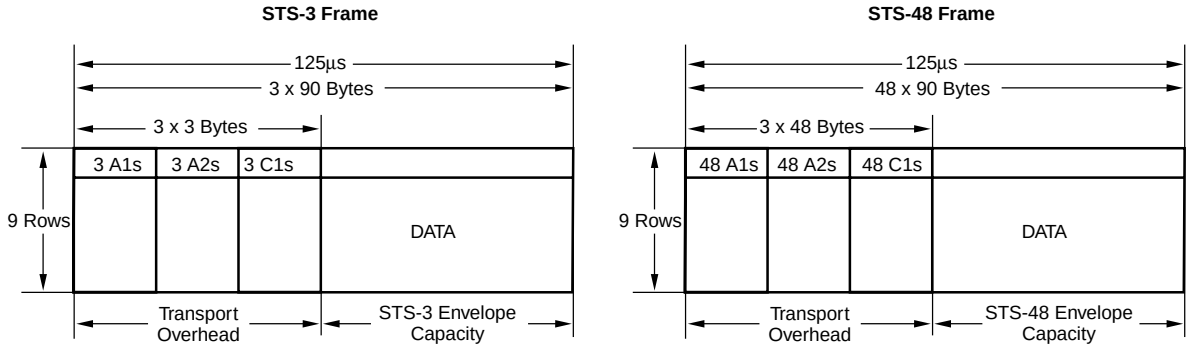
Figure 5: SONET Frame Structure



A1s and A2s: SONET Framing Sequence
C1s: STS Frame ID

High-Speed Inputs

In the past, the high-speed inputs, which are typically used for serial data and high-speed clock inputs with frequencies greater than 1GHz, were specified with absolute minimum and maximum voltage values. Since these inputs are intended for AC-coupled applications, they have been re-specified in terms of a voltage swing (ΔV_{IN}).

High-speed clocks are intended for AC-coupled operation. In most situations high-speed serial data will have high transition density and contain no DC offsets, making them candidates for AC-coupling as well. However, it is possible to employ DC-Pcoupling when the serial input data contains a DC component.

The structure of the high-speed input circuit is shown in Figure 6. DC-coupled circuits may be used to operate this input provided that the input swing is centered around the reference voltage. It is recommended that, in single-ended DC-coupling situations, the user provide an external reference which has better temperature and power supply rejection than the simple on-chip voltage divider. This external reference should have a nominal value of -3.5V and can be connected to the complementary input. This complication can be avoided in DC-coupled situations by using differential signals.

Figure 6: High-Speed Input Circuit Structure

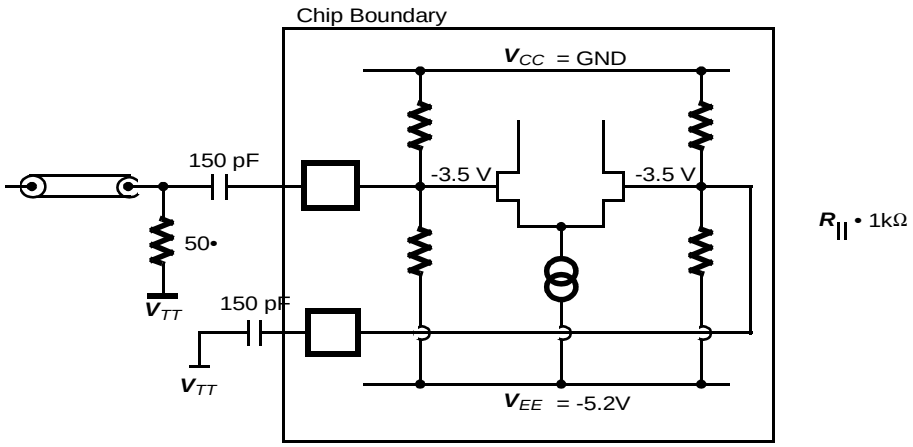


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Figure 7: VSC8021 Pin Diagram

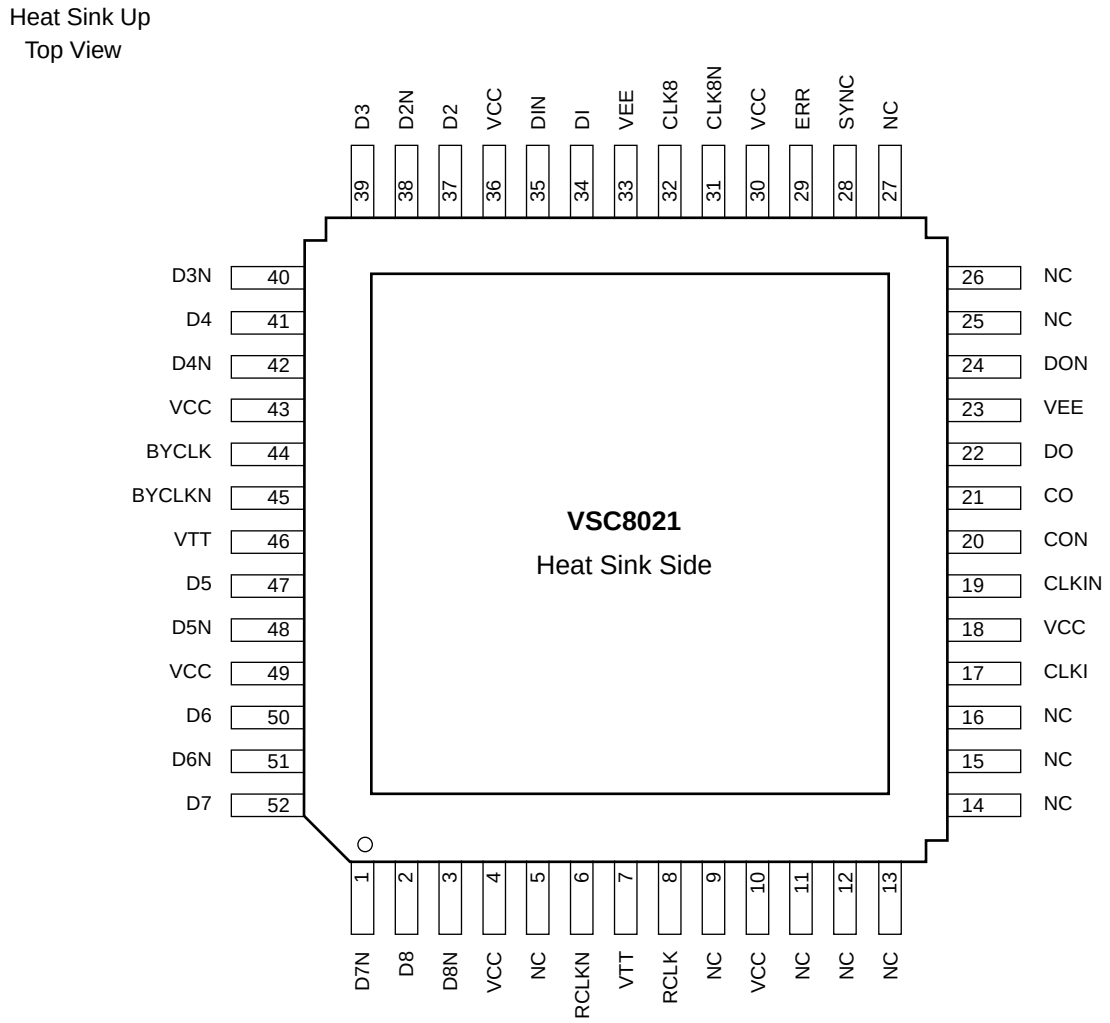

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Table 7: VSC8021 Pin Identifications

Pin #	*Signal Name*	*I/O*	*Level Type*	*Description*
1	D7N	I	ECL	Parallel Data Bit 7, Complement
2	D8	I	ECL	Parallel Data Bit 8, True
3	D8N	I	ECL	Parallel Data Bit 8, Complement
4	VCC	Pwr	0V	Ground
5	NC			No Connection
6	RCLKN	O	ECL	Independent CLK Divide-by-8 Clock, Complement
7	VTT	Pwr	-2.0V	Power Supply for Internal Reference Generation and Low Power Logic
8	RCLK	O	ECL	Independent CLK Divide-by-8 Clock, True
9	NC			No Connection
10	VCC	Pwr	0V	Ground
11	NC			No Connection
12	NC			No Connection
13	NC			No Connection
14	NC			No Connection
15	NC			No Connection
16	NC			No Connection
17	CLKI	I	HS	High-Speed Clock, True
18	VCC	Pwr	0V	Ground
19	CLKIN	I	HS	High-Speed Clock, Complement
20	CON	O	HS	High-Speed Clock, Complement
21	CO	O	HS	High-Speed Clock, True
22	DO	O	HS	High-Speed Serial Data Output, True
23	VEE[(1)]	Pwr	-5.2V	Power Supply for High-Speed Logic
24	DON	O	OHS	High-Speed Data, Complement
25	NC			No Connection
26	NC			No Connection
27	NC			No Connection
28	SYNC	I	ECL	Error Correction
29	ERR	O	ECL	Error Detection
30	VCC	Pwr	0V	Ground
31	CLK8N	O	ECL	Phase-Adjustable CLK Divide-by-8 Clock, Complement
32	CLK8	O	ECL	Phase-Adjustable CLK Divide-by-8 Clock, True

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33	VEE	Pwr	-5.2V	Power Supply for High-Speed Logic
34	D1	I	ECL	Parallel Data Bit 1, True
35	D1N	I	ECL	Parallel Data Bit 1, Complement
36	VCC	Pwr	0V	Ground
37	D2	I	ECL	Parallel Data Bit 2, True
38	D2N	I	ECL	Parallel Data Bit 2, Complement
39	D3	I	ECL	Parallel Data Bit 3, True
40	D3N	I	ECL	Parallel Data Bit 3, Complement
41	D4	I	ECL	Parallel Data Bit 4, True
42	D4N	I	ECL	Parallel Data Bit 4, Complement
43	VCC	Pwr	0V	Ground
44	BYCLK	I	ECL	Divide-by-8 Clock, True
45	BYCLKN	I	ECL	Divide-by-8 Clock, Complement
46	VTT	Pwr	-2.0V	Power Supply for Internal Reference and Low Power Logic
47	D5	I	ECL	Parallel Data Bit 5, True
48	D5N	I	ECL	Parallel Data Bit 5, Complement
49	VCC	Pwr	0V	Ground
50	D6	I	ECL	Parallel Data Bit 6, True
51	D6N	I	ECL	Parallel Data Bit 6, Complement
52	D7	I	ECL	Parallel Data Bit 7, True

NOTE: (1) Pin #23 is connected to the heat sink. Connect to V_{EE} or most negative chip voltage.

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Figure 8: VSC8022 Pin Diagram

Heat Sink Up
Top View

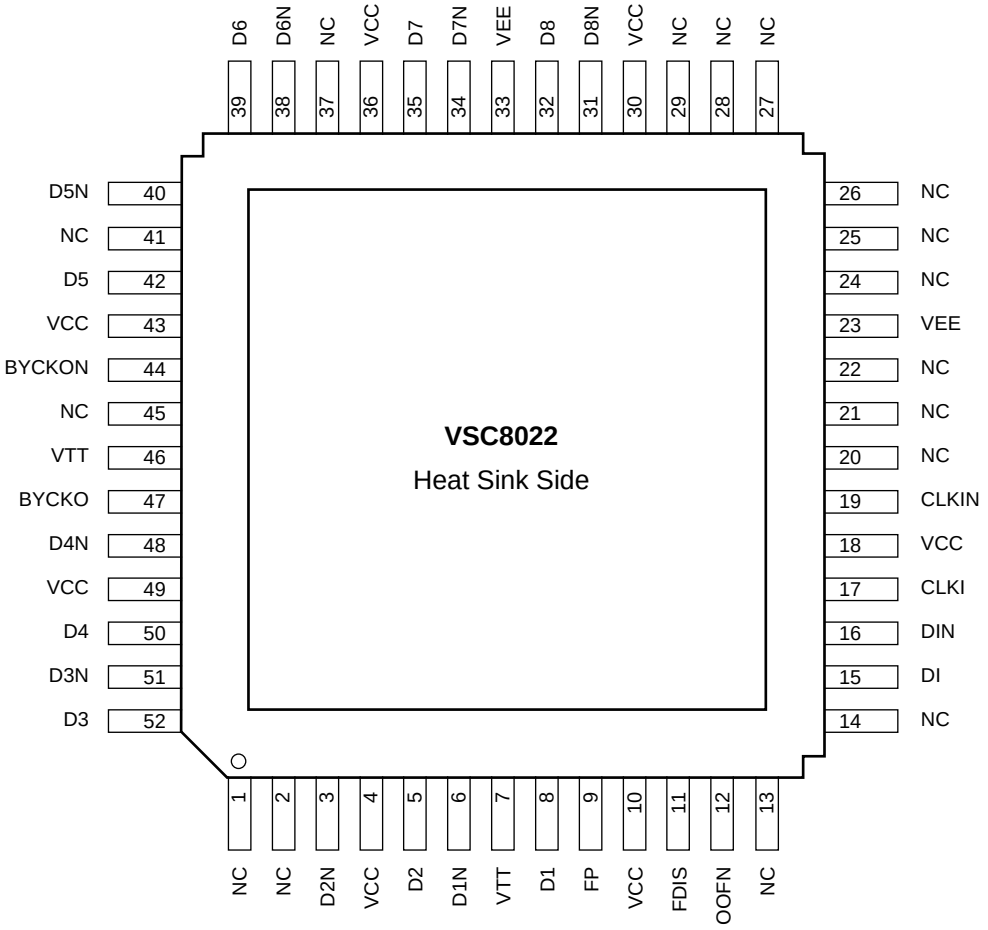

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Table 8: VSC8022 Pin Identifications

Pin #	*Signal Name*	*I/O*	*Level Type*	*Description*
1	NC			No Connection
2	NC			No Connection
3	D2N	O	ECL	Parallel Data Bit 2, Complement
4	VCC	Pwr	0V	Ground
5	D2	O	ECL	Parallel Data Bit 2, True
6	D1N	O	ECL	Parallel Data Bit 1, Complement
7	VTT	Pwr	-2.0	Power Supply for Internal Reference Generation and Low Power Logic
8	D1	O	ECL	Parallel Data Bit 1, True
9	FP	O	ECL	Frame Pulse. This pulse will appear one byte period after the first A2 byte appears on the parallel data output pins.
10	VCC	Pwr	0V	Ground
11	FDIS	I	ECL	Frame Recovery Disable
12	OOFN	I	ECL	Frame Recovery Enable
13	NC			No Connection
14	NC			No Connection
15	DI	I	HS	High-Speed Serial Data Bit 1, True
16	DIN	I	HS	High-Speed Serial Data Bit 1, Complement
17	CLKI	I	HS	High-Speed Clock, True
18	VCC	Pwr	0V	Ground
19	CLKIN	I	HS	High-Speed Clock, Complement
20	NC			No Connection
21	NC			No Connection
22	NC			No Connection
23	VEE[(1)]	Pwr	-5.2V	Power Supply for High-Speed Logic
24	NC			No Connection
25	NC			No Connection
26	NC			No Connection
27	NC			No Connection
28	NC			No Connection
29	NC			No Connection
30	VCC	Pwr	0V	Ground
31	D8N	O	ECL	Parallel Data Bit 8, Complement

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32	D8	O	ECL	Parallel Data Bit 8, True
33	VEE	Pwr	-5.2V	Power Supply for High-Speed Logic
34	D7N	O	ECL	Parallel Data Bit 7, Complement
35	D7	O	ECL	Parallel Data Bit 7, True
36	VCC	Pwr	0V	Ground
37	NC			No Connection
38	D6N	O	ECL	Parallel Data Bit 6, Complement
39	D6	O	ECL	Parallel Data Bit 6, True
40	D5N	O	ECL	Parallel Data Bit 5, Complement
41	NC			No Connection
42	D5	O	ECL	Parallel Data Bit 5, True
43	VCC	Pwr	0V	Ground
44	BYCKON	O	ECL	Divide-by-8 Clock, Complement
45	NC			No Connection
46	VTT	Pwr	-2.0V	Power Supply for Internal Reference and Low Power Logic
47	BYCKO	O	ECL	Divide-by-8 Clock, True
48	D4N	O	ECL	Parallel Data Bit 4, Complement
49	VCC	Pwr	0V	Ground
50	D4	O	ECL	Parallel Data Bit 4, True
51	D3N	O	ECL	Parallel Data Bit 3, Complement
52	D3	O	ECL	Parallel Data Bit 3, True

NOTE: (1) Pin #23 is connected to the heat sink. Connect to V_{EE} or most negative chip voltage.

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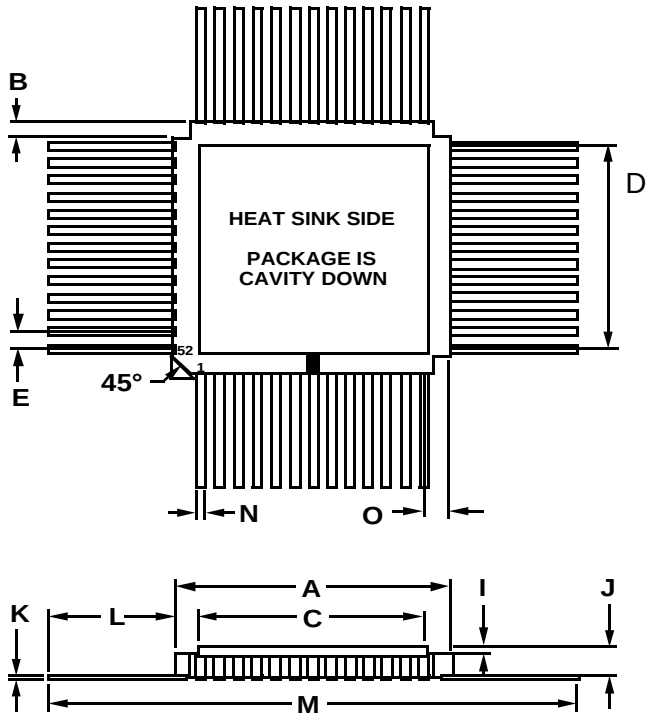
Package Information

52-Pin Leaded
Ceramic Package (LDCC)



NOTES:
Drawing not to scale.
Packages: Ceramic (alumina);
Heat sink: Copper-tungsten;
Leads: Alloy 42 with gold plating.

Item	*mm (Min/Max)*	*in (Min/Max)*	*Item*	*mm (Min/Max)*	*in (Min/Max)*
A	18.54/19. 56	0.730/0.770	I	0.41/0.61	0.016/0.024
B	1.02/1.52	0.040/0.060	J	2.03/2.79	0.080/0.110
C(1)	15.49/16.51	0.610/0.650	K(1)	0.09/0.24	0.003/0.009
D(1)	15.24 TYP	0.600 TYP	L	4.57/5.34	0.180/0.210
E	1.27 TYP	0.050 TYP	M	27.69/30.22	1.090/1.190
F	0.76/1.02	0.030/0.040	N	0.36/0.56	0.014/0.022
G	16.94 TYP	0.667 TYP	O	1.75/1.90	0.069/0.075
H	1.91/2.41	0.075/0.095	—	—	—

NOTE: (1) At package body.

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Order information

The order number for this product is formed by a combination of the device number, and package type.**Notice**

VSC802x **X** **X**

Device Type
VSC8021: SONET 2.5Gb/s 8-Bit Multiplexer
VSC8022: SONET 2.5Gb/s 8-Bit Demultiplexer

Temperature
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)

Package
F: Ceramic Leaded Chip Carrier (LDCC)

Notice

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