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Data Sheet
VSC8122-FEC

Multi-Rate SONET/SDH FEC
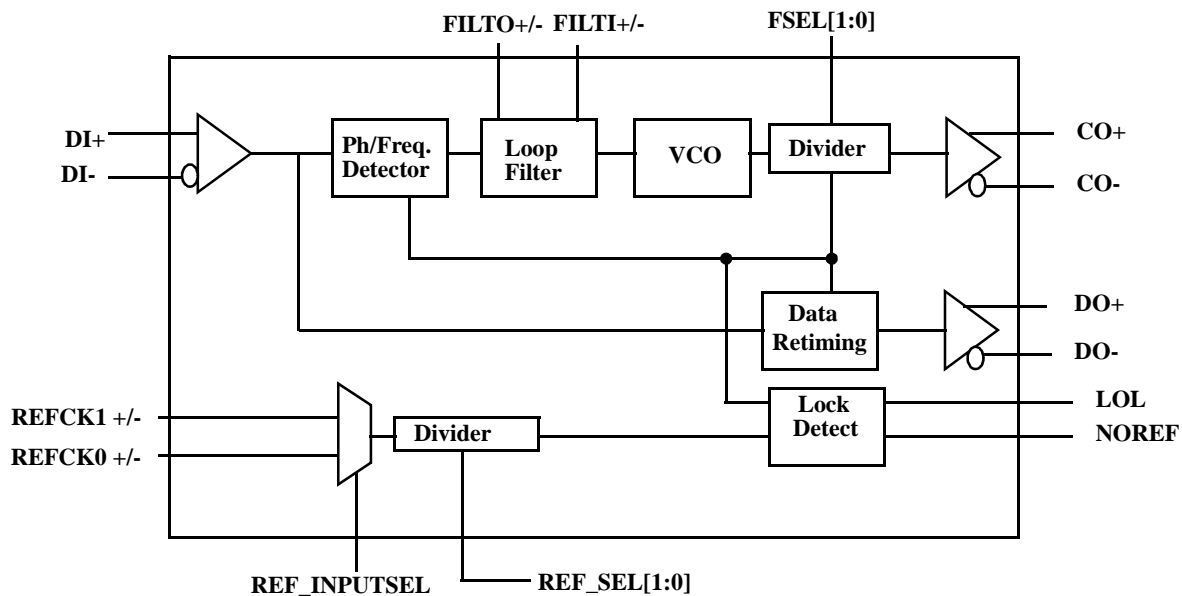*Clock and Data Recovery IC*

Features

- Multi-Rate OC-3, OC-12, OC-24, OC-48 Clock and Data Recovery
- Supports OC-48 FEC Rates
- Supports Gigabit Ethernet
- Differential Back Terminated I/O
- Maintains Clock Output in the Absence of Data
- Selectable Reference Clock

- Loss of Lock Indicator
- Exceeds SONET/SDH Requirements for Jitter Tolerance, Jitter Transfer and Jitter Generation
- 3.3V Supply Operation
- 1W Typical Power
- 10x10 mm 64-Pin PQFP Packaging

General Description

The VSC8122-FEC is a single chip clock recovery IC for use in SONET OC-48, OC-24, OC-12, OC-3, or Gigabit Ethernet systems operating at their respective 2.488Gb/s (up to 2.66606Gb/s FEC), 1.244Gb/s, 622Mb/s, 155Mb/s, or 1.25Gb/s data rates. It complies with SONET jitter tolerance, jitter transfer and jitter generation specifications.

Alarm functions support typical telecom system applications. The Loss of Lock (LOL) output indicates when the device goes out of lock, which would most often occur in the event of a loss of valid data. The NOREF output flags when the reference input to the VSC8122-FEC either is removed, or goes severely out of tolerance.
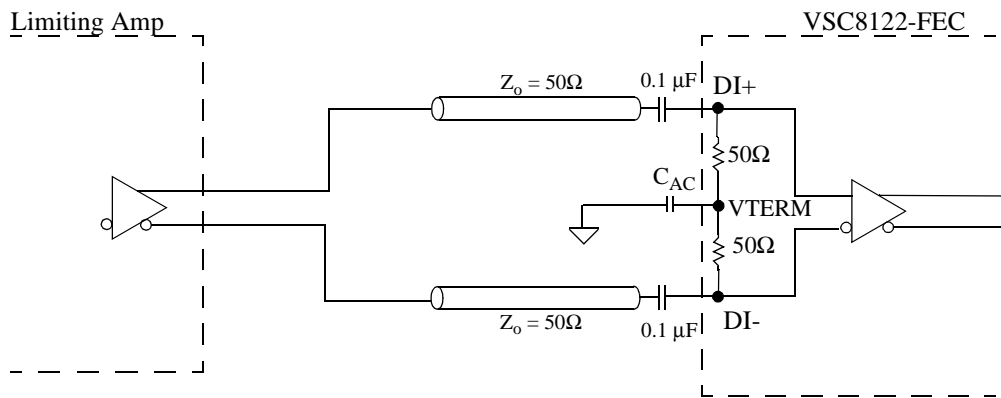
VSC8122-FEC Block Diagram

G52300-0, Rev 4.1
03/01/01

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Functional Description

Data Input

The data input receiver is internally terminated by a center-tapped resistor network. For differential input AC-coupling, the network is terminated to the appropriate termination voltage, VTERM through a blocking capacitor, C_{AC}, to ground. The input requires a differential signal with a peak-to-peak voltage on both the true and complement of a minimum of 250mV. These inputs are required to be AC-coupled to permit use with a variety of limiting amplifiers
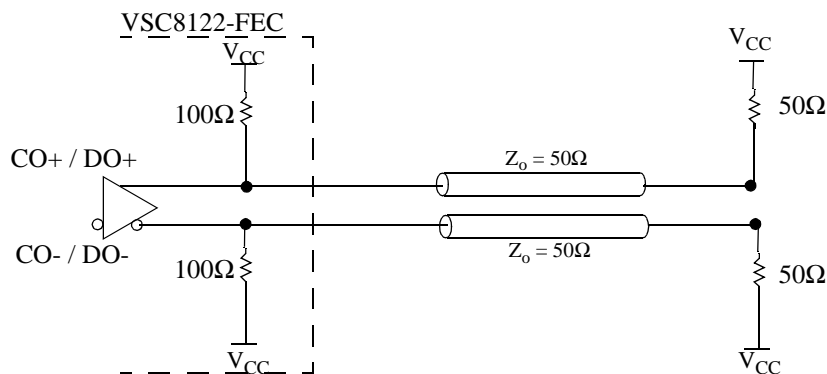
Figure 1: Input Termination (AC coupled)

High-Speed Clock and Data Outputs

The VSC8122-FEC high-speed clock and data outputs can be DC terminated, 50Ω to V_{CC} as indicated in Figure 2.

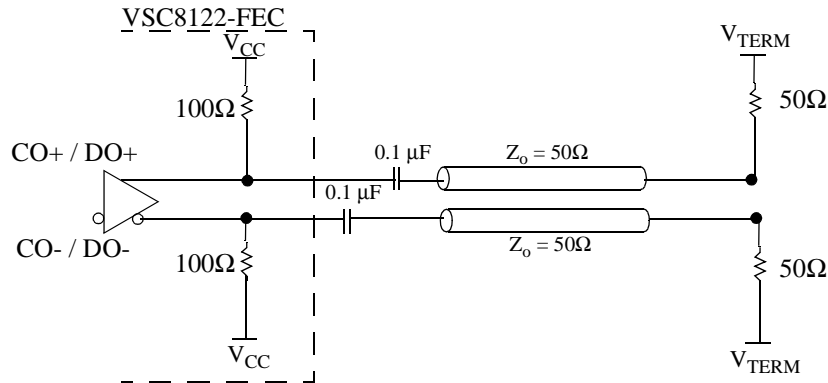**Figure 2: High-Speed Clock and Data Output DC Termination.**

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Outputs can also be AC terminated as shown in Figure 3. The output differential voltage and common-mode voltage range are specified in Table 4, High-Speed Inputs and Outputs.

Figure 3: High-Speed Clock and Data Output AC Termination.

Clock Recovery

The VSC8122-FEC has a selectable input data rate. Two pins (FSEL0 and FSEL1) select the data rate to be provided to the VSC8122-FEC.

Table 1: Input Data Rate Select

Input Data Rate	*FSEL0*	*FSEL1*
2.488Gb/s - 2.66606Gb/s	0	0
1.244Gb/s or 1.25Gb/s	1	0
622Mb/s or 625Mb/s	0	1
155.52Mb/s or 156.25Mb/s	1	1

The incoming data is presented both to the clock recovery circuit and the data retiming circuit. When there is a phase error between the incoming data and the on-chip VCO, the loop filter raises or lowers the control voltage of the VCO to null the phase difference.

The lock detector monitors the frequency difference between the REFCK (optionally divided by a prescaler), and the recovered clock divided by 128. In the event of the loss of an input signal, or if the input is switching randomly, the VCO will move in one direction. At the time the VCO differs by more than 1MHz from the REFCK based 2.488GHz rate (up to 2.66606Gb/s FEC), the lock detector will assert the LOL output. LOL is designed to be asserted from between 2.3μs and 100μs after the interruption of data. The VCO will continue to be frequency-locked at approximately 1MHz off of the REFCK based 2.48832GHz rate (up to 2.66606Gb/s FEC).

When NRZ data is again presented at the data input, the phase detector will permit the VCO to lock to the incoming data. Hysteresis is provided which delays the deassertion of LOL until approximately 160us following the restoration of valid data.

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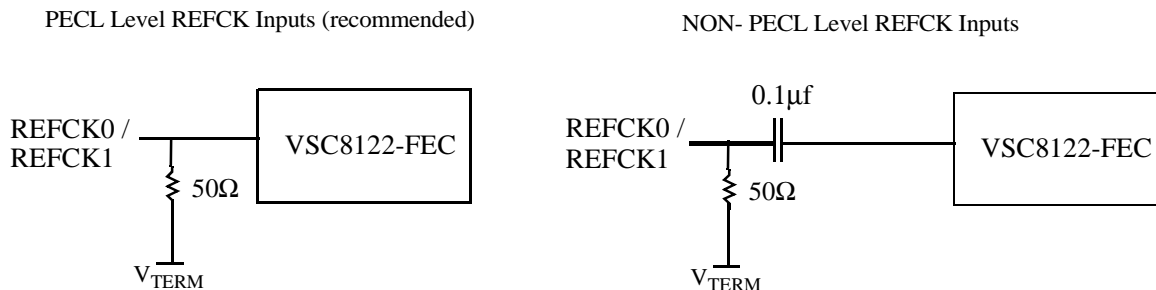*Clock and Data Recovery IC*

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The NOREF output will go high to indicate that there is no signal on the REFCK input, or that the REFCK is more than approximately 25% above or below the expected value.

Two sets of reference frequencies for the VSC8122-FEC are shown in Table 2. SONET reference clock frequencies are as indicated, with Gigabit Ethernet frequencies listed in parenthesis. FEC rate frequencies are indicated at rates for use with the VSC9210 FEC device operating at 2.65Gb/s. The two different sets of reference clocks are needed since the reference clock for SONET and Gigabit Ethernet applications will be slightly different. Internally, the VSC8122-FEC requires a 19.44MHz reference (or 19.53MHz reference for Gigabit Ethernet).

The customer can select to provide either the 19.44MHz reference (or 19.53MHz reference for Gigabit Ethernet), or the 2x, 4x or 8x of that reference at 38.88MHz (39.06MHz), 77.76MHz (78.13MHz) or 155MHz (156.25MHz). For FEC rates, the customer can select the appropriate frequency as indicated in Table 2. The REF_SEL[1:0] inputs will program the internal divider as required to use the selected REFCK frequency.

Two reference clock inputs are provided, REFCK1 and REFCK0, to allow "on the fly switching" between SONET and Gigabit Ethernet applications if desired. Since SONET and Gigabit Ethernet require different reference clock frequencies, the VSC8122-FEC allows the user to toggle between the two reference clock frequencies REFCK1 and REFCK0 to supply the appropriate input clock. REF_INPUTSEL is used to toggle between the two reference clock input frequencies. REF_INPUTSEL= "0" selects REFCK0, REF_INPUTSEL= "1" selects REFCK1. Either reference clock input (REFCK1, REFCK0) can be used for SONET or Gigabit Ethernet reference frequencies. PECL levels are recommended for REFCK inputs (see Figure 4). If a reference clock is unused, it is recommended that one of its inputs be tied to VCC through a 5.1kΩ resistor, the other one to GND through a 5.1kΩ resistor.

Figure 4: REFCK Input Levels

PECL Level REFCK Inputs (recommended)

NON- PECL Level REFCK Inputs

* V_{TERM} can be to any power supply, as long as PECL levels are supplied to REFCK inputs.

Typically, V_{EE} (typ. GND) is used as V_{TERM}.

** For differential REFCK input signals, 100Ω termination between true and complement REFCK signals can be substituted for the 50Ω to V_{TERM} termination on each line.

Table 2: Reference Frequency

Reference Frequency			REF_SEL0	REF_SEL1
OC-48	*OC-48 FEC*	*Gigabit Ethernet*		
19.44MHz	20.74MHz[1]	19.53MHz	0	0
38.88MHz	41.47MHz[1]	39.06MHz	1	0
77.76MHz	82.9MHz[1,2]	78.13MHz	0	1
155.52MHz	165.89MHz[1,2]	156.25MHz	1	1

NOTES: (1) Indicates FEC reference clock frequency for use with VSC9210 FEC device running at 2.65Gb/s. (Reference clock frequencies can operate at frequencies up to 2.66606GHz / Y, where Y = 16, 32, 64, 128.). (2) Indicates recommended reference clock frequencies.

Loop Filter

The Phase Locked Loop (PLL) on the VSC8122-FEC employs two external capacitors. The PLL design is fully differential; therefore, the loop filter must also be fully differential. One capacitor should be connected between FILTAO and FILTAI, with the other connected between FILTAON and FILTAIN. Recommended capacitors are low inductance 1.0µF (0603 or 0805) ceramic SMT X7R devices, 6.3 WVDC or greater.

AC Characteristics (Over recommended operating conditions)

Table 3: AC Characteristics

Parameters	Description	Min		Max	Units	Conditions
t_{pd}	Center of output data eye from rising edge of CO+	-75		+75	ps	
t_r, t_f	DO± rise and fall times	—		150	ps.	20% to 80% into 50Ω load.
t_r, t_f	CO± rise and fall times	—		135	ps	20% to 80% into 50Ω load.
$Jitter_{gen}$	Jitter Generation	—		3.6	ps - rms	Measured at the high-speed data output for jitter in the 12kHz - 20MHz band. Assume 1.2ps rms input data jitter.
$Jitter_{tol}$	Jitter Tolerance	—		—	—	Exceeds SONET/SDH mask
LBW	Loop Bandwidth	—		2.0	MHz	-3dB point of jitter transfer curve
$Jitter_{peak}$	Jitter Peaking	—		0.1	dB	

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Figure 5: High-Speed Clock and Data Outputs

Table 4: High-Speed Inputs and Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
ΔV_{OD}	Data output voltage swing	600	900	1000	mV	
ΔV_{OC}	Clock output voltage swing	400	700	1000	mV	
V_{CMO}	Common-mode range (DO/CO)	2.6	—	3.2	V	
V_{DIFF}	Serial input absolute voltage, single-ended peak-to-peak swing (V_{IH}-V_{IL}) for DI +/-	250	—	1200	mV	AC-coupled
R_{IN}	Input resistance between DI+ and VTERM or DI- and VTERM	43	—	58	Ω	

Table 5: PLL Parameters

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
	REF_CLK duty cycle	45	—	55	%	
	REF_CLK frequency range	-100	—	+100	ppm	
V_{IH}	REF_CLK input HIGH voltage	V_{CC}-1.165	—	V_{CC}-0.7	V	
V_{IL}	REF_CLK input LOW voltage	V_{CC}-2.0	—	V_{CC}-1.475	V	

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DC Characteristics *(Over recommended operating conditions).*

Table 6: TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW voltage	—	—	0.5	V	I_{OL}= 1.0mA
V_{IH}	Input HIGH voltage	2.0	—	3.47	V	
V_{IL}	Input LOW voltage	0	—	0.8	V	
I_{IH}	Input HIGH current	—	50	500	μA	V_{IN} = 2.4V
I_{IL}	Input LOW current	—	—	500	μA	V_{IN} = 0.5V

Table 7: Power Supply

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{CC}	Supply voltage	3.14	3.3	3.47	V	3.3V± 5%
P_D	Power dissipation	-	1.0	1.2	W	Outputs unterminated
I_{CC}	Supply current	-	300	347	mA	Outputs unterminated

Absolute Maximum Ratings [1]

Power Supply Voltage (V_{CC}) .... -0.5V to +3.8V
DC Input Voltage (differential inputs) ....-0.5V to V_{CC} +0.5V
DC Input Voltage (TTL inputs)... -0.5V to +5.5V
DC Output Voltage (TTL outputs) .... -0.5V to V_{CC} + 0.5V
Output Current (TTL outputs)... +/-50mA
Output Current (differential outputs) ....+/-50mA
Case Temperature Under Bias.. -55°C to +125°C

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) .... +3.3V$\pm$5%
Operating Temperature Range ....0°C Ambient to +85°C Case Temperature
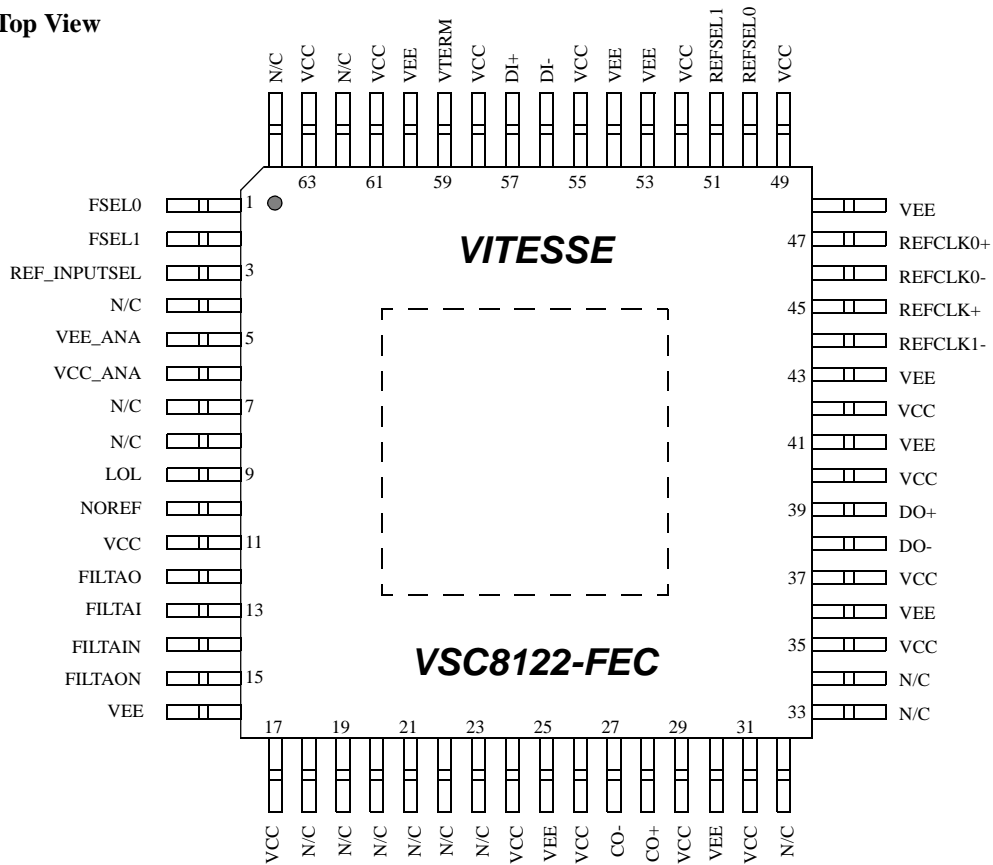
ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8122-FEC is rated to the following ESD voltages based on the human body model:
1. All pins are rated at or above 1500V.

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Package Pin Descriptions

Figure 6: Pin Diagram

Top View

Top side pins (left to right, pins 64–49):
N/C, VCC, N/C, VCC, VEE, VTERM, VCC, DI+, DI-, VCC, VEE, VEE, VCC, REFSEL1, REFSEL0, VCC

Left side pins (top to bottom):
1 FSEL0
FSEL1
3 REF_INPUTSEL
N/C
5 VEE_ANA
VCC_ANA
7 N/C
N/C
9 LOL
NOREF
11 VCC
FILTAO
13 FILTAI
FILTAIN
15 FILTAON
VEE

Right side pins (top to bottom):
VEE
47 REFCLK0+
REFCLK0-
45 REFCLK+
REFCLK1-
43 VEE
VCC
41 VEE
VCC
39 DO+
DO-
37 VCC
VEE
35 VCC
N/C
33 N/C

Bottom side pins (left to right, pins 17–32):
VCC, N/C, N/C, N/C, N/C, N/C, N/C, VCC, VEE, VCC, CO-, CO+, VCC, VEE, VCC, N/C

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Table 8: Pin Identification

Pin #	Name	I/O	Level	Description
1	FSEL0	I	TTL	Selectable input rate, pin 0
2	FSEL1	I	TTL	Selectable input rate, pin 1
3	REF_INPUTSEL	I	TTL	Toggle between REFCK1 and REFCK0
4	NC	—	—	No connect, leave unconnected
5	VEE_ANA	I	GND	Negative power supply pins for analog parts of CMU
6	VCC_ANA	I	+3.3V	Positive power supply pins for analog parts of CMU
7	NC	—	—	No connect, leave unconnected[1]
8	NC	—	—	No connect, leave unconnected[1]
9	LOL	O	TTL	Loss of Lock indication
10	NOREF	O	TTL	No reference output. Active HIGH for REFCK far off the expected frequency.
11	VCC	I	+3.3V	Positive power supply
12	FILTAO	I	—	Loop filter pin - connect via capacitor to FILTAI
13	FILTAI	I	—	Loop filter pin - connect via capacitor to FILTAO
14	FILTAIN	I	—	Loop filter pin - connect via capacitor to FILTAON
15	FILTAON	I	—	Loop filter pin - connect via capacitor to FILTAIN
16	VEE	I	GND	Negative power supply
17	VCC	I	+3.3V	Positive power supply
18	NC	—	—	No connect, leave unconnected[1]
19	NC	—	—	No connect, leave unconnected[1]
20	NC	—	—	No connect, leave unconnected[1]
21	NC	—	—	No connect, leave unconnected[1]
22	NC	—	—	No connect, leave unconnected[1]
23	NC	—	—	No connect, leave unconnected[1]
24	VCC	I	+3.3V	Positive power supply
25	VEE	I	GND	Negative power supply
26	VCC	I	+3.3V	Positive power supply
27	CO-	O	High-Speed	High-speed clock output, complement.
28	CO+	O	High-Speed	High-speed clock output, true.
29	VCC	I	+3.3V	Positive power supply
30	VEE	I	GND	Negative power supply
31	VCC	I	+3.3V	Positive power supply
32	NC	—	—	No connect, leave unconnected[1]
33	NC	—	—	No connect, leave unconnected[1]
34	NC	—	—	No connect, leave unconnected[1]
35	VCC	I	+3.3V	Positive power supply
36	VEE	I	GND	Negative power supply
37	VCC	I	+3.3V	Positive power supply

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Pin #	Name	I/O	Level	Description
38	DO-	O	High-Speed	High-speed data output, complement.
39	DO+	O	High-Speed	High-speed data output, true.
40	VCC	I	+3.3V	Positive power supply
41	VEE	I	GND	Negative power supply
42	VCC	I	+3.3V	Positive power supply
43	VEE	I	GND	Negative power supply
44	REFCK1-	I	LVPECL	Reference clock 1 input, complement.
45	REFCK1+	I	LVPECL	Reference clock 1 input, true.
46	REFCK0-	I	LCPECL	Reference clock 0 input, complement.
47	REFCK0+	I	LVPECL	Reference clock 0 input, true.
48	VEE	I	GND	GND power supply
49	VCC	I	+3.3V	Positive power supply
50	REF_SEL[0]	I	—	Reference clock rate select, pin 0.
51	REF_SEL[1]	I	—	Reference clock rate select, pin 1.
52	VCC	I	+3.3V	Positive power supply
53	VEE	I	GND	Negative power supply
54	VEE	I	GND	Negative power supply
55	VCC	I	+3.3V	Positive power supply
56	DI-	I	High-Speed	High-speed data input, complement.
57	DI+	I	High-Speed	High-speed data input, true.
58	VCC	I	+3.3V	Positive power supply
59	VTERM	I	0V->3.3V	High-speed data input termination voltage, connect to ground through a series AC-coupling capacitor.
60	VEE	I	GND	Negative power supply
61	VCC	I	+3.3V	Positive power supply
62	NC	—	—	No connect, leave unconnected[1]
63	VCC	I	+3.3V	Positive power supply
64	NC	—	—	No connect, leave unconnected[1]

NOTE: (1) No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or neg-
ative power supply rails may cause improper operation or failure of the device; or in extreme cases, cause permanent
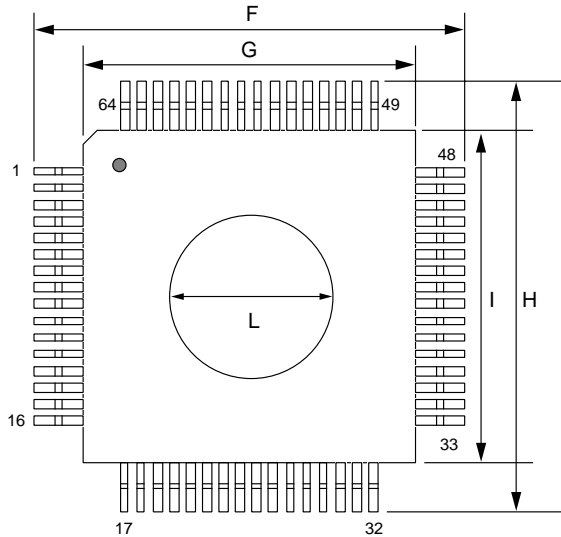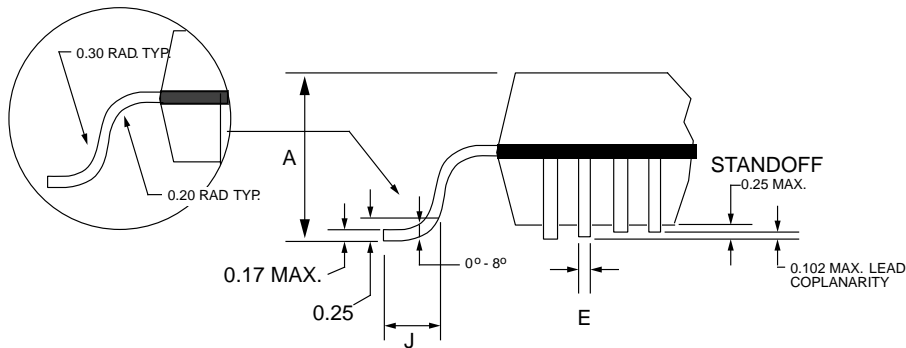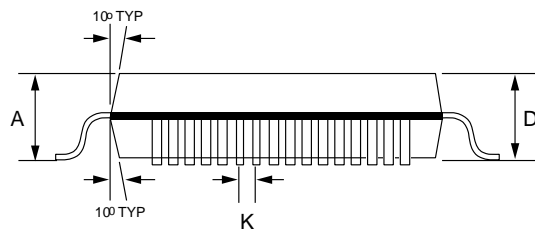*damage to the device.*

Package Information

64-pin PQFP Package Drawing

Item	10 mm	Tol.
A	2.45	MAX
D	2.00	+0.10
E	0.22	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	±.15
K	0.50	BASIC

10º TYP.

A

D

10º TYP.

K

0.30 RAD. TYP.

0.20 RAD. TYP.

A

STANDOFF
0.25 MAX.

0.17 MAX.

0.25

0º - 8º

0.102 MAX. LEAD COPLANARITY

E

J

NOTES:
Drawing not to scale.
Heat spreader up on 10mm package only.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

Package #: 101-XXX-X   *Package #: 101-XXX-X*
Issue #: 1   *Issue #: 1*

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Package Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in Table 9.

Table 9: Thermal Resistance

Symbol	Description	$^oC/W$
θ-jc	Thermal resistance from junction to case.	1.5
θ-ca	Thermal resistance from case to ambient with no airflow, including conduction through the leads.	31.5

Thermal Resistance With Airflow

Shown in Table 10 is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 10: Thermal Resistance With Airflow

Airflow	θ-ca ($^oC/W$)
100 lfpm	25.8
200 lfpm	23.0
400 lfpm	19.3
600 lfpm	17.0

Maximum Ambient Temperature Without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} = Theta case-to-ambient at appropriate airflow
$T_{A(MAX)}$ = Ambient air temperature
$T_{C(MAX)}$ = Case temperature (85^oC for VSC8122-FEC)
$P_{(MAX)}$ = Power (1.2W for VSC8122-FEC)

Table 11: Maximum Ambient Air Temperature Without Heatsink

Airflow	$T_{A(MAX)}$ ^oC
Still air	47.2
100 lfpm	54.0
200 lfpm	57.4
400 lfpm	61.8
600 lfpm	64.6

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.
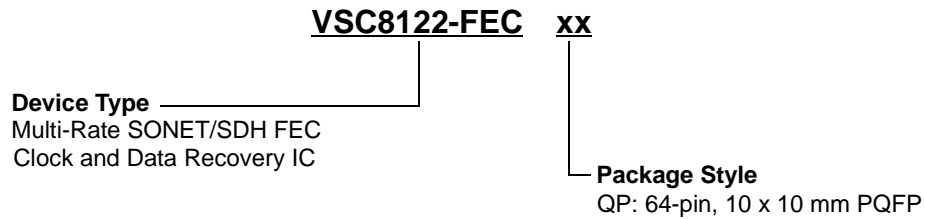
Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8122-FEC   **xx**

Device Type
Multi-Rate SONET/SDH FEC
Clock and Data Recovery IC

Package Style
QP: 64-pin, 10 x 10 mm PQFP

Notice

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