Winbond Electronics Corp.

STEP-LESS 3-DIMM CLOCK

1.0 GENERAL DESCRIPTION

The W83194BR-39B is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium II or Pentium III. W83194BR-39B provides 64 CPU/PCI frequencies which are selectable with smooth transitions by hardware or software. W83194BR-39B also provides 13 SDRAM clocks controlled by the none-delay buffer_in pin.

The W83194BR-39B provides step-less frequency programming by controlling the VCO freq. and the programmable PCI clock output divisor ratio. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

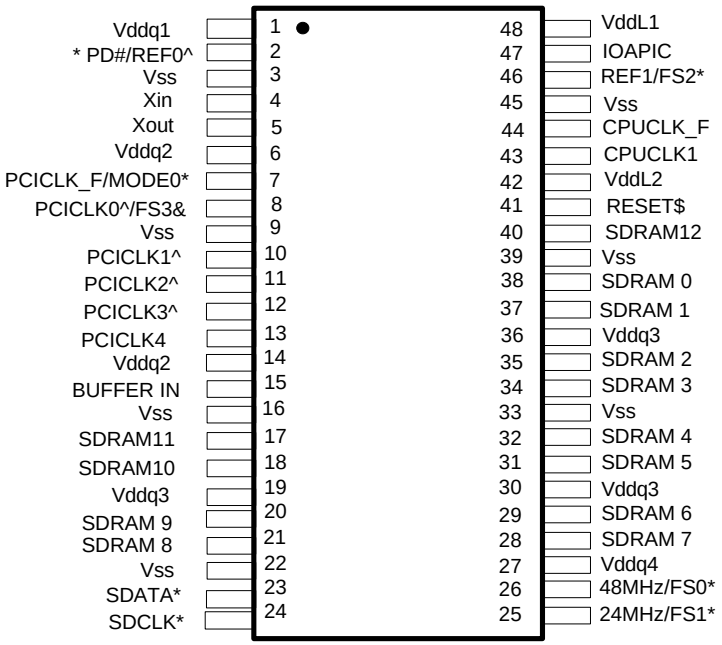
The W83194BR-39B accepts a 14.318 MHz reference crystal as its input. Spread spectrum built in at ±0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots(ISA, PCI, CPU, DIMM) is not recommend.

2.0 PRODUCT FEATURES

- Supports Pentium™ II and !!! CPU with I^2C.
- 2 CPU clocks (one free-running CPU clock)
- 13 SDRAM clocks for 3 DIMMs
- 6 PCI synchronous clocks
- One IOAPIC clock for multiprocessor support
- Optional single or mixed supply:
  (Vddq1=Vddq2 = Vddq3 = Vddq4 = VddL1 =VddL2= 3.3V) or (Vddq1= Vddq2 = Vddq3=Vddq4 = 3.3V, VddL1 = VddL2 = 2.5V)
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- < 5ns propagation delay SDRAM from buffer input
- Skew from CPU (earlier) to PCI clock 1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 66 MHz to 200 MHz CPU
- Step-less frequency programming by controlling the VCO freq. and the clock output divisor ratio
- I^2C 2-Wire serial interface and I^2C read back
- ±0.25% or ±0.5% spread spectrum function to reduce EMI in freq. table mode
- Programmable spread spectrum in the M/N step-less mode
- Programmable registers to enable/stop each output and select modes
- MODE pin for power Management
- RESET# out when watch dog timer time out
- One 48 MHz for USB & one 24 MHz for super I/O

- 48-pin SSOP package

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

& - Internal 120KΩ pull-down

* - Internal 120kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F	44	OUT	Free running CPU clock. Not affected by PD#
CPUCLK1	43	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddL2. Low if PD# is low.
RESET#	41	OD	RESET# (open drain, 4ms low active pulse when Watch Dog time out)
IOAPIC	47	OUT	High drive buffered output of the crystal, and is powered by VddL1.
SDRAM [0:12]	17,18,20,21,28 ,29,31,32,34, 35,37,38,40	OUT	SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin.(Controlled by chipset)
PCICLK_F/ *MODE0	7	I/O	Free running PCI clock during normal operation. Latched Input. *Mode0=1, Pin 2 is REF0; *Mode0=0, Pin2 is PD#
PCICLK0^/FS3&	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU and PCI clocks.
PCICLK [1:3]^ PCICLK 4	10,11,12,13	OUT	Low skew (< 250ps) PCI clock outputs. PCICLK 0:3 are double strength pins PCICLK 4 is not.
BUFFER IN	15	IN	Inputs to fanout for SDRAM outputs.

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA*	23	I/O	Serial data of I²C 2-wire control interface
SDCLK*	24	IN	Serial clock of I²C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0^ / PD#	2	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads.(pin7 *Mode0=1) Halt all clocks at logic 0 level, when input low (pin7 *Mode0=0)
REF1 / FS2*	46	I/O	14.318MHz reference clock. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24MHz / FS1*	25	I/O	24MHz output clock. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
48MHz / FS0*	26	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
Vddq1	1	Power supply for Ref [0:1] crystal and core logic.
VddL1	48	Power supply for IOAPIC output, either 2.5V or 3.3V.
VddL2	42	Power supply for CPUCLK[0:3], either 2.5V or 3.3V.
Vddq2	6, 14	Power supply for PCICLK_F, PCICLK[0:4], 3.3V.
Vddq3	19, 30, 36	Power supply for SDRAM[0:12], and CPU PLL core, nominal 3.3V.
Vddq4	27	Power for 24 & 48MHz output buffers and fixed PLL core.
Vss	3,9,16,22,33,39,45	Circuit Ground.

5.0 FREQUENCY BY HARDWARE

FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM(MHz)	PCI(MHz)
0	0	0	0	80.00	80.00	40.00
0	0	0	1	75.00	75.00	37.50
0	0	1	0	83.30	83.30	41.65
0	0	1	1	66.82	66.82	33.41
0	1	0	0	103.00	103.00	34.33
0	1	0	1	112.00	112.00	37.34
0	1	1	0	68.01	68.01	34.01
0	1	1	1	100.23	100.23	33.41
1	0	0	0	120.00	120.00	30.00
1	0	0	1	115.00	115.00	38.33
1	0	1	0	120.00	120.00	40.00
1	0	1	1	105.00	105.00	35.00
1	1	0	0	140.00	140.00	35.00
1	1	0	1	155.00	155.00	38.75
1	1	1	0	124.00	124.00	31.00
1	1	1	1	133.30	133.30	33.30

6.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

MODE0, Pin7 (Latched Input)	PIN 2
0	PD# (Input)
1	REF0 (Output)

7.0 FUNCTION DESCRIPTION

7.1 2-WIRE I²C CONTROL INTERFACE

The clock generator is a slave I²C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194BR-39Binitializes with default register settings. Use of the 2-wire control interface is then optional.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a "start" condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an "acknowledge" (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I²C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I²C controller :

Clock Address A(6:0) & R/W	Ack	8 bits dummy Command code	Ack	8 bits dummy Byte count	Ack	Byte0,1,2... until Stop

Set R/W to 1 when ?ead back", the data sequence is as follows :

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop

7.2 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

FREQUENCY BY SOFTWARE

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU(MHz)	SDRAM(MHz)	PCI(MHz)
0	0	0	0	0	0	80.00	80.00	40.00
0	0	0	0	0	1	75.00	75.00	37.50
0	0	0	0	1	0	83.30	83.30	41.65
0	0	0	0	1	1	66.82	66.82	33.41
0	0	0	1	0	0	103.00	103.00	34.33
0	0	0	1	0	1	112.00	112.00	37.34
0	0	0	1	1	0	68.01	68.01	34.01
0	0	0	1	1	1	100.23	100.23	33.41
0	0	1	0	0	0	120.00	120.00	30.00
0	0	1	0	0	1	115.00	115.00	38.33
0	0	1	0	1	0	120.00	120.00	40.00
0	0	1	0	1	1	105.00	105.00	35.00
0	0	1	1	0	0	140.00	140.00	35.00
0	0	1	1	0	1	155.00	155.00	38.75
0	0	1	1	1	0	124.00	124.00	31.00
0	0	1	1	1	1	133.30	133.30	33.30
0	1	0	0	0	0	160.00	160.00	40.00
0	1	0	0	0	1	127.00	127.00	31.75
0	1	0	0	1	0	130.00	130.00	32.50
0	1	0	0	1	1	135.00	135.00	33.75
0	1	0	1	0	0	136.00	136.00	34.00
0	1	0	1	0	1	137.00	137.00	34.25
0	1	0	1	1	0	139.00	139.00	34.75
0	1	0	1	1	1	140.00	140.00	35.00
0	1	1	0	0	0	141.00	141.00	35.25
0	1	1	0	0	1	142.00	142.00	35.50
0	1	1	0	1	0	143.00	143.00	35.75

0	1	1	0	1	1	144.00	144.00	36.00
0	1	1	1	0	0	145.00	145.00	36.25
0	1	1	1	0	1	146.00	146.00	36.50
0	1	1	1	1	0	148.00	148.00	37.00
0	1	1	1	1	1	149.00	149.00	37.25
SSEL5	**SSEL4**	**SSEL3**	**SSEL2**	**SSEL1**	**SSEL0**	**CPU(MHz)**	**SDRAM(MHz)**	**PCI(MHz)**
1	0	0	0	0	0	151.00	151.00	37.75
1	0	0	0	0	1	152.00	152.00	38.00
1	0	0	0	1	0	153.00	153.00	38.25
1	0	0	0	1	1	154.00	154.00	38.50
1	0	0	1	0	0	155.00	155.00	38.75
1	0	0	1	0	1	156.00	156.00	39.00
1	0	0	1	1	0	157.00	157.00	39.25
1	0	0	1	1	1	158.00	158.00	39.50
1	0	1	0	0	0	159.00	159.00	39.75
1	0	1	0	0	1	162.00	162.00	40.50
1	0	1	0	1	0	163.00	163.00	32.60
1	0	1	0	1	1	164.00	164.00	32.80
1	0	1	1	0	0	165.00	165.00	33.00
1	0	1	1	0	1	167.00	167.00	33.40
1	0	1	1	1	0	168.00	168.00	33.60
1	0	1	1	1	1	169.00	169.00	33.80
1	1	0	0	0	0	170.00	170.00	34.00
1	1	0	0	0	1	172.00	172.00	34.40
1	1	0	0	1	0	174.00	174.00	34.80
1	1	0	0	1	1	176.00	176.00	35.20
1	1	0	1	0	0	178.00	178.00	35.60
1	1	0	1	0	1	180.00	180.00	36.00
1	1	0	1	1	0	182.00	182.00	36.40
1	1	0	1	1	1	184.00	184.00	36.80
1	1	1	0	0	0	186.00	186.00	37.20
1	1	1	0	0	1	188.00	188.00	37.60
1	1	1	0	1	0	190.00	190.00	38.00
1	1	1	0	1	1	192.00	192.00	38.40
1	1	1	1	0	0	194.00	194.00	38.80

1	1	1	1	0	1	196.00	196.00	39.20
1	1	1	1	1	0	198.00	198.00	39.60
1	1	1	1	1	1	200.00	200.00	40.00

7.2.1 Register 0: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL5 (for frequency table selection by software via I^2C)
6	0	-	SSEL4 (for frequency table selection by software via I^2C)
5	0	-	SSEL3 (for frequency table selection by software via I^2C)
4	0	-	SSEL2 (for frequency table selection by software via I^2C)
3	0	-	SSEL1 (for frequency table selection by software via I^2C)
2	0	-	SSEL0 (for frequency table selection by software via I^2C)
1	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 7:2
0	0	-	0 = Running 1 = Tristate all outputs

7.2.2 Register 1 : CPU , 48/24 MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	0	-	0 = Normal 1 = Spread Spectrum enabled
4	0	-	0 = ±0.25% Spread Spectrum Modulation 1 = ±0.5% Spread Spectrum Modulation
3	1	40	SDRAM12 (Active / Inactive)
2	1	-	Reserved
1	1	43	CPUCLK1 (Active / Inactive)
0	1	44	CPUCLK_F (Active / Inactive)

7.2.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	7	PCICLK_F (Active / Inactive)
5	1	-	Reserved
4	1	14	PCICLK4 (Active / Inactive)
3	1	12	PCICLK3 (Active / Inactive)
2	1	11	PCICLK2 (Active / Inactive)
1	1	10	PCICLk1 (Active / Inactive)
0	1	8	PCICLK0 (Active / Inactive)

7.2.4 Register 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	46	REF1 (Active / Inactive)
6	1	2	REF0 (Active / Inactive)
5	1	26	48MHz (Active / Inactive)
4	1	25	24MHz (Active / Inactive)
3	1	47	IOAPIC (Active / Inactive)
2	1	21,20,18,17	SDRAM(8:11) (Active / Inactive)
1	1	32,31,29,28	SDRAM(4:7) (Active / Inactive)
0	1	38,37,35,34	SDRAM(0:3) (Active / Inactive)

7.2.5 Register 4: Reserved Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	X	-	Latched FS3#
5	X	-	Latched FS2#
4	X	-	Latched FS1#
3	X	-	Latched FS0#

2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

7.2.6 Register 5: Reserved Register

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	0	-	Reserved
5	0	-	Reserved
4	1	-	Reserved
3	0	-	Reserved
2	0	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

7.2.7 Register 6~11: M/N step-less mode control registers

7.2.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID

7.2.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**1**	**-**	**Winbond Chip ID**
5	**0**	**-**	**Winbond Chip ID**
4	**1**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Version ID**

2	0	-	Winbond Version ID
1	0	-	Winbond Version ID
0	1	-	Winbond Version ID

8.0 SPECIFICATIONS

8.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

8.2 AC CHARACTERISTICS

Vdd = Vddq3 = 3.3V – 5 %, Vddq2 = VddL1=VddL2 = 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t_{OFF}	1	2.6	4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t_{CCJ}			±250	ps	
CPU/SDRAM Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V_{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

8.3 DC CHARACTERISTICS

Vdd = Vddq3 = 3.3V – 5 %, Vddq2 = VddL1=VddL2 = 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-66	µA	
Input High Current	I_{IH}			5	µA	
Output Low Voltage I_{OL} = 4 mA	V_{OL}			0.4	V_{dc}	All outputs
Output High Voltage I_{OH} = 4mA	V_{OH}	2.4			V_{dc}	All outputs using 3.3V power
Tri-State leakage Current	Ioz			10	µA	
Dynamic Supply Current for Vdd + Vddq3	I_{dd3}				mA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Dynamic Supply Current for Vddq2 + Vddq2b	I_{dd2}				mA	Same as above
CPU Stop Current for Vdd + Vddq3	I_{CPUS3}				mA	Same as above
CPU Stop Current for Vddq2 + Vddq2b	I_{CPUS2}				mA	Same as above
PCI Stop Current for Vdd + Vddq3	I_{PD3}				mA	

8.4 BUFFER CHARACTERISTICS

8.4.1 TYPE 1 BUFFER FOR CPU CLOCK

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-27			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-27	mA	Vout = 2.0V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.2 V
Pull-Down Current Max	$I_{OL(max)}$			27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20pF Load

8.4.2 TYPE 2 BUFFER FOR IOAPIC

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.4 V
Pull-Up Current Max	$I_{OH(max)}$			-29	mA	Vout = 2.7 V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.0 V
Pull-Down Current Max	$I_{OL(max)}$			28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.7 V and 1.7 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.7 V and 1.7 V	$T_{RF(max)}$			1.8	ns	20pF Load

8.4.3 TYPE 3 BUFFER FOR REF1, 24MHZ, 48MHZ

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-29			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-23	mA	Vout = 3.135V
Pull-Down Current Min	$I_{OL(min)}$	29			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$				mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	1.0			ns	10pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			4.0	ns	20pF Load

8.4.4 TYPE 4 BUFFER FOR SDRAM (0:12)

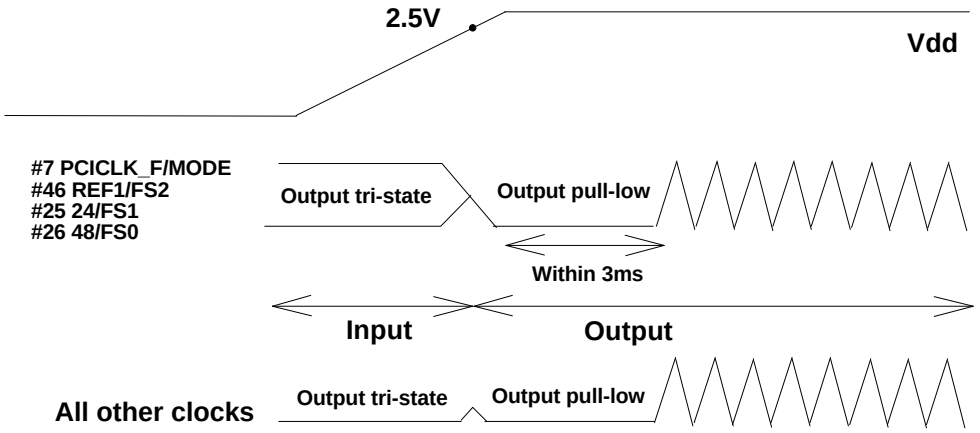
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.65 V
Pull-Up Current Max	$I_{OH(max)}$			-46	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.65 V
Pull-Down Current Max	$I_{OL(max)}$			53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	20pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			1.3	ns	30pF Load

8.4.5 TYPE 5 BUFFER FOR PCICLK(0:4,F)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-33			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-33	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$	30			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$			38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	15pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			2.0	ns	30pF Load

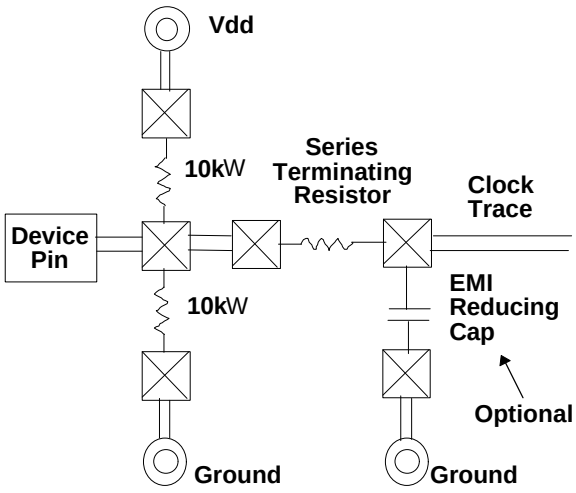
9.0 OPERATION OF DUAL FUCTION PINS

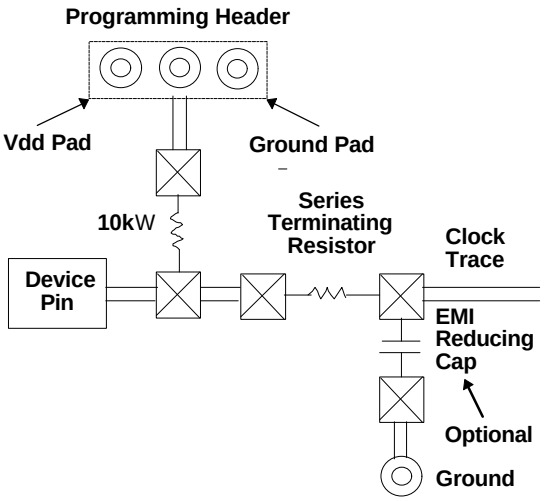
Pins 2, 7, 8, 25, and 26 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Fig1), therefore, and are considered input select pins. When Vdd reaches 2.5V, the logic level that is present on these pins is latched into their appropriate internal registers. Once the correct information is properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins has a large pull-up resistor (250 kΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 kΩ resistor is recommended to be connected to Vdd if logic 1 is expected. Otherwise, there should be direct connection to ground if a logic 0 is desired. The 10 kΩ resistor should be placed before the serious terminating resistor. Note that these logic will only be latched at initial power on.

If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitors have typical values ranging from 4.7pF to 22pF.

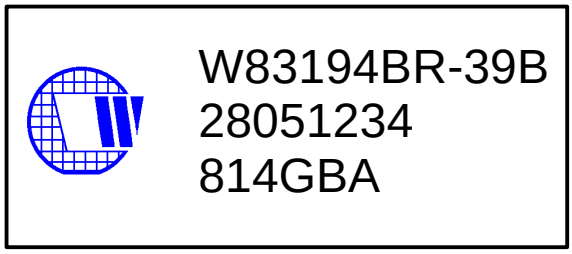

Vdd
10kW
Series
Terminating
Resistor
Clock
Trace
Device
Pin
EMI
Reducing
Cap
10kW
Optional
Ground
Ground


Programming Header
Vdd Pad
Ground Pad
10kW
Series
Terminating
Resistor
Clock
Trace
Device
Pin
EMI
Reducing
Cap
Optional
Ground

10.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-39B	48 PIN SSOP	Commercial, 0°C to +70°C

11.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-39B

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

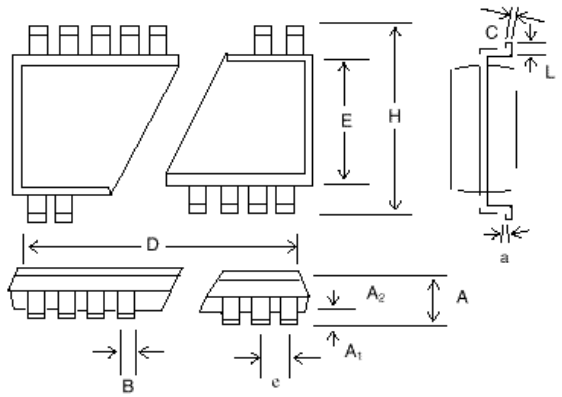
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

B: Winbond internal use code

A: IC revision

12.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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