Winbond Electronics Corp.

100MHZ 2-DIMM SDRAM BUFFER FOR NOTEBOOK

1.0 GENERAL DESCRIPTION

The W83L177R is a 10 outputs SDRAM clock buffer for 2-DIMMs models incorporate with W83L197R-16 which is the clock synthesizer especially for the 100MHz models such as Intel BX chipsets.(Refer the datasheet fo Winbond W83L197R-16)

The W83L177R receives the clock from chipset by the Buffer_In pin and provides almost zero-delay (less than 4ns propagation delay) SDRAM buffer outputs for the 10 SDRAM clocks which are synchronous with the CPU clock outputs priovided by W83L197R-16. The clock skew between any two clock outputs is less than 250ps and the output buffer impedance is about 15 ohms.

The W83L177R also provides I^2C serial bus interface to program the registers to enable or disable each SDRAM clock outputs.

2.0 PRODUCT FEATURES

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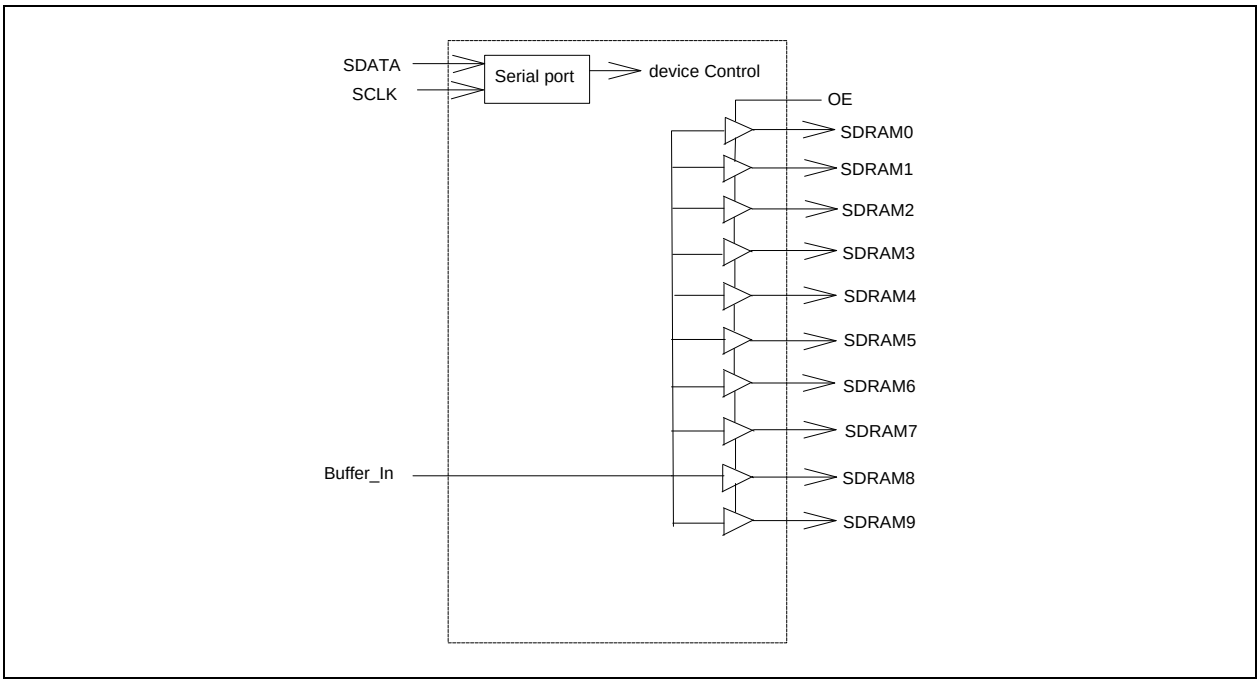
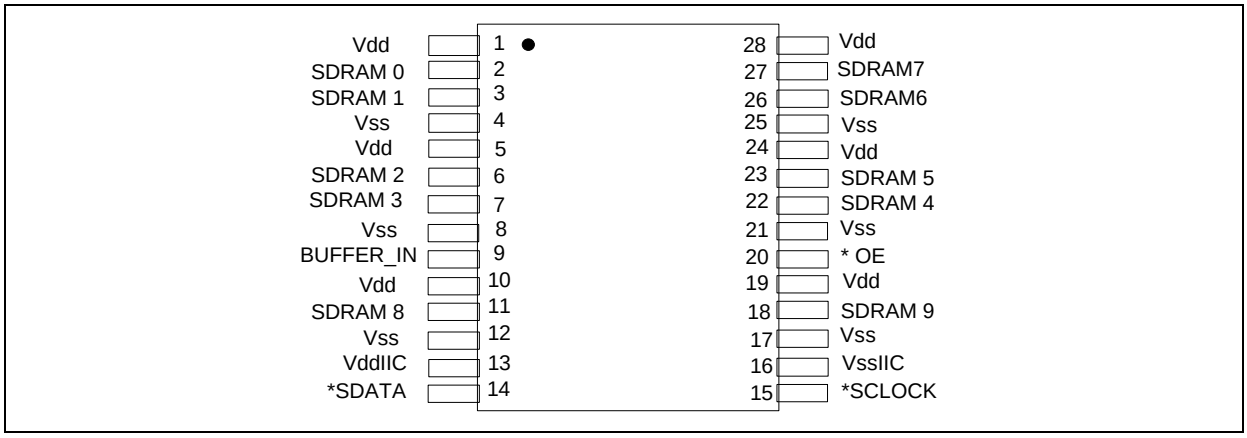
- 10 SDRAM clocks for 2-DIMMs
- Clock skew less than 250ps
- Almost none delay Buffer-in controlling SDRAM clocks(< 4ns propagation delay)
- I^2C 2-wire serial interface
- Programmable registers to enable/stop each output
- Incorporate with W83L197R-16
- 28pin-SOP package (209mil)

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION



5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

* - Internal 250kΩ pull-up

SYMBOL	PIN	I/O	FUNCTION
SDRAM [0:9]	2,3,6,7,11,18, 22,23,26,27	O	SDRAM clock outputs which have the same frequency as CPU clocks.
*SDATA	14	I/O	Serial data of I^2C 2-wire control interface
*SDCLK	15	IN	Serial clock of I^2C 2-wire control interface
*OE	20	IN	Internal 250K ohm pull-up resistor. Tri-states outputs when LOW.
BUFFER_IN	9	IN	Clock Input from the chipset
VDDIIC	13	Power supply for I2C core logic, 3.3 V supply	
VSSIIC	16	Ground for I2C core logic	
Vdd	1,5,10,19,24, 28	Power supply	
Vss	4,8,12,17,21, 25	Circuit Ground	

6.0 FUNTION DESCRIPTION

6.1 2-WIRE I^{2}C CONTROL INTERFACE

The clock generator is a slave I2C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83L177R initializes with default register settings, and then it′optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^{2}C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^{2}C controller :

Clock Address A(6:0) & R/W	**Ack**	**8 bits dummy Command code**	**Ack**	**8 bits dummy Byte count**	**Ack**	**Byte0,1,2... until Stop**

Set R/W to 1 when read back the data sequence is as follows :

Clock Address A(6:0) & R/W	**Ack**	**Byte 0**	**Ack**	**Byte 1**	**Ack**	**Byte2, 3, 4... until Stop**

6.2 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

6.2.1 Register 0: (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	-	-	Reserved
6	-	-	Reserved
5	-	-	Reserved
4	-	-	Reserved
3	1	7	SDRAM3 (Active / Inactive)
2	1	6	SDRAM2 (Active / Inactive)
1	1	3	SDRAM1 (Active / Inactive)
0	1	2	SDRAM0 (Active / Inactive)

6.2.2 Register 1: (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	27	SDRAM7 (Active / Inactive)
6	1	26	SDRAM6 (Active / Inactive)
5	1	23	SDRAM5 (Active / Inactive)
4	1	22	SDRAM4 (Active / Inactive)
3	-	-	Reserved
2	-	-	Reserved
1	-	-	Reserved
0	-	-	Reserved

6.2.3 Register 2: (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	18	SDRAM9 (Active / Inactive)
6	1	11	SDRAM8 (Active / Inactive)
5	-	-	Reserved
4	-	-	Reserved
3	-	-	Reserved
2	-	-	Reserved
1	-	-	Reserved
0	-	-	Reserved

7.0 SPECIFICATIONS

7.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

7.2 AC CHARACTERISTICS

Vdd = 3.3V – 5 % , T_A = 0°C to +70°C, Test load = 30 pF						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input frequency	f_{IN}	0		150	MHz	
Output Rise Time	t_R	1.5		4.0	V/ns	Measured from 0.4V to 2.4V
Output Fall Time	t_F	1.5		4.0	V/ns	Measured from 0.4V to 2.4V
Output Skew, Rising Edges	t_{SR}			250	ps	
Output Skew, Falling Edges	t_{SF}			250	ps	
Output Enable Time	t_{EN}	1.0		8.0	ns	
Output Disable Time	t_{DIS}	1.0		8.0	ns	
Rising Edge Propagation Delay	t_{PR}	1.0		<4.0	ns	
Falling Edge Propagation Delay	t_{PF}	1.0		<4.0	ns	
Duty Cycle	t_D	45		55	%	Measure at 1.5V
AC Output Impedance	Z_O		15		Ω	

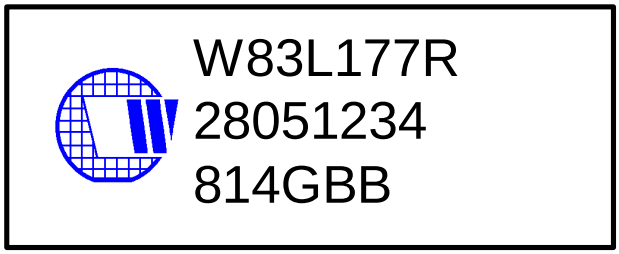
7.3 DC CHARACTERISTICS

Vdd = 3.3V – 5 %, T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Low Voltage	V_{IL}	Vss-03		0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0		Vdd+0.5	V_{dc}	
Input Leakage Current, BUFFER_IN	I_{IL}	-5		+5	µA	
Input Leakage Current	I_{IL}	-20		+5	µA	
Output Low Voltage	V_{OL}			50	mV_{dc}	IOL=1mA
Output High Voltage	V_{OH}	3.1			V_{dc}	IOH=-1mA
Output Low Current	I_{OL}	65	100	160	mA	VOL=1.5V
Output High Current	I_{OH}	70	110	185	mA	VOH=1.5V
Input Pin Capacitance	C_{IN}			5	pF	
Output Pin Capacitance	C_{OUT}			6	pF	
Input Pin Inductance	L_{IN}			7	nH	

8.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83L177R	28 PIN SOP	Commercial, 0°C to +70°C

9.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83L177R

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

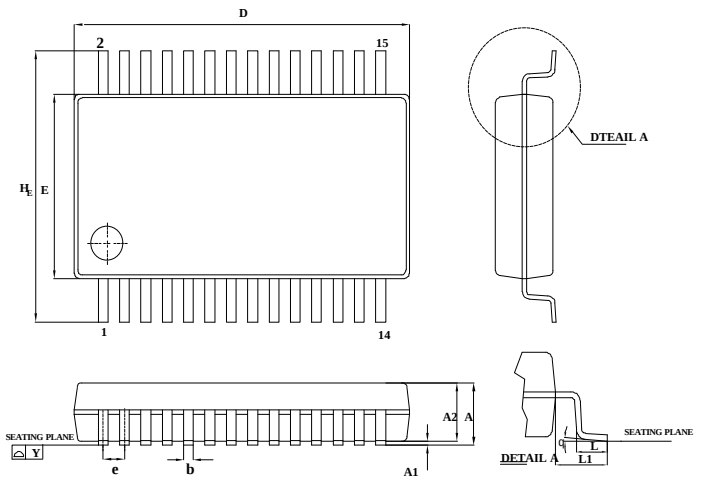
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

10.0 PACKAGE DRAWING AND DIMENSIONS

28-SOP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	9.90	10.20	10.50	0.389	0.401	0.413
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
q	0	—	8	0	—	8

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