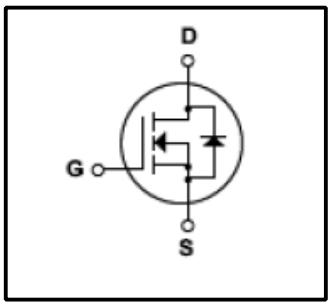
Silicon N-Channel MOSFET

Features

- 4.5A,500V,$R_{DS(on)}$(Max 1.5Ω)@V_{GS}=10V
- Ultra-low Gate Charge(Typical 32nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150℃)



General Description

This Power MOSFET is produced using Winsemi's advanced planar stripe, DMOS technology. This latest technology has been especially designed to minimize on-state resistance, have a high rugged avalanche characteristics. This devices is specially well suited for high efficiency switch model power supplies, power factor correction and half bridge and full bridge resonant topology line a electronic lamp ballast.

Absolute Maximum Ratings

Symbol	Parameter		Value	Units
V_{DSS}	Drain Source Voltage		500	V
I_D	Continuous Drain Current(@Tc=25℃)		4.5*	A
	Continuous Drain Current(@Tc=100℃)		2.9*	A
I_{DM}	Drain Current Pulsed	(Note1)	18*	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	300	mJ
E_{AR}	Repetitive Avalanche Energy	(Note 1)	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Total Power Dissipation(@Tc=25℃)		38	W
	Derating Factor above 25℃		0.3	W/℃
T_J, T_{stg}	Junction and Storage Temperature		-55~150	℃
T_L	Channel Temperature		300	℃

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	-	-	3.3	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	62.5	℃/W

Electrical Characteristics (Tc = 25° C)

Characteristics		Symbol	Test Condition	Min	Type	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	-	-	±100	nA
Gate−source breakdown voltage		$V_{(BR)GSS}$	I_G = ±10 μA, V_{DS} = 0 V	±30	-	-	V
Drain cut−off current		I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	μA
Drain−source breakdown voltage		$V_{(BR)DSS}$	I_D = 250 μA, V_{GS} = 0 V	500	-	-	V
Break Voltage Temperature Coefficient		$\Delta BV_{DSS}/\Delta TJ$	I_D=250μA, Referenced to 25℃	-	0.55	-	V/℃
Gate threshold voltage		$V_{GS(th)}$	V_{DS} = 10 V, I_D =250 μA	2	-	4	V
Drain−source ON resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 2.25A	-	1.16	1.5	Ω
Forward Transconductance		gfs	V_{DS} = 40 V, I_D = 2.25A	-	4.2	-	S
Input capacitance		C_{iss}	V_{DS} = 25 V,	-	800	1050	pF
Reverse transfer capacitance		C_{rss}	V_{GS} = 0 V,	-	18	23	
Output capacitance		C_{oss}	f = 1 MHz	-	76	100	
Switching time	Rise time	tr	V_{DD} =250 V,	-	15	40	ns
	Turn−on time	ton	I_D =4.5A	-	40	90	
	Fall time	tf	R_G=25Ω	-	85	180	
	Turn−off time	toff	(Note4,5)	-	45	100	
Total gate charge (gate−source plus gate−drain)		Qg	V_{DD} = 400 V,	-	32	44	nC
Gate−source charge		Qgs	V_{GS} = 10 V,	-	3.7	-	
Gate−drain (“miller”) Charge		Qgd	I_D =4.5 A (Note4,5)	-	15	-	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I_{DR}	-	-	-	4.5	A
Pulse drain reverse current	I_{DRP}	-	-	-	18	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 4.5 A, V_{GS} = 0 V	-	-	1.4	V
Reverse recovery time	t_{rr}	I_{DR} = 4.5 A, V_{GS} = 0 V,	-	305	-	ns
Reverse recovery charge	Q_{rr}	dI_{DR} / dt = 100 A / μs	-	2.6	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=24mH,I_{AS}=4.5A,V_{DD}=50V,R_G=25Ω,Starting T_J=25℃

3.I_{SD}≤4.5A,di/dt≤300A/us, V_{DD}<BV_{DSS},STARTING T_J=25℃

4.Pulse Test: Pulse Width≤300us,Duty Cycle≤2%

5.Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

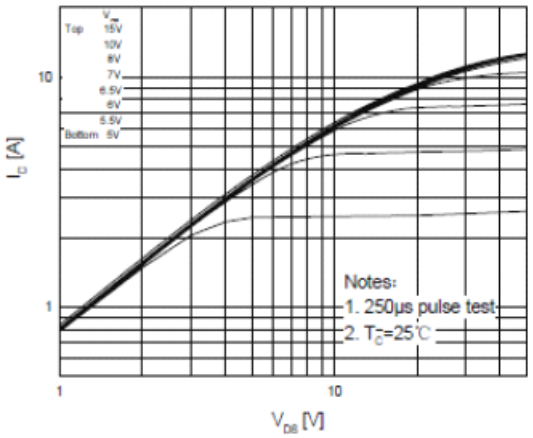


Fig.1 On-State Characteristics

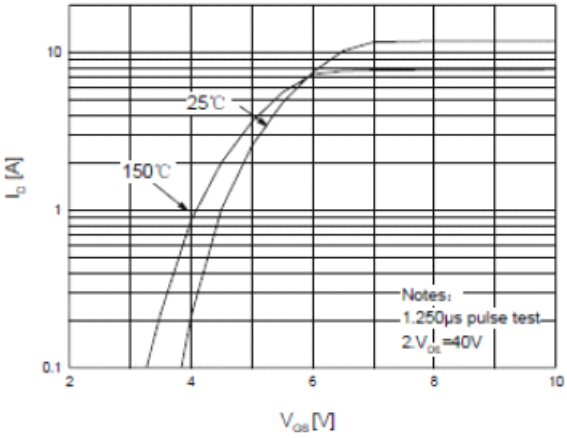


Fig.2 Transfer Current characteristics

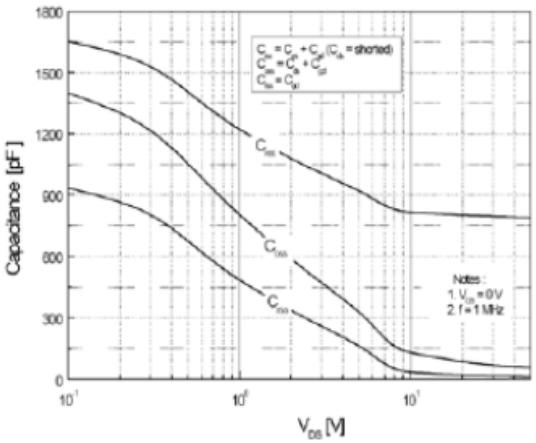


Fig.3 Capacitance Variation vs drain voltage

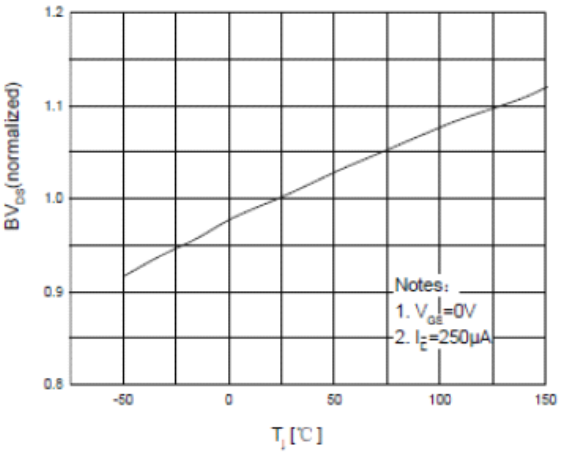


Fig.4 Breakdown Voltage Variation Vs Temperature

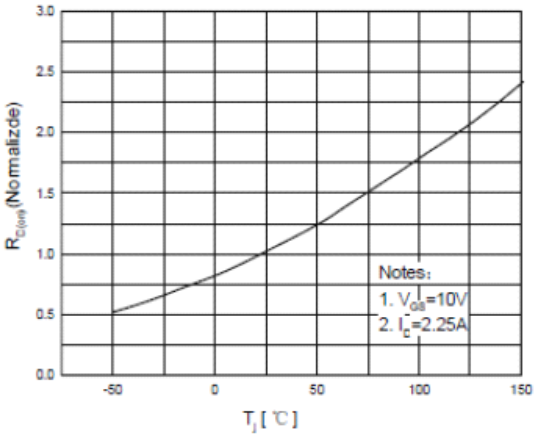


Fig.5 On-Resistance Variation vs.JunctionTemperature

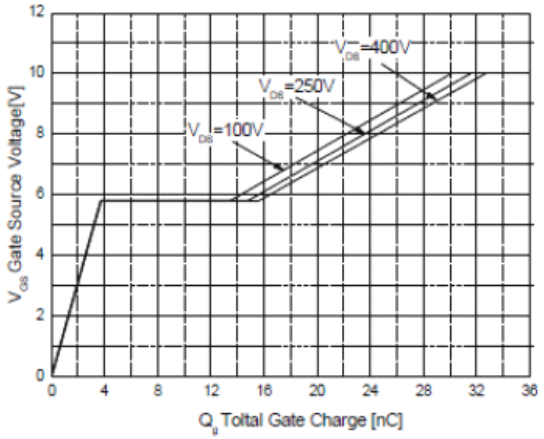


Fig.6 Gate Charge Characteristics

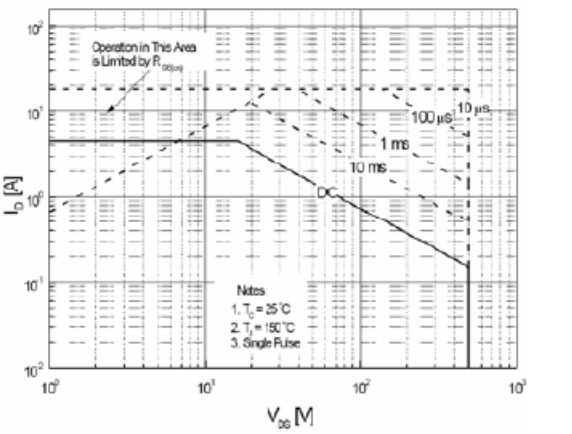


Fig.7 Maximum Safe Operation Area

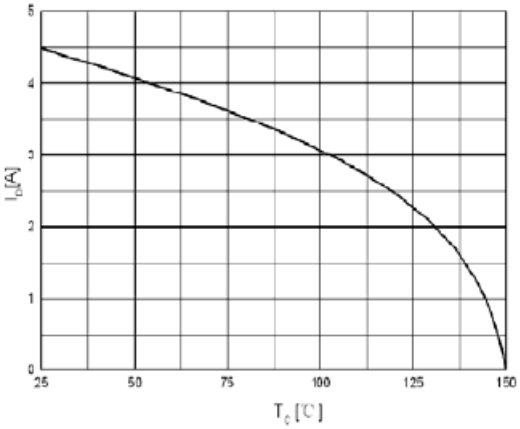


Fig.8 Maximum Drain Current vs Case Temperature

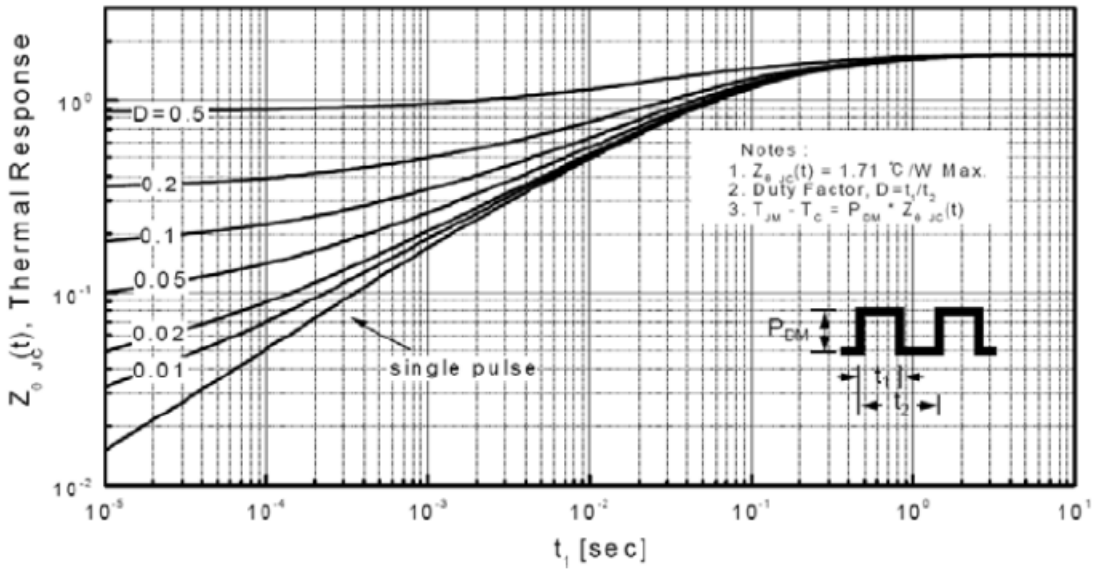


Fig.9Transient Thermal Response Curve

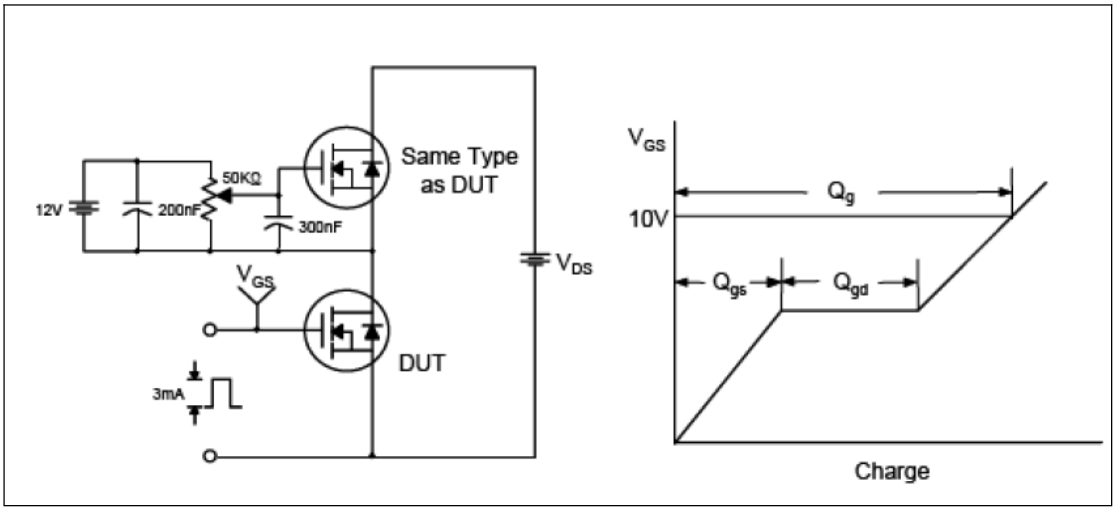


Fig.10 Gate Test Circuit & Waveform

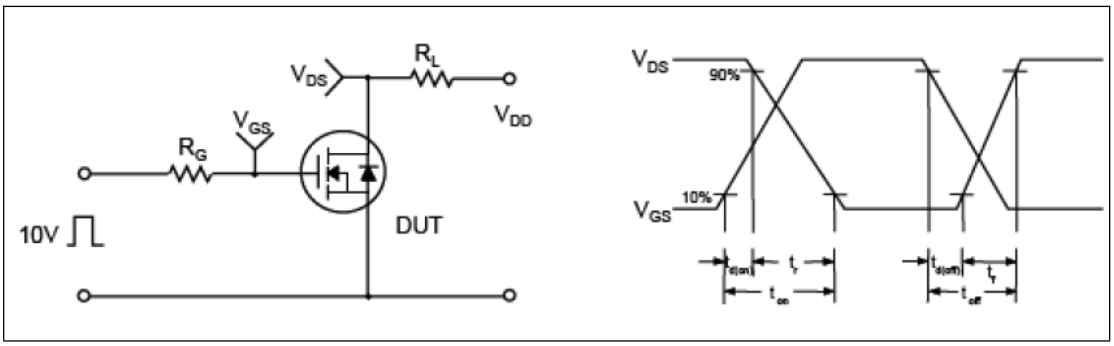


Fig.11 Resistive Switching Test Circuit & Waveform

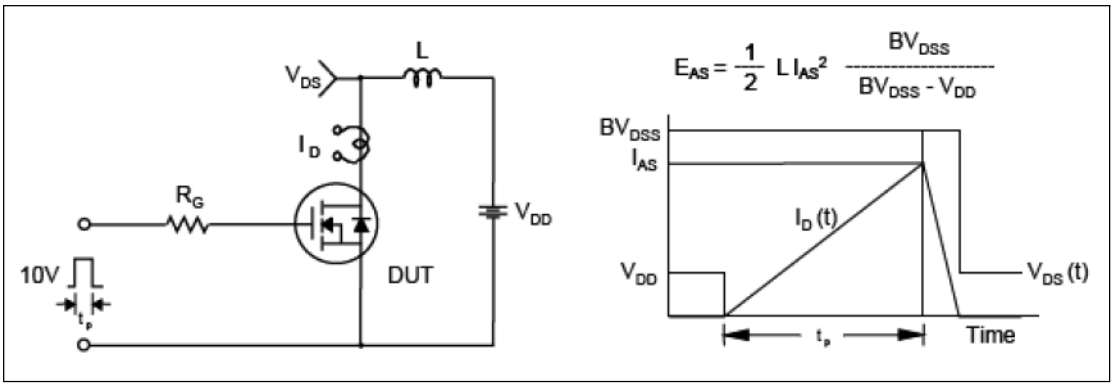


Fig.12 Unclamped Inductive Switching Test Circuit & Waveform

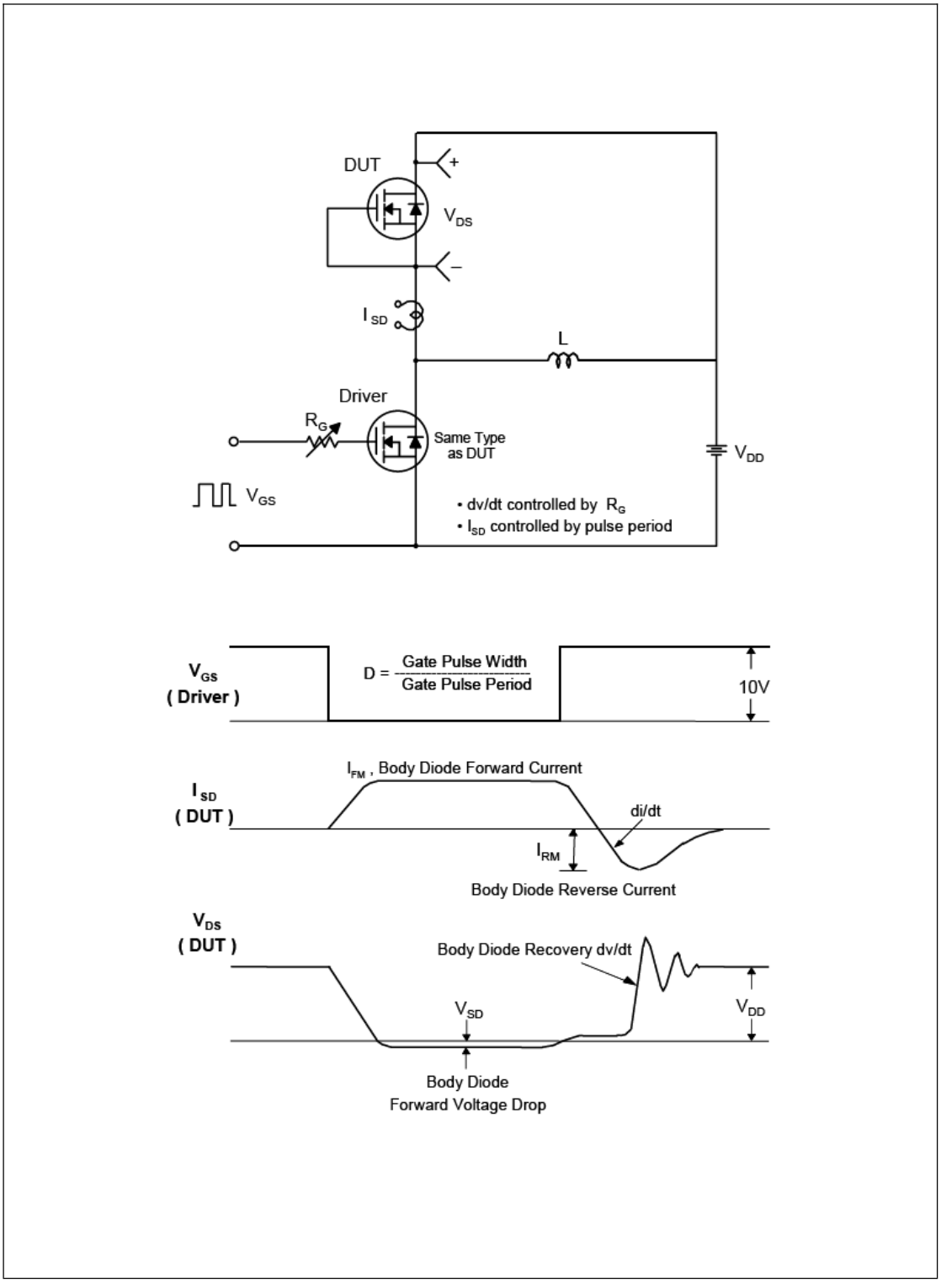


Fig.13 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-220F Package Dimension

Unit: mm