

AC'97 Audio + Touchpanel CODEC

DESCRIPTION

The WM9713L is a highly integrated input/output device designed for mobile computing and communications.

The chip is architected for dual CODEC operation, supporting Hi-Fi stereo Codec functions via the AC link interface, and additionally supporting voice Codec functions via a PCM type Synchronous Serial Port (SSP). A third, auxiliary DAC is provided which may be used to support generation of supervisory tones, or ring-tones at different sample rates to the main codec.

The device can connect directly to a 4-wire or 5-wire touchpanel, mono or stereo microphones, stereo headphones and a stereo speaker, reducing total component count in the system. Cap-less connections to the headphones, speakers, and earpiece may be used, saving cost and board area. Additionally, multiple analog input and output pins are provided for seamless integration with analog connected wireless communication devices.

All device functions are accessed and controlled through a single AC-Link interface compliant with the AC'97 standard. The 24.576 MHz masterclock can be input directly or generated internally from a 13MHz (or other frequency) clock by an on-chip PLL. The PLL supports a wide range of input clock from 2.048MHz to 78.6MHz.

The WM9713L operates at supply voltages from 1.8V to 3.6V. Each section of the chip can be powered down under software control to save power. The device is available in a small leadless 7x7mm QFN package, ideal for use in hand-held portable systems.

FEATURES

- AC'97 Rev 2.2 compatible stereo codec
 - DAC SNR 94dB, THD -85dB
 - ADC SNR 87dB, THD -86dB
 - Variable Rate Audio, supports all WinCE sample rates
 - Tone Control, Bass Boost and 3D Enhancement
- On-chip 45mW headphone driver
- On-chip 400mW mono or stereo speaker drivers
- Stereo, mono or differential microphone input
 - Automatic Level Control (ALC)
 - Mic insert and mic button press detection
- Auxiliary mono DAC (ring tone or DC level generation)
- Seamless interface to wireless chipset
- Resistive touchpanel interface
 - Supports 4-wire and 5-wire panels
 - 12-bit resolution, INL ± 2 LSBs (<0.5 pixels)
 - X, Y and touch-pressure (Z) measurement
 - Pen-down detection supported in Sleep Mode
- Additional PCM/I²S interface to support voice CODEC
- PLL derived audio clocks.
- Supports input clock ranging from 2.048MHz to 78.6MHz
- 1.8V to 3.6V supplies (digital down to 1.62V, speaker up to 4.2V)
- 7x7mm 48-lead QFN package

APPLICATIONS

- Personal Digital Assistants (PDA) with or without phone
- Smartphones
- Handheld and Tablet Computers

BLOCK DIAGRAM

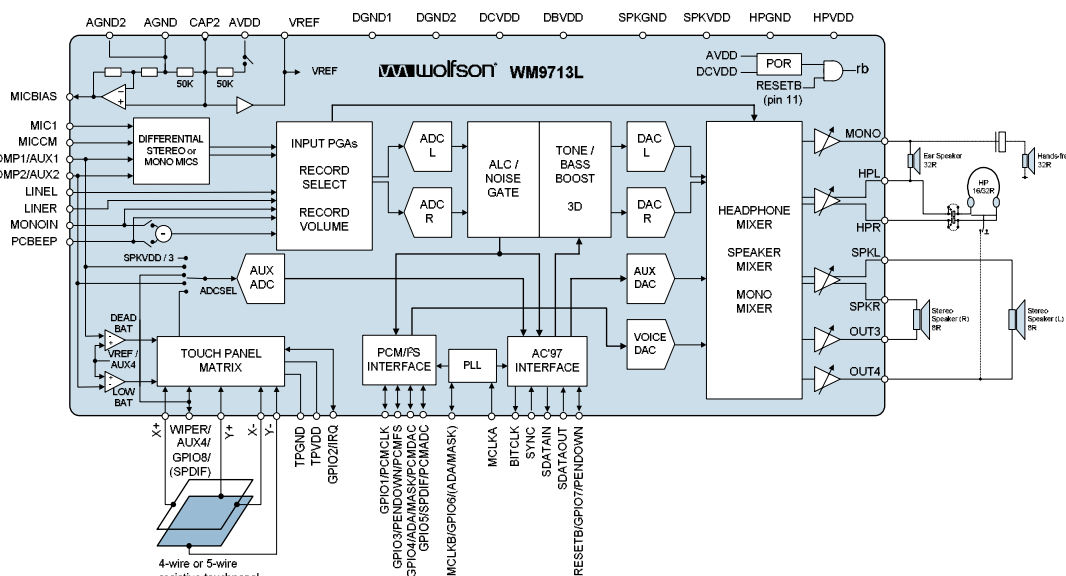
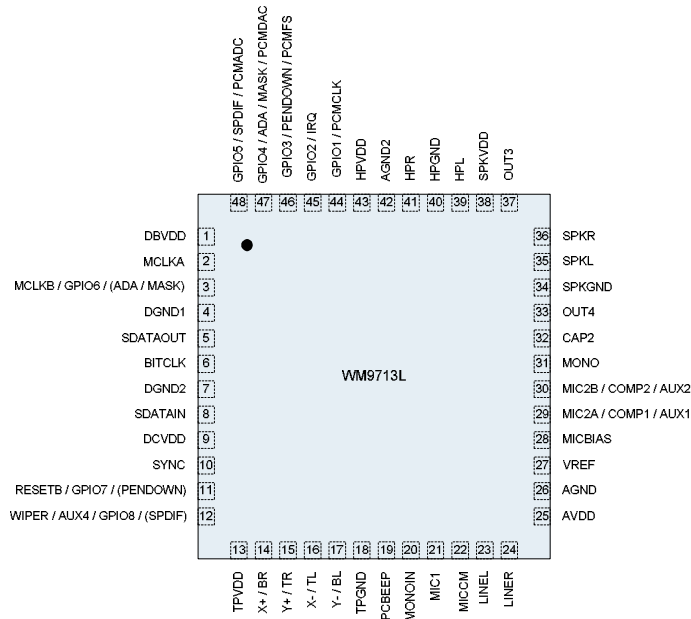


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PIN CONFIGURATION



ORDERING INFORMATION

| DEVICE | TEMPERATURE RANGE | PACKAGE | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|----------------|-------------------|--------------------------------------|----------------------------|----------------------------|
| WM9713LGEFL/V | -25 to +85°C | 48-lead QFN (Pb-free) | MSL3 | 260°C |
| WM9713LGEFL/RV | -25 to +85°C | 48-lead QFN (Pb-free, tape and reel) | MSL3 | 260°C |

Note:

Reel quantity = 2,200

PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|-----|--------------------------------|-------------------|--|
| 1 | DBVDD | Supply | Digital I/O Buffer Supply |
| 2 | MCLKA | Digital Input | Master Clock A Input |
| 3 | MCLKB / GPIO6 / (ADA / MASK) | Digital In/Out | Master Clock B Input / GPIO6 / (ADA output / MASK input) |
| 4 | DGND1 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 5 | SDATAOUT | Digital Input | Serial Data Output from Controller / Input to WM9713L |
| 6 | BITCLK | Digital Output | Serial Interface Clock Output to Controller |
| 7 | DGND2 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 8 | SDATAIN | Digital Output | Serial Data Input to Controller / Output from WM9713L |
| 9 | DCVDD | Supply | Digital Core Supply |
| 10 | SYNC | Digital Input | Serial Interface Synchronisation Pulse from Controller |
| 11 | RESETB / GPIO7 / (PENDOWN) | Digital In / Out | Reset (asynchronous, active Low, resets all registers to their default) / GPIO7 / (pen down output) |
| 12 | WIPER / AUX4 / GPIO8 / (SPDIF) | Analogue In / Out | Top Sheet Connection for 5-wire Touchpanels / Auxiliary ADC input / GPIO8 / (SPDIF digital audio output) |
| 13 | TPVDD | Supply | Touchpanel Driver Supply |
| 14 | X+ / BR | Analogue Input | Touchpanel Connection: X+ (Right) for 4-wire / bottom right for 5-wire |
| 15 | Y+ / TR | Analogue Input | Touchpanel Connection: Y+ (Top) for 4-wire / top right for 5-wire |
| 16 | X- / TL | Analogue Input | Touchpanel Connection: X- (Left) for 4-wire / top left for 5-wire |
| 17 | Y- / BL | Analogue Input | Touchpanel Connection: Y- (Bottom) for 4-wire / bottom left for 5-wire |
| 18 | TPGND | Supply | Touchpanel Driver Ground |
| 19 | PCBEEP | Analogue Input | Line Input to analogue audio mixers, typically used for beeps |
| 20 | MONOIN | Analogue Input | Mono Input (RX) |
| 21 | MIC1 | Analogue Input | Microphone preamp A input 1 |
| 22 | MICCM | Analogue Input | Microphone common mode input |
| 23 | LINEL | Analogue Input | Left Line Input |
| 24 | LINER | Analogue Input | Right Line Input |
| 25 | AVDD | Supply | Analogue Supply (audio DACs, ADCs, PGAs, mic amps, mixers) |
| 26 | AGND | Supply | Analogue Ground |
| 27 | VREF | Analogue Output | Internal Reference Voltage (buffered CAP2) |
| 28 | MICBIAS | Analogue Output | Bias Voltage for Microphones (buffered CAP2 × 1.8) |
| 29 | MIC2A / COMP1 / AUX1 | Analogue Input | Microphone preamp A input 2 / COMP1 input / Auxillary ADC input |
| 30 | MIC2B / COMP2 / AUX2 | Analogue Input | Microphone preamp B input / COMP2 input / Auxillary ADC input |
| 31 | MONO | Analog output | Mono output driver (line or headphone) |
| 32 | CAP2 | Analogue In / Out | Internal Reference Voltage (normally AVDD/2, if not overdriven) |
| 33 | OUT4 | Analogue Output | Auxillary output driver (speaker, line or headphone) |
| 34 | SPKGND | Supply | Speaker ground (feeds output buffers on pins 33, 35, 36 and 37) |
| 35 | SPKL | Analogue Output | Left speaker driver (speaker, line or headphone) |
| 36 | SPKR | Analogue Output | Right speaker driver (speaker, line or headphone) |
| 37 | OUT3 | Analogue Output | Auxillary output driver (speaker, line or headphone) |
| 38 | SPKVDD | Supply | Speaker supply (feeds output buffers on pins 33, 35, 36 and 37) |
| 39 | HPL | Analogue Output | Headphone left driver (line or headphone) |
| 40 | HPGND | Supply | Headphone ground (feeds output buffers on pins 39 and 41) |
| 41 | HPR | Analogue Output | Headphone right driver (line or headphone) |
| 42 | AGND2 | Supply | Analogue ground, chip substrate |
| 43 | HPVDD | Supply | Headphone supply (feeds output buffers on pins 39 and 41) |

| PIN | NAME | TYPE | DESCRIPTION |
|-----|-----------------------------|------------------|---|
| 44 | GPIO1 / PCMCLK | Digital In / Out | GPIO Pin 1 / PCM interface clock |
| 45 | GPIO2 / IRQ | Digital In / Out | GPIO Pin 2 / IRQ (Interrupt Request) output |
| 46 | GPIO3 / PENDOWN / PCMFS | Digital In / Out | GPIO Pin 3 / pen down output or PCM frame signal |
| 47 | GPIO4 / ADA / MASK / PCMDAC | Digital In / Out | GPIO Pin 4 / ADA (ADC data available) output or Mask input / PCM input (DAC) data |
| 48 | GPIO5 / SPDIF / PCMADC | Digital In / Out | GPIO Pin 5 / SPDIF digital audio output / PCM output (ADC) data |
| 49 | GND_PADDLE | | Die Paddle (Note 1) |

Notes:

1. It is recommended that the GND_PADDLE is connected to analogue ground. Refer to the "Recommended External Components" diagram and "Package Dimensions" section for further information.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|------------|-------------|
| Digital supply voltages (DCVDD, DBVDD) | -0.3V | +3.63V |
| Analogue supply voltages (AVDD, HPVDD, TPVDD) | -0.3V | +3.63V |
| Speaker supply voltage (SPKVDD) | -0.3V | +4.2V |
| Touchpanel supply voltage (TPVDD) | | AVDD +0.3V |
| Voltage range digital inputs | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Voltage range touchpanel Inputs X+, X-, Y+ and Y- | | TPVDD +0.3V |
| Voltage range touchpanel Inputs X+, X-, Y+ and Y- | | AVDD +0.3V |
| Operating temperature range, T _A | -25°C | +85°C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------|-----------------|------|-----|------|------|
| Digital input/output buffer supply range | DBVDD | | 1.71 | 3.3 | 3.6 | V |
| Digital core supply range | DCVDD | | 1.71 | 1.8 | 3.6 | V |
| Analogue supply range | AVDD, HPVDD, TPVDD | | 1.8 | 3.3 | 3.6 | V |
| Speaker supply range | SPKVDD | | 1.8 | 3.3 | 4.2 | V |
| Digital ground | DGND1, DGND2 | | | 0 | | V |
| Analogue ground | AGND, HPGND, SPKGND, TPGND | | | 0 | | V |
| Difference AGND to DGND | | Note 1 | -0.3 | 0 | +0.3 | V |

Note:

1. AGND is normally the same as DGND1/DGND2
2. $DCVDD \leq DBVDD$ and $DCVDD \leq AVDD$
3. DCVDD should be $\geq 2V$ when using the PLL

ELECTRICAL CHARACTERISTICS

AUDIO OUTPUTS

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD=HPVDD=SPKVDD =3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--|-----|-------------|-----|----------|
| DAC to Line-Out (HPL/R, SPKL/R or MONO with 10kΩ / 50pF load) | | | | | | |
| Full-scale output (0dBFS) | | AVDD = 3.3V, PGA gains set to 0dB | | 1 | | V rms |
| Signal to Noise Ratio (A-weighted) | SNR | | 85 | 94 | | dB |
| Total Harmonic Distortion | THD | -3dB output | | -85 | -74 | dB |
| Power Supply Rejection | PSRR | 100mV, 20Hz to 20kHz signal on AVDD | | 50 | | dB |
| Speaker Output (SPKL/SPKR with 8Ω bridge tied load, INV=1) | | | | | | |
| Output Power at 1% THD | P _O | THD = 1% | | 400 | | mW (rms) |
| Abs. max output power | P _{Omax} | | | 500 | | mW (rms) |
| Total Harmonic Distortion | THD | P _O = 200mW | | -66 0.05 | | dB % |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |
| Stereo Speaker Output (SPKL/OUT4 and SPKR/OUT3 with 8Ω bridge tied load, INV=1) | | | | | | |
| Output Power at 1% THD | P _O | THD = 1% | | 400 | | mW (rms) |
| Abs. max output power | P _{Omax} | | | 500 | | mW (rms) |
| Total Harmonic Distortion | THD | P _O = 200mW | | -66 0.05 | | dB % |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |
| Headphone Output (HPL/R, OUT3/4 or SPKL/SPKR with 16Ω or 32Ω load) | | | | | | |
| Output Power per channel | P _O | Output power is very closely correlated with THD; see below. | | | | |
| Total Harmonic Distortion | THD | P _O =10mW, R _L =16Ω | | -80 | | dB |
| | | P _O =10mW, R _L =32Ω | | -80 | | |
| | | P _O =20mW, R _L =16Ω | | -78 | | |
| | | P _O =20mW, R _L =32Ω | | -79 | | |
| Signal to Noise Ratio (A-weighted) | SNR | | | 90 | | dB |

Note:

- All THD values are valid for the output power level quoted above – for example, at HPVDD=3.3V and R_L=16Ω, THD is -80dB when output power is 10mW. Higher output power is possible, but will result in deterioration in THD.

AUDIO INPUTS**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--|------|-------|------|------------------|
| LINEL/R, MIC1/2A/2B and MONOIN pins | | | | | | |
| Full Scale Input Signal Level (0dBFS) | V _{INFS} | AVDD = 3.3V | | 1.0 | | V _{rms} |
| | | AVDD = 1.8V | | 0.545 | | |
| | | differential input mode (MS = 01) AVDD = 3.3V | | 0.5 | | |
| | | differential input mode (MS = 01) AVDD = 1.8V | | 0.273 | | |
| Input Resistance | R _{IN} | 0dB PGA gain | 25.6 | 32 | 38.4 | kΩ |
| | | 12dB PGA gain | 10.4 | 13 | 15.6 | |
| Input Capacitance | | | | 5 | | pF |
| Line input to ADC (LINEL, LINER, MONOIN) | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | | 80 | 87 | | dB |
| Total Harmonic Distortion | THD | -3dBFS input | | -86 | -80 | dB |
| Power Supply Rejection | PSRR | 20Hz to 20kHz | | 50 | | dB |
| Microphone input to ADC (MIC1/2A/2B pins) | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | 20dB boost enabled | | 80 | | dB |
| Total Harmonic Distortion | THD | 20dB boost enabled | | -80 | | dB |

AUXILIARY MONO DAC (AUXDAC)**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--------|-----------------|-----|-----|-----|------------------|
| Resolution | | | | 12 | | bits |
| Full scale output voltage | | AVDD=3.3V | | 1 | | V _{rms} |
| Signal to Noise Ratio (A-weighted) | SNR | | | TBD | | dB |
| Total Harmonic Distortion | THD | | | TBD | | dB |

PCM VOICE DAC (VXDAC)**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--------|-----------------|-----|-----|-----|------------------|
| Resolution | | | | 16 | | bits |
| Sample rates | | | | 8 | 16 | Ks/s |
| Full scale output voltage | | AVDD=3.3V | | 1 | | V _{rms} |
| Signal to Noise Ratio (A-weighted) | SNR | | | 80 | | dB |
| Total Harmonic Distortion | THD | | | 74 | | dB |

TOUCHPANEL AND AUXILIARY ADC

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|---------------------------------------|------|-------|------|------|
| Input Pins X+, X-, Y+, Y-, WIPER/AUX4, COMP1/AUX1, COMP2/AUX2 | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | AUX pin not selected as AUX ADC input | | <10 | | nA |
| ADC Resolution | | | | 12 | | bits |
| Differential Non-Linearity Error | DNL | | | ±0.25 | ±1 | LSB |
| Integral Non-Linearity Error | INL | | | | ±2 | LSB |
| Offset Error | | | | | ±4 | LSB |
| Gain Error | | | | | ±6 | LSB |
| Power Supply Rejection | PSRR | | | 50 | | dB |
| Channel-to-channel isolation | | | | 80 | | dB |
| Throughput Rate | | DEL = 1111 (zero settling time) | | | 48 | kHz |
| Settling Time (programmable) | | MCLK = 24.576MHz | 0 | | 6 | ms |
| Switch matrix resistance | | | | 20 | | Ω |
| Programmable Pull-up resistor | R _{PU} | RPU = 000001 | 1 | | 63 | kΩ |
| Pen down detector threshold | | | | VDD/2 | | V |
| Pressure measurement current | I _P | PIL = 1 | | 400 | | μA |
| | | PIL = 0 | | 200 | | |

COMPARATORS

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------|-----------------------------------|------|-----|------|------|
| COMP1/AUX1 and COMP2/AUX2 (pins 29, 30 – when not used as mic inputs) | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | pin not selected as AUX ADC input | | <10 | | nA |
| Comparator Input Offset (COMP1, COMP2 only) | | | -50 | | +50 | mV |
| COMP2 delay (COMP2 only) | | MCLK = 24.576MHz | 0 | | 10.9 | s |

REFERENCE VOLTAGES

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|----------------------|-----------------|------|------|------|--------|
| Audio ADCs, DACs, Mixers | | | | | | |
| Reference Input/Output | CAP2 pin | | 1.63 | 1.65 | 1.66 | V |
| Buffered Reference Output | VREF pin | | 1.64 | 1.65 | 1.67 | V |
| Microphone Bias | | | | | | |
| Bias Voltage | V _{MICBIAS} | | 2.92 | 2.97 | 3.00 | V |
| Bias Current Source | I _{MICBIAS} | | | | 3 | mA |
| Output Noise Voltage | V _n | 1K to 20kHz | | 15 | | nV/√Hz |

DIGITAL INTERFACE CHARACTERISTICS

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|----------------------|-----------|--------|-----------|------|
| Digital Logic Levels (all digital input or output pins) – CMOS Levels | | | | | | |
| Input HIGH level | V _{IH} | | DBVDD×0.7 | | | V |
| Input LOW level | V _{IL} | | | | DBVDD×0.3 | V |
| Output HIGH level | V _{OH} | source current = 2mA | DBVDD×0.9 | | | |
| Output LOW level | V _{OL} | sink current = 2mA | | | DBVDD×0.1 | |
| Clock Frequency | | | | | | |
| Master clock (MCLKA pin) | | | | 24.576 | | MHz |
| AC'97 bit clock (BIT_CLK pin) | | | | 12.288 | | MHz |
| AC'97 sync pulse (SYNC pin) | | | | 48 | | kHz |

Note:

- All audio and non-audio sample rates and other timing scales proportionately with the master clock.
- For signal timing on the AC-Link, please refer to the AC'97 specification (Revision 2.2)

POWER CONSUMPTION

The power consumption of the WM9713L depends on the following factors:

- Supply voltages: Reducing the supply voltages also reduces digital supply currents, and therefore results in significant power savings especially in the digital sections of the WM9713L.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM9713L that are not used (e.g. audio ADC, DAC, touchpanel digitiser).
- Sample rates: Running at lower sample rates will reduce power consumption significantly. The figures below are for 48kHz (unless otherwise specified), but in many scenarios it is not necessary to run at this frequency, e.g. 8kHz PCM voice call scenario uses only 11.4mW (see below).

| MODE DESCRIPTION | AVDD Supply Current V / mA | | DCVDD Supply Current V / mA | | DBVDD Supply Current V / mA | | Total Power (mW) |
|--|-------------------------------------|--------|--------------------------------------|--------|--------------------------------------|-------|------------------------|
| | | | | | | | |
| Off (lowest possible power) Clocks stopped. This is the default configuration after power-up. | 3.3 | 0.01 | 3.3 | 0 | 3.3 | 0.005 | 0.05 |
| LPS (Low Power Standby) VREF maintained using 1MΩ string | 3.3 | 0.014 | 3.3 | 0 | 3.3 | 0.005 | 0.06 |
| Touchpanel only (waiting for pen-down) | 3.3 | 0.042 | 3.3 | 0 | 3.3 | 0.005 | 0.15 |
| PCM Voice call (fs=8kHz) | 2.8 | 2.37 | 2.8 | 1.7 | 2.8 | 0.006 | 11.4 |
| Record from mono microphone | 3.3 | 3.644 | 3.3 | 10.973 | 3.3 | 2.974 | 58.05 |
| Stereo DAC Playback (AC link to headphone) | 3.3 | 3.733 | 3.3 | 9.720 | 3.3 | 2.789 | 53.60 |
| Stereo DAC Playback (AC link to headphone) PLL running with 13MHz input to MCLKB | 3.3 | 4.801 | 3.3 | 10.504 | 3.3 | 2.814 | 59.79 |
| Maximum Power - everything on | 3.3 | 13.656 | 3.3 | 15.472 | 3.3 | 2.938 | 105.82 |

Table 1 Supply Current Consumption

Notes:

- Unless otherwise specified, all figures are at T_A = +25°C, audio sample rate fs = 48kHz, with zero signal (quiescent), and voltage references settled.
- The power dissipated in the headphone, speaker and touchpanel is not included in the above table.

DEVICE DESCRIPTION

INTRODUCTION

The WM9713L is a largely pin compatible upgrade to WM9712, with a PCM voice codec added. This codec is interfaced via a PCM type audio interface which makes use of GPIO pins for connection.

It is designed to meet the mixed-signal requirements of portable and wireless smartphone systems. It includes audio recording and playback, touchpanel digitisation, battery monitoring, auxiliary ADC and GPIO functions, all controlled through a single 5-wire AC-Link interface. Additionally, PCM voice codec functions are supported through provision of an additional voice DAC and a PCM audio serial interface.

A PLL is included to allow unrelated reference clocks to be used for generation of the AC link system clock. Typically 13MHz or 2.048MHz references might be used as a reference.

SOFTWARE SUPPORT

The basic audio features of the WM9713L are software compatible with standard AC'97 device drivers. However, to better support the touchpanel and other additional functions, Wolfson Microelectronics supplies custom device drivers for selected CPUs and operating systems. Please contact your local Wolfson Sales Office for more information.

AC'97 COMPATIBILITY

The WM9713L uses an AC'97 interface to communicate with a microprocessor or controller. The audio and GPIO functions are largely compliant with AC'97 Revision 2.2. The following **differences** from the AC'97 standard are noted:

- Pinout: The function of some pins has been changed to support device specific features. The PHONE and PCBEEP pins have been moved to different locations on the device package.
- Package: The default package for the WM9713L is a 7×7mm leadless QFN package.
- Audio mixing: The WM9713L handles all the audio functions of a smartphone, including audio playback, voice recording, phone calls, phone call recording, ring tones, as well as simultaneous use of these features. The AC'97 mixer architecture does not fully support this. The WM9713L therefore uses a modified AC'97 mixer architecture with three separate mixers.
- Tone Control, Bass Boost and 3D Enhancement: These functions are implemented in the digital domain and therefore affect only signals being played through the audio DACs, not all output signals as stipulated in AC'97.

Some other functions are **additional** to AC'97:

- On-chip BTL loudspeaker driver for mono or stereo speakers
- On-chip BTL driver for ear speaker (phone receiver)
- Auxiliary mono DAC for ring tones, system alerts etc.
- Touchpanel controller
- Auxiliary ADC Inputs
- 2 Analogue Comparators for Battery Alarm
- Programmable Filter Characteristics for Tone Control and 3D Enhancement
- PCM interface to additional Voice DAC and existing audio ADCs
- PLL to create AC'97 system clock from unrelated reference clock input

PCM CODEC

The PCM voice codec functions typically required by mobile telephony devices are provided by an extra voice DAC on the WM9713L, which is interfaced via a standard PCM type data interface, which is constructed through optional use of 4 of the GPIO pins on WM9713L. The audio output data from one or both of the audio ADCs can also be output over this PCM interface, allowing a full voice codec function to be implemented. This PCM interface supports sample rates from 8 to 48ks/s using the standard AC'97 master clock.

AUDIO PATHS OVERVIEW

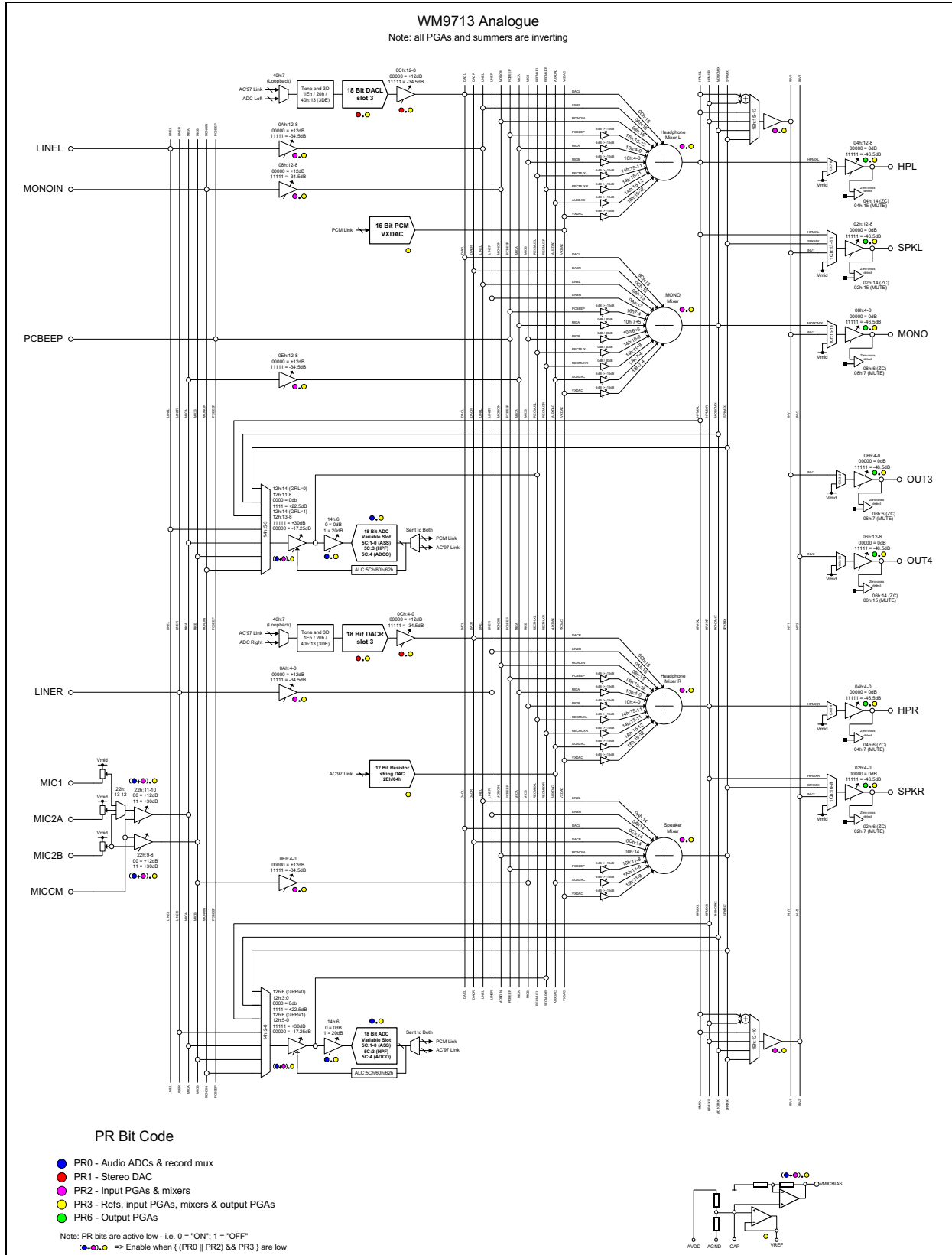


Figure 1 Audio Paths Overview

CLOCK GENERATION

WM9713L supports clocking from 2 separate sources, which can be selected via the AC'97 interface:

- External clock input MCLKA
- External clock input MCLKB

The source clock is divided to appropriate frequencies in order to run the AC'97 interface, PCM interface, voice DAC and Hi-fi DSP by means of a programmable divider block. Clock rates may be changed during operation via the AC'97 link in order to support alternative modes, for example low power mode when voice data is being transmitted only. A PLL is present to add flexibility in selection of input clock frequencies, typical choices being 2.048MHz, 4.096MHz or 13MHz.

Default mode on power-up assumes a clock will be present on MCLKA with the PLL powered down. This enables data to be clocked via the AC'97 link to define the desired clock divider mode and whether PLL needs to be activated.

Note: This clock can be any available frequency.

When muxing between MCLKA and MCLKB both clocks must be active for at least two clock cycles after the switching event.

CLOCK DIVISION MODES

Figure 2 shows the clocking strategy for WM9713L. Clocking is controlled by CLK_MUX, CLK_SRC and S[6:0].

- CLKAX2, CLKBX2 – clock doublers on inputs MCLKA and MCLKB.
- CLK_MUX - selects between MCLKA and MCLKB.
- CLK_SRC – selects between external or PLL derived clock reference.
- S[3:0] – sets the voice DAC clock rate and PCM interface clock when in master mode (division ratio 1 to 16 available).
- S[6:4] - sets the hi-fi clocking rate (division ratio 1 to 8 available).

The registers used to set these switches can be accessed from register address 44h (see Table 2).

If a mode change requires switching from an external clock to a PLL generated clock then it is recommended to set the clock division ratios required for the PLL clock scheme prior to switching between clocks. This option is accommodated by means of two sets of registers. S_{PLL}[6:0] is used to set the divide ratio of the clock when in PLL mode and S_{EXT}[6:0] is used to divide the clock when it is derived from an external source. If the PLL is selected (CLK_SRC = 0), S[6:0] = S_{PLL}[6:0]. S_{PLL}[6:0] is defined in register 46h (see Table 4) and is written to using the page address mode. More details on page address mode for controlling the PLL are found on page 20. Register 46h also contains a number of separate control bits relating to the PLL's function. If an external clock is selected (CLK_SRC = 1) S[6:0] = S_{EXT}[6:0]. S_{EXT}[6:0] is defined in register address 44h. Writing to registers 44h and 46h enables pre-programming of the required clock mode before the PLL output is selected.

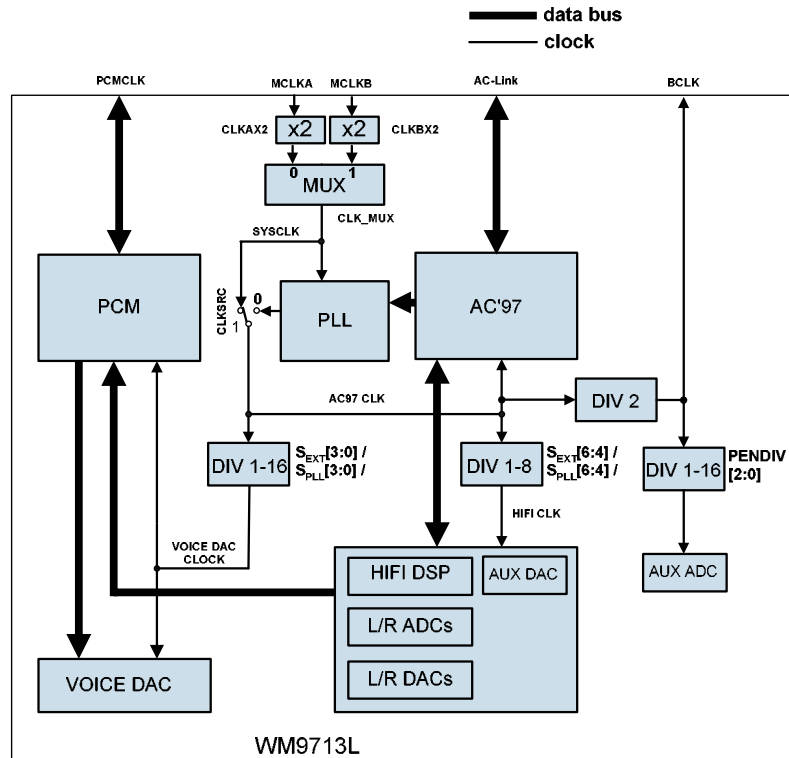


Figure 2 Clocking Architecture for WM9713L

Clock mode and division ratios are controlled by register 44h as shown in Table 2.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|------------------------|--------------|--|
| 44h | 14:12 | S _{EXT} [6:4] | 000 (div 1) | Defines clock division ratio for Hi-fi: DSP, ADCs and DACs 000: f 001: f/2 ... 111: f/8 |
| | 11:8 | S _{EXT} [3:0] | 0000 (div 1) | Defines clock division ratio for PCM interface and voice DAC in external clock mode only: 0000: f 0001: f/2 ... 1111: f/16 |
| | 7 | CLKSRC | 1 (ext clk) | Selects between PLL clock and External clock 0: PLL clock 1: external clock |
| | 5:3 | PENDIV | 000 (div 16) | Sets AUXADC clock divisor 000: f/16 001: f/12 010: f/8 011: f/6 100: f/4 101: f/3 110: f/2 111: f |
| | 2 | CLKBX2 | 0 (Off) | Clock doubler for MCLKB |
| | 1 | CLKAX2 | 0 (Off) | Clock doubler for MCLKA |
| | 0 | CLKMUX | 0 (MCLKA) | Selects between MCLKA and MCLKB (N.B. On power-up clock must be present on MCLKA and must be active for 2 clock cycles after switching to MCLKB) 0: SYSCLK=MCLKA 1: SYSCLK=MCLKB |

Table 2 Clock Muxing and Division Control

INTERNAL CLOCK FREQUENCIES

The internal clock frequencies are defined as follows (refer to Figure 2):

- AC97 CLK – nominally 24.576MHz, used to generate AC97 BITCLK at 12.288MHz.
- HIFI CLK – for HIFI playback at 48ks/s HIFI CLK = 24.576MHz. See Table 3 for voice only playback.
- Voice DAC CLK – see Table 3 for sample rate vs clock frequency.

| SAMPLE RATE | VOICE DAC CLK FREQUENCY | HIFI CLK FREQUENCY |
|--------------------------------|-------------------------|--------------------|
| 8ks/s voice and HIFI | 2.048MHz | 24.576MHz |
| 8ks/s voice only (power save) | 2.048MHz | 4.096MHz |
| 16ks/s voice and HIFI | 4.096MHz | 24.576MHz |
| 16ks/s voice only (power save) | 4.096MHz | 8.192MHz |
| 32ks/s voice and HIFI | 8.192MHz | 24.576MHz |
| 48ks/s voice and HIFI | 12.288MHz | 24.576MHz |

Table 3 Clock Division Mode Table

PEN ADC

The clock for the AUXADC nominally runs at 768kHz and is derived from BITCLK. The divisor for the clock generator is set by PENDIV. This enables the AUXADC clock frequency to be set according to power consumption and conversion rate considerations.

PLL MODE

The PLL operation is controlled by register 46h (see Table 4) and has two modes of operation:

- Integer N
- Fractional N

The PLL has been optimized for nominal input clock (PLL_IN) frequencies in the range 8.192MHz – 19.661MHz (LF=0) and 2.048MHz – 4.9152MHz (LF=1).

Through use of a clock divider (div by 2 / 4) on the input to the PLL frequencies up to 78.6MHz can be accommodated. The input clock divider is enabled by DIVSEL (0=Off) and the division ratio is set by DIVCTL (0=div2, 1=div4).

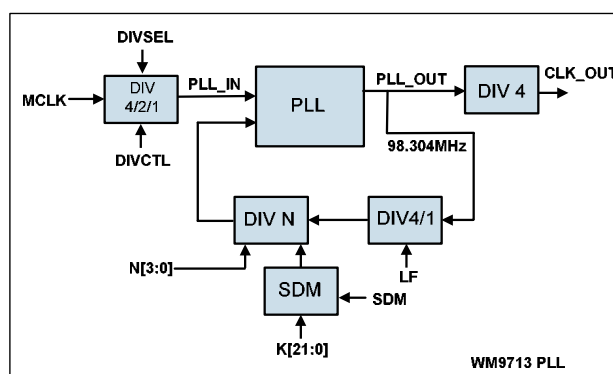


Figure 3 PLL Architecture

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|--------|---------|---|
| 46h | 15:12 | N[3:0] | 0000 | PLL integer division control (must be set between 05h and 0Ch for integer N mode) |
| | 11 | LF | 0 = off | Allows PLL operation with low frequency input clocks (< 8.192MHz) |
| | 10 | SDM | 0 = off | Sigma Delta Modulator enable. Allows fractional N division |
| | 9 | DIVSEL | 0 = off | Enables input clock to PLL to be divided by 2 or 4. Use if input clock is above 14.4MHz |
| | 8 | DIVCTL | 0 | Controls division mode when DIVSEL is high. 0 = div by 2, 1 = div by 4. |
| | 6:4 | PGADDR | 000 | Pager address bits to access programming of K[21:0] and S _{PLL} [6:0] |
| | 3:0 | PGDATA | 0000 | Pager data bits |

Table 4 PLL Clock Control

INTEGER N MODE

The nominal output frequency of the PLL (PLL_OUT) is 98.304MHz which is divided by 4 to achieve a nominal system clock of 24.576MHz.

The integer division ratio (N) is determined by: F_{PLL_out} / F_{PLL_in} , and is set by N[3:0] and must be in the range 5 to 12 for integer N operation (0101 = div by 5, 1100 = div by 12). Note that setting LF=1 enables a further division by 4 required for input frequencies in the range 2.048MHz – 4.096MHz.

Integer N mode is selected by setting SDM=0.

FRACTIONAL N MODE

Fractional N mode provides a divide resolution of $1/2^{22}$ and is set by K[21:0] (register 46h, see section). The relationship between the required division X, the fractional division K[21:0] and the integer division N[3:0] is:

$$K = 2^{22}(X - N)$$

where $0 < (X - N) < 1$ and K is rounded to the nearest whole number.

For example, if the PLL_IN clock is 13MHz and the desired PLL_OUT clock is 98.304MHz then the desired division, X, is 7.5618. So N[3:0] will be 7h and K[21:0] will be 23F488h to produce the desired 98.304MHz clock (see Table 5).

| INPUT CLOCK (PLL_IN) | DESIRED PLL OUTPUT (PLL_OUT) | DIVISION REQUIRED (X) | FRACTIONAL DIVISION (K) | INTEGER DIVISION (N) |
|---|------------------------------|-----------------------|-------------------------|----------------------|
| 2.048MHz | 98.304MHz | 48 | 0 | 12x4* |
| 4.096MHz | 98.304MHz | 24 | 0 | 6x4* |
| 12.288MHz | 98.304MHz | 8 | 0 | 8 |
| 13MHz | 98.304MHz | 7.5618 | 0.5618 | 7 |
| 27MHz (13.5MHz)** | 98.304MHz | 7.2818 | 0.2818 | 7 |
| *Divide by 4 enabled in PLL feedback path for low frequency inputs. (LF = 1) | | | | |
| **Divide by 2 enabled at PLL input for frequencies > 14.4MHz > 38MHz (DIVSEL = 1, DIVCTL = 0) | | | | |

Table 5 PLL Modes of Operation

PLL REGISTER PAGE ADDRESS MAPPING

The clock division control bits $S_{PLL}[6:0]$ and the PLL fractional N division bits are accessed through register 46h using a sub-page address system. The 3 bit pager address allows 8 blocks of 4 bit data words to be accessed whilst the register address is set to 46h. This means that when register address 46h is selected a further 7 cycles of programming are required to set all of the page data bits. Control bit allocation for these page addresses is described in Table 6.

| PAGE ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------|-------|----------------|---------|--|
| 111 | 31:28 | $S_{PLL}[6:4]$ | 0h | Clock division control bus $S_{PLL}[6:0]$. Clock divider reads this control word if PLL is enabled. Bits [6:4] and [3:0] have the same functionality as 44h [14:12] and [11:8] respectively |
| 110 | 27:24 | $S_{PLL}[3:0]$ | 0h | |
| 101 | 23:22 | Reserved | 0h | Reserved bits |
| | 21:20 | K[21:0] | 0h | Sigma Delta Modulator control word for fractional N division. Division resolution is $1/22^2$ |
| 100 | 19:16 | | 0h | |
| 011 | 15:12 | | 0h | |
| 010 | 11:8 | | 0h | |
| 001 | 7:4 | | 0h | |
| 000 | 3:0 | | 0h | |

Table 6 Pager Control Bit Allocation

Powerdown for the PLL and internal clocks is via registers 26h and 3Ch (see Table 7).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-------|---------|--------------------------------------|
| 26h | 13 | PR5 | 1 (Off) | Internal clock disable (active high) |
| 3Ch | 9 | PLL | 1 (Off) | PLL powerdown (active high) |
| N.B. both PR5 and PLL must be asserted low before PLL is enabled | | | | |

Table 7 PLL Powerdown Control

DIGITAL INTERFACES

The WM9713L has two interfaces, a data and control AC'97 interface and a data only PCM interface. The AC'97 interface is available through dedicated pins (SDATAOUT, SDATAIN, SYNC, BITCLK and RESETB) and is the sole control interface with access to all data streams on the device except for the Voice DAC. The PCM interface is available through the GPIO pins (PCMCLK, PCMFS, PCMDAC and PCMADC) and provides access to the Voice DAC. It can also transmit the data from the Stereo ADC. This can be useful, for example, to allow both sides of a phone conversation to be recorded by mixing the transmit and receive paths on one of the ADC channels and transmitting it over the PCM interface.

AC97 INTERFACE

INTERFACE PROTOCOL

The WM9713L uses an AC'97 interface for both data transfer and control. The AC-Link has 5 wires:

- SDATAIN (pin 8) carries data from the WM9713L to the controller
- SDATAOUT (pin 5) carries data from the controller to the WM9713L
- BITCLK (pin 6) is a clock, derived from either MCLKA or MCLKB inputs and supplied to the controller.
- SYNC is a synchronization signal generated by the controller and passed to the WM9713L
- RESETB resets the WM9713L to its default state

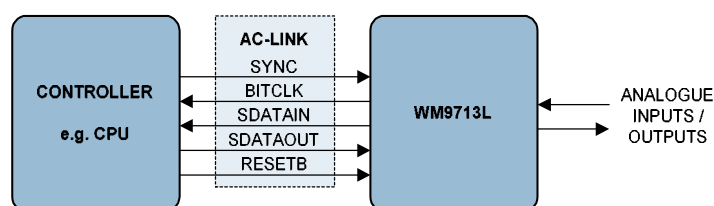


Figure 4 AC-Link Interface (typical case with BITCLK generated by the AC97 codec)

The SDATAIN and SDATAOUT signals each carry 13 time-division multiplexed data streams (slots 0 to 12). A complete sequence of slots 0 to 12 is referred to as an AC-Link frame, and contains a total of 256 bits. The frame rate is 48kHz. This makes it possible to simultaneously transmit and receive multiple data streams (e.g. audio, touchpanel, AUXDAC, control) at sample rates up to 48kHz.

Detailed information can be found in the AC'97 (Revision 2.2) specification, which can be obtained at www.intel.com/design/chipsets/audio/

Note:

SDATAOUT and SYNC must be held low when RESETB is applied. These signals must be held low for the entire duration of the RESETB pulse and especially during the low-to-high transition of RESETB. If SDATAOUT or SYNC is high during reset, the WM9713L may enter test modes. Information relating to this operation is available in the AC'97 specification or in Wolfson applications note WAN-0104 available at www.wolfsonmicro.com.

PCM INTERFACE

OPERATION

WM9713L can implement a PCM voice codec function using the dedicated VXDAC and either one or both of the existing hi-fi ADC's. In PCM codec mode, VXDAC input and ADC output are interfaced via a PCM style port via GPIO pins.

This interface can support one ADC channel, or stereo/dual ADC channels if required, (two channels of data are sent per PCM frame as back to back words).

In voice only mode, the AC link is used only for control information, not audio data. Therefore it will generally be shut down (PR4=1), except when control data must be sent.

The PCM interface makes use of 4 of the GPIO interface pins, for clock, frame, and data in/out. If the PCM codec function is not enabled then the GPIO pins may be used for other functions.

INTERFACE PROTOCOL

The WM9713L PCM audio interface is used for the input of data to the Voice DAC and the output of data from the Stereo ADC. When enabled, the PCM audio interface uses four GPIO pins:

- GPIO1/PCMCLK: Bit clock
- GPIO3/PCMFS: Frame Sync
- GPIO4/PCMDAC: Voice DAC data input
- GPIO5/PCMADC: Stereo ADC data output

Depending on the mode of operation (see "PCM Interface Modes"), at least one of these four pins must be set up as an output by writing to register 4Ch (see Table 62). When not enabled the GPIOs may be used for other functions on the WM9713L.

PCM INTERFACE MODES

The WM9713L PCM audio interface may be configured in one of four modes:

- Disabled Mode: The WM9713L disables and tri-states all PCM interface pins. Any clock input is ignored and ADC/DAC data is not transferred.
- Slave Mode: The WM9713L accepts PCMCLK and PCMFS as inputs from an external source.
- Master Mode: The WM9713L generates PCMCLK and PCMFS as outputs.
- Partial Master Mode: The WM9713L generates PCMCLK as an output, and accepts PCMFS as an external input.

PCM AUDIO DATA FORMATS

Four different audio data formats are supported:

- DSP mode
- Left justified
- Right justified
- I²S

All four of these modes are MSB first. They are described below. Refer to the Electrical Characteristic section for timing information.

The PCM Interface may be configured for Mono mode, where only one channel of ADC data is output. In this mode the interface should be configured for DSP mode. A short or long frame sync is supported and the MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of VXCLK.

Note that when operating in stereo mode the mono Voice DAC always uses the left channel data as its input.

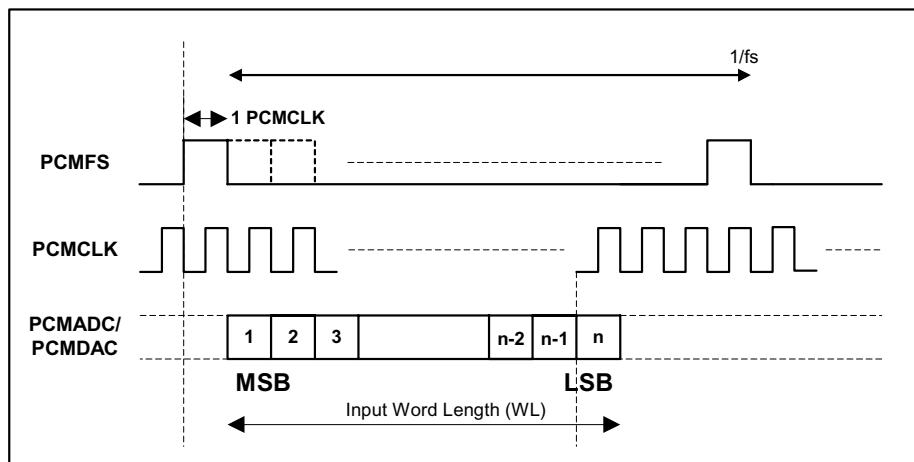


Figure 5 PCM Interface Mono Mode (mode A, FSP=0)

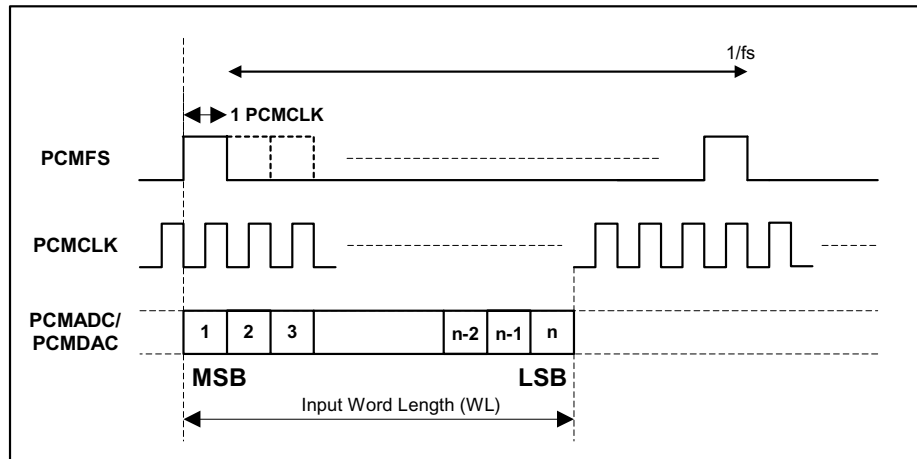


Figure 6 PCM Interface Mono Mode (mode B, FSP=1)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of PCMCLK (selectable by FSP) following a rising edge of PCMFs. Right channel data immediately follows left channel data. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles between the LSB of the right channel data and the next sample.

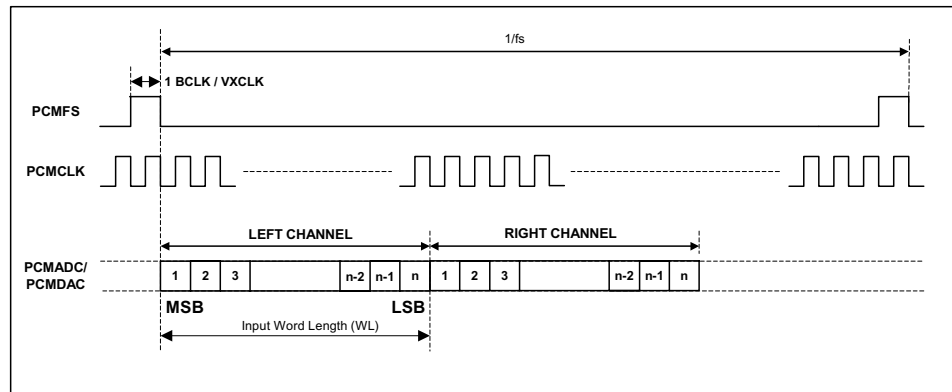


Figure 7 DSP Mode Audio Interface (mode A, FSP=0)

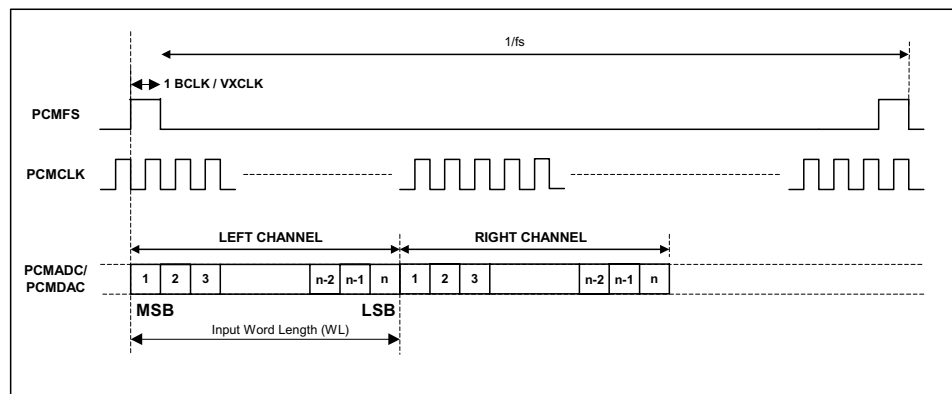


Figure 7 DSP Mode Audio Interface (mode B, FSP=1)

In Left Justified mode, the MSB is available on the first rising edge of PCMCLK following a PCMFS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles before each PCMFS transition.

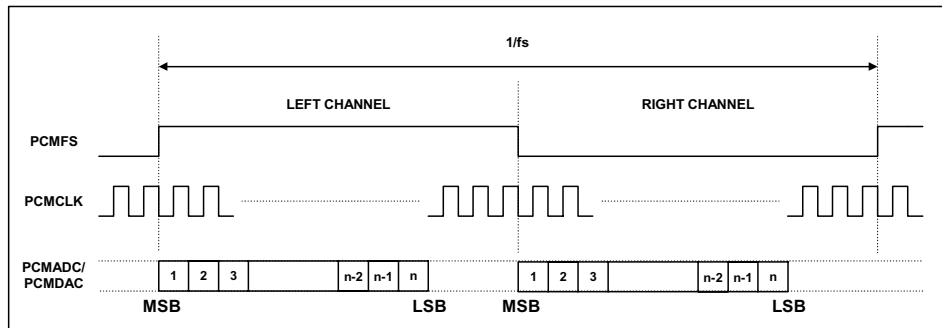


Figure 8 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of PCMCLK before a PCMFS transition. All other bits are transmitted before (MSB first). Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles after each PCMFS transition.

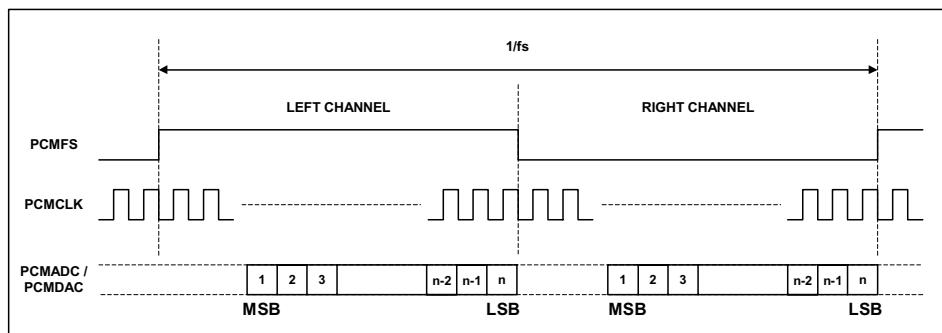


Figure 9 Right Justified Audio Interface (assuming n-bit word length)

In I²S mode, the MSB is available on the second rising edge of PCMCLK following a PCMFS transition. The other bits up to the LSB are then transmitted in order. Depending on word length, PCMCLK frequency and sample rate, there may be unused PCMCLK cycles between the LSB of one sample and the MSB of the next.

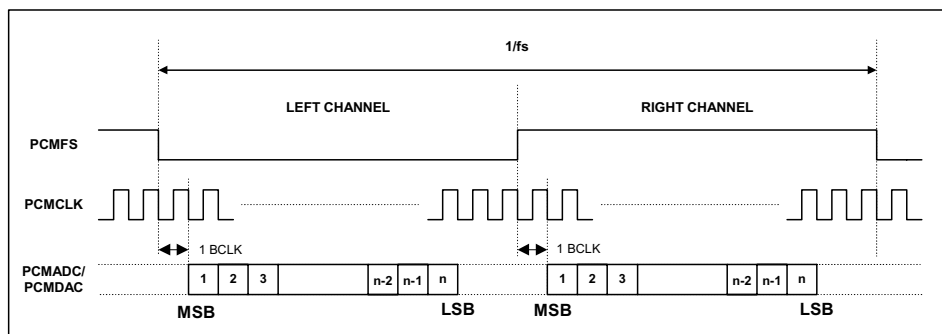


Figure 10 I²S Justified Audio Interface (assuming n-bit word length)

CONTROL

The register bits controlling PCM audio format, word length and operating modes are summarised below. CTRL must be set to override the normal use of the PCM interface pins as GPIOs, MODE must be set to specify master/slave modes.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-----------------------|-------|---------|---------|--|
| 36h PCM Control | 15 | CTRL | 0 | Sets function and control registers for GPIO / PCM interface pins. 0 = GPIO pins as GPIOs 1 = GPIO pins configured as PCM interface and controlled by this register |
| | 14:13 | MODE | 10 | PCM interface mode when CTRL=1 00 = PCM interface disabled [PCMCLK tri-stated, PCMFS tri-stated] 01 = PCM interface in slave mode [PCMCLK as input, PCMFS as input] 10 = PCM interface in master mode [PCMCLK as output, PCMFS as output] 11 = PCM interface in partial master mode [PCMCLK as output, PCMFS as input] |
| | 11:9 | DIV | 010 | Voice DAC clock to PCMCLK divider. In master mode PCMCLK is derived from Voice DAC clock. 000 : PCMCLK = Voice DAC clock 001 : PCMCLK = Voice DAC clock / 2 010 : PCMCLK = Voice DAC clock / 4 011 : PCMCLK = Voice DAC clock / 8 100 : PCMCLK = Voice DAC clock / 16 |
| | 8 | VDACOSR | 1 | VXDAC oversample rate: 0: 128 x fs 1: 64 x fs |
| | 7 | CP | 0 | PCMCLK polarity 1 = invert PCMCLK polarity 0 = normal PCMCLK polarity |
| | 6 | FSP | 0 | Right, Left and I ² S modes – PCMFS polarity 1 = invert PCMFS polarity 0 = normal PCMFS polarity DSP Mode – mode A/B select 0 = MSB is available on 2nd PCMCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st PCMCLK rising edge after LRC rising edge (mode B) |
| | 5:4 | SEL | 10 | PCM ADC channel select 00 = Output left and right ADC data 01 = Swap and output left and right ADC data 10 = Output left ADC data only 11 = Output right ADC data only |

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|--|
| | 3:2 | WL | 00 | PCM Data Word Length 11 = 32 bits (see Note) 10 = 24 bits 01 = 20 bits 00 = 16 bits |
| | 1:0 | FMT | 11 | PCM Data Format Select 11 = DSP Mode 10 = I ² S Format 01 = Left justified 00 = Right justified |

Table 8 PCM Codec Control

Note: Right justified does not support 32-bit data.

AUDIO ADCS

STEREO ADC

The WM9713L has a stereo sigma-delta ADC to digitize audio signals. The ADC achieves high quality audio recording at low power consumption. The ADC sample rate can be controlled by writing to a control register (see "Variable Rate Audio"). It is independent of the DAC sample rate.

To save power, the left and right ADCs can be separately switched off using the Powerdown bits ADCL and ADCR (register 3Ch, bits 5:4), whereas PR0 disables both ADCs (see "Power Management" section). If only one ADC is running, the same ADC data appears on both the left and right AC-Link slots.

The output from the ADC can be sent over either the AC link as usual, or output via the PCM interface which may be configured on the GPIO pins.

HIGH PASS FILTER

The WM9713L audio ADC incorporates a digital high pass filter that eliminates any DC bias from the ADC output data. The filter is enabled by default. For DC measurements, it can be disabled by writing a '1' to the HPF bit (register 5Ch, bit 3).

This high pass filter corner frequency can be selected to have different values in WM9713L, to suit applications such as voice where a higher cutoff frequency is required.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|--------|---------|--|
| 5Ch | 3 | HPF | 0 | High-pass filter disable 0: Filter enabled (for audio) 1: Filter disabled (for DC measurements) |
| 5Ah | 5:4 | HPMODE | 00 | HPF corner frequency 00: 7Hz @ Fs=48kHz 01: 82Hz @ Fs=16kHz 10: 82Hz @ Fs=8kHz 11: 170Hz @ Fs=8kHz |
| Note: the filter corner frequency is proportional to the sample rate. | | | | |

Table 9 Controlling the ADC Highpass Filter

ADC SLOT MAPPING

By default, the output of the left audio ADC appears on slot 3 of the SDATAIN signal (pin 8), and the right ADC data appears on slot 4. However, the ADC output data can also be sent to other slots, by setting the ASS (ADC slot select) control bits as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------------|-----|-------|---------|---|
| 5Ch Additional Functions (2) | 1:0 | ASS | 00 | ADC to slot mapping 00: Left = Slot 3, Right = Slot 4 (default) 01: Left = Slot 7, Right = Slot 8 10: Left = Slot 6, Right = Slot 9 11: Left = Slot 10, Right = Slot 11 |

Table 10 ADC Slot Mapping

RECORD SELECTOR

The record selector determines which input signals are routed into the audio ADC. The left and right channels can be selected independently. This is useful for recording a phone call: one channel can be used for the RX signal and the other for the TX signal, so that both sides of the conversation are digitized.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------------------|-----|--------|---------|--|
| 14h Record Routing / Mux Select | 6 | RECBST | 0 | 20dB Boost 1: Boost ADC input signal by 20dB 0 :No boost Note: RECBST gain is in addition to the microphone pre-amps (MPABST and MPBBST bits) and record gain (GRL and GRR / GRL bits). |
| | 5:3 | RECSL | 000 | Left ADC signal source 000: MICA (pre-PGA) 001: MICB (pre-PGA) 010: LINEL (pre-PGA) 011: MONOIN (pre-PGA) 100: Headphone Mix (left) 101: Speaker Mix 110: Mono Mix 111: Reserved (do not use this setting) |
| | 2:0 | RECSR | 000 | Right ADC signal source 000: MICA (pre-PGA) 001: MICB (pre-PGA) 010: LINER (pre-PGA) 011: MONOIN (pre-PGA) 100: Headphone Mix (right) 101: Speaker Mix 110: Mono Mix 111: Reserved (do not use this setting) |

Table 11 Audio Record Selector

RECORD GAIN

The amplitude of the signal that enters the audio ADC is controlled by the Record PGA (Programmable Gain Amplifier). The PGA gain can be programmed either by writing to the Record Gain register, or by the Automatic Level Control (ALC) circuit (see next section). When the ALC is enabled, any writes to the Record Gain register have no effect.

Two different gain ranges can be implemented: the standard gain range defined in the AC'97 standard, or an extended gain range with smaller gain steps. The ALC circuit always uses the extended gain range, as this has been found to result in better sound quality.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|--------------------|---------|---------|---|---|--|
| 12h Record Gain | 15 | RMU | 1 | Mute Audio ADC (both channels) 1: Mute (OFF) 0: No Mute (ON) | |
| | 14 | GRL | 0 | Gain range select (left) 0: Standard (0 to 22.5dB, 1.5dB step size) 1: Extended (-17.25 to +30dB, 0.75dB steps) | |
| | 13:8 | RECVOLL | 000000 | Record Volume (left) | |
| | | | | Standard (GRL=0) | Extended (GRL=1) |
| | | | | XX0000: 0dB XX0001: +1.5dB ... (1.5dB steps) XX1111: +22.5dB | 000000: -17.25dB 000001: -16.5dB ... (0.75dB steps) 111111: +30dB |
| | 7 | ZC | 0 | Zero Cross Enable 0: Record Gain changes immediately 1: Record Gain changes when signal is zero or after time-out | |
| | 6 | GRR | 0 | Gain range select (right) Similar to GRL | |
| 5:0 | RECVOLR | 000000 | Record Volume (right) Similar to RECVOLR | | |

Table 12 Record Gain Register

The output of the Record PGA can also be mixed into the phone and/or headphone outputs (see "Audio Mixers"). This makes it possible to use the ALC function for the microphone signal in a smartphone application.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-----------------------|-------|--------|-----------|--|
| 14h Record Routing | 15:14 | R2H | 11 (mute) | Controls record mux to headphone mixer paths. 00=stereo, 01=left rec mux only, 10=right rec mux only, 11=mute left and right |
| | 13:11 | R2HVOL | 010 (0dB) | Controls gain of record mux l/r to headphone mixer paths. 000: +6dB 001: +3dB ... (3dBsteps) 111: -15dB |
| | 10:9 | R2M | 11 (mute) | Controls record mux to mono mixer path. 00=stereo, 01=left rec mux only, 10=right rec mux only, 11=mute left and right |
| | 8 | R2MBST | 0 (OFF) | Enables 20dB gain boost for record mux to mono mixer path |

Table 13 Record PGA Routing Control

AUTOMATIC LEVEL CONTROL

The WM9713L has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

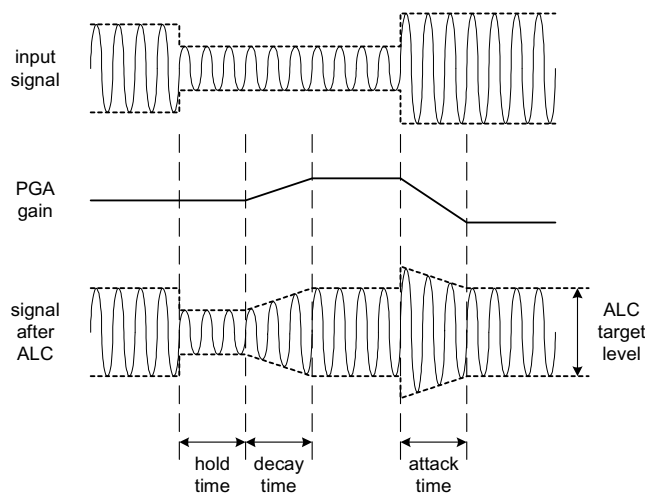


Figure 11 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between -6dB and -28.5dB (relative to ADC full scale) using the ALCL register bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively.

HOLD TIME

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

DECAY (GAIN RAMP-UP) TIME

Decay time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from -15dB up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

ATTACK (GAIN RAMP-DOWN) TIME

Attack time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-------|-----------|-----------------|--|
| 62h ALC / Noise Gate Control | 15:14 | ALCSEL | 00 (OFF) | ALC function select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) |
| | 13:11 | MAXGAIN | 111 (+30dB) | PGA gain limit for ALC 111 = +30dB 110 = +24dB ... (6dB steps) 001 = -6dB 000 = -12dB |
| | 10:9 | ZCTIMEOUT | 11 | Programmable zero cross timeout (delay for 12.288MHz BITCLK): 11: $2^{17} * t_{bitclk}$ (10.67 ms) 10: $2^{16} * t_{bitclk}$ (5.33 ms) 01: $2^{15} * t_{bitclk}$ (2.67 ms) 00: $2^{14} * t_{bitclk}$ (1.33 ms) |
| 60h ALC Control | 15:12 | ALCL | 1011 (-12dB) | ALC target – sets signal level at ADC input 0000 = -28.5dB FS 0001 = -27.0dB FS ... (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS |
| | 11:8 | HLD | 0000 (0ms) | ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms ... (time doubles with every step) 1111 = 43.691s |
| | 7:4 | DCY | 0011 (192ms) | ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms ... (time doubles with every step) 1010 or higher = 24.58s |
| | 3:0 | ATK | 0010 (24ms) | ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms ... (time doubles with every step) 1010 or higher = 6.14s |

Table 14 ALC Control

MAXIMUM GAIN

The MAXGAIN register sets the maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when $\text{ATK} = 0000$), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

(Note: If $\text{ATK} = 0000$, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used).

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM9713L has a noise gate function that prevents noise pumping by comparing the signal level at the input pins (i.e. before the record PGA) against a noise gate threshold, NGTH. Provided that the noise gate function is enabled ($\text{NGAT} = 1$), the noise gate cuts in when:

$$\text{Signal level at ADC [dB]} < \text{NGTH [dB]} + \text{PGA gain [dB]} + \text{Mic Boost gain [dB]}$$

This is equivalent to:

$$\text{Signal level at input pin [dB]} < \text{NGTH [dB]}$$

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet). If the NGG bit is set, the ADC output is also muted when the noise gate cuts in.

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set-up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-----|-----------|---------|--|
| 62h ALC / Noise Gate Control | 7 | NGAT | 0 | Noise gate function enable 1 = enable 0 = disable |
| | 5 | NGG | 0 | Noise gate type 0 = PGA gain held constant 1 = mute ADC output |
| | 4:0 | NGTH(4:0) | 00000 | Noise gate threshold 00000: -76.5dBFS 00001: -75dBFS ... 1.5 dB steps 11110: -31.5dBFS 11111: -30dBFS |

Table 15 Noise Gate Control

AUDIO DACS

STEREO DAC

The WM9713L has a stereo sigma-delta DAC that achieves high quality audio playback at low power consumption. Digital tone control, adaptive bass boost and 3-D enhancement functions operate on the digital audio data before it is passed to the stereo DAC. (Contrary to the AC'97 specification, they have no effect on analogue input signals or signals played through the auxiliary DAC. Nevertheless, the ID2 and ID5 bits in the reset register, 00h, are set to '1' to indicate that the WM9713L supports tone control and bass boost.)

The DAC output has a PGA for volume control. The DAC sample rate can be controlled by writing to a control register (see "Variable Rate Audio"). It is independent of the ADC sample rate.

When not in use the DACs can be separately powered down using the Powerdown register bits DACL and DACR (register 3Ch, bits [7:6]).

STEREO DAC VOLUME

The volume of the DAC output signal is controlled by a PGA (Programmable Gain Amplifier). Each DAC can be mixed into the headphone, speaker and mono mixer paths (see "Audio Mixers") controlled by register 0Ch.

Each DAC-to-mixer path has an independent mute bit. When all DAC-to-mixer paths are muted the DAC PGA is muted automatically.

When not in use the DAC PGAs can be powered down using the Powerdown register bits DACL and DACR (register 3Ch, bits [7:6]).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------------|------|-------------|----------------|--|
| 0Ch DAC Volume | 15 | D2H | 1 | Mute DAC path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | D2S | 1 | Mute DAC path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 13 | D2M | 1 | Mute DAC path to mono mixer 1: Mute, 0: No mute (ON) |
| | 12:8 | DACL VOL | 01000 (0dB) | Left DAC Volume 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |
| | 4:0 | DACR VOL | 01000 (0dB) | Right DAC Volume similar to DACLVOL |
| 5Ch Additional Functions (2) | 15 | AMUTE | 0 | Read-only bit to indicate auto-muting 1: DAC auto-muted 0: DAC not muted |
| | 7 | AMEN | 0 | DAC Auto-Mute Enable 1: Automatically mutes analogue output of stereo DAC if digital input is zero 0: Auto-mute OFF |

Table 16 Stereo DAC Volume Control

TONE CONTROL / BASS BOOST

The WM9713L provides separate controls for bass and treble with programmable gains and filter characteristics. This function operates on digital audio data before it is passed to the audio DACs.

Bass control can take two different forms:

- Linear bass control: bass signals are amplified or attenuated by a user programmable gain. This is independent of signal volume, and very high bass gains on loud signals may lead to signal clipping.
- Adaptive bass boost: The bass volume is amplified by a variable gain. When the bass volume is low, it is boosted more than when the bass volume is high. This method is recommended because it prevents clipping, and usually sounds more pleasant to the human ear.

Treble control applies a user programmable gain, without any adaptive boost function.

Treble, linear bass and 3D enhancement can all produce signals that exceed full-scale. In order to avoid limiting under these conditions, it is recommended to set the DAT bit to attenuate the digital input signal by 6dB. The gain at the outputs should be increased by 6dB to compensate for the attenuation. Cut-only tone adjustment (i.e. bass and treble gains = 0) and adaptive bass boost cannot produce signals above full-scale and therefore do not require the DAT bit to be set.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------------|------|-----------------|--|---|
| 20h DAC Tone Control | 15 | BB | 0 | Bass Mode 0 = Linear bass control 1 = Adaptive bass boost |
| | 12 | BC | 0 | Bass Cut-off Frequency 0 = Low (130Hz at 48kHz sampling) 1 = High (200Hz at 48kHz sampling) |
| | 11:8 | BASS | 1111 (OFF) | Bass Intensity |
| | | | | Code BB=0 BB=1 |
| | | | | 0000 +9dB 15 (max) |
| | | | | 0001 +9dB 14 |
| | | | | 0010 +7.5dB 13 |
| | | | | ... (1.5dB steps) ... |
| | | | | 0111 0dB 8 |
| | | | | ... (1.5dB steps) ... |
| | | | 1011-1101 -6dB 4-2 | |
| | | | 1110 -6dB 1 (min) | |
| | | | 1111 Bypass (OFF) | |
| 6 | DAT | 0 | -6dB attenuation 0 = Off 1 = On | |
| 4 | TC | 0 | Treble Cut-off Frequency 0 = High (8kHz at 48kHz sampling) 1 = Low (4kHz at 48kHz sampling) | |
| 3:0 | TRBL | 1111 (Disabled) | Treble Intensity 0000 or 0001 = +9dB 0010 = +7.5dB ... (1.5dB steps) 1011 to 1110 = -6dB 1111 = Treble Control Disabled | |

Table 17 DAC Tone Control

Note:

1. All cut-off frequencies change proportionally with the DAC sample rate.

3D STEREO ENHANCEMENT

The 3D stereo enhancement function artificially increases the separation between the left and right channels by amplifying the (L-R) difference signal in the frequency range where the human ear is sensitive to directionality. The programmable 3D depth setting controls the degree of stereo expansion introduced by the function. Additionally, the upper and lower limits of the frequency range used for 3D enhancement can be selected using the 3DFILT control bits.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------|-----|---------|-----------------|--|
| 40h General Purpose | 13 | 3DE | 0 (disabled) | 3D enhancement enable |
| 1Eh DAC 3D Control | 5 | 3DLC | 0 | Lower Cut-off Frequency 0 = Low (200Hz at 48kHz sampling) 1 = High (500Hz at 48kHz sampling) |
| | 4 | 3DUC | 0 | Upper Cut-off Frequency 0 = High (2.2kHz at 48kHz sampling) 1 = Low (1.5kHz at 48kHz sampling) |
| | 3:0 | 3DDEPTH | 0000 | 3D Depth 0000: 0% (minimum 3D effect) 0001: 6.67% ...(6.67% steps) 1110: 93.3% 1111: 100% (maximum) |

Table 18 Stereo Enhancement Control

Note:

1. All cut-off frequencies change proportionally with the DAC sample rate.

VOICE DAC

VXDAC is a 16-bit mono DAC intended for playback of Rx voice signals input via the PCM interface. Performance has been optimised for operating at 8ks/s or 16ks/s. The VXDAC will function at other sample rates up to 48ks/s, but this is not recommended.

The analogue output of VXDAC is routed directly into the output mixers. The signal gain into each mixer can be adjusted at the mixer inputs using control register 18h.

When not in use the VXDAC can be powered down using the Powerdown register bit VXDAC (register 3Ch, bit 12).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-----------------------------|-------|--------|--------------|---|
| 3Ch Powerdown (1) | 12 | VXDAC | 1 | VXDAC powerdown bit 1: OFF, 0: ON |
| 18h VXDAC Output Control | 15 | V2H | 1 | Mute VXDAC path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14:12 | V2HVOL | 010 (0dB) | VXDAC to headphone mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 11 | V2S | 1 | Mute VXDAC path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 10:8 | V2SVOL | 010 (0dB) | VXDAC to speaker mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 7 | V2M | 1 | Mute VXDAC path to mono mixer 1: Mute, 0: No mute (ON) |
| | 6:4 | V2MVOL | 010 (0dB) | VXDAC to mono mixer gain 000: +6dB ... (3dB steps) 111: -15dB |

Table 19 VXDAC Control

AUXILIARY DAC

AUXDAC is a simple 12-bit mono DAC. It can be used to generate DC signals (with the numeric input written into a control register), or AC signals such as telephone-quality ring tones or system beeps (with the input signal supplied through an AC-Link slot). In AC mode (XSLE = 1), the input data is binary offset coded; in DC mode (XSLE = 0), there is no offset.

The analogue output of AUXDAC is routed directly into the output mixers. The signal gain into each mixer can be adjusted at the mixer inputs using control register 12h. In slot mode (XSLE = 1), the AUXDAC also supports variable sample rates (See "Variable Rate Audio" section).

When not in use the auxiliary DAC can be powered down using the Powerdown register bit AUXDAC (register 3Ch, bit 11).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------------|-------|------------|-----------|--|
| 3Ch Powerdown (1) | 11 | AUXDAC | 0 | AUXDAC powerdown 1: OFF, 0: ON |
| 64h AUXDAC Input Control | 15 | XSLE | 0 | AUXDAC input selection 0: from AUXDACVAL (for DC signals) 1: from AC-Link slot selected by AUXDACSLT (for AC signals) |
| | 14:12 | AUXDAC SLT | 000 | AUXDAC Input Selection 000 – Slot 5, bits 8-19 (with XSLE=1) 001 – Slot 6, bits 8-19 (with XSLE=1) 010 – Slot 7, bits 8-19 (with XSLE=1) 011 – Slot 8, bits 8-19 (with XSLE=1) 100 – Slot 9, bits 8-19 (with XSLE=1) 101 – Slot 10, bits 8-19 (with XSLE=1) 110 – Slot 11, bits 8-19 (with XSLE=1) 111 – RESERVED (do not use) |
| | 11:0 | AUXDAC VAL | 000h | AUXDAC Digital Input (with XSLE=0) 000h: minimum FFFh: full-scale |
| 1Ah AUXDAC Output Control | 15 | A2H | 1 | Mute AUXDAC path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14:12 | A2HVOL | 010 (0dB) | AUXDAC to headphone mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 11 | A2S | 1 | Mute AUXDAC path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 10:8 | A2SVOL | 010 (0dB) | AUXDAC to speaker mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 7 | A2M | 1 | Mute AUXDAC path to mono mixer 1: Mute, 0: No mute (ON) |
| | 6:4 | A2MVOL | 010 (0dB) | AUXDAC to mono mixer gain 000: +6dB ... (3dB steps) 111: -15dB |

Table 20 AUXDAC Control

VARIABLE RATE AUDIO / SAMPLE RATE CONVERSION

By using an AC'97 Rev2.2 compliant audio interface, the WM9713L can record and playback at all commonly used audio sample rates, and offer full split-rate support (i.e. the DAC, ADC and AUXDAC sample rates are completely independent of each other – any combination is possible).

The default sample rate is 48kHz. If the VRA bit in register 2Ah is set, then other sample rates can be selected by writing to registers 2Ch, 32h and 2Eh. The AC-Link continues to run at 48k frames per second irrespective of the sample rate selected. However, if the sample rate is less than 48kHz, then some frames do not carry an audio sample.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------------|------|--------------|------------------|--|
| 2Ah Extended Audio Stat/Ctrl | 0 | VRA | 0 (OFF) | Variable Rate Audio 0: OFF (DAC and ADC run at 48kHz) 1: ON (sample rates determined by registers 2Ch and 32h) |
| 2Ch Audio DAC Sample Rate | 15:0 | DACSR | BB80h (48kHz) | Audio DAC sample rate 1F40h: 8kHz 2B11h: 11.025kHz 2EE0h: 12kHz 3E80h: 16kHz 5622h: 22.05kHz 5DC0h: 24kHz 7D00h: 32kHz AC44h: 44.1kHz BB80h: 48kHz Any other value defaults to the nearest supported sample rate |
| 32h Audio ADC Sample Rate | 15:0 | ADCSR | BB80h (48kHz) | Audio ADC sample rate similar to DACSR |
| 2Eh AUXDAC Sample Rate | 15:0 | AUXDA CSR | BB80h (48kHz) | AUXDAC sample rate similar to DACSR |

Table 21 Audio Sample Rate Control

Note:

Changing the ADC and / or DAC sample rate will only be effective if the ADC's and DAC's are enabled and powered up before the sample rate is changed. This is done by setting the relevant bits in registers 26h and 3Ch, as well as the VRA bit in register 2Ah.

The process is as follows:

1. Enable and power up ADC's and or DAC's in registers 26h and 3Ch.
2. Enable VRA bit in 2Ah, bit 0.
3. Change the sample rate in the respective register.

AUDIO INPUTS

The following sections give an overview of the analogue audio input pins and their function. For more information on recommended external components, please refer to the "Applications Information" section.

LINE INPUT

The LINEL and LINER inputs are designed to record line level signals, and/or to mix into one of the analogue outputs.

Both pins are directly connected to the record selector. The record PGA adjusts the recording volume, controlled by register 12h or by the ALC function.

For analogue mixing, the line input signals pass through a separate PGA, controlled by register 0Ah. The signals can be mixed into the headphone, speaker and mono mixer paths (see "Audio Mixers").

Each LINE-to-mixer path has an independent mute bit. When all LINE-to-mixer paths are muted the line PGA is muted automatically. When the line inputs are not used, the line PGA can be switched off to save power (see "Power Management" section).

LINEL and LINER are biased internally to the reference voltage VREF. Whenever the inputs are muted or the device placed into standby mode, the inputs remain biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|------|--------------|----------------|---|
| 0Ah | 15 | L2H | 1 | Mute LINE path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | L2S | 1 | Mute LINE path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 13 | L2M | 1 | Mute LINE path to mono mixer 1: Mute, 0: No mute (ON) |
| | 12:8 | LINEL VOL | 01000 (0dB) | LINEL input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |
| | 4:0 | LINER VOL | 01000 (0dB) | LINER input gain similar to LINELVOL |

Table 22 Line Input Control

Additionally, line inputs can be used as single-ended microphone inputs through the record mux to provide a clickless ALC function by bypassing offset introduced through the microphone pre-amps. Note that the line inputs to the mixers should all be deselected if this input configuration is used.

MICROPHONE INPUT

MICROPHONE PRE-AMPS

There are two microphone pre-amplifiers, MPA and MPB, which can be configured in a variety of ways to accommodate up to 3 selectable differential microphone inputs or 2 differential microphone inputs operating simultaneously for stereo or noise cancellation. The microphone input circuit is shown in Figure 12.

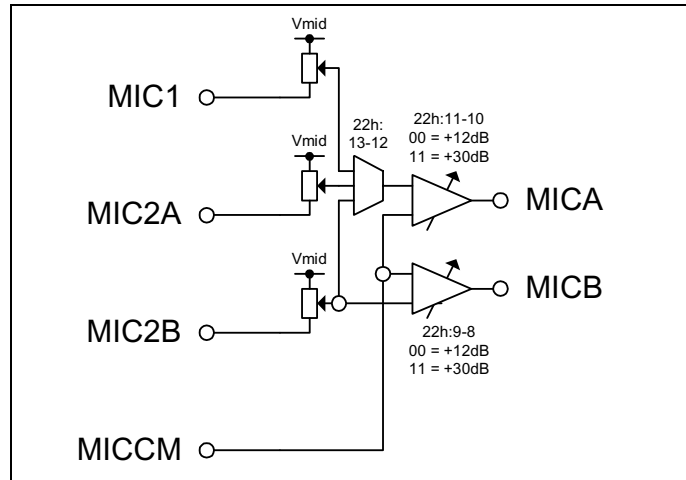


Figure 12 Microphone Input Circuit

The input pins used for the microphones are MIC1, MICCM, MIC2A and MIC2B. Note that input pins MIC2A and MIC2B are multi-function inputs and must be configured for use as microphone inputs when required. This is achieved using MICCMPSEL[1:0] in register 22h (see Table 23). The input to microphone pre-amp A can be selected from any of the three microphone inputs MIC1, MIC2A and MIC2B using MPASEL[1:0]. Each pre-amp has independent boost control from +12dB to +30dB in four steps. This is controlled by MPABST[1:0] and MPBBST[1:0].

When not in use each microphone pre-amp can be powered down using the Powerdown register bits MPA and MPB (register 3Eh, bits [1:0]). When disabled the inputs are tied to Vmid (for MIC2A and MIC2B this only applies when they are selected as microphone inputs, otherwise they are left floating).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|-----------|---------|---|
| 22h | 15:14 | MICCMPSEL | 00 | MIC2A and MIC2B pin configuration 00: MIC2A and MIC2B microphone inputs 01: MIC2A only 10: MIC2B only 11: neither |
| | 13:12 | MPASEL | 00 | MPA pre-amp input select 00 : MIC1 01 : MIC2A 10 : MIC2B 11 : unused (do not select) |
| | 11:10 | MPABST | 00 | MPA pre-amp gain control 00 : +12dB 01 : +18dB 10 : +24dB 11 : +30dB |
| | 9:8 | MPBBST | 00 | MPB pre-amp gain control 00 = +12dB 01 = +18dB 10 = +24dB 11 = +30dB |

Table 23 Microphone Pre-amp Control

SINGLE MIC OPERATION

Up to three microphones can be connected in a single-ended configuration. Any one of the three MICs can be selected as the input to MPA using MPASEL[1:0] (Register 22h, bits 13:12). Only the microphone on MIC2B can be selected to MPB. Note that MPABST always sets the gain for the selected MPA input microphone. If MIC2B is the selected input for MPA it is recommended that MPB is disabled.

DUAL MIC OPERATION

Up to two microphones can be connected in a dual differential configuration. This is suitable for stereo microphone or noise cancellation applications. Mic1 is connected between the MIC2A and MICCM inputs and mic2 is connected between the MIC2B and MICCM inputs as shown in Figure 13. Additionally, another microphone can be supported on MIC1 selected through the MPA input mux. Note that the microphones can be connected in a single-ended configuration.

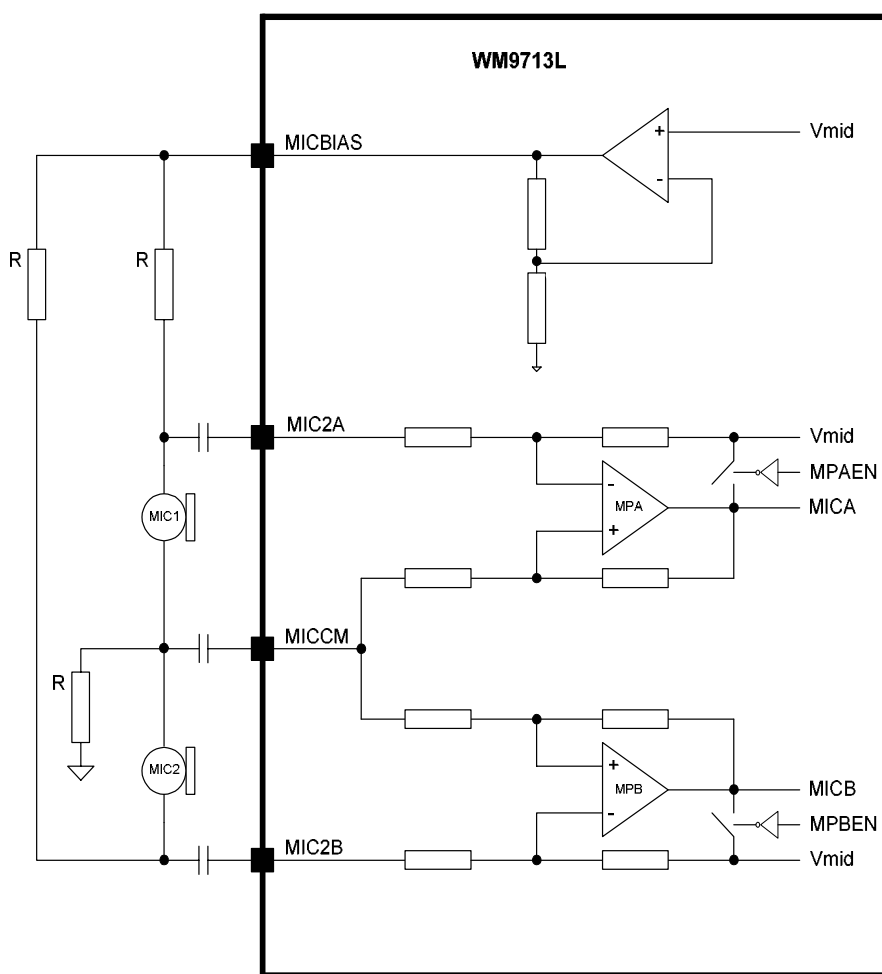


Figure 13 Dual Microphone Configuration

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via MBVOL in register 22h. When MBVOL=0, MICBIAS=0.9*AVDD and when MBVOL=1, MICBIAS=0.75*AVDD.

The microphone bias is driven to a dedicated MICBIAS pin 28 and is enabled by MPOP1EN in register 22h. It can also be configured to drive out on GPIO8 pin 12 enabled by MPOP2EN in register 22h.

When not in use the microphone bias can be powered down using the Powerdown register bit MICBIAS (register 3Eh, bit 14).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|---------|---------|--|
| 22h | 7 | MBOP2EN | 0 (Off) | Microphone bias enable to GPIO8 (pin 12) |
| | 6 | MBOP1EN | 1 (On) | Microphone bias enable to MICBIAS (pin 28) |
| | 5 | MBVOL | 0 | Microphone bias voltage control 0: 0.9 * AVDD 1: 0.75 * AVDD |

Table 24 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 14. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

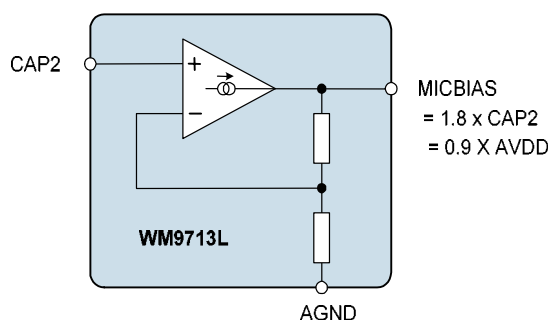


Figure 14 Microphone Bias Schematic

MICBIAS CURRENT DETECT

The WM9713L includes a microphone bias current detect circuit with programmable thresholds for the microphone bias current, above which an interrupt will be triggered. There are two separate interrupt bits, MICDET to e.g. distinguish between one or two microphones connected to the WM9713L, and MICSHT to detect a shorted microphone (mic button press). The microphone current detect threshold is set by MCDTHR[2:0], for MICDET, and MCDSCTHR[1:0] for MICSHT. Thresholds for each code are shown in Table 25

When not in use the microphone bias current detect circuit can be powered down using the Powerdown register bit MCD (register 3Eh, bit 15).

See the GPIO and Interrupt Controller sections for details on the interrupt and status readback for these MICBIAS current detection features.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|--------|---------|---|
| 22h | 4:2 | MCDTHR | 000 | Mic current detect threshold 000:100uA 001:200uA ... 100uA steps up to 111:800uA These values are for 3.3V supply and scale with supply voltage (AVDD). |
| | 1:0 | MCDSTR | 00 | Mic current detect short circuit threshold 00: 600uA 01: 1200uA 10: 1800uA 11: 2400uA These values are for 3.3V supply and scale with supply voltage (AVDD). |

Table 25 Microphone Current Detect Control

MICROPHONE PGAS

The microphone pre-amps MPA and MPB drive into two microphone PGAs whose gain is controlled by register 0Eh. The PGA signals can be routed into the headphone mixers and the mono mixer, but not the speaker mixer (to prevent forming a feedback loop) controlled by register 10h. When the PGA signals are not selected as an input to any of the mixers the outputs of the PGAs are muted automatically.

When not in use the microphone PGAs can be powered down using the Powerdown register bits MA and MB (register 3Eh, bits [3:2]).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------------|------|---------|----------------|--|
| 0Eh Mic PGA Volume | 12:8 | MICAVOL | 01000 (0dB) | MICA input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |
| | 4:0 | MICBVOL | 01000 (0dB) | MICB input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |

Table 26 Microphone PGA Volume Control

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------|-----|----------|--------------|---|
| 10h MIC Routing | 7 | MA2M | 1 | Mute MICA path to mono mixer 1: Mute, 0: No mute (ON) |
| | 6 | MB2M | 1 | Mute MICB path to mono mixer 1: Mute, 0: No mute (ON) |
| | 5 | MIC2MBST | 0 | Mic to mono mixer boost 0: 0dB, 1: +20dB |
| | 4:3 | MIC2H | 11 | Mic to headphone mixers select 00: Stereo (MICA to HPL, MICB to HPR) 01: MICA only (MICA to HPL and HPR) 10: MICB only (MICB to HPL and HPR) 11: none (mutes microphone PGAs) |
| | 2:0 | MIC2HVOL | 010 (0dB) | Mic PGA to headphone mixers gain 000: +6dB ... (3dB steps) 111: -15dB |

Table 27 Microphone PGA Routing Control

MONOIN INPUT

Pin 20 (MONOIN) is a mono input designed to connect to the receive path of a telephony device. The pin connects directly to the record selector for phone call recording (Note: to record both sides of a phone call, one ADC channel should record the MONOIN signal while the other channel records the MIC signal). The record PGA adjusts the recording volume, and is controlled by register 12h or by the ALC function (see "Record Gain" and "Automatic Level Control" sections).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------------|-------|--------|-----------|---|
| 14h Record Routing | 15:14 | R2H | 11 (mute) | Controls record mux to headphone mixer paths. 00=stereo 01=left rec mux only 10=right rec mux only 11=mute left and right |
| | 13:11 | R2HVOL | 010 (0dB) | Controls gain of record mux l/r to headphone mixer paths 000: +6dB ... (3dB steps) 111: -15dB |
| | 10:9 | R2M | 11 (mute) | Controls record mux to mono mixer path. 00=stereo 01=left rec mux only 10=right rec mux only 11=mute left and right |
| | 8 | R2MBST | 0 (OFF) | Enables 20dB gain boost for record mux to mono mixer path |

Table 28 Record PGA Routing Control

To listen to the MONOIN signal, the signal passes through a separate PGA, controlled by register 08h. The signal can be routed into the headphone mixer (for normal phone call operation) and/or the speaker mixer (for speakerphone operation), but not into the mono mixer (to prevent forming a feedback loop). When the signal is not selected as an input to any of the mixers the output of the PGA is muted automatically.

When not in use the MONOIN PGA can be powered down using the Powerdown register bit MOIN (register 3Eh, bit 4).

MONOIN is biased internally to the reference voltage VREF. Whenever the input is muted or the device placed into standby mode, the input remains biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------------|------|---------------|----------------|--|
| 08h MONOIN PGA Vol / Routing | 15 | M2H | 1 | Mute MONIN path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | M2S | 1 | Mute MONOIN path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 12:8 | MONOIN VOL | 01000 (0dB) | MONOIN input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |

Table 29 Mono PGA Control

PCBEEP INPUT

Pin 19 (PCBEEP) is a mono, line level input intended for externally generated signal or warning tones. It is routed directly to the record selector and all three output mixers, without an input amplifier. The signal gain into each mixer can be independently controlled, with a separate mute bit for each signal path.

PCBEEP is biased internally to the reference voltage VREF. When the signal is not selected as an input to any of the mixers the input remains biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------|-------|--------|--------------|--|
| 16h PCBEEP input | 15 | B2H | 1 | Mute PCBEEP path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14:12 | B2HVOL | 010 (0dB) | PCBEEP to headphone mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 11 | B2S | 1 | Mute PCBEEP path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 10:8 | B2SVOL | 010 (0dB) | PCBEEP to speaker mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 7 | B2M | 1 | Mute PCBEEP path to mono mixer 1: Mute, 0: No mute (ON) |
| | 6:4 | B2MVOL | 010 (0dB) | PCBEEP to mono mixer gain 000: +6dB ... (3dB steps) 111: -15dB |

Table 30 PCBEEP Control

DIFFERENTIAL MONO INPUT

PCBEEP and MONOIN inputs can be configured to provide a differential mono input. This is achieved by mixing the two inputs together using the headphone mixers or the speaker mixer. Note that the gain of the MONOIN PGA must match the gain of the PCBEEP mixer input to achieve a balanced differential mono input.

AUDIO MIXERS

MIXER OVERVIEW

The WM9713L has four separate low-power audio mixers to cover all audio functions required by smartphones, PDAs and handheld computers. These mixers are used to drive the audio outputs HPL, HPR, MONO, SPKL, SPKR, OUT3 and OUT4. There are also two inverters used to provide differential output signals (e.g. for driving BTL loads)

HEADPHONE MIXERS

There are two headphone mixers, headphone mixer left and headphone mixer right (HPMIXL and HPMIXR). These mixers are the stereo output driver source. They are used to drive the stereo outputs HPL and HPR. They can also be used to drive SPKL and SPKR outputs and, when used in conjunction with OUT3 and OUT4, they can be configured to drive complementary signals through the two output inverters to support bridge-tied load (BTL) stereo loudspeaker outputs. The following signals can be mixed into the headphone path:

- MONOIN (controlled by register 08h, see "Audio Inputs")
- LINEL/R (controlled by register 0Ah, see "Audio Inputs")
- the output of the Record PGA (controlled by register 14h, see "Audio ADC", "Record Gain")
- the stereo DAC signal (controlled by register 0Ch, see "Audio DACs")
- the MIC signal (controlled by register 10h, see "Audio Inputs")
- PC_BEEP (controlled by register 16h, see "Audio Inputs")
- the VXDAC signal (controlled by register 18h, see "Audio DACs")
- the AUXDAC signal (controlled by register 1Ah, see "Auxiliary DAC")

In a typical smartphone application, the headphone signal is a mix of MONOIN / VXDAC and sidetone (for phone calls) and the stereo DAC signal (for music playback).

When not in use the headphone mixers can be powered down using the Powerdown register bits HPLX and HPRX (register 3Ch, bits [3:2]).

SPEAKER MIXER

The speaker mixer (SPKMIX) is a mono source. It is typically used to drive a mono loudspeaker in BTL configuration. The following signals can be mixed into the speaker path:

- MONOIN (controlled by register 08h, see "Audio Inputs")
- LINEL/R (controlled by register 0Ah, see "Audio Inputs")
- the stereo DAC signal (controlled by register 0Ch, see "Audio DACs")
- PC_BEEP (controlled by register 16h, see "Audio Inputs")
- the VXDAC signal (controlled by register 18h, see "Audio DACs")
- the AUXDAC signal (controlled by register 1Ah, see "Auxiliary DAC")

In a typical smartphone application, the speaker signal is a mix of AUXDAC (for system alerts or ring tone playback), MONOIN / VXDAC (for speakerphone function), and PC_BEEP (for externally generated ring tones).

Note that when selected the stereo input pairs LINEL/R and DACL/R are summed and attenuated by -6dB so that 0dBFS signals on each channel sum to give a 0dBFS mono signal.

When not in use the speaker mixer can be powered down using the Powerdown register bit SPKX (register 3Ch, bit 1).

MONO MIXER

The mono mixer drives the MONO pin. The following signals can be mixed into MONO:

- LINEL/R (controlled by register 0Ah, see "Audio Inputs")
- the output of the Record PGA (controlled by register 14h, see "Audio ADC", "Record Gain")
- the stereo DAC signal (controlled by register 0Ch, see "Audio DACs")
- the MIC signal (controlled by register 10h, see "Audio Inputs")
- PC_BEEP (controlled by register 16h, see "Audio Inputs")
- the VXDAC signal (controlled by register 18h, see "Audio DACs")
- the AUXDAC signal (controlled by register 12h, see "Auxiliary DAC")

In a typical smartphone application, the MONO signal is a mix of the amplified microphone signal (possibly with Automatic Gain Control) and (if enabled) an audio playback signal from the stereo DAC or the auxiliary DAC.

Note that when selected the stereo input pairs LINEL/R and DACL/R are summed and attenuated by -6dB so that 0dBFS signals on each channel sum to give a 0dBFS mono signal.

When not in use the mono mixer can be powered down using the Powerdown register bit MX (register 3Ch, bit 0).

MIXER OUTPUT INVERTERS

There are two general purpose mixer output inverters, INV1 and INV2. Each inverter can be selected to drive HPMIXL, HPMIXR, SPKMIX, MONOMIX or $\{ (\text{HPMIXL} + \text{HPMIXR}) / 2 \}$. The outputs of the inverters can be used to generate complimentary signals (to drive BTL configured loads) and to provide greater flexibility in output driver configurations. INV1 can be selected as the source for SPKL, MONO and OUT3 and INV2 as the source for SPKR and OUT4.

The input source for each inverter is selected using INV1[2:0] and INV2[2:0] in register 1Eh (see Table 31). When no input is selected the inverter is powered down.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|-------|-----------|---|
| 1Eh | 15:13 | INV1 | 000 (OFF) | INV1 source select 000: Z _H (OFF – no source selected) 001: MONOMIX 010: SPKMIX 011: HPMIXL 100: HPMIXR 101: HPMIXMONO 110: unused 111: Vmid |
| | 12:10 | INV2 | 000 (OFF) | INV2 source select Same as INV1 |

Table 31 Mixer Inverter Source Select

ANALOGUE AUDIO OUTPUTS

The following sections give an overview of the analogue audio output pins. The WM9713L has three outputs capable of driving loads down to 16Ω (headphone / line drivers) – HPL, HPR and MONO - and four outputs capable of driving loads down to 8Ω (loudspeaker / line drivers) – SPKL, SPKR, OUT3 and OUT4. The combination of output drivers, mixers and mixer inverters means that many output configurations can be supported.

For examples of typical output and mixer configurations please refer to the “Typical Output Configurations” section. For more information on recommended external components, please refer to the “Applications Information” section.

Each output is driven by a PGA with a gain range of 0dB to -46.5dB in -1.5dB steps. Each PGA has an input source mux, mute and zero-cross detect circuit (delaying gain changes until a zero-cross is detected, or after time-out).

HEADPHONE OUTPUTS – HPL AND HPR

The HPL and HPR outputs (pins 39 and 41) are designed to drive a 16Ω or 32Ω headphone load. They can also be used as line outputs. They can be used in and AC coupled or DC coupled (capless) configuration. The available input sources are HPMIXL/R and Vmid (see Table 32).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------|-----|-------|-----------|---|
| 1Ch Output PGA Mux Select | 7:6 | HPL | 00 (Vmid) | HPL input source select 00: Vmid 01: no input (tri-stated if HPL=1 in register 3Eh) 10: HPMIXL 11: unused |
| | 5:4 | HPR | 00 (Vmid) | HPR input source select 00: Vmid 01: no input (tri-stated if HPR=1 in register 3Eh) 10: HPMIXR 11: unused |

Table 32 HPL / HPR PGA Input Source

The signal volume on HPL and HPR can be independently adjusted under software control by writing to register 04h.

When not in use HPL and HPR can be powered down using the Powerdown register bits HPL and HPR (register 3Eh, bits [10:9]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|----------------------------|------|--------|-----------------|--|
| 04h Headphone Volume | 15 | MUL | 1 (Mute) | Mute HPL 1: Mute (OFF) 0: No Mute (ON) |
| | 14 | ZCL | 0 | Left zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 13:8 | HPLVOL | 000000 (0dB) | HPL Volume 000000: 0dB (maximum) 000001: -1.5dB ... (1.5dB steps) 011111: -46.5dB 1xxxxx: -46.5dB |
| | 7 | MUR | 1 (Mute) | Mute HPR 1: Mute (OFF) 0: No Mute (ON) |
| | 6 | ZCR | 0 | Right zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 5:0 | HPRVOL | 000000 (0dB) | HPR Volume Similar to HPLVOL |

Table 33 HPL / HPR PGA Control

MONO OUTPUT

The MONO output (pin 31) is designed to drive a 16Ω headphone load and can also be used as a line output. The available input sources are MONOMIX, INV1 and Vmid (see Table 34)

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-------|-------|-----------|---|
| 1Ch Output PGA Mux Select | 15:14 | MONO | 00 (Vmid) | MONO input source select 00: Vmid 01: no input (tri-stated if MONO=1 in register 3Eh) 10: MONOMIX 11: INV1 |

Table 34 MONO PGA Input Source

The signal volume on MONO can be independently adjusted under software control by writing to register 08h.

When not in use MONO can be powered down using the Powerdown register bit MONO (register 3Eh, bit 13). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|---------|-----------------|--|
| 08h MONO Vol | 7 | MU | 1 (Mute) | Mute MONO 1: Mute (OFF) 0: No Mute (ON) |
| | 6 | ZC | 0 | Right zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 5:0 | MONOVOL | 000000 (0dB) | MONO Volume 000000: 0dB (maximum) 000001: -1.5dB ... (1.5dB steps) 011111: -46.5dB 1xxxxx: -46.5dB |

Table 35 Mono PGA Control

SPEAKER OUTPUTS – SPKL AND SPKR

The SPKL and SPKR (pins 35 and 36) are designed to drive a loudspeaker load down to 8Ω and can also be used as line outputs and headphone outputs. They are designed to drive an 8Ω load AC coupled or in a BTL (capless) configuration. The available input sources are HPMIXL/R, SPKMIXL/R, INV1/2 and Vmid (see Table 36).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-------|-------|---------------|--|
| 1Ch Output PGA Mux Select | 13:11 | SPKL | 000 (Vmid) | SPKL input source select 000: Vmid 001: no input (tri-stated if SPKL=1 in register 3Eh) 010: HPMIXL 011: SPKMIX 100: INV1 101-111: unused |
| | 10:8 | SPKR | 000 (Vmid) | SPKR input source select 000: Vmid 001: no input (tri-stated if SPKR=1 in register 3Eh) 010: HPMIXR 011: SPKMIX 100: INV2 101-111: unused |

Table 36 SPKL / SPKR PGA Input Source

The signal volume on SPKL and SPKR can be independently adjusted under software control by writing to register 02h.

When not in use SPKL and SPKR can be powered down using the Powerdown register bits SPKL and SPKR (register 3Eh, bits [8:7]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------------|------|---------|-----------------|--|
| 02h Speaker Volume | 15 | MUL | 1 (Mute) | Mute SPKL 1: Mute (OFF) 0: No Mute (ON) |
| | 14 | ZCL | 0 | Left zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 13:8 | SPKLVOL | 000000 (0dB) | SPKL Volume 000000: 0dB (maximum) 000001: -1.5dB ... (1.5dB steps) 011111: -46.5dB 1xxxxx: -46.5dB |
| | 7 | MUR | 1 (Mute) | Mute SPKR 1: Mute (OFF) 0: No Mute (ON) |
| | 6 | ZCR | 0 | Right zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 5:0 | SPKRVOL | 000000 (0dB) | SPKR Volume Similar to SPKLVOL |

Table 37 SPKL / SPKR PGA Control

Note:

- For BTL speaker drive, it is recommended that both PGAs have the same gain setting.

AUXILIARY OUTPUTS – OUT3 AND OUT4

The OUT3 and OUT4 outputs (pins 37 and 33) are designed to drive a loudspeaker load down to 8Ω and can also be used as line outputs and headphone outputs. They are designed to drive an 8Ω load AC coupled or in a BTL (capless) configuration and can be used as a midrail buffer to drive the headphone outputs in a capless DC configuration. The available input sources are INV1/2 and Vmid (see Table 38).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-----|-------|-----------|--|
| 1Ch Output PGA Mux Select | 3:2 | OUT3 | 00 (Vmid) | OUT3 input source select 00: Vmid 01: no i/p (Z _n if buffer disabled) 10: INV1 11: unused |
| | 1:0 | OUT4 | 00 (Vmid) | OUT4 input source select 00: Vmid 01: no i/p (Z _n if buffer disabled) 10: INV2 11: unused |

Table 38 OUT3 / OUT4 PGA Input Source

The signal volume on OUT3 and OUT4 can be independently adjusted under software control by writing to register 06h.

When not in use OUT3 and OUT4 can be powered down using the Powerdown register bits OUT3 and OUT4 (register 3Eh, bits [11:12]). To minimise pops and clicks when the PGA is powered down / up it is recommended that the Vmid input is selected during the power down / up cycle. This ensures the same DC level is maintained on the output pin throughout.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------------|------|---------|-----------------|---|
| 06h Speaker Volume | 15 | MU4 | 1 (Mute) | Mute OUT4 1: Mute (OFF) 0: No Mute (ON) |
| | 14 | ZC4 | 0 | OUT4 zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 13:8 | OUT4VOL | 000000 (0dB) | OUT4 Volume 000000: 0dB (maximum) 000001: -1.5dB ... (1.5dB steps) 011111: -46.5dB 1xxxxx: -46.5dB |
| | 7 | MU3 | 1 (Mute) | Mute OUT3 1: Mute (OFF) 0: No Mute (ON) |
| | 6 | ZC3 | 0 | OUT3 zero cross enable 0: Change gain immediately 1: Change gain only on zero crossings, or after time-out |
| | 5:0 | OUT3VOL | 000000 (0dB) | OUT3 Volume Similar to OUT4VOL |

Table 39 OUT3 / OUT4 PGA Control

THERMAL SENSOR

The speaker and headphone outputs can drive very large currents. To protect the WM9713L from becoming too hot, a thermal sensor has been built in. If the chip temperature reaches approximately 150°C, and the TI bit is set, the WM9713L deasserts GPIO bit 11 in register 54h, a virtual GPIO that can be set up to generate an interrupt to the CPU (see "GPIO and Interrupt Control" section).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|---|
| 3Ch | 13 | TSHUT | 1 | Power down thermal sensor 0: Enabled 1: Disabled |
| 54h | 11 | TI | 0 | Thermal sensor (virtual GPIO) 1: Temperature below 150°C 0: Temperature above 150°C See also "GPIO and Interrupt Control" section. |

Table 40 Thermal Cutout Control

JACK INSERTION AND AUTO-SWITCHING

In a phone application, a BTL ear speaker may be connected across MONO and HPL, a stereo headphone on HPL and HPR and stereo speakers on SPKL, SPKR, OUT3 and OUT4 (see Figure 15). Typically, only one of these three output devices is used at any given time: when no headphone is plugged in, the BTL ear speaker or stereo speakers are active, otherwise the headphone is used.

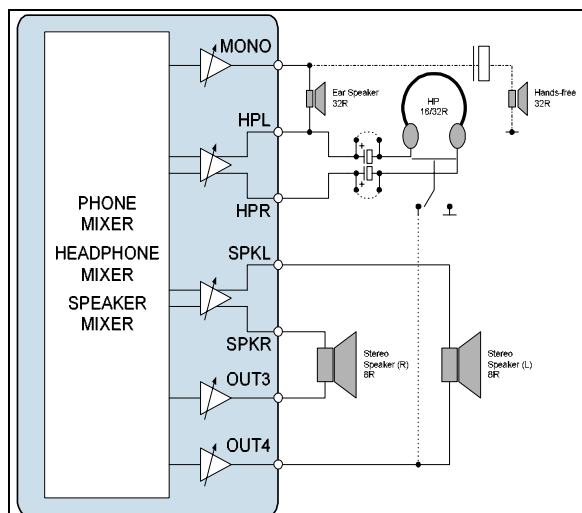


Figure 15 Typical Output Configuration

The presence of a headphone can be detected using one of GPIO1/6/7/8 (pins 44, 3, 11 & 12) and an external pull-up resistor (see Figure 41, page 103 for a circuit diagram). When the jack is inserted, the GPIO is pulled low by a switch on the socket. When the jack is removed the GPIO is pulled high by a resistor. If the JIEN bit is set, the WM9713L automatically switches between headphone and any other output configuration, typically ear speaker or stereo speaker that has been set up in the Powerdown and Output PGA Mux Select registers.

Note:

Please refer to WAN_0182 for further information on jack detect configuration.

In addition to the typical configuration explained above, the WM9713L can also support automatic switching between the following three configurations set as BTL ear speaker and headphone.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-----------|---------|---|
| 24h Output Volume Mapping (Jack Insert) | 1:0 | EARSPKSEL | 00 | 00: Default, no ear speaker configuration selected. 01: MONO and HPL driver selected as BTL ear speaker. 10: OUT3 and HPL driver selected as BTL ear speaker. 11: OUT4 and HPL driver selected as BTL ear speaker. |

Table 41 Ear Speaker Configuration

For example if OUT4 and HPL is selected as the BTL ear speaker, the user should select EARSPKSEL = 3h, then OUT4 is tri-stated on jack insert to prevent sound across the ear speaker during headphone operation and HPL volume is set to OUT4 volume on jack out to ensure correct ear speaker operation. It should be noted that all other outputs except HPL, HPR and selected ear speaker driver are disabled and internally connected to VREF on jack insert. This maintains VREF at those outputs and helps prevent pops when the outputs are enabled.

Finally if the user wishes to DC couple the headphone outputs the user needs to select between OUT3 and OUT4 as the mid-rail output buffer driver. The selected mid-rail output buffer is enabled on jack insert. On jack out it defaults to whatever configuration has been set up in the Powerdown and Output PGA Mux Select registers.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|----------|---------|--|
| 24h Output Volume Mapping (Jack Insert) | 3:2 | DCDRVSEL | 00 | 00: Default, AC coupled headphone. 01: OUT4 as mid-rail output buffer. 11: OUT3 as mid-rail output buffer. |

Table 42 DC Coupled Headphone Configuration

In summary:

JIEN not set: Outputs work as normal as selected in the Powerdown and Output PGA Mux Select registers.

JIEN set: On jack insert GPIO1/6/7/8 is pulled low, HPL and HPR are enabled, DCDRVSEL decides if the headphones are DC or AC coupled and configures OUT3 or OUT4 to suit, EARSPKSEL decides if MONO, OUT3 or OUT4 need to be tri-stated to ensure no sound out on the ear-speaker and finally all other outputs are disabled as explained above to prevent pops on re-enabling.

On jack out GPIO1/6/7/8 is pulled high, the outputs work as normal as selected in the Powerdown and Output PGA Mux Select registers except that HPL Volume is controlled by EARSPKSEL to ensure correct ear speaker operation.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|-----|-------|------------|--|
| 24h Output Volume Mapping (Jack Insert) | 4 | JIEN | 0 (OFF) | Jack Insert Enable – Takes output of GPIO1 logic |
| 5Ah Additional Functions (1) | 7:6 | JSEL | 00 (GPIO1) | GPIO select for jack insert detection: 00: GPIO1 01: GPIO6 10: GPIO7 11: GPIO8 |

Table 43 Jack Insertion / Auto-Switching (1)

| J1EN | EARSSEL | DCDRSEL | GPIO1 | MODE DESCRIPTION | HPL STATE | HPL VOLUME | HPR STATE | HPR VOLUME | MONO STATE | OUT3 STATE | OUT4 STATE | SPKL STATE | SPKR STATE |
|------|---------|---------|-------|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| 0 | XX | XX | X | Jack Insert Detection Disabled. | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |
| 1 | 00 | 00 | 0 | Jack Insert Detection Enabled. Headphone plugged in. No Ear Speaker Selected. AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | HZ | HZ | HZ | HZ |
| 1 | 01 | 00 | 0 | Jack Insert Detection Enabled. Headphone plugged in. MONO Ear Speaker Selected. AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | Tri-States | HZ | HZ | HZ | HZ |
| 1 | 10 | 00 | 0 | Jack Insert Detection Enabled. Headphone plugged in. OUT3 Ear Speaker Selected. AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | Tri-States | HZ | HZ | HZ |
| 1 | 11 | 00 | 0 | Jack Insert Detection Enabled. Headphone plugged in. OUT4 Ear Speaker Selected. AC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | HZ | Tri-States | HZ | HZ |
| 1 | 11 | 01 | 0 | Jack Insert Detection Enabled. Headphone plugged in. OUT4 Ear Speaker Selected. OUT3 DC Coupled Headphone Selected. | Enabled | HPL Volume | Enabled | HPR Volume | HZ | VMID | Tri-States | HZ | HZ |
| 1 | 00 | XX | 1 | Jack Insert Detection Enabled. Headphone plugged out. No Ear Speaker Selected. | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |
| 1 | 11 | XX | 1 | Jack Insert Detection Enabled. Headphone plugged out. OUT4 Ear Speaker Selected. | User Controlled | OUT4 Volume | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled | User Controlled |

Table 44 Jack Insertion / Auto-Switching (2)

DIGITAL AUDIO (SPDIF) OUTPUT

The WM9713L supports the SPDIF standard. Pins 48 & 12 can be used to output the SPDIF data. Note that pins 48 & 12 can also be used as GPIO pins. The GE5 & GE8 bits (register 56h, bit 5 & bit 8) select between GPIO and SPDIF functionality for pins 48 & 12 respectively (see "GPIO and Interrupt control" section).

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With the exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit in register 2Ah is '0'). Once the desired values have been written to this register, the contents should be read back to ensure that the sample rate in particular is supported, then SPDIF validity bit SPCV in register 2Ah should be read to ensure the desired configuration is valid. Only then should the SPDIF enable bit in register 2Ah be set. This ensures that control and status information start up correctly at the beginning of SPDIF transmission.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------------------------|-------|-------|---------|--|
| 2Ah Extended Audio | 10 | SPCV | 0 | SPDIF validity bit (read-only) |
| | 5:4 | SPSA | 01 | SPDIF slot assignment (ADCO = 0) 00: Slots 3, 4 01: Slots 6, 9 10: Slots 7, 8 11: Slots 10, 11 |
| | 2 | SEN | 0 | SPDIF output enable 1 = enabled, 0 = disabled |
| 3Ah SPDIF Control Register | 15 | V | 0 | Validity bit; '0' indicates frame valid, '1' indicates frame not valid |
| | 14 | DRS | 0 | Indicates that the WM9713L does not support double rate SPDIF output (read-only) |
| | 13:12 | SPSR | 10 | Indicates that the WM9713L only supports 48kHz sampling on the SPDIF output (read-only) |
| | 11 | L | 0 | Generation level; programmed as required by user |
| | 10:4 | CC | 0000000 | Category code; programmed as required by user |
| | 3 | PRE | 0 | Pre-emphasis; '0' indicates no pre-emphasis, '1' indicates 50/15us pre-emphasis |
| | 2 | COPY | 0 | Copyright; '0' indicates copyright is not asserted, '1' indicates copyright |
| | 1 | AUDIB | 0 | Non-audio; '0' indicates data is PCM, '1' indicates non-PCM format (e.g. DD or DTS) |
| | 0 | PRO | 0 | Professional; '0' indicates consumer, '1' indicates professional |
| 5Ch Additional Function Control | 4 | ADCO | 0 | Source of SPDIF data 0: SPDIF data comes from SDATAOUT (pin 5), slot selected by SPSA 1: SPDIF data comes from audio ADC |

Table 45 SPDIF Output Control

TOUCHPANEL INTERFACE

The WM9713L includes a touchpanel driver and digitiser circuit for use with 4-wire or 5-wire resistive touchpanels. The following functions are implemented:

X co-ordinate measurement

Y co-ordinate measurement

Pen down detection, with programmable sensitivity

Touch pressure measurement (4-wire touchpanel only)

Auxiliary measurement from COMP1/AUX1 (pin 29), COMP2/AUX2 (pin 30), or WIPER/AUX4 (pin 12)

The touchpanel digitiser uses a very low power, 12-bit successive approximation type ADC. The same ADC can also be used for battery and auxiliary measurements (see the "Battery Alarm and Battery Measurement" and "Auxiliary ADC Inputs" sections).

An on-chip switch matrix connects each touchpanel terminal to the supply voltage TPVDD, to ground (TPGND), or to the ADC input, as required.

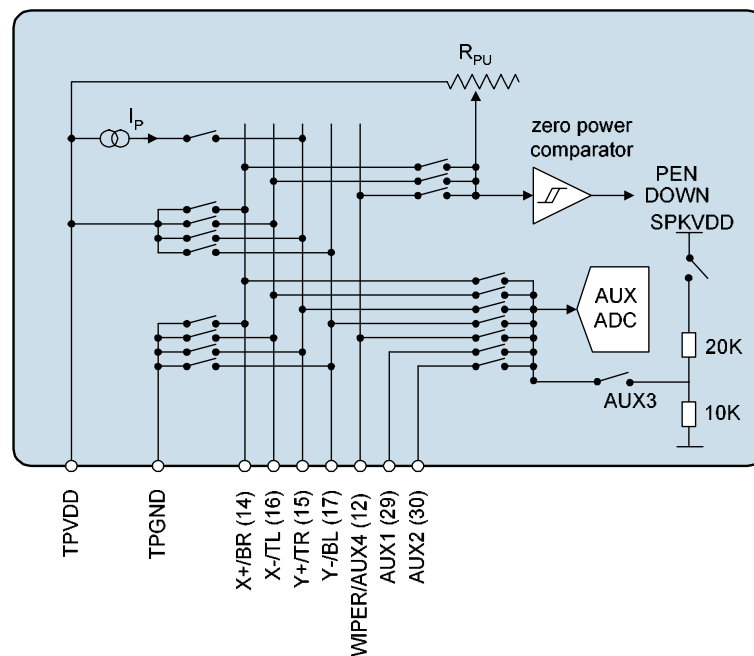


Figure 16 Touchpanel Switch Matrix

PRINCIPLE OF OPERATION - FOUR-WIRE TOUCHPANEL

Four-wire touchpanels are connected to the WM9713L as follows:

- Right side contact = X+ (pin 14)
- Left side contact = X- (pin 16)
- Top side contact = Y+ (pin 15)
- Bottom side contact = Y- (pin 17)

The principle of operation is illustrated below (Note: the illustrations assume that the top plate is used for X and the bottom plate for Y measurements, although the reverse is also possible).

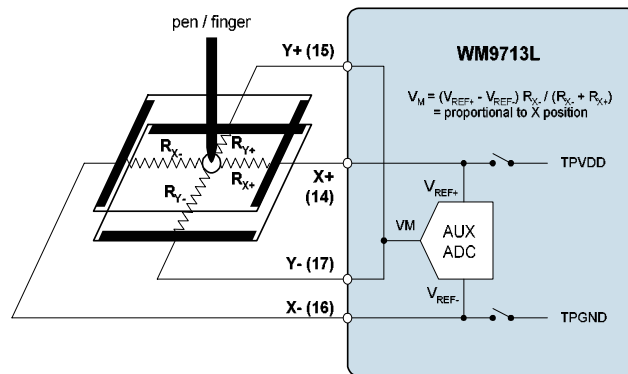


Figure 17 X Co-ordinate Measurement on 4-wire Touchpanel

For an X co-ordinate measurement, the X+ pin is internally switched to TPVDD and X- to TPGND. The X plate becomes a potential divider, and the voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the Y+ and Y- pins, which carry no current (hence there is no voltage drop in R_{Y+} or R_{Y-}).

Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement.

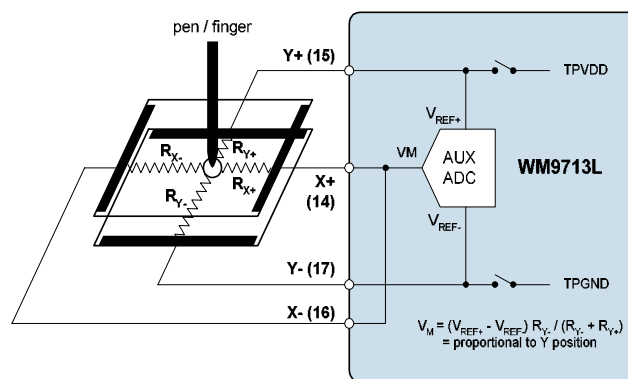


Figure 18 Y Co-ordinate Measurement on 4-wire Touchpanel

Y co-ordinate measurements are similar to X co-ordinate measurements, with the X and Y plates interchanged.

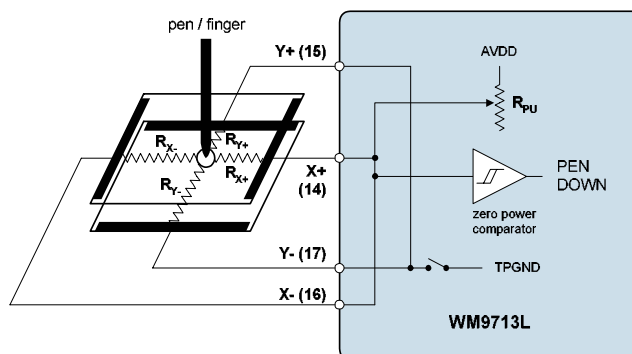


Figure 19 Pen Down Detection on 4-wire Touchpanel

Pen down detection uses a zero power comparator (effectively a CMOS logic gate) with an internal, programmable pull-up resistor R_{PU} that controls pen-down sensitivity. Increasing R_{PU} makes the touchpanel less sensitive to touch, while lowering R_{PU} makes it more sensitive.

When the touchpanel is not being touched, no current flows in the circuit, and the PENDOWN signal is low. When the panel is touched with a pen or finger, current flows through R_{PU} and the panel, and the comparator output goes high.

The PENDOWN signal can be read from bit 15 in register 7Ah (labeled PNDN). It can also be observed on pin 46 (GPIO3 / PENDOWN), if the pin is not used for GPIO (GE3=0). Additionally, PENDOWN is passed to the GPIO logic block (register 54h, bit 13), where it can generate CPU interrupts, and / or to wake up the WM9713L from sleep mode (see “GPIO and Interrupt Control” section).

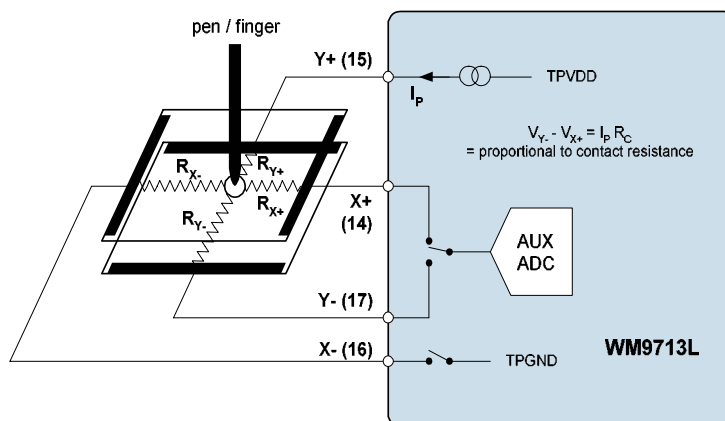


Figure 20 Touch Pressure Measurement on 4-wire Touchpanel

Touch pressure can be determined indirectly by measuring the contact resistance R_C between the top and bottom plates. R_C decreases as the touch pressure on the panel increases. The WM9713L measures R_C by sending a constant current I_P through the touchpanel and measuring the potential on each plate. The two values are subtracted in the digital domain to obtain the potential difference, which is proportional to R_C .

To suit different types of touchpanels, the magnitude of I_P can be set to either 400 μ A or 200 μ A using the PIL control bit.

PRINCIPLE OF OPERATION - FIVE-WIRE TOUCHPANEL

Five-wire touchpanels are connected to the WM9713L as follows:

- Top sheet contact = WIPER/AUX4 (pin 12)
- Top left corner of bottom sheet = TL (pin 16)
- Top right corner of bottom sheet = TR (pin 15)
- Bottom left corner of bottom sheet = BL (pin 17)
- Bottom right corner of bottom sheet = BR (pin 14)

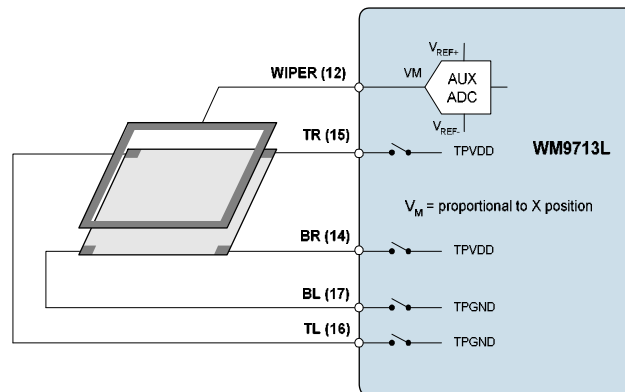


Figure 21 X Co-ordinate Measurement on 5-wire Touchpanel

For an X co-ordinate measurement, the top left and bottom left corners of the touchpanel are grounded internally to the WM9713L, while the top right and bottom right contacts are connected to TPVDD. The bottom plate becomes a potential divider with a voltage gradient in the X direction. The voltage at the point of contact is proportional to its X co-ordinate. This voltage is measured on the WIPER pin and converted to a digital value by the ADC.

Due to the ratiometric measurement method, the supply voltage does not affect measurement accuracy. The voltage references VREF+ and VREF- are taken from after the matrix switches, so that any voltage drop in these switches has no effect on the ADC measurement.

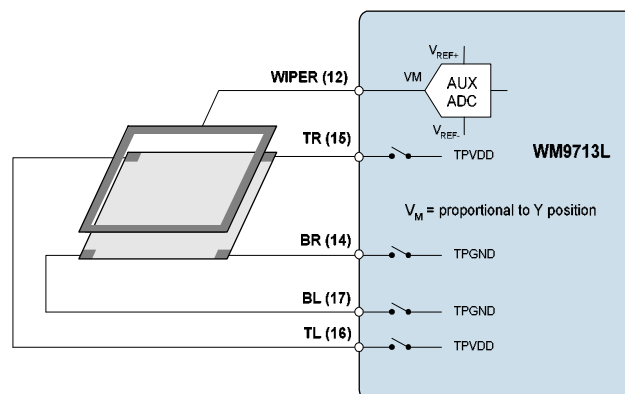


Figure 22 Y Co-ordinate Measurement on 5-wire Touchpanel

Y co-ordinate measurements are similar to X co-ordinate measurements. However, the voltage gradient on the bottom plate is in the Y direction instead of the X direction. This is achieved by grounding the bottom left and bottom right corners of the touchpanel, and connecting the top left and top right contacts to TPVDD.

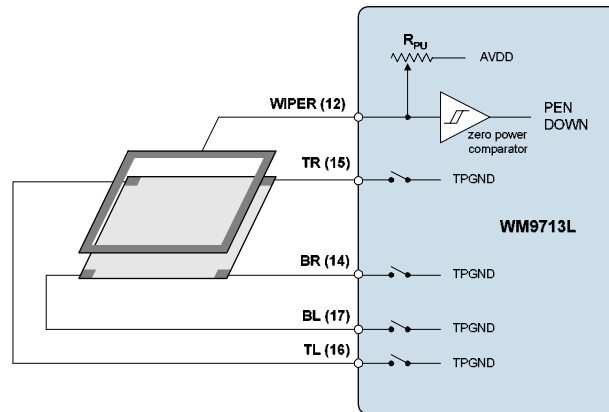


Figure 23 Pen Down Detection on 5-wire Touchpanel

Pen down detection works in a similar fashion for both 4-wire and 5-wire touchpanels (see Four-Wire Touchpanel Operation). On a 5-wire touchpanel, all four contacts of the bottom plate are grounded, and the top plate contact is connected to the internal programmable pull-up resistor, R_{PU} .

CONTROLLING THE TOUCHPANEL DIGITISER

All touchpanel functions are accessed and controlled through the AC-Link interface.

PHYSICAL CHARACTERISTICS

The physical characteristics of the touchpanel interface are controlled through register 78h, as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------------------------|--|
| 78h | 12 | 45W | 0 (4-wire) | Touchpanel Type Selection 0: 4-wire 1: 5-wire |
| | 8 | PIL | 0 (200 μ A) | Current used for pressure measurement 0: $I_P = 200\mu A$ 1: $I_P = 400\mu A$ |
| | 0:5 | RPU | 000001 (64k Ω) | Internal Pull-up resistor for Pen Detection 111111: 64k Ω /63 = 1.02k Ω (least sensitive) 111110: 64k Ω /62 = 1.03K Ω ... (pull-up = 64k Ω / binary value of RPU) 000010: 64k Ω /2 = 32K Ω 000001: 64k Ω /1 = 64k Ω (most sensitive) 000000: RESERVED (do not use this setting) |

Table 46 Touchpanel Digitiser Control (Physical Characteristics)

POWER MANAGEMENT

To save power, the touchpanel digitiser and the pen-down detector can be independently disabled when they are not used. The power consumption of the pen-down detector is normally negligible, except when the pen is down.

The pen ADC is powered-down using PADCPD, register 3Ch bit 15.

The state of the digitiser and pen down detector is controlled by the following bits.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|--------|---------|--|
| 3Ch | 15 | PADCPD | 1 = off | Pen ADC power down |
| 78h | 15:14 | PRP | 00 | Pen ADC/AUX ADC enable 00 – Pen digitiser off, pen detect off, no wake-up on pen down (default) 01 – Pen digitiser powered off, pen detect enabled, touchpanel digitiser wakes up (changes to state 11) on pen-down 10 – Pen digitiser off, pen detect enabled, no wake-up on pen down 11 – Pen digitiser and pen detect enabled |
| | 13 | RPR | 0 | Wake-up on pen-down mode 0: Wake-up the AC-Link only (hold SDATAIN high until controller sends warm reset or cold reset) 1: Wake-up the WM9713L without waiting for a reset signal from the controller |

Table 47 Touchpanel Digitiser Control (Power Management)

INITIATION OF MEASUREMENTS

The WM9713L touchpanel interface supports both polling routines and DMA (direct memory access) to control the flow of data from the touchpanel ADC to the host CPU.

In a polling routine, the CPU starts each measurement individually by writing to the POLL bit (register 74h, bit 9). This bit automatically resets itself when the measurement is completed.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|---|
| 74h | 9 | POLL | 0 | Writing "1" initiates a measurement. (when CTC is not set) |
| | 8 | CTC | 0 | 0: Polling mode 1: Continuous mode (for DMA) |
| 76h | 9:8 | CR | 00 | Continuous mode rate (DEL C1111) 00: 93.75 Hz (every 512 AC-Link frames) 01: 120 Hz (every 400 AC-Link frames) 10: 153.75 Hz (every 312 AC-Link frames) 11: 187.5Hz (every 256 AC-Link frames) Continuous mode "fast rate" (DEL = 1111) 00: 8 kHz (every six AC-Link frames) 01: 12 kHz (every four AC-Link frames) 10: 24 kHz (every other AC-Link frame) 11: 48 kHz (every AC-Link frame) NOTE: PENDIV bits in 44h [5:3] should be set to 111 in 48kHz mode to ensure that samples occur synchronously on the AC97 data channel |
| 78h | 11 | PDEN | 0 | 0: measure regardless of pen status 1: measure only when pen is down (when CTC=0 and POLL=1, measurement is delayed until pen-down; when CTC=1, measurements are stopped on pen-up) |
| | 10 | PDPOL | 0 | Sets polarity of PENDOWN flag: 0: non-inverted 1: inverted |

Table 48 Touchpanel Digitiser Control (Initiation of Measurements)

In continuous mode (CTC = 1), the WM9713L autonomously initiates measurements (or sets of measurements) at the rate set by CR, and supplies the measured data to the CPU on one of the unused AC'97 time slots. DMA-enabled CPUs can write the data directly into a FIFO without any intervention by the CPU core. This reduces CPU loading and speeds up the execution of user programs in handheld systems.

Note that the measurement frequency in continuous mode is also affected by the DEL bits (see "Touchpanel Settling Time"). The faster rates achieved when DEL = 1111 may be useful when the ADC is used for auxiliary measurements.

MEASUREMENT TYPES

The ADCSEL control bits determine which type of measurement is performed (see below).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-----------------|---|--|
| 74h | 9 | POLL | 0 | Writing "1" initiates a measurement. (when CTC is not set) |
| | 8 | CTC | 0 | 0: Polling mode 1: Continuous mode (for DMA) |
| | 7 | ADCSEL_AUX4 | 0 | Enable AUX4 measurement (pin 12) |
| | 6 | ADCSEL_AUX3 | 0 | Enable AUX3 measurement |
| | 5 | ADCSEL_AUX2 | 0 | Enable AUX2 measurement (pin 30) |
| | 4 | ADCSEL_AUX1 | 0 | Enable AUX1 measurement (pin 29) |
| | 3 | ADCSEL_PRESSURE | 0 | Enable touchpanel pressure measurement |
| | 2 | ADCSEL_Y | 0 | Enable touchpanel Y co-ord measurement |
| | 1 | ADCSEL_X | 0 | Enable touchpanel X co-ord measurement |
| 0 | COO | 0 | Enable co-ordinate mode 0: Single measurement. A single measurement is made depending on the setting of ADCSEL[7:1]. 1: Co-ordinate measurement. X, then Y, followed by an additional measurement indicated by ADCSEL[7:1]. If more than one ADCSEL[7:1] bit is selected then the third, additional, measurement will alternate sequentially between those selected. | |

Table 49 Touchpanel Digitiser Control (Measurement Types)

When COO is '0', the WM9713L performs a single measurement – either in polling mode or continuously, as indicated by the CTC bit. The type of measurement is specified by the ADCSEL[7:1] bits. If CTC=0 (polling mode) then only one of the ADCSEL[7:1] bits should be set.

If operating in continuous mode (CTC=1), then more than one ADCSEL[7:1] bit may be set and selected conversions will be performed cyclically in the following order => "X,Y,PRESSURE,AUX1,AUX2,AUX3,AUX4..."

The co-ordinate mode (COO = '1') makes it easier to obtain co-ordinate pairs rather than single co-ordinates. In polling-coordinate mode (CTC = '0', COO = '1'), the WM9713L performs an X co-ordinate, then a Y co-ordinate, followed by a single additional measurement determined by ADCSEL[7:1], then stops. In continuous-coordinate mode (CTC = '1', COO = '1'), the WM9713L continuously repeats a sequence consisting of an X-co-ordinate, Y co-ordinate, then an additional measurement determined by ADCSEL[7:1]. At least one of the ADCSEL bits must be set in continuous coordinate mode when CTC = COO = 1). Should more than one of the ADCSEL[7:1] bits be set during continuous co-ordinate mode then the additional measurement alternates for every set of three measurements. For example if ADCSEL_AUX1 and ADCSEL_AUX3 were both selected whilst CTC = '1', COO = '1' then the following sequence of conversions would be performed: "X,Y,AUX1,X,Y,AUX3,X,Y,AUX1,X,Y,AUX3..."

CONVERSION RATE

As stated previously the conversion rate is specified by the CR bits (reg 76h).

CR may be set to 93.75Hz (every 512 AC-Link Frames), 120Hz (every 400 AC-Link Frames), 153.75Hz (every 312 AC-Link frames) or 187.5Hz (every 256 AC-Link frames).

If only one ADRSEL[7:1] bit is set then each individual conversion occurs at the rate specified by CR.

If multiple ADRSEL[7:1] bits are set then the complete set of conversions requested is completed at the rate specified by CR.

DATA READBACK

This data is stored in register 7Ah, and can be retrieved by reading the register in the usual manner (see AC-Link Interface section). Additionally, the data can also be passed to the controller on one of the AC-Link time slots not used for audio functions.

The output data word of the touchpanel interface consists of three parts:

- Pen Status (1 bit) – this is also passed to the GPIO logic block, which can be programmed to generate an interrupt and/or wake up the WM9713L on pen down (see GPIO and Interrupt Control).
- Output data from the touchpanel ADC (12 bits)
- ADCSRC: 3 additional bits that indicate the source of the ADC data. In co-ordinate mode (COO = '1'), the WM9713L schedules different types of measurements autonomously and so these register bits may be required.

If the data is being read back using the polling method, there are several ways to determine when a measurement has finished:

- Reading back the POLL bit. If it has been reset to '0', then the measurement has finished.
- Monitoring the ADA signal, see GPIO and interrupt section. ADA goes high after every single conversion. If operating in co-ordinate mode (COO=1) then ADA goes high after every group of 3 conversions.
- Reading back 7Ah until the new data appears

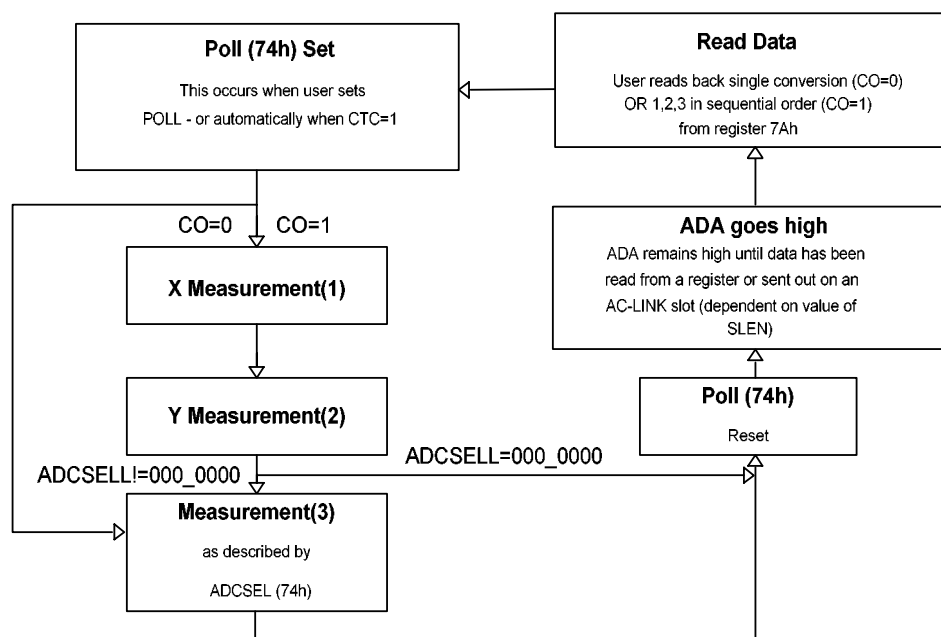
| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|-------|--------|---------|---|
| 7Ah or AC-Link slot selected by SLT | 15 | PNDN | 0 | Pen status (read-only) 0: Pen Up 1: Pen Down |
| | 14:12 | ADCSRC | 000 | Touchpanel ADC Source 000: No measurement 001: X co-ordinate measurement 010: Y co-ordinate measurement 011: Pressure measurement (4-wire only) 100: COMP1/AUX1 measurement (pin 29) 101: COMP2/AUX2 measurement (pin 30) 110: AUX3 measurement (SPKVDD pin) 111: WIPER/AUX4 measurement (pin 12) |
| | 11:0 | ADCD | 000h | Touchpanel ADC Data (read-only) Bit 11 = MSB Bit 0 = LSB |
| 78h | 9 | WAIT | 0 | 0: No effect (new ADC data overwrites unread data in register 7Ah) 1: New data is held back, and measurements delayed, until register 7Ah is read) |

Table 50 Touchpanel Digitiser Data

When operating in co-ordinate mode (COO=1) there will be 3 results to read back from each set of measurements – namely X,Y and the third additional measurement. After the co-ordinate set has finished the X result will be present in register 7Ah. Once this has been read back by the user the Y result will overwrite register 7Ah, as indicated by ADCSRC. Finally, after the Y result has been read back, the result of the third, additional, measurement will become present in 7Ah, again indicated by ADCSRC.

To avoid losing data that has not yet been read, the WM9713L can delay overwriting register 7Ah with new conversions until the old data has been read. This function is enabled using the WAIT bit, and applies to both single and co-ordinate conversion mode.

The flow diagram in Figure 24 shows the timing of touchpanel conversions, and data readback from register 7Ah - dependent on the individual settings of the CO, POLL, ADCSEL and CTC bits.



| | |
|--------------|---|
| POLL (74h) | Starts a single measurement |
| CTC (74h) | Starts a co-ordinate measurement at specified conversion rate |
| COO (74h) | Enables Co-Ordinate mode |
| ADCSEL (74H) | Specifies the type of measurement to be made |

Figure 24 Touchpanel Conversion Flow Diagram

If the SLEN bit is set to '1', then the touchpanel data appears on the AC-Link slot selected by the SLT control bits, as shown below. The Slot 0 'tag' bit corresponding to the selected time slot is asserted whenever there is new data on that slot.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|--|
| 76h | 3 | SLEN | 0 | Slot Readback Enable 0: Disabled (readback through register only) 1: Enable (readback slot selected by SLT) |
| | 2:0 | SLT | 110 | AC'97 Slot Selection for Touchpanel Data 000: Slot 5 001: Slot 6 ... 101: Slot 10 110: Slot 11 111: RESERVED |

Table 51 Returning Touchpanel Data Through an AC-Link Time Slot

TOUCHPANEL SETTLING TIME

For accurate touchpanel measurements, some settling time may be required between the switch matrix applying a voltage across the touchpanel plate and the ADC sampling the signal. This time delay function is built into the WM9713L and can be programmed as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|-------------------|------------------------------|
| 76h | 7:4 | DEL | 0000 (1 frame) | Touchpanel ADC Settling Time |

Table 52 Touchpanel Settling Time Control (1)

| DEL | DELAY (AC-LINK FRAMES) | DELAY (TIME) |
|------|-----------------------------------|-----------------|
| 0000 | 1 | 20.8µs |
| 0001 | 2 | 41.7µs |
| 0010 | 4 | 83.3µs |
| 0011 | 8 | 167µs |
| 0100 | 16 | 333µs |
| 0101 | 32 | 667µs |
| 0110 | 48 | 1ms |
| 0111 | 64 | 1.33ms |
| 1000 | 96 | 2ms |
| 1001 | 128 | 2.67ms |
| 1010 | 160 | 3.33ms |
| 1011 | 192 | 4ms |
| 1100 | 224 | 4.67ms |
| 1101 | 256 | 5.33ms |
| 1110 | 288 | 6ms |
| 1111 | No delay, switch matrix always on | |

Table 53 Touchpanel Settling Time Control (2)

The total time for co-ordinate or auxiliary measurements to complete is the delay time DEL, plus one AC-Link frame (20.8µs). For a pressure measurement, the time taken is DEL plus two AC-Link frames (41.6µs).

Although the DELAY is variable the maximum value that may be programmed depends on the number of ADCSEL[7:1] bits set, as shown in the following table. Setting multiple ADCSEL[7:1] bits leaves less spare AC_Link frames for the DELAY.

| NUMBERS OF ADCSEL[1:7] BITS SET | CR SETTING | MAX DELAY SETTING |
|---------------------------------|---------------|-------------------|
| 1 | 00 (93.75Hz) | 288 |
| 1 | 01 (120Hz) | 288 |
| 1 | 10 (153.75Hz) | 288 |
| 1 | 11 (187.5Hz) | 256 |
| 2 | 00 (93.75Hz) | 256 |
| 2 | 01 (120Hz) | 192 |
| 2 | 10 (153.75Hz) | 128 |
| 2 | 11 (187.5Hz) | 128 |
| 3, 4 | 00 (93.75Hz) | 96 |
| 3, 4 | 01 (120Hz) | 96 |
| 3, 4 | 10 (153.75Hz) | 64 |
| 3, 4 | 11 (187.5Hz) | 48 |
| 5,6,7 | 00 (93.75Hz) | 48 |
| 5,6,7 | 01 (120Hz) | 48 |
| 5,6,7 | 10 (153.75Hz) | 32 |
| 5,6,7 | 11 (187.5Hz) | 16 |
| 1 (if COO=1) | 00 (93.75Hz) | 224 |
| 1 (if COO=1) | 01 (120Hz) | 192 |
| 1 (if COO=1) | 10 (153.75Hz) | 128 |
| 1 (if COO=1) | 11 (187.5Hz) | 96 |
| 2,3,4,5,6,7 (if COO=1) | 00 (93.75Hz) | 160 |
| 2,3,4,5,6,7 (if COO=1) | 01 (120Hz) | 128 |
| 2,3,4,5,6,7,8 (if COO=1) | 10 (153.75Hz) | 96 |
| 2,3,4,5,6,7,8 (if COO=1) | 11 (187.5Hz) | 64 |

Table 54 Maximum Delay Values

Setting DEL to '1111' reduces the settling time to zero, i.e. measurements begin immediately. This mode is intended for fast sampling on AUX inputs. It is NOT intended for touchpanel digitisation. There are several side-effects when DEL is set to '1111':

- Co-ordinate mode does not work, i.e. the WM9713L behaves as if COO = 0, even if COO = 1 (see "Measurement Types")
- If X / Y co-ordinate or touch pressure measurements are selected (ADCSEL = 001, 010 or 011), then the switch matrix is constantly on, and current constantly flows in the touchpanel. This increases power consumption in the system, and is therefore not recommended for battery powered systems
- In continuous mode (CTC = 1), setting DEL = 1111 increases the sampling rate of the touchpanel ADC (see "Initiation of Measurements")

MASK INPUT CONTROL

Sources of glitch noise, such as the signals driving an LCD display, may feed through to the touchscreen plates and affect measurement accuracy. In order to minimise this effect, a signal may be applied to MASK (pin 47 / pin 3) to delay or synchronise the sampling of any input to the ADC. The effect of the MASK signal depends on the the MSK bits of register 78h (bits [7:6]), as described below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|-----------------------------------|
| 78h | 7:6 | MSK | 00 | MASK input control (see Table 56) |

Table 55 MASK Input Control

| MSK[1-0] | EFFECT OF SIGNAL ON MASK PIN |
|----------|---|
| 00 | Mask has no effect on conversions GPIO input disabled (default) |
| 01 | Static; 'hi' on MASK pin stops conversions, 'lo' has no effect. |
| 10 | Edge triggered; rising or falling edge on MASK pin delays conversions by an amount set in the DEL[3-0] register. Conversions are asynchronous to the MASK signal. |
| 11 | Synchronous mode; conversions wait until rising or falling edge on MASK initiates cycle; screen starts to be driven when the edge arrives, the conversion sample being taken a period set by DEL[3-0] after the edge. |

Table 56 Controlling the MASK Feature

Note that pin 47 / pin 3 can also be used as a GPIO(see "GPIO and Interrupt Control" section), or to output the ADA signal (see below).

THE ADA SIGNAL

Whenever data becomes available from the touchpanel ADC, the internal ADA (ADC Data Available) signal goes high and remains high until the data has been read from register 7Ah (if SLEN = 0) or until it has been sent out on an AC-Link slot (if SLEN = 1).

ADA goes high either-

- After every touchpanel ADC conversion (in normal mode, COO=0)
- After every set of 3 conversions (co-ordinate mode, COO=1)

ADA can be used to generate an interrupt, if the AW bit (register 52h, bit 12) is set (see "GPIO and interrupt control" section)

It is also possible to output the ADA signal on pin 47 / pin 3, if this pin is not used as a GPIO. The GE4/6 bit must be set to '0' to achieve this (see "GPIO and interrupt control" section).

Alternatively, ADA can be read from bit 12 in register 54h.

ADDITIONAL FEATURES

AUXILIARY ADC INPUTS

The ADC used for touchpanel digitisation can also be used for the sole purpose of auxiliary measurements, provided that it is enabled (register 78h, PRP = 11). The WM9713L has three pins that can be used as auxiliary ADC inputs:

- MIC2A / COMP1 / AUX1 (pin 29)
- MIC2B / COMP2 / AUX2 (pin 30)
- WIPER / AUX4 (pin 12)

Additionally, the speaker supply (SPKVDD) can be used as an auxiliary ADC input through an on-chip potential divider giving an input to the auxiliary ADC of SPKVDD/3. This input is referred to as the AUX3 input (see Figure 16).

Note that pin 12 connects to the wiper of a 5-wire touchpanel wiper function. Auxiliary measurements taken on pin 12 are only meaningful when it is not connected to a touchpanel (i.e. a 4-wire touchpanel, or no touchpanel at all, is used). Pins 29 and 30 are also used as comparator inputs (see Battery Alarm and Battery Measurement), but auxiliary measurements can still be taken on these pins at any time. The ADCSEL control bits select between different ADC inputs, as shown in Table 57.

The ADCSEL control bits determine which type of measurement is performed (see below). When performing auxiliary conversions the co-ordinate mode bit, COO, should be off (0).

If CTC=0 then only one of the ADCSEL[7:1] bits should be set. If operating in continuous mode (CTC=1), then more than one ADCSEL[7:1] bit may be set, and conversions will be performed cyclically in the following order => "AUX1,AUX2,AUX3,AUX4..." – dependent on which bits are set.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------------|---------|--|
| 74h | 7 | ADCSEL_AUX4 | 0 | Enable AUX4 measurement (pin12) |
| | 6 | ADCSEL_AUX3 | 0 | Enable AUX3 measurement (SPKVDD) |
| | 5 | ADCSEL_AUX2 | 0 | Enable AUX2 measurement (pin30) |
| | 4 | ADCSEL_AUX1 | 0 | Enable AUX1 measurement (pin29) |
| | 0 | COO | 0 | Enable co-ordinate mode – for touchpanel conversions only (see "Controlling the Touchpanel Interface") |

Table 57 Auxiliary ADC Measurements

Auxiliary ADC measurements are initiated in the same way as touchpanel measurements, and the data is returned in the same manner. Please refer to the "Controlling the Touchpanel Interface" section.

BATTERY ALARM AND ANALOGUE COMPARATORS

The battery alarm function differs from battery measurement in that it does not actually measure the battery voltage. Battery alarm only indicates “OK”, “Low” or “Dead”. The advantage of the battery alarm function is that it does not require a clock and can therefore be used in low-power sleep or standby modes.

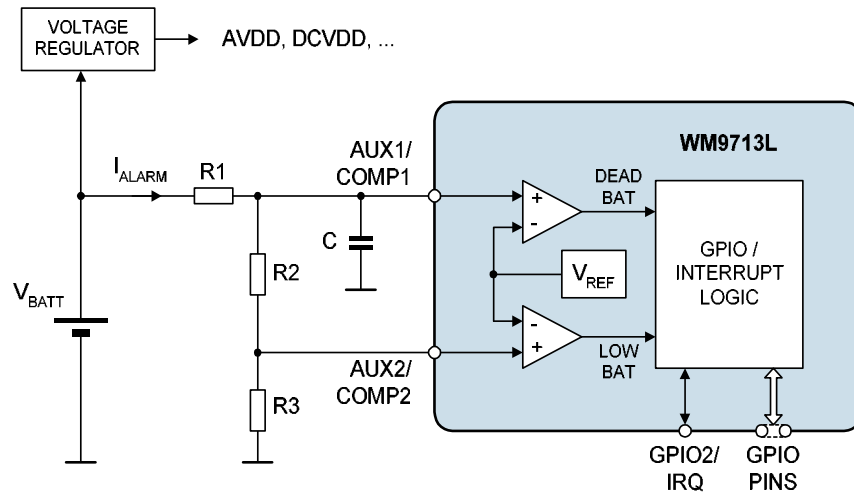


Figure 25 Battery Alarm Example Schematic

The typical schematic for a dual threshold battery alarm is shown above. This alarm has two thresholds, “dead battery” (COMP1) and “low battery” (COMP2). R1, R2 and R3 set the threshold voltages. Their values can be up to about 1M Ω in order to keep the battery current [$I_{ALARM} = V_{BATT} / (R1+R2+R3)$] to a minimum (higher resistor values may affect the accuracy of the system as leakage currents into the input pins become significant).

Dead battery alarm: COMP1 triggers when $V_{BATT} < V_{REF} \times (R1+R2+R3) / (R2+R3)$

A dead battery alarm is the highest priority of interrupt in the system. It should immediately save all unsaved data and shut down the system. The GP15, GS15 and GW15 bits must be set to generate this interrupt.

Low battery alarm: COMP2 triggers when $V_{BATT} < V_{REF} \times (R1+R2+R3) / R3$

A low battery alarm has a lower priority than a dead battery alarm. Since the threshold voltage is higher than for a dead battery alarm, there is enough power left in the battery to give the user a warning and/or shut down “gracefully”. When V_{BATT} gets close to the low battery threshold, spurious alarms are filtered out by the COMP2 delay function.

The purpose of the capacitor C is to remove from the comparator inputs any high frequency noise or glitches that may be present on the battery (for example, noise generated by a charge pump). It forms a low pass filter with R1, R2 and R3.

Low pass cutoff f_c [Hz] = $1 / (2\pi C \times (R1 \parallel (R2+R3)))$

Provided that the cutoff frequency is several orders of magnitude lower than the noise frequency f_n , this simple circuit can achieve excellent noise rejection.

Noise rejection [dB] = $20 \log (f_n / f_c)$

The circuit shown above also allows for measuring the battery voltage V_{BATT} . This is achieved simply by setting the touchpanel ADC input to be either COMP1 (ADCSEL = 100) or COMP2 (ADCSEL = 101) (see also Auxiliary ADC Inputs).

The WM9713L has two on-chip comparators that can be used to implement a battery alarm function, or other functions such as a window comparator. Each comparator has one of its inputs tied to COMP1 (pin 29) or COMP2 (pin 30), and the other tied to a voltage reference. The voltage reference can be either internally generated ($V_{REF} = AVDD/2$) or externally connected on AUX4 (pin 12).

The comparator output signals are passed to the GPIO logic block (see "GPIO and Interrupt Control" section), where they can be used to send an interrupt to the CPU via the AC-Link or via the IRQ pin, and / or to wake up the WM9713L from sleep mode. COMP1/AUX1 (pin 29) corresponds to GPIO bit 15 and COMP2/AUX2 (pin30) to bit 14.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-------|-----------|---------|--|
| 4Eh | 15 | CP1 | 1 | COMP1 Polarity (see also "GPIO and Interrupt Control") 0: Alarm when COMP1 voltage is below VREF 1: Alarm when COMP1 voltage is above VREF |
| | 14 | CP2 | 1 | COMP2 Polarity (see also "GPIO and Interrupt Control") 0: Alarm when COMP2 voltage is below VREF 1: Alarm when COMP2 voltage is above VREF |
| 5Ah | 15:13 | COMP2 DEL | 000 | Low Battery Alarm Delay 000: No delay 001: 0.17s ($2^{13} = 8192$ AC-Link frames) 010: 0.34s ($2^{14} = 16384$ AC-Link frames) 011: 0.68s ($2^{15} = 32768$ AC-Link frames) 100: 1.4s ($2^{16} = 65536$ AC-Link frames) 101: 2.7s ($2^{17} = 131072$ AC-Link frames) 110: 5.5s ($2^{18} = 262144$ AC-Link frames) 111: 10.9s ($2^{19} = 524288$ AC-Link frames) |

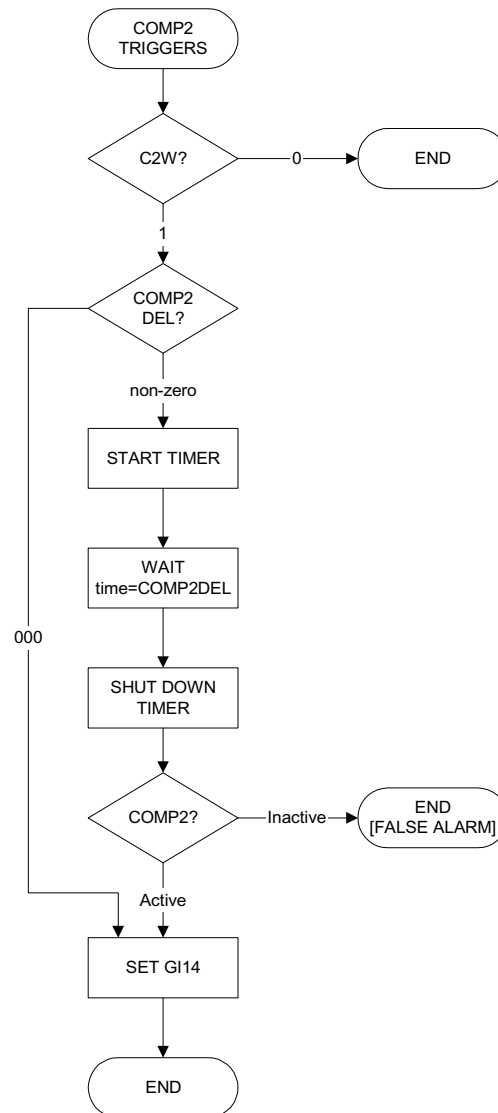
Table 58 Comparator Control

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|--|-------|-------|---------|---|---|
| 5Ch Additional Analogue Functions | 14 | C1REF | 0 | Comparator 1 Reference Voltage | |
| | | | | 0 | $V_{REF} = AVDD/2$ |
| | | | | 1 | WIPER/AUX4 (pin 12) |
| | 13:12 | C1SRC | 00 | Comparator 1 Signal Source | |
| | | | | 00 | $AVDD/2$ when C1REF='1'. Otherwise comparator 1 is powered down |
| | | | | 01 | COMP1/AUX1 (pin 29) |
| | | | | 10 | COMP2/AUX2 (pin 30) |
| | | | | 11 | Reserved |
| | 11 | C2REF | 0 | Comparator 2 Reference Voltage | |
| | | | | 0 | $V_{REF} = AVDD/2$ |
| | | | | 1 | WIPER/AUX4 (pin 12) |
| | 10:9 | C2SRC | 00 | Comparator 2 Signal Source | |
| 00 | | | | $AVDD/2$ when C2REF='1'. Otherwise comparator 2 is powered down | |
| 01 | | | | COMP1/AUX1 (pin 29) | |
| 10 | | | | COMP2/AUX2 (pin 30) | |
| 11 | | | | Reserved | |

Table 59 Comparator Reference and Source Control

COMP2 DELAY FUNCTION

COMP2 has an optional delay function for use when the input signal is noisy. When COMP2 triggers and the delay is enabled (i.e. COMP2DEL is non-zero), then GPIO bit 14 does not change state immediately, and no interrupt is generated. Instead, the WM9713L starts a delay timer and checks COMP2 again after the delay time has passed. If COMP2 is still active, then the GPIO bit is set and an interrupt may be generated (depending on the state of the GW14 bit). If COMP2 is no longer active, the GPIO bit is not set, i.e. all register bits are as if COMP2 had never triggered.

**Figure 26 COMP2 Delay Flow Chart**

GPIO AND INTERRUPT CONTROL

The WM9713L has eight GPIO pins that operate as defined in the AC'97 Revision 2.2 specification. Each GPIO pin can be set up as an input or as an output, and has corresponding bits in register 54h and in slot 12. The state of a GPIO output is determined by sending data through slot 12 of outgoing frames (SDATAOUT). Data can be returned from a GPIO input by reading the register bit, or examining slot 12 of incoming frames (SDATAIN). GPIO inputs can be made sticky, and can be programmed to generate an interrupt, transmitted either through the AC-Link or through a dedicated, level-mode interrupt pin (GPIO2/IRQ, pin 45).

In addition, the GPIO pins 1, 3, 4 and 5 can be used for the PCM interface by setting bit 15 of register 36h (see "PCM Codec" section). Setting this bit disables any GPIO functions selected on these pins.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------------|-----|-------|----------|---|
| 36h PCM Codec Control | 15 | CTRL | 0 | Enables PCM interface on GPIO pins 1, 3, 4 and 5. 0: Normal GPIO functions 1: PCM interface enabled Note: For PCM interface, one or more of these pins (depending on master/slave/partial master mode) must be set up as an output by writing to register 4Ch (see Table 62) |
| 56h GPIO Pin Sharing | 8:2 | GE# | 1 (GPIO) | Toggle GPIO pin function: 0: secondary function enabled 1: GPIO enabled |

Table 60 GPIO Additional Function Control

GPIO pins 2 to 8 are multi-purpose pins that can also be used for other (non-GPIO / -PCM) purposes, e.g. as a SPDIF output or to signal pendown. This is controlled by register 56h (see Table 63)

Note that GPIO6/7/8 each have an additional function independent of the GPIO / auxillary functions discussed above. If these pins are to be used as GPIO then the independent function needs to be disabled using its own control registers, e.g. to use pin 11 as a GPIO then the RESETB function needs to be disabled (RSTDIS, register 5Ah, bit 8).

Independently of the GPIO pins, the WM9713L also has seven virtual GPIOs. These are signals from inside the WM9713L, which are treated as if they were GPIO input signals. From a software perspective, virtual GPIOs are the same as GPIO pins, but they cannot be set up as outputs, and are not tied to an actual pin. This allows for simple, uniform processing of different types of signals that may generate interrupts (e.g. pen down, battery warnings, jack insertion, high-temperature warning, or GPIO signals).

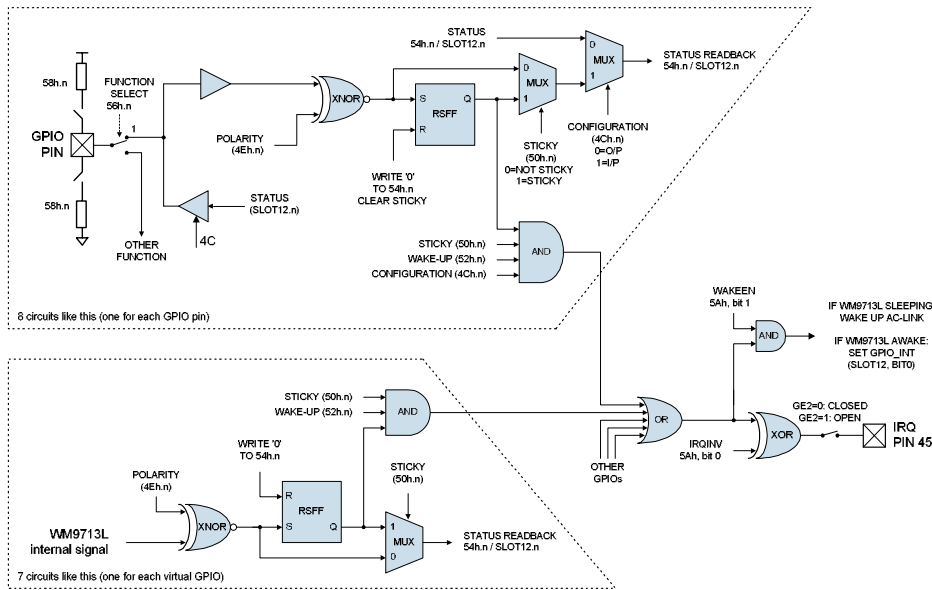


Figure 27 GPIO Logic

| GPIO BIT | SLOT 12 BIT | TYPE | PIN NO. | DESCRIPTION |
|----------|-------------|--------------|-----------------------|--|
| 1 | 5 | GPIO Pin | 44 | GPIO1 |
| 2 | 6 | GPIO Pin | 45 | GPIO2 / IRQ enabled only when pin not used as IRQ |
| 3 | 7 | GPIO Pin | 46 | GPIO3 / PENDOWN enabled only when pin not used as PENDOWN |
| 4 | 8 | GPIO Pin | 47 | GPIO4 / ADA / MASK enabled only when pin not used as ADA |
| 5 | 9 | GPIO Pin | 48 | GPIO5 / SPDIF_OUT enabled only when pin not used as SPDIF_OUT |
| 6 | 10 | GPIO Pin | 3 | GPIO6 / ADA / MASK Enabled only when pin not used as ADA |
| 7 | 11 | GPIO Pin | 11 | GPIO7 / PENDOWN enabled only when pin not used as PENDOWN |
| 8 | 12 | GPIO Pin | 12 | GPIO8 / SPDIF_OUT enabled only when pin not used as SPDIF_OUT |
| 9 | 13 | Virtual GPIO | - [MICDET] | Internal microphone bias current detect, generates an interrupt above a threshold (see MICBIAS Current Detect) |
| 10 | 14 | Virtual GPIO | - [MICSHT] | Internal shorted microphone detect, generates an interrupt above a threshold (see MICBIAS Current Detect) |
| 11 | 15 | Virtual GPIO | - [Thermal Cutout] | Internal thermal cutout signal, indicates when internal temperature reaches approximately 150°C (see "Thermal Sensor") |
| 12 | 16 | Virtual GPIO | - [ADA] | Internal ADA (ADC Data Available) Signal enabled only when touchpanel ADC is active |
| 13 | 17 | Virtual GPIO | - [PEN DOWN] | Internal PENDOWN Signal enabled only when pen-down detection is active |
| 14 | 18 | Virtual GPIO | - [COMP2] | Internal COMP2 output (Low Battery Alarm) enabled only when COMP2 is on |
| 15 | 19 | Virtual GPIO | - [COMP1] | Internal COMP1 output (Dead Battery Alarm) enabled only when COMP1 is on |

Table 61 GPIO Bits and Pins

Note: GPIO7 (Pin 11) has an independent RESETB function. This must be disabled using RSTDIS (Register 5Ah, bit 8) before using Pin 11 as a GPIO / PENDOWN.

The properties of the GPIOs are controlled through registers 4Ch to 52h, as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|---|
| 4Ch | n | GCn | 1 | GPIO Pin Configuration 0: Output 1: Input GC9-15 are always '1' |
| 4Eh | n | GPn | 1 | GPIO Pin Polarity / Type |
| | | | | Input (GCn=1) |
| | | | | 0: Active Low 1: Active High [GIn = pin level XNOR GPn] |
| | | | | 0: Active High 1: Active low |
| 50h | n | GSn | 0 | GPIO Pin Sticky 1: Sticky 0: Not Sticky |
| 52h | n | GWn | 0 | GPIO Pin Wake-up 1: Wake Up (generate interrupts from this pin) 0: No wake-up (no interrupts generated) |
| 54h | n | GIn | N/A | GPIO Pin Status Read: Returns status of each GPIO pin Write: Writing '0' clears sticky bit |

Table 62 GPIO Control

The following procedure is recommended for handling interrupts:

When the controller receives an interrupt, check register 54h. For each GPIO bit in descending order of priority, check if the bit is '1'. If yes, execute corresponding interrupt routine, then write '0' to corresponding bit in 54h. If no, continue to next lower priority GPIO. After all GPIOs have been checked, check if interrupt still present or no. If yes, repeat procedure. If no, then jump back to process that ran before the interrupt.

If the system CPU cannot execute such an interrupt routine, it may be preferable to switch internal signals (such as PENDOWN) directly onto the GPIO pins. However, in this case the interrupt signals cannot be made sticky, and more GPIO pins are tied up both on the WM9713L and on the CPU.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-------|---------|---|
| 56h GPIO pins function select | 2 | GE2 | 1 | GPIO2 / IRQ output select 0: Pin 45 disconnected from GPIO logic set 4Ch, bit 2 to '0' to output IRQ signal 1: Pin 45 connected to GPIO logic (IRQ disabled) |
| | 3 | GE3 | 1 | GPIO3 / PENDOWN output select 0: Pin 46 disconnected from GPIO logic set 4Ch, bit 3 to '0' to output PENDOWN signal 1: Pin 46 connected to GPIO logic |
| | 4 | GE4 | 1 | GPIO4 / ADA / MASK output select 0: Pin 47 disconnected from GPIO logic set 4Ch, bit 4 to '0' to output ADA signal set 4Ch, bit 4 to '1' to input MASK signal 1: Pin 47 connected to GPIO logic |
| | 5 | GE5 | 1 | GPIO5 / SPDIF output select 0: Pin 48 = SPDIF (disconnected from GPIO logic) set 4Ch, bit 5 to '0' to output SPDIF signal 1: Pin 48 connected to GPIO logic (SPDIF disabled) |
| | 6 | GE6 | 1 | GPIO6 / ADA / MASK output select 0: Pin 3 disconnected from GPIO logic set 4Ch, bit 6 to '0' to output ADA signal set 4Ch, bit 6 to '1' to input MASK signal 1: Pin 3 connected to GPIO logic |
| | 7 | GE7 | 1 | GPIO7 / PENDOWN output select 0: Pin 11 disconnected from GPIO logic set 4Ch, bit 7 to '0' to output PENDOWN signal 1: Pin 11 connected to GPIO logic |
| | 8 | GE8 | 1 | GPIO8 / SPDIF output select 0: Pin 12 = SPDIF (disconnected from GPIO logic) set 4Ch, bit 8 to '0' to output SPDIF signal 1: Pin 12 connected to GPIO logic (SPDIF disabled) |

Table 63 Using GPIO Pins for Non-GPIO Functions

POWER MANAGEMENT

INTRODUCTION

The WM9713L includes the standard power down control register defined by the AC'97 specification (register 26h). Additionally, it also allows more specific control over the individual blocks of the device through register Powerdown registers 3Ch and 3Eh. Each particular circuit block is active when both the relevant bit in register 26h AND the relevant bit in the Powerdown registers 3Ch and 3Eh are set to '0'.

Note that the default power-up condition is all OFF.

AC97 CONTROL REGISTER

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---|-----|-------|---------|---|
| 26h Powerdown/ Status register | 14 | PR6 | 1 (OFF) | Disables all output PGAS |
| | 13 | PR5 | 1 (OFF) | Disables internal clock |
| | 12 | PR4 | 1 (OFF) | Disables AC-link interface (external clock off) |
| | 11 | PR3 | 1 (OFF) | Disables VREF, input PGAs, DACs, ADCs, mixers and outputs |
| | 10 | PR2 | 1 (OFF) | Disables input PGAs and mixers |
| | 9 | PR1 | 1 (OFF) | Disables stereo DAC |
| | 8 | PR0 | 1 (OFF) | Disables stereo ADCs and record mux PGA |
| | 3 | REF | 0 | Read-only bit, indicates VREF is ready (inverse of PR3) |
| | 2 | ANL | 0 | Read-only bit, indicates analogue mixers are ready (inverse of PR2) |
| | 1 | DAC | 0 | Read-only bit, indicates stereo DAC is ready (inverse of PR1) |
| | 0 | ADC | 0 | Read-only bit, indicates stereo ADC is ready (inverse of PR0) |

Table 64 Powerdown and Status Register (Conforms to AC'97 Rev 2.2)

EXTENDED POWERDOWN REGISTERS

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|-------------------------|-----|---------|---------------------|--|
| 3Ch Powerdown (1) | 15 | PADCPD | 1 (OFF) | Disables touchpanel/aux ADC |
| | 14 | VMID1M | 1 (OFF) | Disables 1Meg Vmid resistor string |
| | 13 | TSHUT | 1 (OFF) | Disables thermal shutdown |
| | 12 | VXDAC | 1 (OFF) | Disables VXDAC |
| | 11 | AUXDAC | 1 (OFF) | Disables AUXDAC |
| | 10 | VREF | 1 (OFF) | Disables master bias reference generator |
| | 9 | PLL | 1 (OFF) | Disables PLL |
| | 7 | DACL | 1 (OFF) | Disables left DAC (see Note 1) |
| | 6 | DACR | 1 (OFF) | Disables right DAC (see Note 1) |
| | 5 | ADCL | 1 (OFF) | Disables left ADC |
| | 4 | ADCR | 1 (OFF) | Disables right ADC |
| | 3 | HPLX | 1 (OFF) | Disables left headphone mixer |
| | 2 | HPRX | 1 (OFF) | Disables right headphone mixer |
| | 1 | SPKX | 1 (OFF) | Disables speaker mixer |
| 0 | MX | 1 (OFF) | Disables mono mixer | |

Note: When analogue inputs or outputs are disabled, they are internally connected to VREF through a large resistor ($VREF=AVDD/2$ except when VREF and VMID1M are both OFF). This maintains the potential at that node and helps to eliminate pops when the pins are re-enabled.

Table 65 Extended Power Down Register (1) (Additional to AC'97 Rev 2.2)

Note:

1. When disabling a PGA, always ensure that it is muted first.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|---------|--------------------------|---------------------------------------|
| 3Eh Powerdown (2) | 15 | MCD | 1 (OFF) | Disables microphone current detect |
| | 14 | MICBIAS | 1 (OFF) | Disables microphone bias |
| | 13 | MONO | 1 (OFF) | Disables MONO output PGA (see Note 1) |
| | 12 | OUT4 | 1 (OFF) | Disables OUT4 output PGA (" ") |
| | 11 | OUT3 | 1 (OFF) | Disables OUT3 output PGA (" ") |
| | 10 | HPL | 1 (OFF) | Disables HPL output PGA (" ") |
| | 9 | HPR | 1 (OFF) | Disables HPR output PGA (" ") |
| | 8 | SPKL | 1 (OFF) | Disables SPKL output PGA (" ") |
| | 7 | SPKR | 1 (OFF) | Disables SPKR output PGA (" ") |
| | 6 | LL | 1 (OFF) | Disables LINEL PGA (" ") |
| | 5 | LR | 1 (OFF) | Disables LINER PGA (" ") |
| | 4 | MOIN | 1 (OFF) | Disables MONOIN PGA (" ") |
| | 3 | MA | 1 (OFF) | Disables mic PGA MA (" ") |
| | 2 | MB | 1 (OFF) | Disables mic PGA MB (" ") |
| | 1 | MPA | 1 (OFF) | Disables mic pre-amp MPA |
| 0 | MPB | 1 (OFF) | Disables mic pre-amp MPB | |
| <p>Note: When analogue inputs or outputs are disabled, they are internally connected to VREF through a large resistor (VREF=AVDD/2 except when VREF and VMID1M are both OFF). This maintains the potential at that node and helps to eliminate pops when the pins are re-enabled.</p> | | | | |

Table 66 Extended Power Down Register (2) (Additional to AC'97 Rev 2.2)

Note:

1. When disabling a PGA, always ensure that it is muted first.

ADDITIONAL POWER MANAGEMENT

Mixer output inverters: see "Mixer output Inverters" section. Inverters are OFF by default.

Touchpanel Interface: see "Controlling the Touchpanel Digitiser / Power Management". The touchpanel digitiser is OFF by default.

SLEEP MODE

Whenever the PR4 bit (reg. 26h) is set, the AC-Link interface is disabled, and the WM9713L is in sleep mode. There is in fact a very large number of different sleep modes, depending on the other control bits. For example, the low-power standby mode described below is a sleep mode. It is desirable to use sleep modes whenever possible, as this will save power. The following functions do not require a clock and can therefore operate in sleep mode:

- Analogue-to-analogue audio (DACs and ADCs unused), e.g. phone call mode
- Pen-down detection
- GPIO and interrupts
- Battery alarm / analogue comparators

The WM9713L can awake from sleep mode as a result of

- A warm reset on the AC-Link (according to the AC'97 specification)
- A signal on a GPIO pin (if the pin is configured as an input, with wake-up enabled – see "GPIO and Interrupt Control" section)
- A virtual GPIO event such as pen-down, battery alarm, etc. (see "GPIO and Interrupt Control" section)

LOW POWER STANDBY MODE

If all the bits in registers 26h, 3Ch and 3Eh are set except VMID1M (register 3Ch, bit 14), then the WM9713L is in low-power standby mode and consumes very little current. A 1M Ω resistor string remains connected across AVDD to generate VREF. This is necessary if the on-chip analogue comparators are used (see “Battery Alarm and Battery Measurement” section), and helps shorten the delay between wake-up and playback readiness. If VREF is not required, the 1M Ω resistor string can be disabled by setting the VMID1M bit, reducing current consumption further.

SAVING POWER AT LOW SUPPLY VOLTAGES

The analogue supplies to the WM9713L can run from 1.8V to 3.6V. By default, all analogue circuitry on the IC is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 1.8V. However, at lower voltages, it is possible to save power by reducing the internal bias currents used in the analogue circuitry. This is controlled as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|-----|-------|---------|--|
| 5Ch | 6:5 | VBIAS | 00 | Analogue Bias optimization 11 : Lowest bias current, optimized for 1.8V 10 : Low bias current, optimized for 2.5V 01, 00 : Default bias current, optimized for 3.3V |

Table 67 Analogue Bias Selection

POWER ON RESET (POR)

The WM9713L has an internal power on reset (PORB) which ensures that a reset is applied to all registers until a supply threshold has been exceeded. The POR circuitry monitors the voltage for both AVDD and DCVDD and will release the internal reset signal once these supplies are both nominally greater than 1.36V. The internal reset signal is an AND of the PORB and RESETB input signal.

It is recommended that for operation of the WM9713L, all device power rails should be stable before configuring the device for operation.

AC97 INTERFACE TIMING

Test Characteristics:

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

CLOCK SPECIFICATIONS

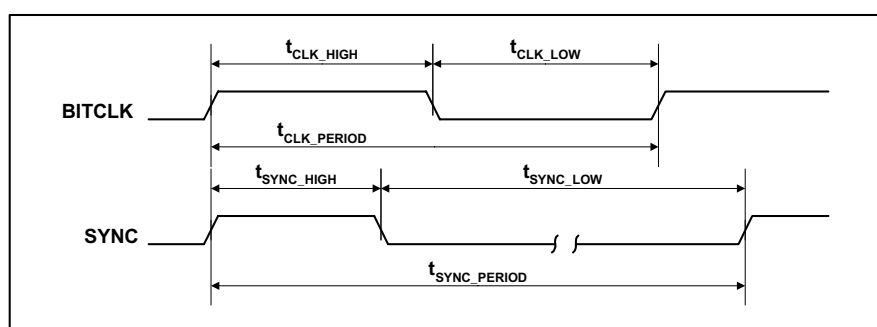
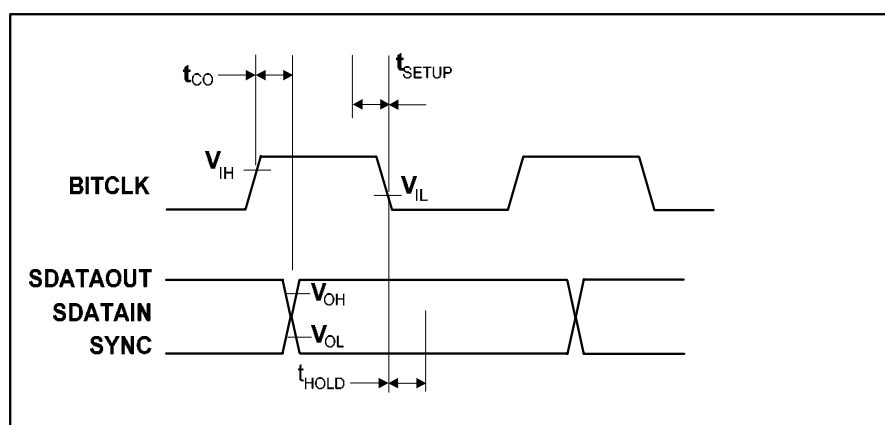


Figure 28 Clock Specifications (50pF External Load)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|----------------------------------|--------------------|-----|--------|-----|---------|
| BITCLK frequency | | | 12.288 | | MHz |
| BITCLK period | t_{CLK_PERIOD} | | 81.4 | | ns |
| BITCLK output jitter | | | | 750 | ps |
| BITCLK high pulse width (Note 1) | t_{CLK_HIGH} | 36 | 40.7 | 45 | ns |
| BITCLK low pulse width (Note 1) | t_{CLK_LOW} | 36 | 40.7 | 45 | ns |
| SYNC frequency | | | 48 | | kHz |
| SYNC period | t_{SYNC_PERIOD} | | 20.8 | | μ s |
| SYNC high pulse width | t_{SYNC_HIGH} | | 1.3 | | μ s |
| SYNC low pulse width | t_{SYNC_LOW} | | 19.5 | | μ s |

Note:

1. Worst case duty cycle restricted to 45/55

DATA SETUP AND HOLD**Figure 29 Data Setup and Hold (50pF External Load)****Note:**

Setup and hold times for SDATAIN are with respect to the AC'97 controller, not the WM9713L.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|-------------|-----|-----|-----|------|
| Setup to falling edge of BITCLK | t_{SETUP} | 10 | | | ns |
| Hold from falling edge of BITCLK | t_{HOLD} | 10 | | | Ns |
| Output valid delay from rising edge of BITCLK | t_{CO} | | | 15 | ns |

SIGNAL RISE AND FALL TIMES

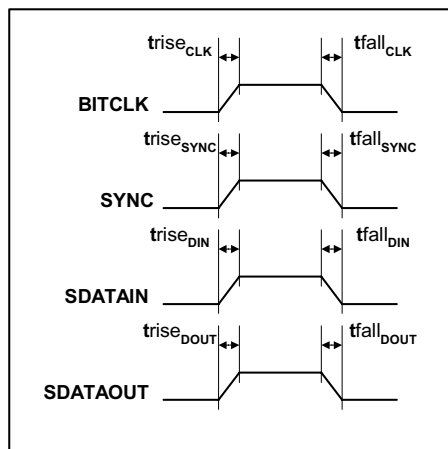


Figure 30 Signal Rise and Fall Times (50pF External Load)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------|-----|-----|-----|------|
| BITCLK rise time | trise _{CLK} | 2 | | 6 | ns |
| BITCLK fall time | tfall _{CLK} | 2 | | 6 | ns |
| SYNC rise time | trise _{SYNC} | 2 | | 6 | ns |
| SYNC fall time | tfall _{SYNC} | 2 | | 6 | ns |
| SDATAIN rise time | trise _{DIN} | 2 | | 6 | ns |
| SDATAIN fall time | tfall _{DIN} | 2 | | 6 | ns |
| SDATAOUT rise time | trise _{DOUT} | 2 | | 6 | ns |
| SDATAOUT fall time | tfall _{DOUT} | 2 | | 6 | ns |

AC-LINK POWERDOWN

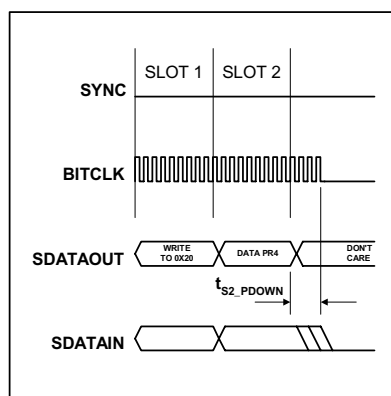


Figure 31 AC-Link Powerdown Timing

AC-Link powerdown occurs when PR4 (register 26h, bit 12) is set (see "Power Management" section).

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|----------------|-----|-----|-----|---------|
| End of Slot 2 to BITCLK and SDATAIN low | t_{S2_PDOW} | | | 1.0 | μ s |

COLD RESET (ASYNCHRONOUS, RESETS REGISTER SETTINGS)

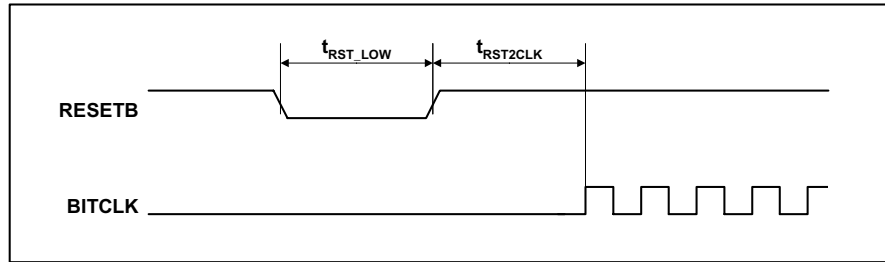


Figure 32 Cold Reset Timing

Note:

For correct operation SDATAOUT and SYNC must be held LOW for entire RESETB active low period otherwise the device may enter test mode. See AC'97 specification or Wolfson applications note WAN104 for more details.

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---|----------------|-------|-----|-----|---------|
| RESETB active low pulse width | t_{RST_LOW} | 1.0 | | | μ s |
| RESETB inactive to BITCLK startup delay | $t_{RST2CLK}$ | 162.8 | | | ns |

WARM RESET (ASYNCHRONOUS, PRESERVES REGISTER SETTINGS)

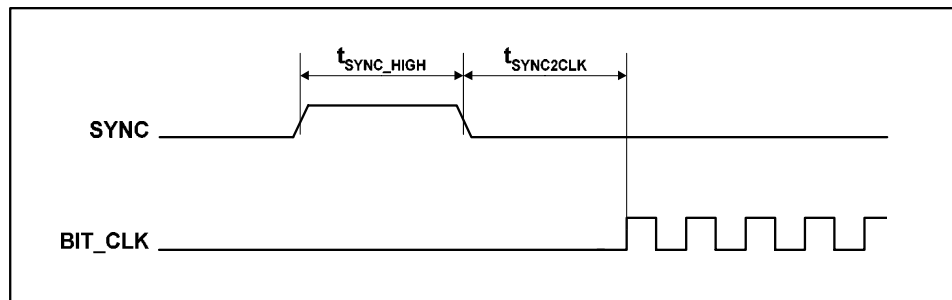


Figure 33 Warm Reset Timing

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|---------------------------------------|------------------|-------|-----|-----|---------|
| SYNC active high pulse width | t_{SYNC_HIGH} | | 1.3 | | μ s |
| SYNC inactive to BITCLK startup delay | $t_{RST2CLK}$ | 162.4 | | | ns |

REGISTER MAP

| Reg | Name | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default | | |
|-----|---------------------------------------|--------------------------------------|-------------|--------------------|-----------|-----------------|------------------------------|---------------------|-------------|------------------|-------------|--------------------|------------------|-------------------|------------|------------|------------|-----------|-------|-------|
| 00h | Reset | 0 | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 6174h | | |
| 02h | Speaker Volume | MUL | ZCL | SPKLVOL | | | | | | MUR | ZCR | SPKRVOL | | | | | | 8080h | | |
| 04h | Headphone Volume | MUL | ZCL | HPLVOL | | | | | | MUR | ZCR | HPRVOL | | | | | | 8080h | | |
| 06h | OUT3/4 Volume | MU4 | ZC4 | OUT4VOL | | | | | | MU3 | ZC3 | OUT3VOL | | | | | | 8080h | | |
| 08h | MONO Vol & MONOIN PGA Vol / Routing | M2H | M2S | 0 | MONOINVOL | | | | | | MU | ZC | MONOVOL | | | | | | C880h | |
| 0Ah | LINEIN PGA Volume / Routing | L2H | L2S | L2M | LINELVOL | | | | | | 0 | 0 | 0 | LINERVOL | | | | | | E808h |
| 0Ch | DAC PGA Volume / Routing | D2H | D2S | D2M | DACLVOL | | | | | | 0 | 0 | 0 | DACRVOL | | | | | | E808h |
| 0Eh | MIC PGA Volume | 0 | 0 | 0 | MICAVAL | | | | | | 0 | 0 | 0 | MICBVOL | | | | | | 0808h |
| 10h | MIC Routing | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MA2M | MB2M | MIC2M BST | MIC2H | MIC2H/OL | | | | 00DAh | | |
| 12h | Record PGA Volume | RMU | GRL | (Extended) RECVOLL | | | | | | ZC | GRR | (Extended) RECVOLR | | | | | | 8000h | | |
| 14h | Record Routing / Mux Select | R2H | R2HVOL | | | R2M | | | R2M BST | 0 | REC BST | RECSL | | | RECSR | | | D600h | | |
| 16h | PCBEEP Volume / Routing | B2H | B2HVOL | | | B2S | | | B2SVOL | | | B2M | B2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 18h | VxDAC Volume / Routing | V2H | V2HVOL | | | V2S | | | V2SVOL | | | V2M | V2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 1Ah | AUXDAC Volume / Routing | A2H | A2HVOL | | | A2S | | | A2SVOL | | | A2M | A2MVOL | | | 0 | 0 | 0 | 0 | AAA0h |
| 1Ch | Output PGA Mux Select | MONO | | | SPKL | | | SPKR | | | HPL | | HPR | | OUT3 | | OUT4 | | 0000h | |
| 1Eh | DAC 3D Control & INV Mux Select | INVA | | | INVB | | | 0 | 0 | 0 | 0 | 3DLC | 3DUC | 3DDEPTH | | | | 0000h | | |
| 20h | DAC Tone Control | BB | 0 | 0 | BC | BASS | | | | 0 | DAT | 0 | TC | TRBL | | | | 0F0Fh | | |
| 22h | MIC Input Select & Bias / Detect Ctrl | MICMPSEL | | MPASEL | | MPABST | | MPBBST | | MBOP 2EN | MBOP1 EN | MBVOL L | MCDTHR | | MCDSCTHR | | | 0040h | | |
| 24h | Output Volume Mapping (Jack Insert) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | J1EN | D2DRVSEL | EARSPELSEL | | | 0000h | | |
| 26h | Powerdown Ctrl/Stat | 0 | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | 0 | 0 | 0 | 0 | REF | ANL | DAC | ADC | 7F00h | | |
| 28h | Extended Audio ID | ID1 | ID0 | 0 | 0 | REV1 | REV0 | AMAP | LDAC | SDAC | CDAC | 0 | 0 | VRM | SPDIF | DRA | VRA | 0405h | | |
| 2Ah | Ext'd Audio Stat/Ctrl | 0 | 0 | 0 | 0 | 0 | 0 | SPCV | 0 | 0 | 0 | 0 | SPSA | 0 | SEN | 0 | VRA | 0410h | | |
| 2Ch | Audio DACs Sample Rate | DACSR (Audio DACs Sample Rate) | | | | | | | | | | | | | | | | BB80h | | |
| 2Eh | AUXDAC Sample Rate | AUXDACSR (Auxiliary DAC Sample Rate) | | | | | | | | | | | | | | | | BB80h | | |
| 32h | Audio ADCs Sample Rate | ADCSR (Audio ADCs Sample Rate) | | | | | | | | | | | | | | | | BB80h | | |
| 36h | PCM codec control | CTRL | MODE | 0 | DIV | | | | VDAC OSR | CP | FSP | SEL | | WL | | FMT | | 4523h | | |
| 3Ah | SPDIF control | V | DRS | SPSR | | L | CC (Category Code) | | | | | | PRE | COPY | AUDIB | PRO | 2000h | | | |
| 3Ch | Powerdown (1) | PADCP D | VMID #M | TSHUT | VXDA C | AUXD AC | VREF | PLL | 1 | DACL | DACR | ADCL | ADCR | HPLX | HPRX | SPKX | MX | FDFPh | | |
| 3Eh | Powerdown (2) | MCD | MIC BIAS | MONO | OUT4 | OUT3 | HPL | HPR | SPKL | SPKR | LL | LR | M0IN | MA | MB | MPA | MPB | FFFFh | | |
| 40h | General Purpose | 0 | 0 | 3DE | 0 | 0 | 0 | 0 | 0 | LB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000h | | |
| 42h | Fast Power-Up Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MONO | SPKL | SPKR | HPL | HPR | OUT3 | OUT4 | 0000h | | |
| 44h | MCLK / PLL Control | 0 | SEXT[6:4] | | | | SEXT[3:0] | | | CLKSRC | 0 | PENDIV | | CLKBX 2 | CLKAX 2 | CLKMU X | 0080h | | | |
| 46h | MCLK / PLL Control | N[3:0] | | | | LF | SDM | DIVSEL | DIVCTL | 0 | PGADDR | | | PGDATA | | | | 0000h | | |
| 4Ch | GPIO Pin Configuration | 1 | 1 | 1 | 1 | 1 | 1 | 1 | GC8 | GC7 | GC6 | GC5 | GC4 | GC3 | GC2 | GC1 | 0 | FFFh | | |
| 4Eh | GPIO Pin Polarity / Type | C1P | C2P | PP | AP | TP | SP | MP | GP8 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | 1 | FFFh | | |
| 50h | GPIO Pin Sticky | C1S | C2S | PS | AS | TS | SS | MS | GS8 | GS7 | GS6 | GS5 | GS4 | GS3 | GS2 | GS1 | 0 | 0000h | | |
| 52h | GPIO Pin Wake-Up | C1W | C2W | PW | AW | TW | SW | MW | GW8 | GW7 | GW6 | GW5 | GW4 | GW3 | GW2 | GW1 | 0 | 0000h | | |
| 54h | GPIO Pin Status | C1I | C2I | PI | AI | TI | SI | M1 | GI8 | GI7 | GI6 | GI5 | GI4 | GI3 | GI2 | GI1 | 0 | GPIO pins | | |
| 56h | GPIO Pin Sharing | 1 | 1 | 1 | 1 | 1 | 1 | 1 | GE8 | GE7 | GE6 | GE5 | GE4 | GE3 | GE2 | 1 | 0 | FFFh | | |
| 58h | GPIO Pull UP/DOWN Ctrl | PU8 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | 4000h | | |
| 5Ah | Additional Functions (1) | COMP2DEL | | | 0 | 0 | 0 | 0 | RSTDIS | JSEL | | HPM ODE | | Die Revision | | WAKEE N | IRQ INV | 0000h | | |
| 5Ch | Additional Functions (2) | AMUTE | C1REF | C1SRC | | C2REF | C2SRC | | 0 | AMEN | VBIAS | | ADCO | HPF | 0 | ASS | | 0000h | | |
| 60h | ALC Control | ALCL (target level) | | | | HLD (hold time) | | | | DCY (decay time) | | | | ATK (attack time) | | | | B032h | | |
| 62h | ALC / Noise Gate Control | ALCSEL | | | MAXGAIN | | | ZCTIMEOUT | 0 | NGAT | 0 | NGG | NGTH (threshold) | | | | | | 3E00h | |
| 64h | AUXDAC input control | XSLE | AUXDACSLT | | | | AUXDAC VAL | | | | | | | | | | | | 0000h | |
| 74h | Digitiser Reg 1 | 0 | 0 | 0 | 0 | 0 | 0 | POLL | CTC | ADCSEL | | | | | | COO | | 0000h | | |
| 76h | Digitiser Reg 2 | 0 | 0 | 0 | 0 | 0 | 0 | CR | DEL | | | | SLEN | | SLT | | 0006h | | | |
| 78h | Digitiser Reg 3 | PRP | | RPR | 45W | PDEN | PDPOL | WAIT | PIL | MSK | | RPU | | | | | | 0001h | | |
| 7Ah | Digitiser Read Back | PNDN | ADCSRC | | | | ADCD (TOUCHPANEL ADC Y DATA) | | | | | | | | | | | | 0000h | |
| 7Ch | Vendor ID1 | ASCII character "W" | | | | | | ASCII character "M" | | | | | | 574Dh | | | | | | |
| 7Eh | Vendor ID2 | ASCII character "L" | | | | | | Device Identifier | | | | | | 4C13h | | | | | | |

Table 68 WM9713L Register Map

Note:

Register 46h provides access to a sub-page address system to set the S_{PLL}[6:0] and K[21:0] register bits (see Table 6).

REGISTER BITS BY ADDRESS

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|----------|---------|---|--|
| 00h | 14:10 | SE [4:0] | 11000 | Indicates a codec from Wolfson Microelectronics | Intel's AC'97 Component Specification, Revision 2.2, page 50 |
| | 9:6 | ID9:6 | 0101 | Indicates 18 bits resolution for ADCs and DACs | |
| | 5 | ID5 | 1 | Indicates that the WM9713L supports bass boost | |
| | 4 | ID4 | 1 | Indicates that the WM9713L has a headphone output | |
| | 3 | ID3 | 0 | Indicates that the WM9713L does not support simulated stereo | |
| | 2 | ID2 | 1 | Indicates that the WM9713L supports bass and treble control | |
| | 1 | ID1 | 0 | Indicates that the WM9713L does not support modem functions | |
| | 0 | ID0 | 0 | Indicates that the WM9713L does not have a dedicated microphone ADC | |

Register 00h is a read-only register. Writing any value to this register resets all registers to their default, but does not change the contents of reg. 00h. Reading the register reveals information about the codec to the driver, as required by the AC'97 Specification, Revision 2.2

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|--------------|-------------------------------------|------------------------|
| 02h | 15 | MUL | 1 (mute) | Mutes SPKL | Analogue Audio Outputs |
| | 14 | ZCL | 0 (OFF) | Enables zero-cross detector on SPKL | |
| | 13:8 | SPKLVOL | 000000 (0dB) | SPKL volume | |
| | 7 | MUR | 1 (mute) | Mutes SPKR | |
| | 6 | ZCR | 0 (OFF) | Enables zero-cross detector on SPKR | |
| | 5:0 | SPKRVOL | 000000 (0dB) | SPKR volume | |

Register 02h controls the output pins SPKL and SPKR.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|--------------|------------------------------------|------------------------|
| 04h | 15 | MUL | 1 (mute) | Mutes HPL | Analogue Audio Outputs |
| | 14 | ZCL | 0 (OFF) | Enables zero-cross detector on HPL | |
| | 13:8 | HPL VOL | 000000 (0dB) | HPL volume | |
| | 7 | MUR | 1 (mute) | Mutes HPR | |
| | 6 | ZCR | 0 (OFF) | Enables zero-cross detector on HPR | |
| | 5:0 | HPR VOL | 000000 (0dB) | HPR volume | |

Register 04h controls the headphone output pins, HPL and HPR.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|--------------|-----------------------------|------------------------|
| 06h | 15 | MU4 | 1 (mute) | Mutes OUT4 | Analogue Audio Outputs |
| | 14 | ZC4 | 0 (OFF) | Enables zero-cross detector | |
| | 13:8 | OUT4VOL | 000000 (0dB) | OUT4 volume | |
| | 7 | MU3 | 1 (mute) | Mutes OUT3 | |
| | 6 | ZC3 | 0 (OFF) | Enables zero-cross detector | |
| | 5:0 | OUT3VOL | 000000 (0dB) | OUT3 volume | |

Register 06h controls the analogue output pins OUT3 and OUT4.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|-----------|--------------|---|--|
| 08h | 15 | M2H | 1 (mute) | Mutes MONOIN to headphone mixer paths | Analogue Inputs; Analogue Audio Outputs |
| | 14 | M2S | 1 (mute) | Mutes MONOIN to speaker mixer path | |
| | 12:8 | MONOINVOL | 01000 (0dB) | Controls MONOIN input gain to all mixers (but not to ADC) | |
| | 7 | MU | 1 (mute) | Mutes MONO. | |
| | 6 | ZC | 0 (OFF) | Enables zero-cross detector | |
| | 5:0 | MONOVOL | 000000 (0dB) | MONO volume | |

Register 08h controls the analogue output pin MONO and the analogue input pin MONOIN.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|----------|-------------|--|-----------------------------|
| 0Ah | 15 | L2H | 1 (mute) | Mutes LINE to headphone mixer paths | Analogue Inputs, Line Input |
| | 14 | L2S | 1 (mute) | Mutes LINE to speaker mixer path | |
| | 13 | L2M | 1 (mute) | Mutes LINE to mono mixer path | |
| | 12:8 | LINELVOL | 01000 (0dB) | Controls LINEL input gain to all mixers (but not to ADC) | |
| | 4:0 | LINERVOL | 01000 (0dB) | Controls LINER input gain to all mixers (but not to ADC) | |

Register 0Ah controls the analogue input pins LINEL and LINER.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|-------------|---|------------|
| 0Ch | 15 | D2H | 1 (mute) | Mutes DAC to headphone mixer path | Audio DACs |
| | 14 | D2S | 1 (mute) | Mutes DAC to speaker mixer path | |
| | 13 | D2M | 1 (mute) | Mutes DAC to mono mixer path | |
| | 12:8 | DACLVOL | 01000 (0dB) | Controls left DAC input gain to all mixers | |
| | 4:0 | DACRVOL | 01000 (0dB) | Controls right DAC input gain to all mixers | |

Register 0Ch controls the audio DACs (but not AUXDAC).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|-------------|--------------------------|--------------------------------------|
| 0Eh | 12:8 | MICAVOL | 01000 (0dB) | Controls MICA PGA volume | Analogue Inputs, Microphone Input |
| | 4:0 | MICBVOL | 01000 (0dB) | Controls MICB PGA volume | |

Register 0Eh controls the microphone PGA volume (MICA and MICB).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|----------|-----------|--|--------------------------------------|
| 10h | 7 | MA2M | 1 (mute) | Mutes MICA to mono mixer path | Analogue Inputs, Microphone Input |
| | 6 | MB2M | 1 (mute) | Mutes MICB to mono mixer path | |
| | 5 | MIC2MBST | 0 (OFF) | Enables 20dB gain boost at mono mixer for MICA and MICB | |
| | 4:3 | MIC2H | 11 (mute) | Controls microphone to headphone mixer paths. 00=stereo, 01=MICA only, 10=MICB only, 11=mute MICA and MICB | |
| | 2:0 | MIC2HVOL | 010 (0dB) | Controls gain of microphone to headphone mixer path | |

Register 10h controls the microphone routing (MICA and MICB).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|---------|--------------|---|------------------------|
| 12h | 15 | RMU | 1 (mute) | Mutes audio ADC input | Audio ADC, Record Gain |
| | 14 | GRL | 0 (standard) | Selects gain range for PGA of left ADC. 0=0...+22.5dB in 1.5dB steps, 1=-17.25...+30dB in 0.75dB steps | |
| | 13:8 | RECVOLL | 000000 (0dB) | Controls left ADC recording volume | |
| | 7 | ZC | 0 (OFF) | Enables zero-cross detector | |
| | 6 | GRR | 0 (standard) | Selects gain range for PGA of right ADC. 0=0...+22.5dB in 1.5dB steps, 1=-17.25...+30dB in 0.75dB steps | |
| | 5:0 | RECVOLR | 000000 (0dB) | Controls right ADC recording volume | |

Register 12h controls the record volume.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|--------|-----------|---|----------------------------|
| 14h | 15:14 | R2H | 11 (mute) | Controls record mux to headphone mixer paths. 00=stereo, 01=left ADC only, 10=right ADC only, 11=mute left and right | Audio ADC, Record Selector |
| | 13:11 | R2HVOL | 010 (0dB) | Controls gain of record mux l/r to headphone mixer paths | |
| | 10:9 | R2M | 11 (mute) | Controls record mux to mono mixer path. 00=stereo, 01=left rec mux only, 10=right rec mux only, 11=mute left and right | |
| | 8 | R2MBST | 0 (OFF) | Enables 20dB gain boost for record mux to mono mixer path | |
| | 6 | RECBST | 0 (OFF) | Enables 20dB gain boost for ADC record path | |
| | 5:3 | RECSL | 000 (mic) | Selects left record mux signal source: 000=MICA, 001=MICB, 010=LINEL, 011=MONOIN, 100=HPMIXL, 101=SPKMIC, 110=MONOMIX, 111=Reserved (Do not use) | |
| | 2:0 | RECSR | 000 (mic) | Selects right record mux signal source: 000=MICA, 001=MICB, 010=LINER, 011=MONOIN, 100=HPMIXR, 101=SPKMIC, 110=MONOMIX, 111=Reserved (Do not use) | |

Register 14h controls the record selector and the ADC to mono mixer path.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|--------|-----------|--|-------------------------------|
| 16h | 15 | B2H | 1 (mute) | Mutes PCBEEP to headphone mixer paths | Analogue Inputs, PCBEEP Input |
| | 14:12 | B2HVOL | 010 (0dB) | Controls gain of PCBEEP to headphone mixer paths | |
| | 11 | B2S | 1 (mute) | Mutes PCBEEP to speaker mixer path | |
| | 10:8 | B2SVOL | 010 (0dB) | Controls gain of PCBEEP to speaker mixer path | |
| | 7 | B2M | 1 (mute) | Mutes PCBEEP to mono mixer path | |
| | 6:4 | B2MVOL | 010 (0dB) | Controls gain of PCBEEP to mono mixer path | |

Register 16h controls the analogue input pin PCBEEP.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|--------|-----------|---|---------------------------------------|
| 18h | 15 | V2H | 1 (mute) | Mutes VXDAC to headphone mixer paths | Audio Mixers, Side Tone Control |
| | 14:12 | V2HVOL | 010 (0dB) | Controls gain of VXDAC to headphone mixer paths | |
| | 11 | V2S | 1 (mute) | Mutes VXDAC to speaker mixer path | |
| | 10:8 | V2SVOL | 010 (0dB) | Controls gain of VXDAC to speaker mixer path | |
| | 7 | V2M | 1 (mute) | Mutes VXDAC to mono mixer path | |
| | 6:4 | V2MVOL | 010 (0dB) | Controls gain of VXDAC to mono mixer path | |

Register 18h controls the output signal of the Voice DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|--------|-----------|--|---------------|
| 1Ah | 15 | A2H | 1 (mute) | Mutes AUXDAC to headphone mixer paths | Auxiliary DAC |
| | 14:12 | A2HVOL | 010 (0dB) | Controls gain of AUXDAC to headphone mixer paths | |
| | 11 | A2S | 1 (mute) | Mutes AUXDAC to speaker mixer path | |
| | 10:8 | A2SVOL | 010 (0dB) | Controls gain of AUXDAC to speaker mixer path | |
| | 7 | A2M | 1 (mute) | Mutes AUXDAC to mono mixer path | |
| | 6:4 | A2MVOL | 010 (0dB) | Controls gain of AUXDAC to mono mixer path | |

Register 1Ah controls the output signal of the auxiliary DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-------|------------|---|---------------------------|
| 1Ch | 15:14 | MONO | 00 (VMID) | MONO PGA input select: 00=Vmid; 01=no i/p (Z _H if buffer disabled); 10=MONOMIX; 11=INV1 | Analogue Audio Outputs |
| | 13:11 | SPKL | 000 (VMID) | SPKL PGA input select: 000=Vmid; 001=no i/p (Z _H if buffer disabled); 010=HPMIXL; 011=SPKMIX; 100=INV1; 101-111=unused | |
| | 10:8 | SPKR | 000 (VMID) | SPKR PGA input select: 000=Vmid; 001=no i/p (Z _H if buffer disabled); 010=HPMIXR; 011=SPKMIX; 100=INV2; 101-111=unused | |
| | 7:6 | HPL | 00 (VMID) | HPL PGA input select: 00=Vmid; 01=no i/p (Z _H if buffer disabled); 10=HPMIXL; 11=unused | |
| | 5:4 | HPR | 00 (VMID) | HPR PGA input select: 00=Vmid; 01=no i/p (Z _H if buffer disabled); 10=HPMIXR; 11=unused | |
| | 3:2 | OUT3 | 00 (VMID) | OUT3 PGA input select: 00=Vmid; 01=no i/p (Z _H if buffer disabled); 10=INV1; 11=unused | |
| | 1:0 | OUT4 | 00 (VMID) | OUT4 PGA input select: 00=Vmid; 01=no i/p (Z _H if buffer disabled); 10=INV2; 11=unused | |

Register 1Ch controls the inputs to the output PGAs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|---------|-----------------------|--|---|
| 1Eh | 15:13 | INV1 | 000 (Z _H) | INV1 input select: 000=Z _H (OFF – no source selected); 001=MONOMIX; 010=SPKMIX; 011=HPMIXL; 100=HPMIXR; 101=HPMIXMONO; 110=unused; 111=Vmid | Audio DACs, 3D Stereo Enhancement; Analogue Audio Outputs |
| | 12:10 | INV2 | 000 (Z _H) | INV2 input select: 000=Z _H (OFF – no source selected); 001=MONOMIX; 010=SPKMIX; 011=HPMIXL; 100=HPMIXR; 101=HPMIXMONO; 110=unused; 111=Vmid | |
| | 5 | 3DLC | 0 (low) | Selects lower cut-off frequency | |
| | 4 | 3DUC | 0 (high) | Selects upper cut-off frequency | |
| | 3:0 | 3DDEPTH | 0000 (0%) | Controls depth of 3D effect | |

Register 1Eh controls 3D stereo enhancement for the audio DACs and input muxes to the output inverters INV1 and INV2.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|-------|------------|--|---|
| 20h | 15 | BB | 0 (linear) | Selects linear bass control or adaptive bass boost | Audio DACs, Tone Control / Bass Boost |
| | 12 | BC | 0 (low) | Selects bass cut-off frequency | |
| | 11:8 | BASS | 1111 (OFF) | Controls bass intensity | |
| | 6 | DAT | 0 (OFF) | Enables 6dB pre-DAC attenuation | |
| | 4 | TC | 0 (high) | Selects treble cut-off frequency | |
| | 3:0 | TRBL | 1111 (OFF) | Controls treble intensity | |

Register 20h controls the bass and treble response of the left and right audio DAC (but not AUXDAC).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|------------|--------------|--|--|
| 22h | 15:14 | MICCOMPSEL | 00 (mics) | Selects input function for MIC2A/COMP1 and MIC2B/COMP2 | Analogue Inputs, Microphone Input |
| | 13:12 | MPASEL | 00 (MIC1) | Selects input to MICA preamp (from MIC1, MIC2A, MIC2B) | |
| | 11:10 | MPABST | 00 (12dB) | Controls MICA preamp gain boost | |
| | 9:8 | MPBBST | 00 (12dB) | Controls MICB preamp gain boost | |
| | 7 | MBOP2EN | 0 (Off) | Enables microphone bias output path to pin 12 | |
| | 6 | MBOP1EN | 1 (On) | Enables microphone bias output path to MICBIAS | |
| | 5 | MBVOL | 0 (0.9xAVDD) | Selects microphone bias voltage | |
| | 4:2 | MCDTHR | 000 (100uA) | Controls microphone current detect threshold | |
| | 1:0 | MCDSCTHR | 00 (600uA) | Controls microphone short-circuit detect threshold | |

Register 22h controls the microphone input configuration and microphone bias and detect configuration.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-----------|---------|---|---------------------------|
| 24h | 4 | JIEN | 0 (OFF) | Jack insert detect enable | Analogue Audio Outputs |
| | 3:2 | DCDRVSEL | 00 (AC) | Output PGA source for headphone DC reference (default is AC coupled – no source selected) | |
| | 1:0 | EARSPKSEL | 00 | Ear speaker source select (default is no source selected) | |

Register 24h controls the output volume mapping on headphone jack insertion.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|---|---|---------------------|
| 26h | 14 | PR6 | 1 (OFF) | Disables all output PGAS | Power Management |
| | 13 | PR5 | 1 (OFF) | Disables internal clock | |
| | 12 | PR4 | 1 (OFF) | Disables AC-link interface (external clock off) | |
| | 11 | PR3 | 1 (OFF) | Disables VREF, input PGAs, DACs, ADCs, mixers and outputs | |
| | 10 | PR2 | 1 (OFF) | Disables input PGAs and mixers | |
| | 9 | PR1 | 1 (OFF) | Disables stereo DAC | |
| | 8 | PR0 | 1 (OFF) | Disables stereo ADCs and record mux PGA | |
| | 3 | REF | 0 | Read-only bit, indicates VREF is ready (inverse of PR3) | |
| | 2 | ANL | 0 | Read-only bit, indicates analogue mixers are ready (inverse of PR2) | |
| | 1 | DAC | 0 | Read-only bit, indicates stereo DAC is ready (inverse of PR1) | |
| 0 | ADC | 0 | Read-only bit, indicates stereo ADC is ready (inverse of PR0) | | |

Register 26h is for power management according to the AC'97 specification. Note that the actual state of many circuit blocks depends on both register 26h AND registers 3Ch and 3Eh.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-------|---------|--|--|
| 28h | 15:14 | ID | 00 | Indicates that the WM9713L is configured as the primary codec in the system. | Intel's AC'97 Component Specification, Revision 2.2, page 59 |
| | 11:10 | REV | 01 | Indicates that the WM9713L conforms to AC'97 Rev2.2 | |
| | 9 | AMAP | 0 | Indicates that the WM9713L does not support slot mapping | |
| | 8 | LDAC | 0 | Indicates that the WM9713L does not have an LFE DAC | |
| | 7 | SDAC | 0 | Indicates that the WM9713L does not have Surround DACs | |
| | 6 | CDAC | 0 | Indicates that the WM9713L does not have a Centre DAC | |
| | 3 | VRM | 0 | Indicates that the WM9713L does not have a dedicated, variable rate microphone ADC | |
| | 2 | SPDIF | 1 | Indicates that the WM9713L supports SPDIF output | |
| | 1 | DRA | 0 | Indicates that the WM9713L does not support double rate audio | |
| | 0 | VRA | 1 | Indicates that the WM9713L supports variable rate audio | |

Register 28h is a read-only register that indicates to the driver which advanced AC'97 features the WM9713L supports.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|-----------------|--|------------------------------|
| 2Ah | 10 | SPCV | 1 (valid) | SPDIF validity bit (read-only) | Digital Audio (SPDIF) Output |
| | 5:4 | SPSA | 01 (slots 6, 9) | Controls SPDIF slot assignment. 00=slots 3 and 4, 01=6/9, 10=7/8, 11=10/11 | |
| | 2 | SEN | 0 (OFF) | Enables SPDIF output enable | |
| | 0 | VRA | 0 (OFF) | Enables variable rate audio | |

Register 2Ah controls the SPDIF output and variable rate audio.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|----------|---------|------------------------------------|--|
| 2Ch | all | DACSR | BB80h | Controls stereo DAC sample rate | Variable Rate Audio / Sample Rate Conversion |
| 2Eh | all | AUXDACSR | BB80h | Controls auxiliary DAC sample rate | |
| 32h | all | ADCSR | BB80h | Controls audio ADC sample rate | |

Note: The VRA bit in register 2Ah must be set first to obtain sample rates other than 48kHz

Registers 2Ch, 2Eh 32h and control the sample rates for the stereo DAC, auxiliary DAC and audio ADC, respectively.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-------|-----------------------|---|-----------|
| 36h | 15 | CTRL | 0 (GPIO reg) | Specifies how the PCM interface pins are controlled. | PCM Codec |
| | 14:13 | MODE | 10 (master mode) | PCM interface mode when PCMCTRL=1 | |
| | 11:9 | DIV | 010 (1/4) | Voice DAC clock to PCMCLK divider reserved | |
| | 7 | CP | 0 (normal) | PCMCLK polarity | |
| | 6 | FSP | 0 | right, left and I ² S modes – PCMFS polarity DSP Mode – mode A/B select | |
| | 5:4 | SEL | 00 (LandR data) | PCM ADC channel select | |
| | 3:2 | WL | 10 (24 bits) | PCM Data Word Length | |
| | 1:0 | FMT | 10 (I ² S) | PCM Data Format Select | |

Register 36h controls the PCM codec.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-------|--|---|------------------------------|
| 3Ah | 15 | V | 0 | Validity bit; '0' indicates frame valid, '1' indicates frame not valid | Digital Audio (SPDIF) Output |
| | 14 | DRS | 0 | Indicates that the WM9713L does not support double rate SPDIF output (read-only) | |
| | 13:12 | SPSR | 10 | Indicates that the WM9713L only supports 48kHz sampling on the SPDIF output (read-only) | |
| | 11 | L | 0 | Generation level; programmed as required by user | |
| | 10:4 | CC | 0000000 | Category code; programmed as required by user | |
| | 3 | PRE | 0 | Pre-emphasis; '0' indicates no pre-emphasis, '1' indicates 50/15us pre-emphasis | |
| | 2 | COPY | 0 | Copyright; '0' indicates copyright is not asserted, '1' indicates copyright | |
| | 1 | AUDIB | 0 | Non-audio; '0' indicates data is PCM, '1' indicates non-PCM format (e.g. DD or DTS) | |
| 0 | PRO | 0 | Professional; '0' indicates consumer, '1' indicates professional | | |

Register 3Ah Read/Write. Controls the SPDIF output.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|---------|---------------------|------------------------------------|------------------|
| 3Ch | 15 | PD15 | 1 (OFF) | Touchpanel / PenADC power down | Power Management |
| | 14 | VMID1M | 1 (OFF) | Disables 1Meg Vmid resistor string | |
| | 13 | TSHUT | 1 (OFF) | Disables thermal shutdown | |
| | 12 | VXDAC | 1 (OFF) | Disables VXDAC | |
| | 11 | AUXDAC | 1 (OFF) | Disables AUXDAC | |
| | 10 | VREF | 1 (OFF) | Disables reference generator | |
| | 9 | PLL | 1 (OFF) | Disables PLL | |
| | 7 | DACL | 1 (OFF) | Disables left DAC | |
| | 6 | DACR | 1 (OFF) | Disables right DAC | |
| | 5 | ADCL | 1 (OFF) | Disables left ADC | |
| | 4 | ADCR | 1 (OFF) | Disables right ADC | |
| | 3 | HPLX | 1 (OFF) | Disables left headphone mixer | |
| | 2 | HPRX | 1 (OFF) | Disables right headphone mixer | |
| | 1 | SPKX | 1 (OFF) | Disables speaker mixer | |
| 0 | MX | 1 (OFF) | Disables mono mixer | | |

* "0" corresponds to "ON", if and only if the corresponding bit in register 26h is also 0.

Register 3Ch is for power management additional to the AC'97 specification. Note that the actual state of each circuit block depends on both register 3Ch AND register 26h.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|---------|--------------------------|------------------------------------|------------------|
| 3Eh | 15 | MCD | 1 (OFF) | Disables microphone current detect | Power Management |
| | 14 | MICBIAS | 1 (OFF) | Disables microphone bias | |
| | 13 | MONO | 1 (OFF) | Disables MONO output PGA | |
| | 12 | OUT4 | 1 (OFF) | Disables OUT4 output PGA | |
| | 11 | OUT3 | 1 (OFF) | Disables OUT3 output PGA | |
| | 10 | HPL | 1 (OFF) | Disables HPL output PGA | |
| | 9 | HPR | 1 (OFF) | Disables HPR output PGA | |
| | 8 | SPKL | 1 (OFF) | Disables SPKL output PGA | |
| | 7 | SPKR | 1 (OFF) | Disables SPKR output PGA | |
| | 6 | LL | 1 (OFF) | Disables LINEL PGA | |
| | 5 | LR | 1 (OFF) | Disables LINER PGA | |
| | 4 | MOIN | 1 (OFF) | Disables MONOIN PGA | |
| | 3 | MA | 1 (OFF) | Disables mic PGA MA | |
| | 2 | MB | 1 (OFF) | Disables mic PGA MB | |
| | 1 | MPA | 1 (OFF) | Disables mic pre-amp MPA | |
| 0 | MPB | 1 (OFF) | Disables mic pre-amp MPB | | |

* "0" corresponds to "ON", if and only if the corresponding bit in register 26h is also 0.

Register 3Eh is for power management additional to the AC'97 specification. Note that the actual state of each circuit block depends on both register 3Eh AND register 26h.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|---------|--|--|
| 40h | 13 | 3DE | 0 (OFF) | Enables 3D enhancement | Audio DACs, 3D Stereo Enhancement |
| | 7 | LB | 0 (OFF) | Enables loopback (i.e. feed ADC output data directly into DAC) | Intel's AC'97 Component Specification, Revision 2.2, page 55 |

Register 40h is a "general purpose" register as defined by the AC'97 specification. Only two bits are implemented in the WM9713L.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|---------|------------------------------------|----------------------------------|
| 42h | 6 | MONO | 0 (Off) | Enables fast power for MONO output | Analogue Audio Outputs, Power-Up |
| | 5 | SPKL | 0 (Off) | Enables fast power for SPKL output | |
| | 4 | SPKR | 0 (Off) | Enables fast power for SPKR output | |
| | 3 | HPL | 0 (Off) | Enables fast power for HPL output | |
| | 2 | HPR | 0 (Off) | Enables fast power for HPR output | |
| | 1 | OUT3 | 0 (Off) | Enables fast power for OUT3 output | |
| | 0 | OUT4 | 0 (Off) | Enables fast power for OUT4 output | |

Register 42h controls power-up conditions for output PGAs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----------|------------------------|--------------|--|------------------|
| 44h | 14:1 2 | S _{EXT} [6:4] | 000 (div 1) | Defines clock division ratio for Hi-fi block: 000=f; 001=f/2; ... ; 111=f/8 | Clock Generation |
| | 11:8 | S _{EXT} [3:0] | 0000 (div 1) | Defines clock division ratio for voice DAC clock: 0000=f; 0001=f/2; ... ; 1111=f/16 | |
| | 7 | CLKSRC | 1 (ext clk) | Selects between PLL clock and External clock | |
| | 5:3 | PENDIV | 000 (div 16) | Sets AUXADC clock divisor: 000=f/16; 001=f/12; 010=f/8; 011=f/6; 100=f/4; 101=f/3; 110=f/2; 111=f | |
| | 2 | CLKBX2 | 0 (Off) | Clock doubler for MCLKB | |
| | 1 | CLKAX2 | 0 (Off) | Clock doubler for MCLKA | |
| | 0 | CLKMUX | 0 (MCLKA) | Selects between MCLKA and MCLKB (N.B. On power-up clock must be present on MCLKA and must be active for 2 clock cycles after switching to MCLKB) | |

Register 44h controls clock division and muxing.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----------|--------|---------|---|----------------------------------|
| 46h | 15:1 2 | N[3:0] | 0000 | PLL integer division control (must be set between 5-12 for integer N mode) | Analogue Audio Outputs, Power-Up |
| | 11 | LF | 0 = off | Allows PLL operation with low frequency input clocks (< 8.192MHz) | |
| | 10 | SDM | 0 | Sigma Delta Modulator enable. Allows fractional N division | |
| | 9 | DIVSEL | 0 = off | Enables input clock to PLL to be divided by 2 or 4. Use if input clock is above 14.4MHz | |
| | 8 | DIVCTL | 0 | Controls division mode when DIVSEL is high. 0 = div by 2, 1 = div by 4. | |
| | 6:4 | PGADDR | 000 | Pager address bits to access programming of K[21:0] and S _{PLL} [6:0] | |
| | 3:0 | PGDATA | 0000 | Pager data bits | |

Register 46h controls PLL clock generation.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO | |
|------------------|-----|----------------------------------|---------------------------------------|--|----------------------------|--|
| 4Ch | | please refer to the register map | all 1 (all inputs) except unused bits | Controls GPIO configuration as inputs or as outputs (note: virtual GPIOs can only be inputs) | GPIO and Interrupt Control | |
| 4Eh | | | all 1 | Controls GPIO polarity (actual polarity depends on register 4Ch AND register 4Eh) | | |
| 50h | | | all 0 (not sticky) | Makes GPIO signals sticky | | |
| 52h | | | all 0 (OFF) | Enables wake-up for each GPIO signal | | |
| 54h | | | = status of GPIO inputs | GPIO pin status (read from inputs, write '0' to clear sticky bits) | | |
| | 15 | | | | | Controls Comparator 1 signal (virtual GPIO) |
| | 14 | | | | | Controls Comparator 2 signal (virtual GPIO) |
| | 13 | | | | | Controls Pen-Down Detector signal (virtual GPIO) |
| | 12 | | | | | Controls ADA signal (virtual GPIO) |
| | 11 | | | | | Controls Thermal sensor signal (virtual GPIO) |
| | 10 | | | | | Controls Microphone short detect (virtual GPIO) |
| | 9 | | | | | Controls Microphone insert detect (virtual GPIO) |
| | 8 | | | | | Controls GPIO8 (pin 3) |
| | 7 | | | | | Controls GPIO7 (pin 11) |
| | 6 | | | | | Controls GPIO6 (pin 12) |
| | 5 | | | | | Controls GPIO5 (pin 48) |
| | 4 | | | | | Controls GPIO4 (pin 47) |
| | 3 | | | Controls GPIO3 (pin 46) | | |
| | 2 | | | Controls GPIO2 (pin 45) | | |
| | 1 | | | Controls GPIO1 (pin 44) | | |

Register 4Ch to 54h control the GPIO pins and virtual GPIO signals.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-----|-------|----------|---|----------------------------|
| 56h | 8 | GE8 | 1 (GPIO) | Selects between GPIO8 and SPDIF_OUT function for pin 12 | GPIO and Interrupt Control |
| | 7 | GE7 | 1 (GPIO) | Selects between GPIO7 and PENDOWN function for pin 11 | |
| | 6 | GE6 | 1 (GPIO) | Selects between GPIO6 and ADA/MASK functions for pin 3 | |
| | 5 | GE5 | 1 (GPIO) | Selects between GPIO5 and SPDIF_OUT function for pin 48 | |
| | 4 | GE4 | 1 (GPIO) | Selects between GPIO4 and ADA/MASK functions for pin 47 | |
| | 3 | GE3 | 1 (GPIO) | Selects between GPIO3 and PENDOWN function for pin 46 | |
| | 2 | GE2 | 1 (GPIO) | Selects between GPIO2 and IRQ function for pin 45 | |

Register 56h controls the use of GPIO pins for non-GPIO functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|-------|----------|--|----------------------------|
| 58h | 15:8 | PU | 01000000 | Enables weak pull-up on GPIO pins (1=On) | GPIO and Interrupt Control |
| | 7:0 | PD | 00000000 | Enables weak pull-down on GPIO pins (1=On) | |

Register 58h controls GPIO pull-up/down.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|----------|---|--|---------------------------------|
| 5Ah | 15:13 | COMP2DEL | 000 (no delay) | Selects Comparator 2 delay | Battery Alarm |
| | 8 | RSTDIS | 0 (RESETB enabled) | Disables RESETB pin to enable use as a GPIO | GPIO Interrupt and Control |
| | 7:6 | JSEL | 00 (GPIO1) | Selects GPIO for jack insert detect: 00: GPIO1 01: GPIO6 10: GPIO7 11: GPIO8 | Jack Insertion & Auto-Switching |
| | 5:4 | HPMODE | 00 | HPF corner frequency 00: 7Hz @ Fs=48kHz 01: 82Hz @ Fs=16kHz 10: 82Hz @ Fs=8kHz 11: 170Hz @ Fs=8kHz | Audio ADCs |
| | 3:2 | DIE REV | Indicates device revision. 00=Rev.A, 01=Rev.B, 10=Rev.C | | N/A |
| | 1 | WAKEEN | 0 (no wake-up) | Enables GPIO wake-up | GPIO and Interrupt Control |
| | 0 | IRQ INV | 0 (not inverted) | Inverts the IRQ signal (pin 45) | |

Register 5Ah controls several additional functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-------|--|---|------------------------------|
| 5Ch | 15 | AMUTE | 0 | Read-only bit to indicate DAC auto-muting | Audio DACs, Stereo DACs |
| | 14 | C1REF | 0 (AVDD/2) | Selects Comparator 1 Reference Voltage | Battery Alarm |
| | 13:12 | C1SRC | 00 (OFF) | Selects Comparator 1 Signal Source | |
| | 11 | C2REF | 0 (AVDD/2) | Selects Comparator 1 Reference Voltage | |
| | 10:9 | C2SRC | 00 (OFF) | Selects Comparator 1 Signal Source | |
| | 7 | AMEN | 0 (OFF) | Enables DAC Auto-Mute | |
| | 6:5 | VBIAS | 00 | Selects analogue bias for lowest power, depending on AVDD supply. 0X=3.3V, 10=2.5V, 11=1.8V | Power Management |
| | 4 | ADCO | 0 | Selects source of SPDIF data. 0=from SDATAOUT, 1= from audio ADC | Digital Audio (SPDIF) Output |
| | 3 | HPF | 0 | Disables ADC high-pass filter | Audio ADC |
| 1:0 | ASS | 00 | Selects time slots for stereo ADC data. 00=slots 3 and 4, 01=7/8, 10=6/9, 11=10/11 | Audio ADC, ADC Slot Mapping | |

Register 5Ch controls several additional functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|---------------|-----------------|---|--|
| 60h | 15:12 | ALCL | 1011 (-12dB) | Controls ALC threshold | Audio ADC, Automatic Level Control |
| | 11:8 | HLD | 0000 (0 ms) | Controls ALC hold time | |
| | 7:4 | DCY | 0011 (192 ms) | Controls ALC decay time | |
| | 3:0 | ATK | 0010 (24 ms) | Controls ALC attack time | |
| 62h | 15:14 | ALCSEL | 00 (OFF) | Controls which channel ALC operates on. 00=none, 01=right only, 10=left only, 11=both | |
| | 13:11 | MAXGAIN | 111 (+30dB) | Controls upper gain limit for ALC | |
| | 10:9 | ZC TIMEOUT | 11 (slowest) | Controls time-out for zero-cross detection | |
| | 7 | NGAT | 0 (OFF) | Enables noise gate function | |
| | 5 | NGG | 0 (hold gain) | Selects noise gate type. 0=hold gain, 1=mute | |
| | 4:0 | NGTH | 00000 (-76.5dB) | Controls noise gate threshold | |

Registers 60h and 62h control the ALC and Noise Gate functions.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|-----------|--------------|---|---------------|
| 64h | 15 | XSLE | 0 | Selects input for AUXDAC. 0=from AUXDACVAL (for DC signals), 1=from AC-Link slot (for AC signals) | Auxiliary DAC |
| | 14:12 | AUXDACSLT | 000 (Slot 5) | Selects input slot for AUXDAC (with XSLE=1) | |
| | 11:0 | AUXDACVAL | 000000000 | AUXDAC Digital Input for AUXDAC (with XSLE=0). 000h= minimum, FFFh=full-scale | |

Register 64h controls the input signal of the auxiliary DAC.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|-------|------------------|---------------|--|----------------------|
| 74h | 9 | POLL | 0 | Writing "1" initiates a measurement (when CTC is not set) | |
| | 8 | CTC | 0 | 0=Polling mode; 1=Continuous mode (for DMA) | |
| | 7 | ADCSEL_AUX4 | 0 | Enable COMP1/AUX4 measurement (pin32) | |
| | 6 | ADCSEL_AUX3 | 0 | Enable COMP1/AUX3 measurement (pin31) | |
| | 5 | ADCSEL_AUX2 | 0 | Enable COMP1/AUX2 measurement (pin30) | |
| | 4 | ADCSEL_AUX1 | 0 | Enable COMP1/AUX1 measurement (pin29) | |
| | 3 | ADCSEL_PRES SURE | 0 | Enable touchpanel pressure measurement | |
| | 2 | ADCSEL_Y | 0 | Enable touchpanel Y co-ord measurement | |
| | 1 | ADCSEL_X | 0 | Enable touchpanel X co-ord measurement | |
| | 0 | COO | 0 (OFF) | Enables co-ordinate mode | Touchpanel Interface |
| 76h | 9:8 | CR | 00 (93.75Hz) | Controls conversion rate in continuous mode | |
| | 7:4 | DEL | 0000 (20.8µs) | Controls touchpanel settling time | |
| | 3 | SLEN | 1 | Enables slot readback of touchpanel data | |
| | 2:0 | SLT | 110 (slot 11) | Selects time slot for readback of touchpanel data | |
| 78h | 15:14 | PRP | 00 | Selects mode of operation. 00=OFF, 01=pen detect with wake-up, 10=pen detect without wake-up, 11=running | |
| | 13 | RPR | 0 | Selects wake-up mode. 0=AC-Link only, 1=AC-Link and WM9713L auto-wake-up | |
| | 12 | 45W | 0 (4-wire) | Selects 4-wire or 5-wire touchpanel | |
| | 11 | PDEN | 0 (always) | Selects when touchpanel measurements take place. 0=always, 1=only when pen is down | |
| | 10 | PDPOL | 0 | PENDOWN polarity: 0=non-inverted; 1=inverted | |
| | 9 | WAIT | 0 | Controls data readback from register 7Ah. 0=overwrite old data with new, 1=wait until old data has been read | |
| | 8 | PIL | 0 (200µA) | Controls current used for pressure measurement. 1=400µA | |
| | | 7:6 | MSK | 00 (OFF) | |
| | 5:0 | RPU | 000001 (64kΩ) | Controls internal pull-up resistor for pen-down detection | |
| 7Ah read only | 15 | PNDN | 0 (pen up) | Indicates pen status. | |
| | 14:12 | ADCSRC | 000 (none) | Indicates measurement type | |
| | 11:0 | ADCD | 000h | Returns data from touchpanel / AUXADC | |

Registers 76h, 78h and 7Ah control the touchpanel interface.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | REFER TO |
|------------------|------|--------|---------|---------------------------------|--|
| 7Ch | 15:8 | F7:0 | 57h | ASCII character "W" for Wolfson | Intel's AC'97 Component Specification, Revision 2.2, page 50 |
| | 7:0 | S7:0 | 4Dh | ASCII character "M" | |
| 7Eh | 15:8 | T7:0 | 4Ch | ASCII character "L" | |
| | 7:0 | REV7:0 | 13h | Device identifier | |

Register 7Ch and 7Eh are read-only registers that indicate to the driver that the codec is a WM9713L.

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

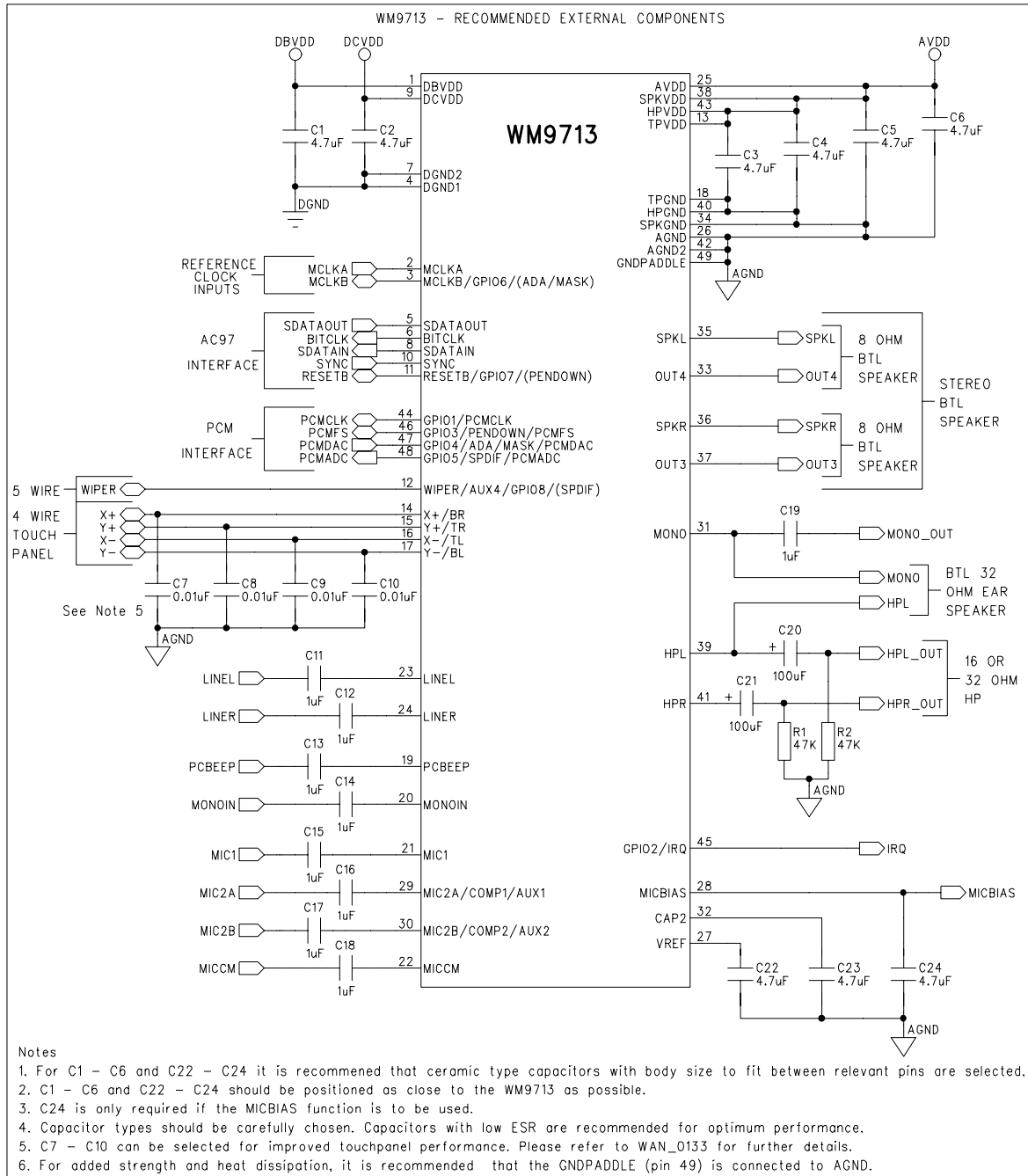


Figure 34 Recommended External Component Diagram

LINE OUTPUT

The headphone outputs, HPL and HPR, can be used as stereo line outputs. The speaker outputs, SPKL and SPKR, can also be used as line outputs. Recommended external components are shown below.

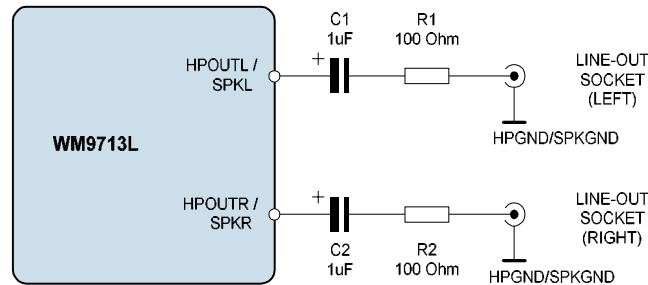


Figure 35 Recommended Circuit for Line Output

The DC blocking capacitors and the load resistance together determine the lower cut-off frequency, f_c . Assuming a 10 kΩ load and $C_1, C_2 = 10\mu\text{F}$:

$$f_c = 1 / 2\pi (R_L + R_1) C_1 = 1 / (2\pi \times 10.1\text{k}\Omega \times 1\mu\text{F}) = 16 \text{ Hz}$$

Increasing the capacitance lowers f_c , improving the bass response. Smaller values of C_1 and C_2 will diminish the bass response. The function of R_1 and R_2 is to protect the line outputs from damage when used improperly.

AC-COUPLED HEADPHONE OUTPUT

The circuit diagram below shows how to connect a stereo headphone to the WM9713L.

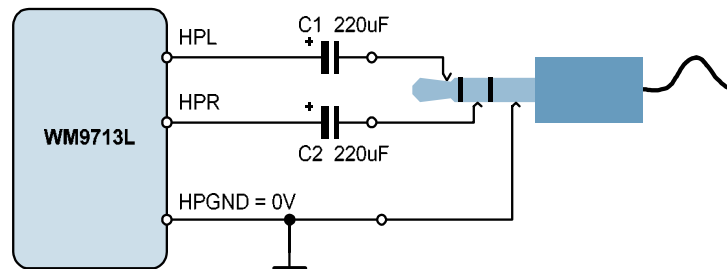


Figure 36 Simple Headphone Output Circuit Diagram

The DC blocking capacitors C_1 and C_2 together with the load resistance determine the lower cut-off frequency, f_c . Increasing the capacitance lowers f_c , improving the bass response. Smaller capacitance values will diminish the bass response. For example, with a 16Ω load and $C_1 = 220\mu\text{F}$:

$$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 16\Omega \times 220\mu\text{F}) = 45 \text{ Hz}$$

DC COUPLED (CAPLESS) HEADPHONE OUTPUT

In the interest of saving board space and cost, it may be desirable to eliminate the 220 μ F DC blocking capacitors. This can be achieved by using OUT3 as a headphone pseudo-ground, as shown below.

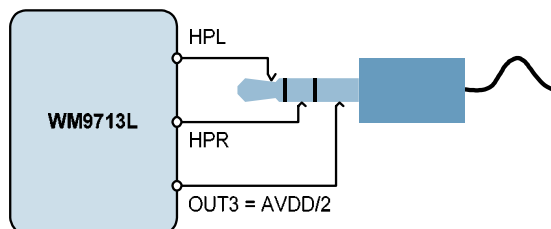


Figure 37 Capless Headphone Output Circuit Diagram

As the OUT3 pin produces a DC voltage of AVDD/2, there is no DC offset between HPL/HPR and OUT3, and therefore no DC blocking capacitors are required. However, this configuration has some drawbacks:

The power consumption of the WM9713L is increased, due to the additional power consumed in the OUT3 output buffer.

If the DC coupled output is connected to the line-in of a grounded piece of equipment, then OUT3 becomes short-circuited. Although the built-in short circuit protection will prevent any damage to the WM9713L, the audio signal will not be transmitted properly.

OUT3 cannot be used for another purpose

BTL LOUDSPEAKER OUTPUT

SPKL and SPKR can differentially drive a mono 8 Ω loudspeaker as shown below.

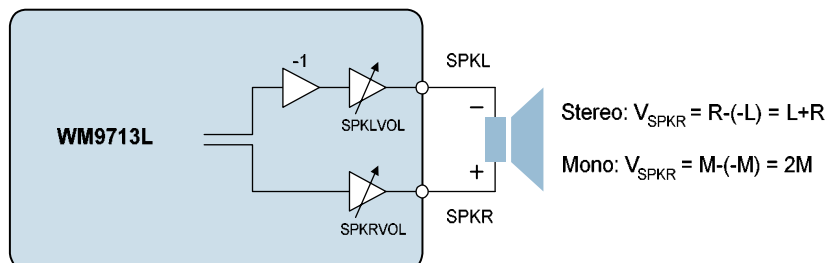


Figure 38 Speaker Output Connection (INV = 1)

To drive out differentially one of the speaker outputs must be inverted using INV1 or INV2.

COMBINED HEADSET / BTL EAR SPEAKER

In smartphone applications with a loudspeaker and separate ear speaker (receiver), a BTL ear speaker can be connected at the OUT3 pin, as shown below.

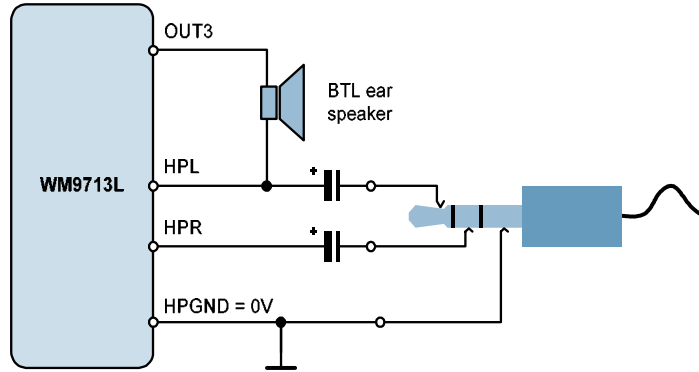


Figure 39 Combined Headset / BTL Ear Speaker

The ear speaker and the headset play the same signal. Whenever the headset is plugged in, the headphone outputs are enabled and OUT3 disabled. When the headset is not plugged in, OUT3 is enabled (see “Jack Insertion and Auto-Switching”)

COMBINED HEADSET / SINGLE-ENDED EAR SPEAKER

Instead of a BTL ear speaker, a single-ended ear speaker can also be used, as shown below.

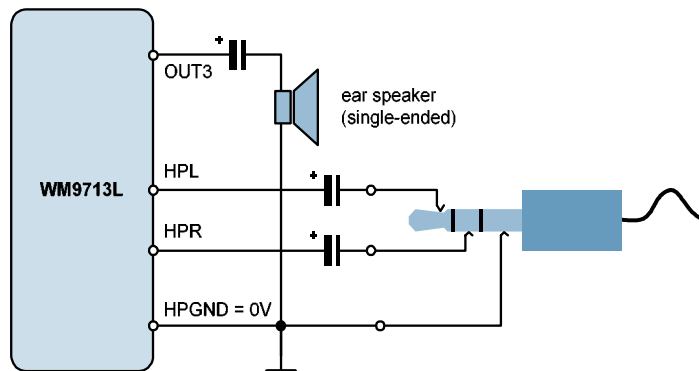


Figure 40 Combined Headset / Single-ended Ear Speaker

JACK INSERT DETECTION

The circuit diagram below shows how to detect when a headphone or headset has been plugged into the headphone socket. It generates an interrupt, instructing the controller to enable HPL and HPR and disable OUT3.

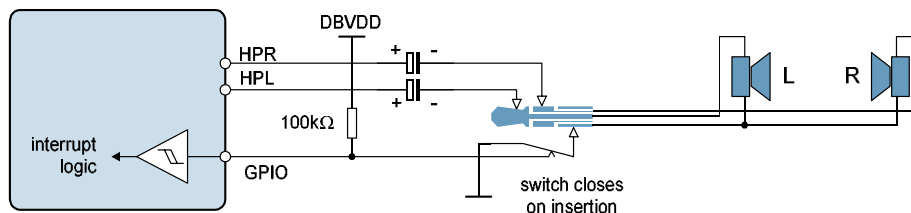


Figure 41 Jack Insert Detection Circuit

The circuit requires a headphone socket with a switch that closes on insertion (for using sockets with a switch that opens on insertion, please refer to Application Note WAN0182). It detects both headphones and phone headsets. Any GPIO pin can be used, provided that it is configured as an input.

HOOKSWITCH DETECTION

Alternatively a headphone socket with a switch that opens on insertion can be used. For this mode of operation the GPIO input must be inverted.

The circuit diagram below shows how to detect when the “hookswitch” of a phone headset is pressed (pressing the hookswitch is equivalent to lifting the receiver in a stationary telephone).

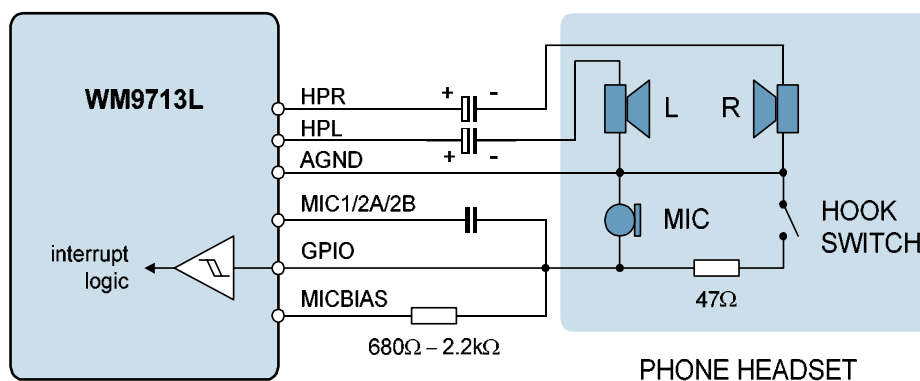


Figure 42 Hookswitch Detection Circuit

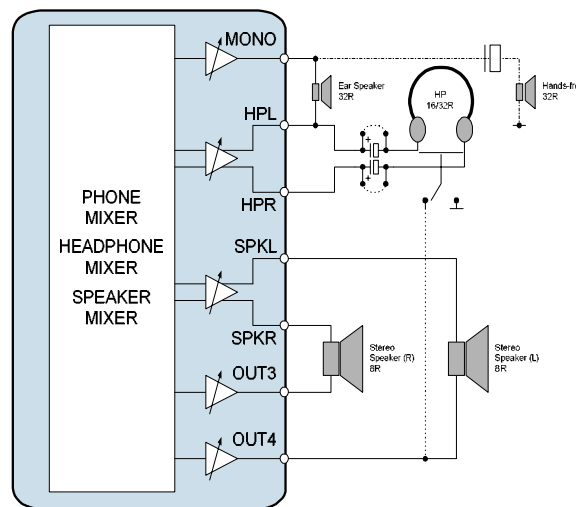
The circuit uses a GPIO pin as a sense input. The impedance of the microphone and the resistor in the MICBIAS path must be such that the potential at the GPIO pin is above $0.7 \times \text{DBVDD}$ when the hookswitch is open, and below $0.3 \times \text{DBVDD}$ when it is closed.

TYPICAL OUTPUT CONFIGURATIONS

The WM9713L has three outputs capable of driving loads down to 16Ω (headphone / line drivers) – HPL, HPR and MONO - and four outputs capable of driving loads down to 8Ω (loudspeaker / line drivers) – SPKL, SPKR, OUT3 and OUT4. The combination of output drivers, mixers and mixer inverters means that many output configurations can be supported. Below are some examples of typical output configurations for smartphone applications.

STEREO SPEAKER

Figure 43 shows a typical output configuration for stereo speakers with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).

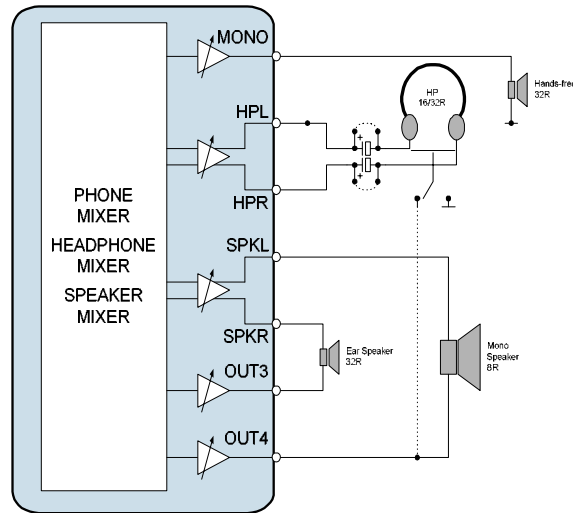


| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Stereo Speaker | Headphone |
|-------------------|------------------------|--------------------------|-------------------------|--------------------------|------------------------------|------------------------------|-------------------|---------------------|
| mono | mmix | spkmix | mmix | -hpmixR | mmix | -hpmixR | - | Z _H |
| spkl | - | - | - | - | hpmixL | hpmixL | hpmixL | (Z _L) |
| spkr | - | - | - | - | hpmixR | hpmixR | hpmixR | - |
| hpl | Z _H | Z _H | V _{mid} | hpmixL | V _{mid} | hpmixL | - | hpmixL |
| hpr | - | - | - | - | - | - | - | hpmixR |
| out3 | - | - | - | - | -hpmixR | -hpmixR | -hpmixR | - |
| out4 | - | - | - | - | -hpmixL | -hpmixL | -hpmixL | (V _{mid}) |

Figure 43 Stereo Speaker Output Configuration

MONO SPEAKER

Figure 44 shows a typical output configuration for mono speaker with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).



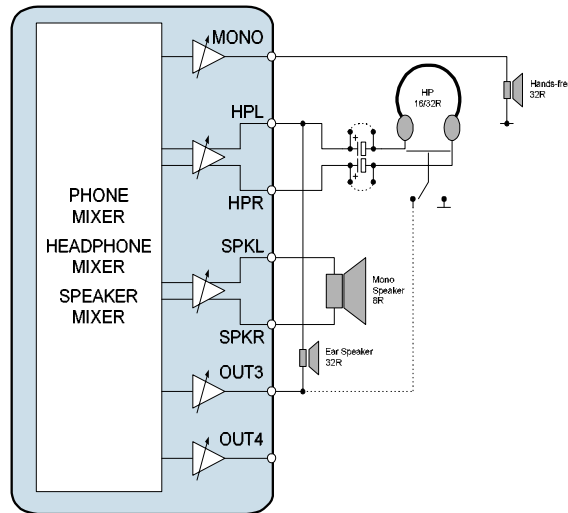
| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Mono Speaker | Headphone |
|-------------------|------------------------|--------------------------|-------------------------|--------------------------|------------------------------|------------------------------|-----------------|---------------------|
| mono | mmix | spkmix | - | - | - | - | - | - |
| spkl | - | - | - | - | hpmixL | hpmixL | spkmix | (Zt) |
| spkr | - | - | mmix | hpmixR | mmix | hpmixR | - | - |
| hpl | - | - | - | - | - | - | - | hpmixL |
| hpr | - | - | - | - | - | - | - | hpmixR |
| out3 | - | - | -mmix | -hpmixL | -mmix | -hpmixL | - | - |
| out4 | - | - | - | - | -hpmixR | -hpmixR | -spkmix | (V _{mid}) |

Figure 44 Mono Speaker Output Configuration

WM9713L MONO SPEAKER

Figure 45 shows a typical output configuration compatible with the WM9712 for mono speaker with headphones, ear speaker and hands-free operation. The table shows suggested mixer outputs to select for each output PGA for a given operating scenario. (Note the inverted mixer outputs can be achieved using the mixer output inverters INV1 and INV2).

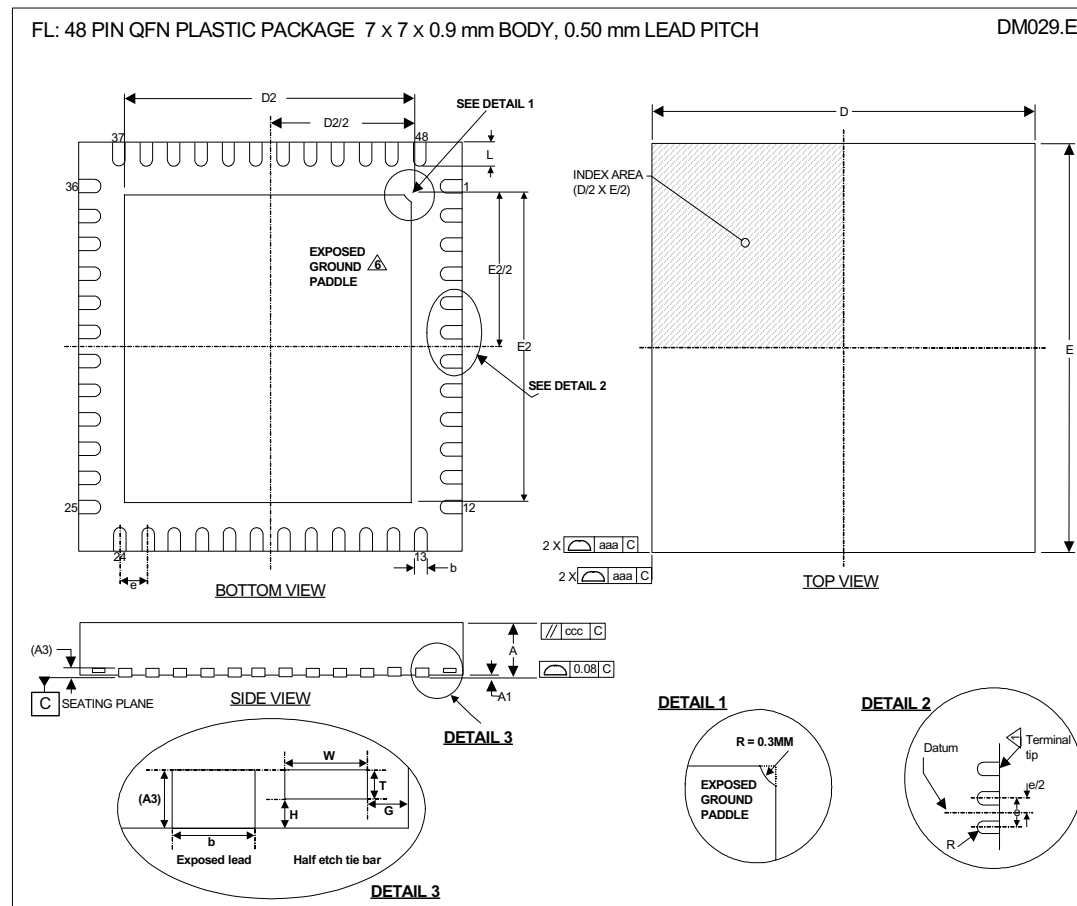
When using this configuration note that AVDD, HPVDD and SPKVDD must all be at the same voltage to achieve the best performance.



| Config/ Driver | Hands-free (1:mmix) | Hands-free (2:spkmix) | Ear Speaker (1:mmix) | Ear Speaker (2:hpmix) | Ear Speaker (1) + Speaker | Ear Speaker (2) + Speaker | Mono Speaker | Headphone |
|-------------------|------------------------|--------------------------|-------------------------|--------------------------|------------------------------|------------------------------|-----------------|-----------|
| mono | mmix | spkmix | - | - | - | - | - | - |
| spkl | - | - | - | - | hpmixL | hpmixL | spkmix | - |
| spkr | - | - | - | - | -hpmixR | hpmixR | -spkmix | - |
| hpl | - | - | V _{mid} | hpmixL | mmix | hpmixL | - | hpmixL |
| hpr | - | - | - | - | - | - | - | hpmixR |
| out3 | - | - | mmix | -hpmixR | -mmix | -hpmixR | - | (Z) |
| out4 | - | - | - | - | - | - | - | - |

Figure 45 WM9713L Mono Speaker Configuration

PACKAGE DIMENSIONS



| Symbols | Dimensions (mm) | | | NOTE |
|--|---------------------------------|----------|------|------|
| | MIN | NOM | MAX | |
| A | 0.80 | 0.90 | 1.00 | |
| A1 | 0 | 0.02 | 0.05 | |
| A3 | | 0.20 REF | | |
| b | 0.18 | 0.25 | 0.30 | 1 |
| D | | 7.00 BSC | | |
| D2 | 5.00 | 5.15 | 5.25 | |
| E | | 7.00 BSC | | |
| E2 | 5.00 | 5.15 | 5.25 | |
| e | | 0.5 BSC | | |
| G | | 0.213 | | |
| H | | 0.1 | | |
| L | 0.30 | 0.4 | 0.50 | |
| T | | 0.1 | | |
| W | | 0.2 | | |
| Tolerances of Form and Position | | | | |
| aaa | | 0.15 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| REF | JEDEC, MO-220, VARIATION VKKD-2 | | | |

- NOTES:
- DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
 - ALL DIMENSIONS ARE IN MILLIMETRES
 - THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.
 - COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
 - THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
 - REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.

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ADDRESS:

Wolfson Microelectronics plc
Westfield House
26 Westfield Road
Edinburgh
EH11 2QB
United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com