128Kx32 Radiation Hardened SRAM MODULE *ADVANCED**

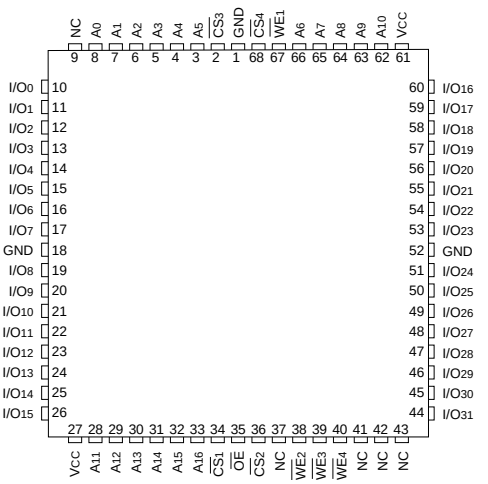
FEATURES

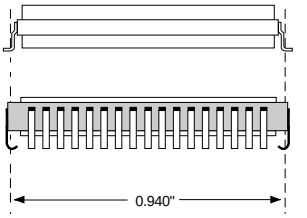
- Access Time of 25ns
- Radiation Tolerant
  - Total Dose Hardness through $1x10^6$ rad (SiO_2)
- Neutron Hardness through $1x10^{14}$ cm^{-2}
- Dynamic and Static Transient Upset Hardness through $1x10^{11}$ rad (Si)/s
- Dose Rate Survivability through < $1x10^{12}$ rad (Si)/s
- Soft Error Rate of < $1x10^{-10}$ upsets/bit-day in Geosynchronous Orbit
- No Latchup
- Packaging:
  - 68 lead, Hermetic CQFP (G2S), 7.62mm (0.300") height (Package 515). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

** This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG.1 PIN CONFIGURATION FOR WS128K32-25G2SMX

TOP VIEW



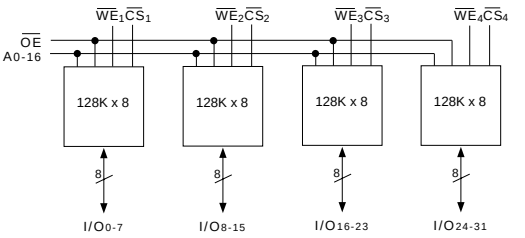


The White 68 lead G2S CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2S has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.3	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	6.5	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	35	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	35	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		150	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		30	mA
Output Low Voltage	V_{OL}	I_{OL} = 10mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -5.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ = V_{CC} -0.2V	2.5		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 2.5V			4.0	mA

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		Units
Read Cycle		**Min**	**Max**	
Read Cycle Time	t_{RC}	25		ns
Address Access Time	t_{AA}		25	ns
Output Hold from Address Change	t_{OH}	0		ns
Chip Select Access Time	t_{ACS}		25	ns
Output Enable to Output Valid	t_{OE}		9	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	2		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		10	ns
Output Disable to Output in High Z	t_{OHZ}[1]		9	ns

1. This parameter is guaranteed by design but not tested.

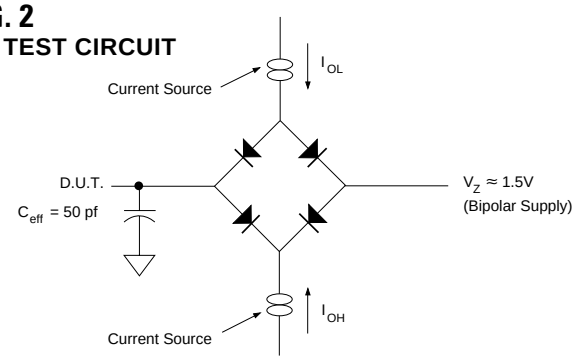
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-25		Units
Write Cycle		**Min**	**Max**	
Write Cycle Time	t_{WC}	25		ns
Chip Select to End of Write	t_{CW}	20		ns
Address Valid to End of Write	t_{AW}	20		ns
Data Valid to End of Write	t_{DW}	15		ns
Write Pulse Width	t_{WP}	20		ns
Address Setup Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	0		ns
Output Active from End of Write	t_{OW}[1]	5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		9	ns
Data Hold Time	t_{DH}	0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
AC TEST CIRCUIT

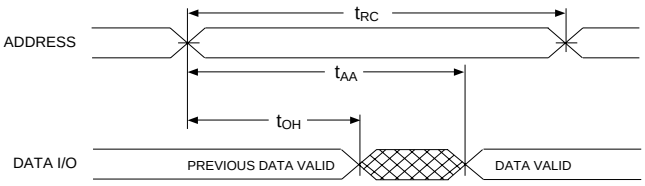


AC TEST CONDITIONS

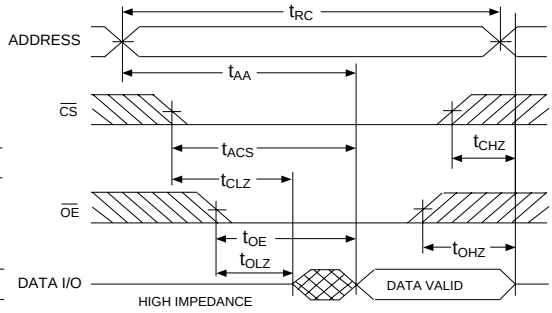
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75\ \Omega$.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 3
TIMING WAVEFORM - READ CYCLE

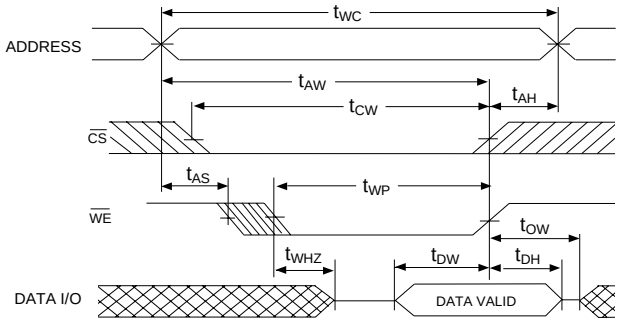


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



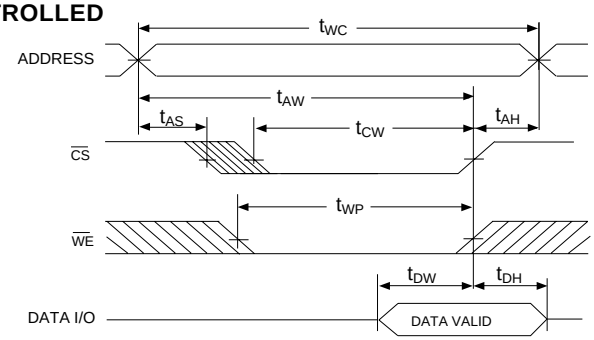
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 4
WRITE CYCLE - $\overline{WE}$ CONTROLLED



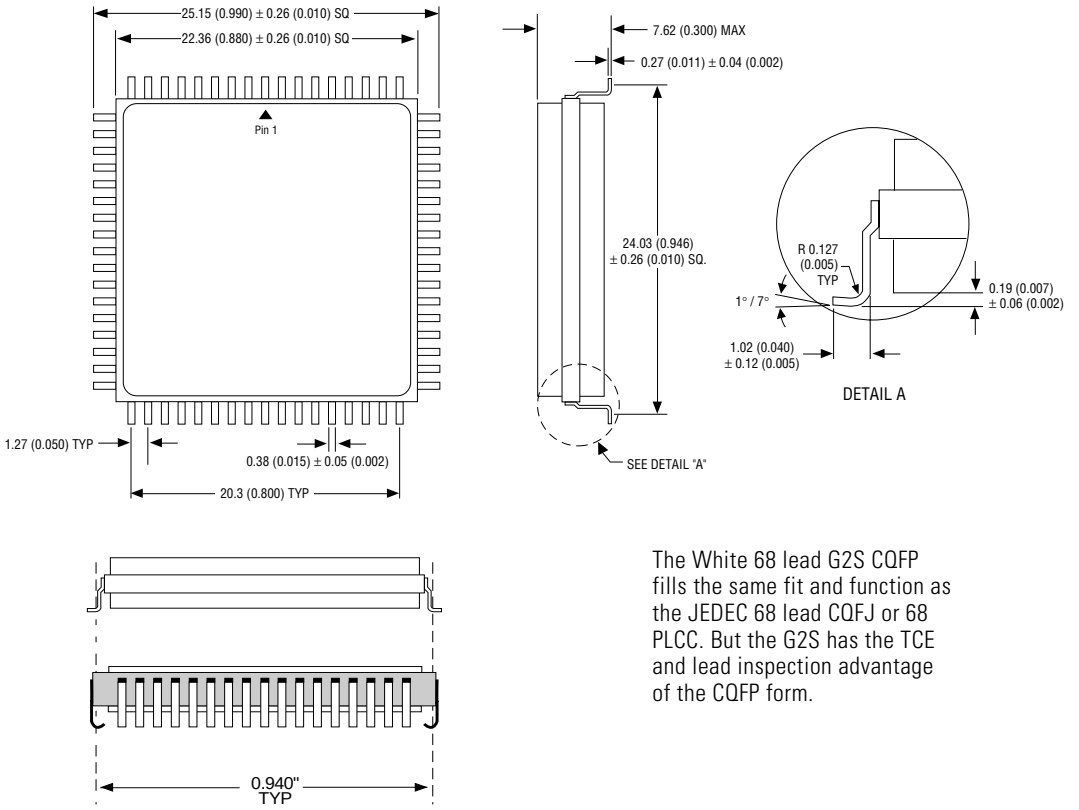
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 5
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 515: 68 LEAD CERAMIC QUAD FLAT PACK, CQFP (G2S)



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ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION