Half-bridge power IC for CFL lamps

FEATURES

- Integrated 600V half-bridge gate driver
- Lower power level-shifting circuit
- Adjustable oscillator frequency and preheat time
- Maximum voltage of 600 V
- Internal clamping zener diode
- Soft start functionality

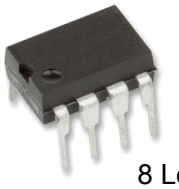
Product Summary

V_{OFFSET}	600V Max.
Duty Cycle	50%
T_r/T_p	80/40ns
V_{clamp}	15.6V typ.
Deadtime (typ.)	2μs

GERNERAL DESCRIPTION

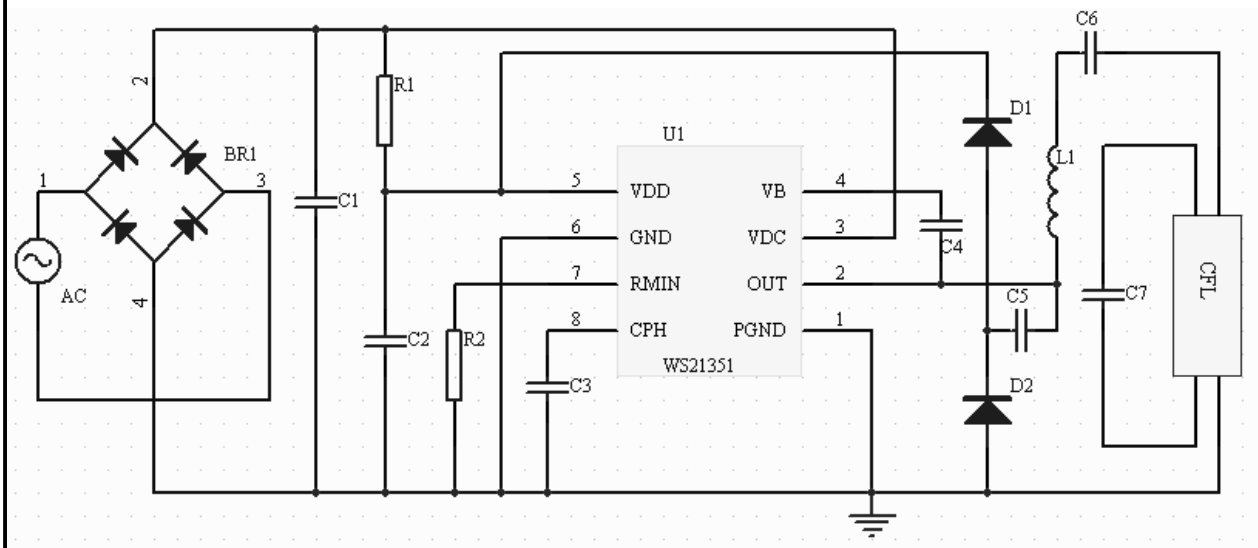
The WS21351 is a high-voltage monolithic integrated circuit which is designed for driving Compact Fluorescent Lamps (CFL) in a half-bridge configuration.WS21351 features a soft start function, an adjustable oscillator and an internal drive function with a high-voltage level shifter for driving the half bridge.

Packages



8 Lead PDIP

TYPICAL APPLICATION



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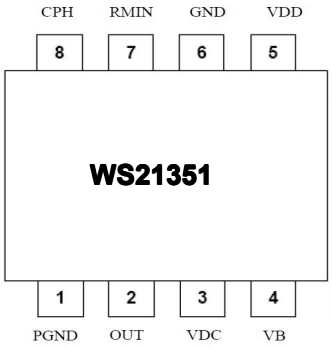
GENERAL INFORMATION

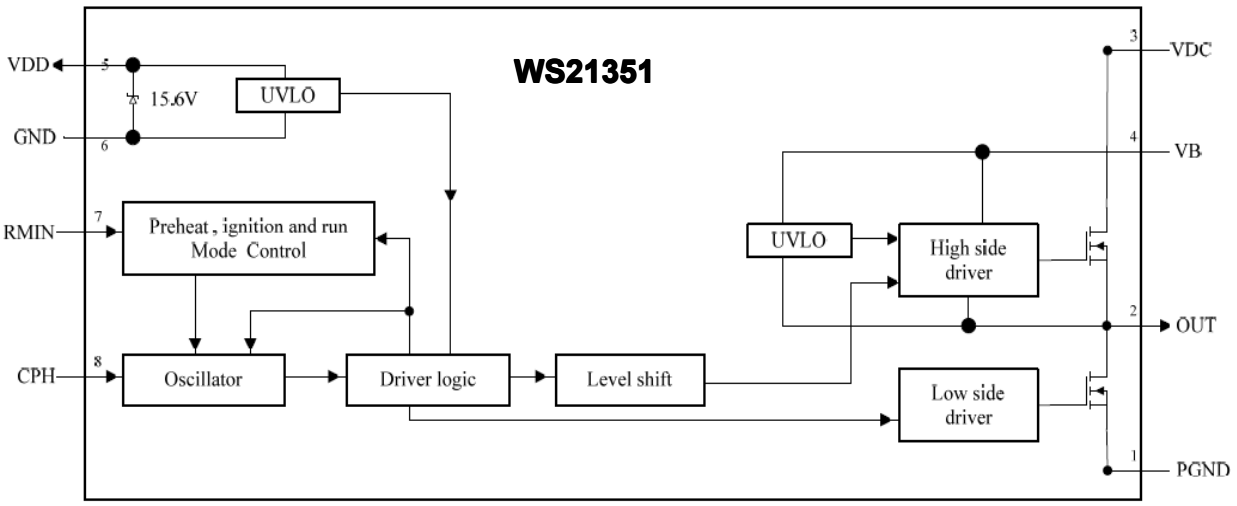
Pin Configuration



TERMINAL ASSIGNMENTS

Pin #	Name	Description
1	P_{GND}	Power ground
2	OUT	Half bridge output
3	V_{DC}	High-voltage supply
4	V_B	High-side floating supply
5	V_{DD}	Supply voltage
6	GND	Signal ground
7	R_{MIN}	Oscillator frequency set resistor
8	C_{PH}	Preheating time set capacitor

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VB	High-side floating supply	-0.3		600	V
VOUT	Half bridge output	-0.3		575	
VIN	RMIN, CPH pins input voltage	-0.3		7	
ICL	Clamping current level	-25		25	mA
dV_{OUT}/dt	Allowable offset voltage slew rate	-50		50	V/ns
TA	Operating temperature range	-25		125	°C
TSTG	Storage temperature range	-65		150	
TL	Lead temperature (soldering,10 seconds)			300	

Note: more than the limit specified in the table parameters will result in permanent damage to the device. The device is not recommended in these extreme conditions of work, working conditions in the limit above which may affect device reliability.

Electrical Characteristics (V_{BIAS}(V_{DD}, V_B-Vout)=14.0V, T_A=25°C, unless otherwise specified.)

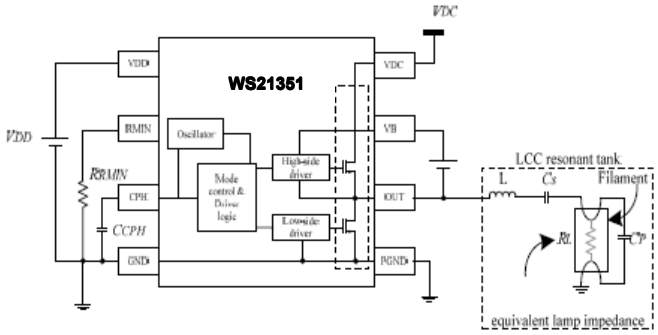
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Supply characteristics						
VDDTH(ST+)	VDD UVLO positive going threshold	VDD rising from 0V	11.2	12.8	14	V
VDDTH(ST-)	VDD UVLO negative going threshold	VDD decreasing	9	10	11	
VDDHY(ST)	VDD-side UVLO hysteresis			2．8		
VCL	Supply clamping voltage	IDD =20mA	14．4	15．6		
IST	Start-up supply current	VDD = 10V		50	80	μA
IDD	Dynamic operating supply current	Running freq=85KHZ		4．5		mA
Floating supply characteristics (VB-VOUT)						
VHSTH(ST+)	High-side UVLO positive going threshold	VB –VOUT increasing	7．5	9	10．5	V
VHSTH(ST-)	High-side UVLO negative going threshold	VB –VOUT decreasing	7．8	8	9．2	
VHSHY(ST)	High-side UVLO hysteresis			1		
IHST	High-side quiescent supply current	VB –VOUT = 14V			60	uA
Oscillator characteristics						
fPRE	Preheating frequency	RMIN = 82kΩ, VCPH =0V	66	86	96	kHz
fOSC	Running frequency	RMIN = 82kΩ, VCPH =6V	29	34	39	kHz
Duty	Oscillator duty cycle			50		%
DT	Output dead time			2．0		Us
VCPH	Maximum CPH voltage			6		V
MOSFET characteristics						
ILKMOS	MOSFET leakage current	VDS = 500V			10	μA
RON	On resistance (dynamic)	VGS = 12V, ID = 100mA		8		Ω
		VGS = 12V, ID = 500mA		10		

OPERATION DESCRIPTION

Under-Voltage Lockout (UVLO)Function

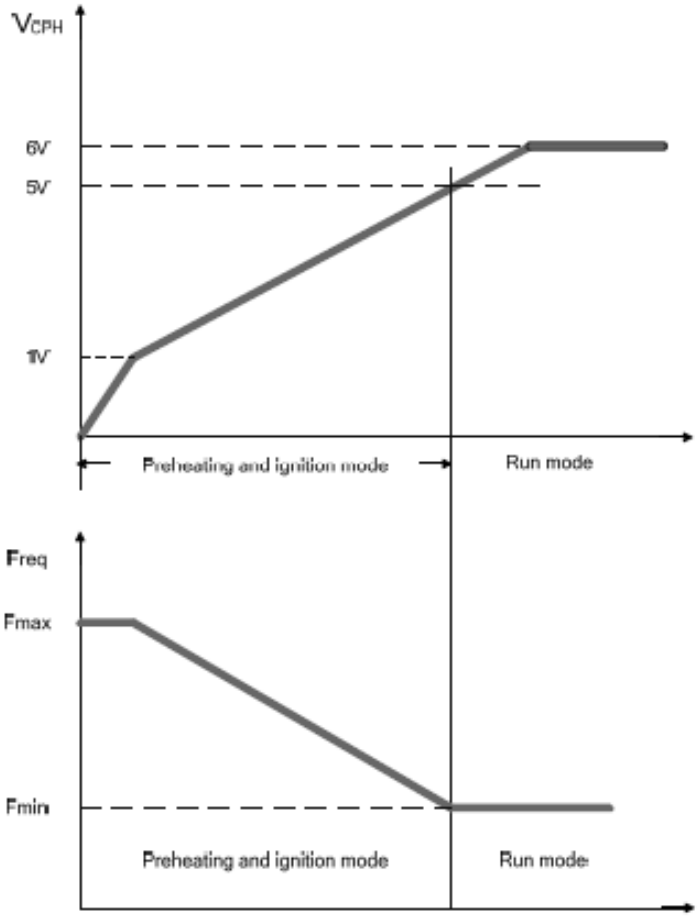
The WS21351 has UVLO circuits for both high-side and low-side circuits. When VDD reaches VDDTH+, UVLO is released and the WS21351 operates normally. Under UVLO condition,WS21351 consumes little current, typically 50uA. After UVLO is released,WS21351 operates normally until VDD goes below VDDTH-, the UVLO has hysteresis which typically is 2.8V . At UVLO condition, all latches that determine the status of the IC are reset.

WS21351 has a high-side gate driver circuit. The supply for the high-side driver is applied between VB and VOUT. To protect from malfunction of the driver at low supply voltage between VB and VOUT,WS21351 provides an additional UVLO circuit between this supply rails. If VB-VOUT is under VHSTH+, the driver holds low state to turn off the high-side switch, when VB-VOUT is higher than VHSTH– after VB-VOUT exceeds VHSTH+, operation of the driver continues.



ignition and improve lamp life longevity.Accordingly, the oscillation frequency is changed in the following sequence:

Preheating freq > Ignition freq > running freq.



Oscillator Operation

The ballast circuit for a fluorescent lamp is based on the LCC resonant tank and a half-bridge inverter circuit, as shown in Fig4 . To accomplish Zero-Voltage Switching (ZVS) of the half-bridge inverter circuit, the LCC must be driven at a higher frequency than its resonant Frequency, which is determined by L, CS, CP, and RL; where RL is the equivalent lamp's impedance. The transfer function of LCC resonant tank is heavily dependent on the lamp impedance, RL, as illustrated in Figure 4. The oscillator inWS21351 generates effective driving frequencies to assist lamp

Preheating and ignition Mode

When VDD exceeds VDDTH+ threshold, theWS21351 enters preheating mode. An internal current source charges the external capacitor on pin CPH, and the voltage on pin CPH starts ramping up linearly. The frequency ramps down towards the resonance frequency of the high-Q ballast output stage causing the lamp voltage and load current to Increase.

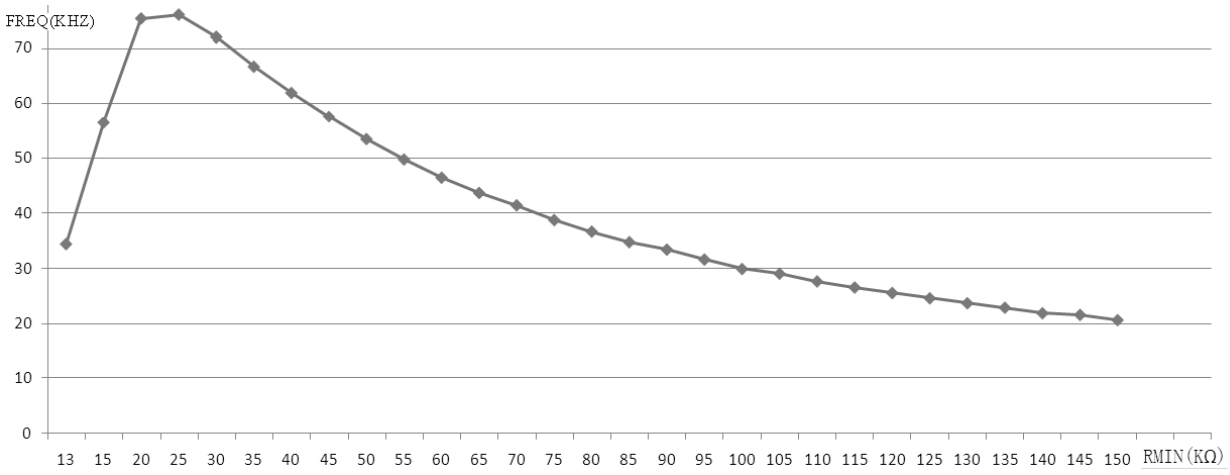
The voltage on pin CPH continues to increase and the frequency keeps decreasing until the lamp ignites. If the

Lamp ignites successfully, the voltage on pin CPH continues to increase until it internally limits at 6V (V_{CPH_MAX}). The frequency stops decreasing when V_{CPH} reach 5V and stays at the minimum frequency as programmed by an external resistor, on pin RMIN (as show in Fig 4). The minimum frequency should be set below the High-Q resonance frequency of the ballast output stage to ensure that the frequency ramps through resonance for lamp Ignition

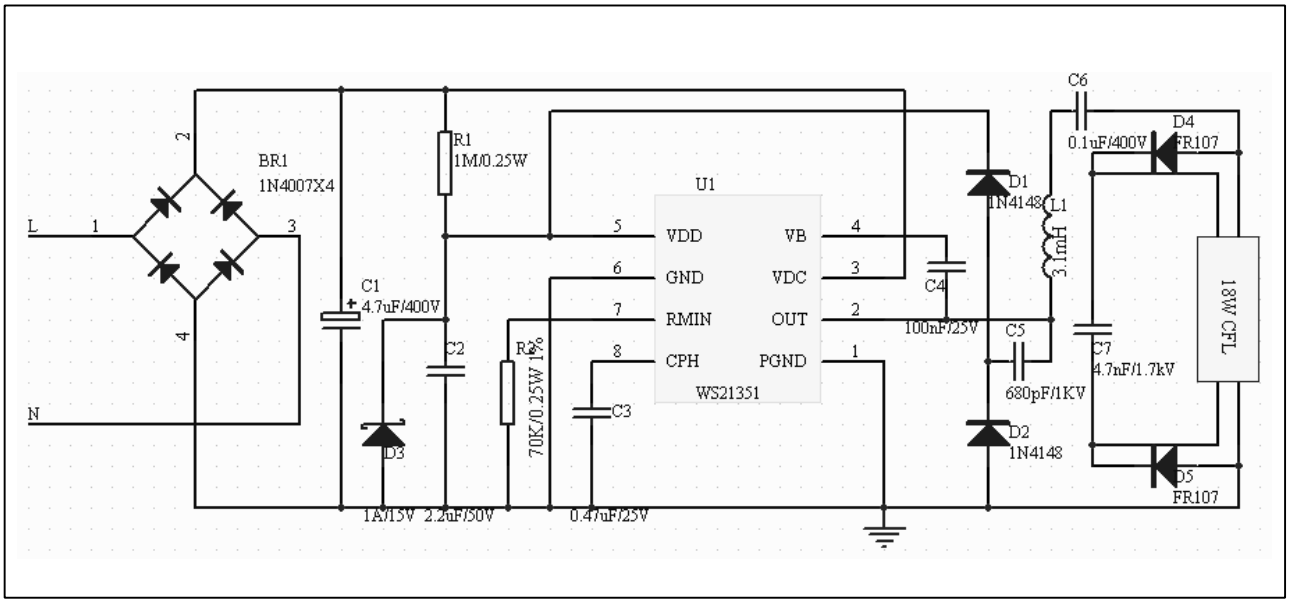
.The desired preheat time can be set by adjusting the slope of the V_{CPH} ramp with the external capacitor on pin CPH. The relation of LCC tank frequency and Pin CPH voltage V_{CPH} as show in Fig5.

Run Mode

TheWS21351 enters RUN mode when the voltage on pin CPH exceeds 5V . The lamp has ignited and the ballast output stage becomes a low-Q, series-L, parallel-RC circuit. The voltage on the CPH pin continues to increase but the frequency don't change as the minimum frequency is reached. The resonant inductor, resonant capacitor, DC bus voltage and minimum frequency determine the running lamp power. The relation of minimum run frequency and the setting resistor R_{RMIN} as show in Fig 6. The IC stays at this minimum frequency unless VDD decreases below the V_{DDTH-} threshold



WS21351 for 18W CFL Application



DIP-8 Package Dimension

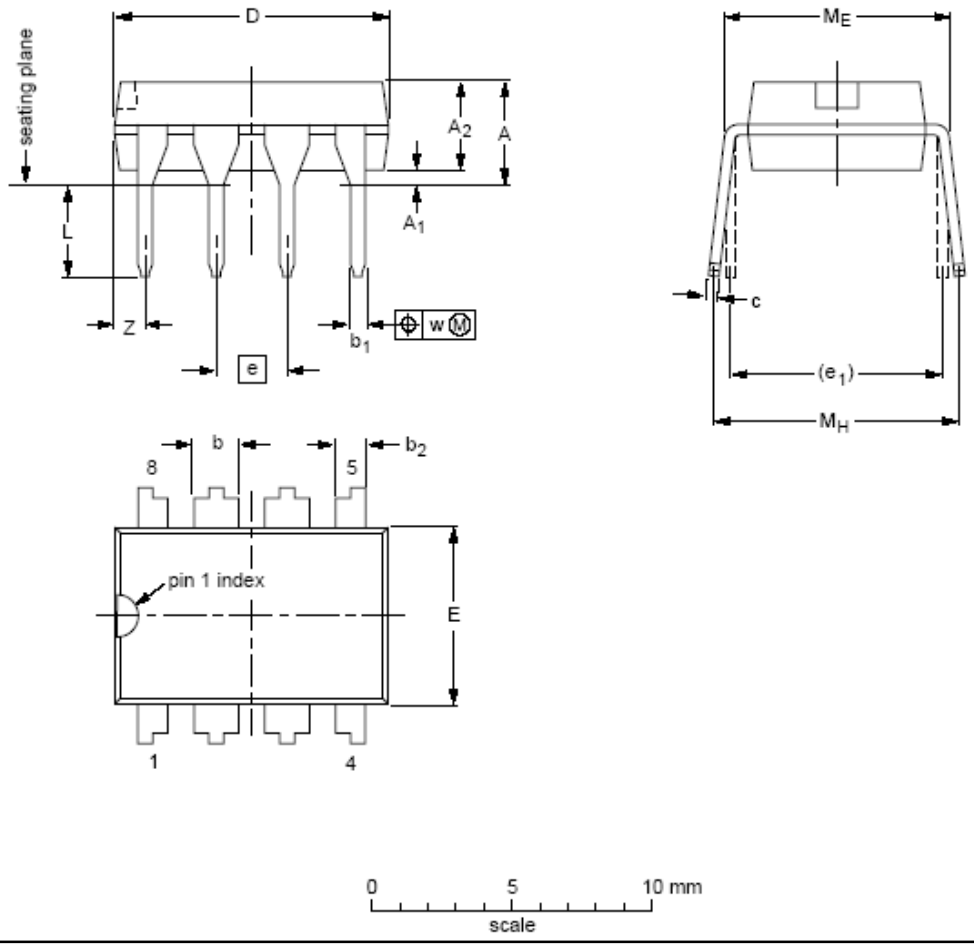
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.02	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT97-1	050G01	MO-001	SC-504-8			~~99-12-27~~ 03-02-13



Steady, keep you advance