

Nonvolatile Static RAM

FEATURES

- High Reliability
  - Endurance: 1,000,000 Nonvolatile Store Operations
  - Retention: 100 Years Minimum
- Power-on Recall
  - E<sup>2</sup>PROM Data Automatically Recalled Into SRAM Upon Power-up
- Lock Out Inadvertent Store Operations
- Low Power CMOS
  - Standby: 250µA
- Infinite E<sup>2</sup>PROM Array Recall, and RAM Read and Write Cycles
- Compatible with X2004

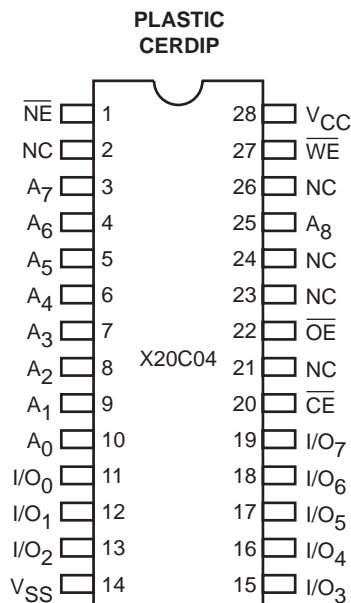
DESCRIPTION

The Xicor X20C04 is a 512 x 8 NOVRAM featuring a static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E<sup>2</sup>PROM). The X20C04 is fabricated with advanced CMOS floating gate technology to achieve low power and wide power-supply margin. The X20C04 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs, and E<sup>2</sup>PROMs.

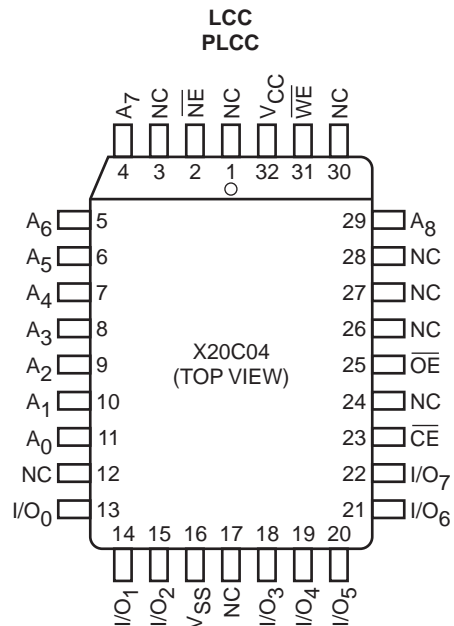
The NOVRAM design allows data to be easily transferred from RAM to E<sup>2</sup>PROM (store) and E<sup>2</sup>PROM to RAM (recall). The store operation is completed in 5ms or less and the recall operation is completed in 5µs or less.

Xicor NOVRAMS are designed for unlimited write operations to RAM, either from the host or recalls from E<sup>2</sup>PROM, and a minimum 1,000,000 store operations to the E<sup>2</sup>PROM. Data retention is specified to be greater than 100 years.

PIN CONFIGURATION



3825 FHD F02



3825 FHD F03

# X20C04

## PIN DESCRIPTIONS

### Addresses (A<sub>0</sub>–A<sub>8</sub>)

The Address inputs select an 8-bit memory location during a read or write operation.

### Chip Enable ( $\overline{CE}$ )

The Chip Enable input must be LOW to enable all read/write operations. When  $\overline{CE}$  is HIGH, power consumption is reduced.

### Output Enable ( $\overline{OE}$ )

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of  $\overline{CE}$ ,  $\overline{WE}$ , or  $\overline{NE}$ .

### Data In/Data Out (I/O<sub>0</sub>–I/O<sub>7</sub>)

Data is written to or read from the X20C04 through the I/O pins. The I/O pins are placed in the high impedance state when either  $\overline{CE}$  or  $\overline{OE}$  is HIGH or when  $\overline{NE}$  is LOW.

### Write Enable ( $\overline{WE}$ )

The Write Enable input controls the writing of data to both the static RAM and stores to the E<sup>2</sup>PROM.

### Nonvolatile Enable ( $\overline{NE}$ )

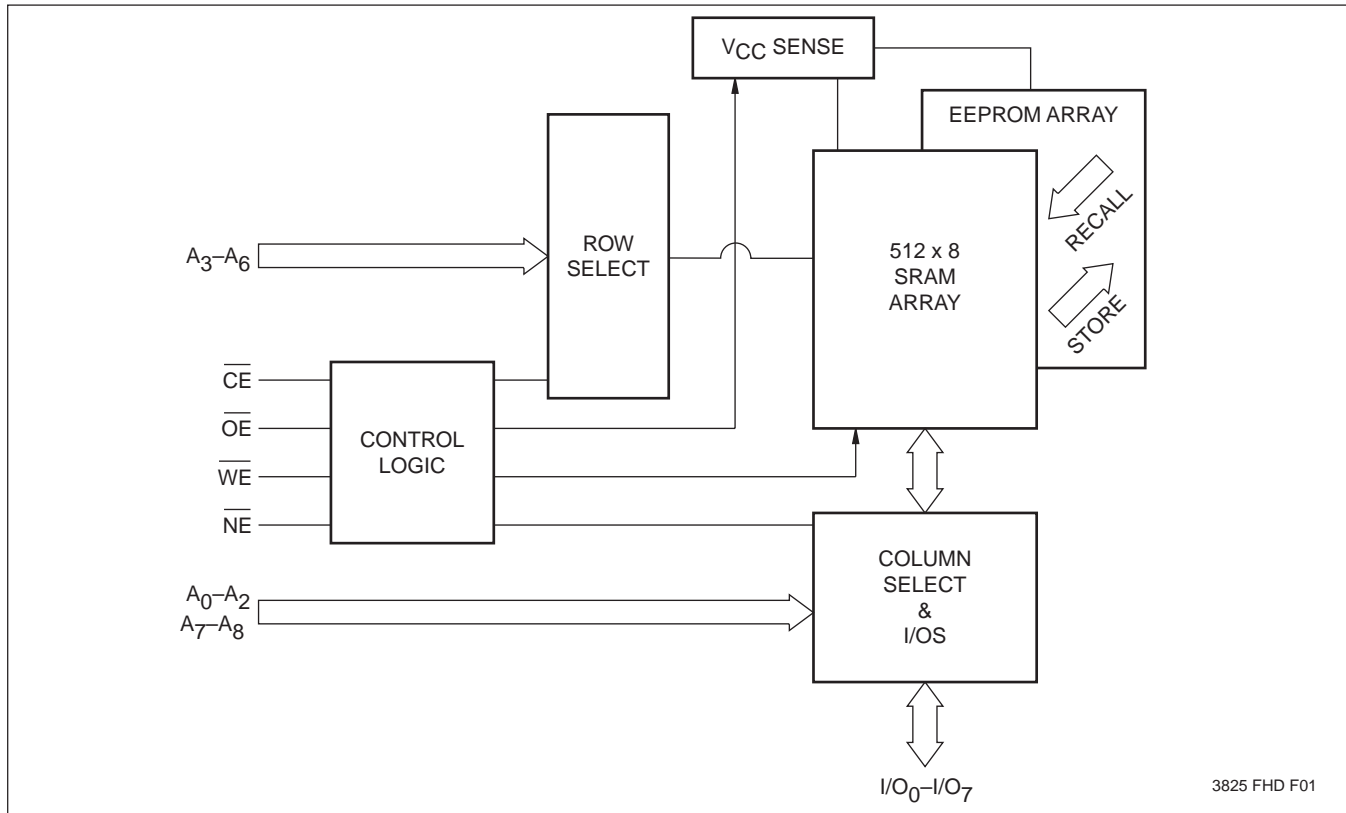
The Nonvolatile Enable input controls all accesses to the E<sup>2</sup>PROM array (store and recall functions).

## PIN NAMES

Symbol	Description
A <sub>0</sub> –A <sub>8</sub>	Address Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{NE}$	Nonvolatile Enable
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground
NC	No Connect

3825 PGM T01

## FUNCTIONAL DIAGRAM



3825 FHD F01

# X20C04

## DEVICE OPERATION

The  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$  inputs control the X20C04 operation. The X20C04 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either  $\overline{OE}$  or  $\overline{CE}$  is HIGH, or when  $\overline{NE}$  is LOW.

## RAM Operations

RAM read and write operations are performed as they would be with any static RAM. A read operation requires  $\overline{CE}$  and  $\overline{OE}$  to be LOW with  $\overline{WE}$  and  $\overline{NE}$  HIGH. A write operation requires  $\overline{CE}$  and  $\overline{WE}$  to be LOW with  $\overline{NE}$  HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X20C04.

## Nonvolatile Operations

With  $\overline{NE}$  LOW, recall operation is performed in the same manner as RAM read operation. A recall operation causes the entire contents of the E<sup>2</sup>PROM to be written into the RAM array. The time required for the operation to complete is 5 $\mu$ s or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E<sup>2</sup>PROM. The time for the operation to complete is 5ms or less.

## Power-Up Recall






Upon power-up ( $V_{CC}$ ), the X20C04 performs an automatic array recall. When  $V_{CC}$  minimum is reached, the recall is initiated, regardless of the state of  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{WE}$  and  $\overline{NE}$ .

## Write Protection

The X20C04 has five write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- $V_{CC}$  Sense—All functions are inhibited when  $V_{CC}$  is  $\leq 3.5V$ .
- A RAM write is required before a Store Cycle is initiated.
- Write Inhibit—Holding either  $\overline{OE}$  LOW,  $\overline{WE}$  HIGH,  $\overline{CE}$  HIGH, or  $\overline{NE}$  HIGH during power-up and power-down will prevent an inadvertent store operation.
- Noise Protection—A combined  $\overline{WE}$ ,  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  pulse of less than 20ns will not initiate a Store Cycle.
- Noise Protection—A combined  $\overline{WE}$ ,  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  pulse of less than 20ns will not initiate a recall cycle.

## SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

# X20C04

## ABSOLUTE MAXIMUM RATINGS\*

Temperature under Bias ..... -65°C to +135°C  
 Storage Temperature ..... -65°C to +150°C  
 Voltage on any Pin with  
     Respect to V<sub>SS</sub> ..... -1V to +7V  
 D.C. Output Current ..... 10mA  
 Lead Temperature (Soldering, 10 seconds) ..... 300°C

## \*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3825 PGM T02.1

Supply Voltage	Limits
X20C04	5V ±10%

3825 PGM T03

## D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Units	
I <sub>CC1</sub>	V <sub>CC</sub> Current (Active)		100	mA	$\overline{NE} = \overline{WE} = V_{IH}, \overline{CE} = \overline{OE} = V_{IL}$ Address Inputs = 0.4V/2.4V levels @ f = 5MHz. All I/Os = Open
I <sub>CC2</sub>	V <sub>CC</sub> Current During Store		10	mA	All Inputs = V <sub>IH</sub> All I/Os = Open
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current (TTL Input)		10	mA	$\overline{CE} = V_{IH}$ All Other Inputs = V <sub>IH</sub> , All I/Os = Open
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current (CMOS Input)		250	µA	All Inputs = V <sub>CC</sub> - 0.3V All I/Os = Open
I <sub>LI</sub>	Input Leakage Current		10	µA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current		10	µA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> , $\overline{CE} = V_{IH}$
V <sub>IL</sub> (1)	Input LOW Voltage	-1	0.8	V	
V <sub>IH</sub> (1)	Input HIGH Voltage	2	V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output LOW Voltage		0.4	V	I <sub>OL</sub> = 2.1mA
V <sub>OH</sub>	Output HIGH Voltage	2.4		V	I <sub>OH</sub> = -400µA

3825 PGM T04.3

## POWER-UP TIMING

Symbol	Parameter	Max.	Units
t <sub>PUR</sub> (2)	Power-Up to RAM Operation	100	µs
t <sub>PUW</sub> (2)	Power-Up to Nonvolatile Operation	5	ms

3825 PGM T05

## CAPACITANCE T<sub>A</sub> = +25°C, F = 1MHz, V<sub>CC</sub> = 5V.

Symbol	Test	Max.	Units	Conditions
C <sub>I/O</sub> (2)	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> (2)	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

3825 PGM T06.1

Notes: (1) V<sub>IL</sub> min. and V<sub>IH</sub> max. are for reference only and are not tested.  
 (2) This parameter is periodically sampled and not 100% tested.

# X20C04

## ENDURANCE AND DATA RETENTION

Parameter	Min.	Units
Endurance	100,000	Data Changes Per Bit
Store Cycles	1,000,000	Store Cycles
Data Retention	100	Years

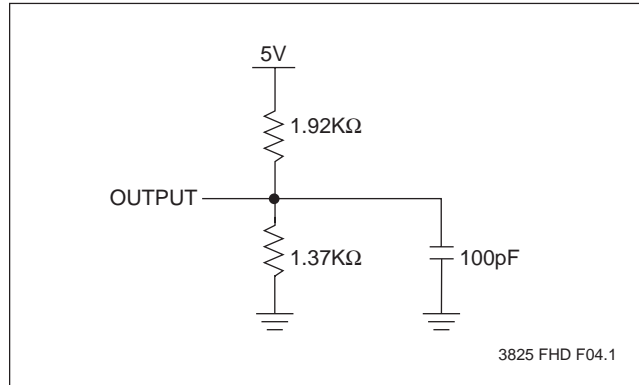
3825 PGM T07.1

## MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	H	Write "1" RAM	Input Data High	Active
L	L	H	H	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	Not Allowed	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

3825 PGM T09.1

## EQUIVALENT A.C. LOAD CIRCUIT



3825 FHD F04.1

## A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V

3825 PGM T08.2

# X20C04

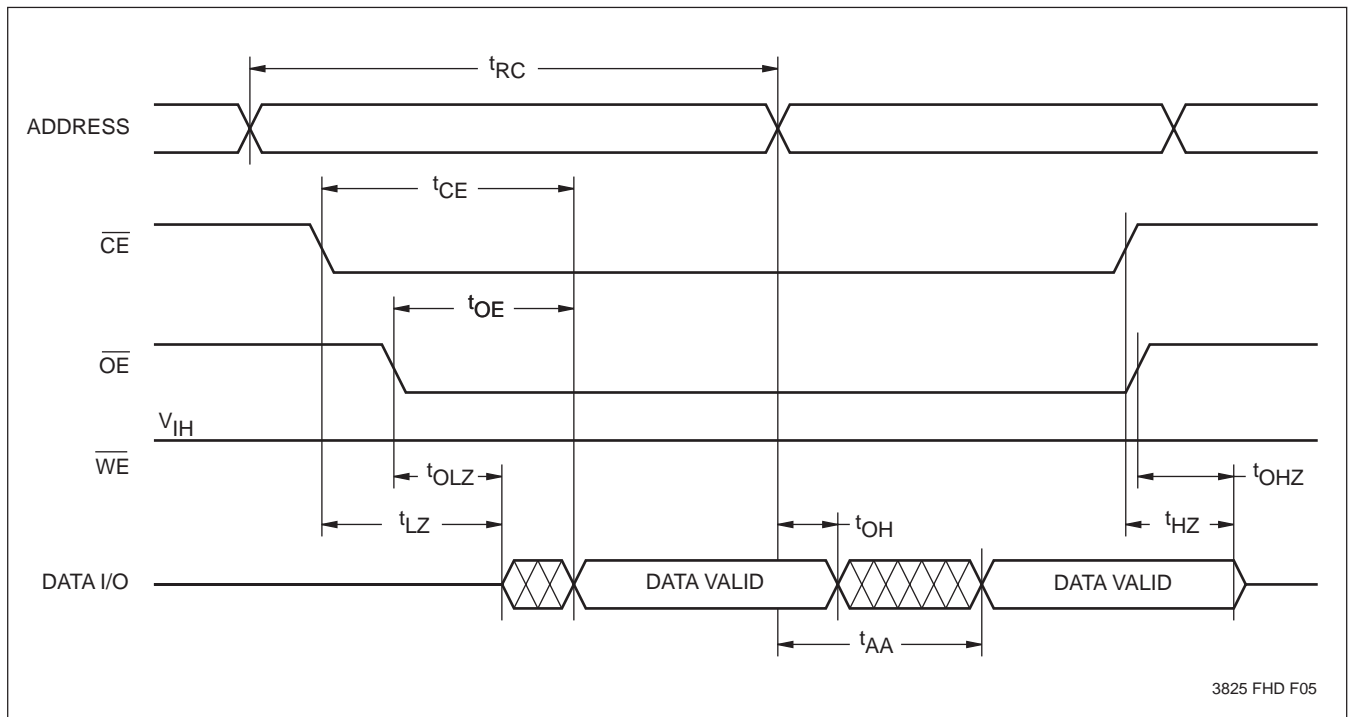
## A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

### Read Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	150		200		250		300		ns
$t_{CE}$	Chip Enable Access Time		150		200		250		300	ns
$t_{AA}$	Address Access Time		150		200		250		300	ns
$t_{OE}$	Output Enable Access Time		50		70		100		150	ns
$t_{LZ}^{(3)}$	Chip Enable to Output in Low Z	0		0		0		0		ns
$t_{OLZ}^{(3)}$	Output Enable to Output in Low Z	0		0		0		0		ns
$t_{HZ}^{(3)}$	Chip Disable to Output in High Z		80		100		100		100	ns
$t_{OHZ}^{(3)}$	Output Disable to Output in High Z		80		100		100		100	ns
$t_{OH}$	Output Hold From Address Change	0		0		0		0		ns

3825 PGM T10

### Read Cycle



**Note:** (3)  $t_{LZ}$  min.,  $t_{HZ}$ ,  $t_{OLZ}$  min., and  $t_{OHZ}$  are periodically sampled and not 100% tested.  $t_{HZ}$  max. and  $t_{OHZ}$  max. are measured, with  $C_L = 5pF$  from the point when  $\overline{CE}$  or  $\overline{OE}$  return HIGH (whichever occurs first) to the time when the output are no longer driven.

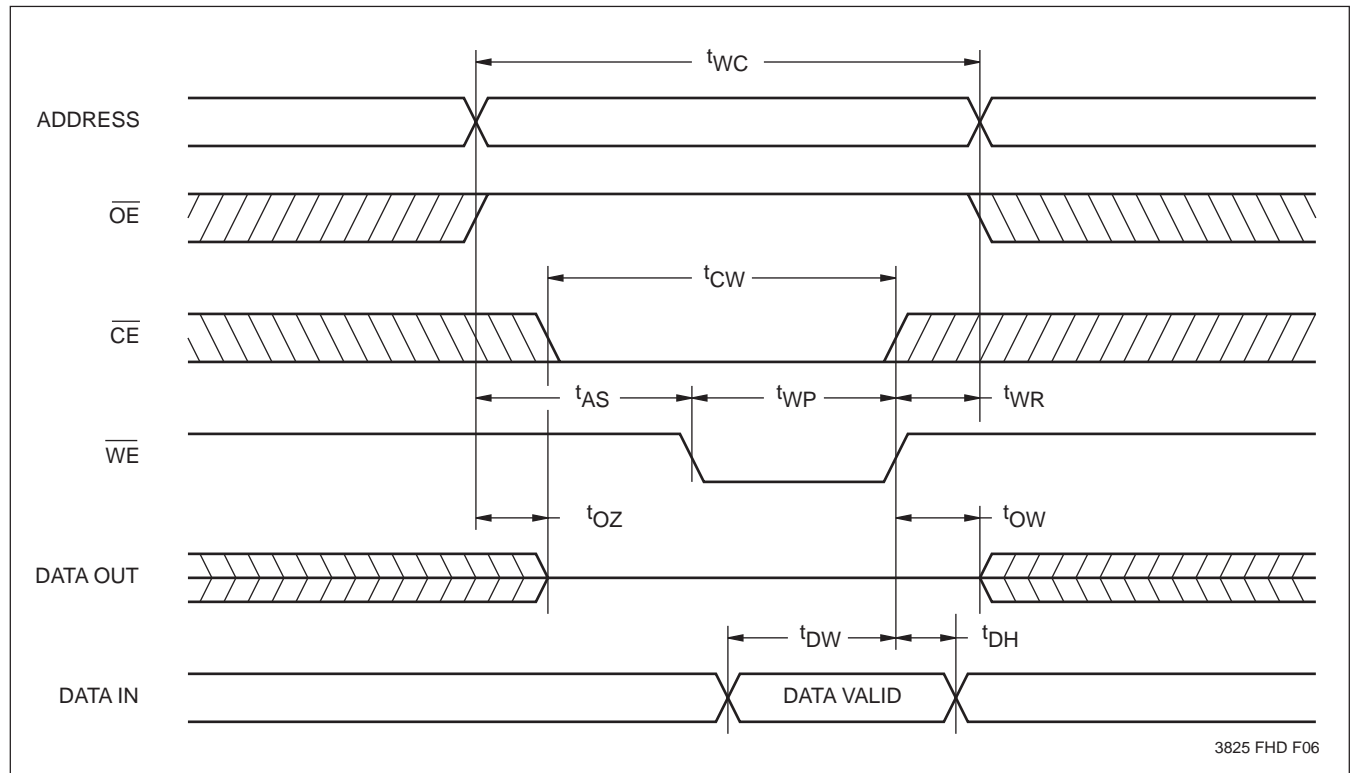
# X20C04

## Write Cycle Limits

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	150		200		250		300		ns
$t_{CW}$	Chip Enable to End of Write Input	150		200		250		300		ns
$t_{AS}$	Address Setup Time	0		0		0		0		ns
$t_{WP}$	Write Pulse Width	100		120		150		200		ns
$t_{WR}$	Write Recovery Time	0		0		0		0		ns
$t_{DW}$	Data Setup to End of Write	100		120		150		200		ns
$t_{DH}$	Data Hold Time	0		0		0		0		ns
$t_{WZ}^{(4)}$	Write Enable to Output in High Z		80		100		100		100	ns
$t_{OW}^{(4)}$	Output Active from End of Write	5		5		5		5		ns
$t_{OZ}^{(4)}$	Output Enable to Output in High Z		80		100		100		100	ns

3825 PGM T11

## $\overline{WE}$ Controlled Write Cycle

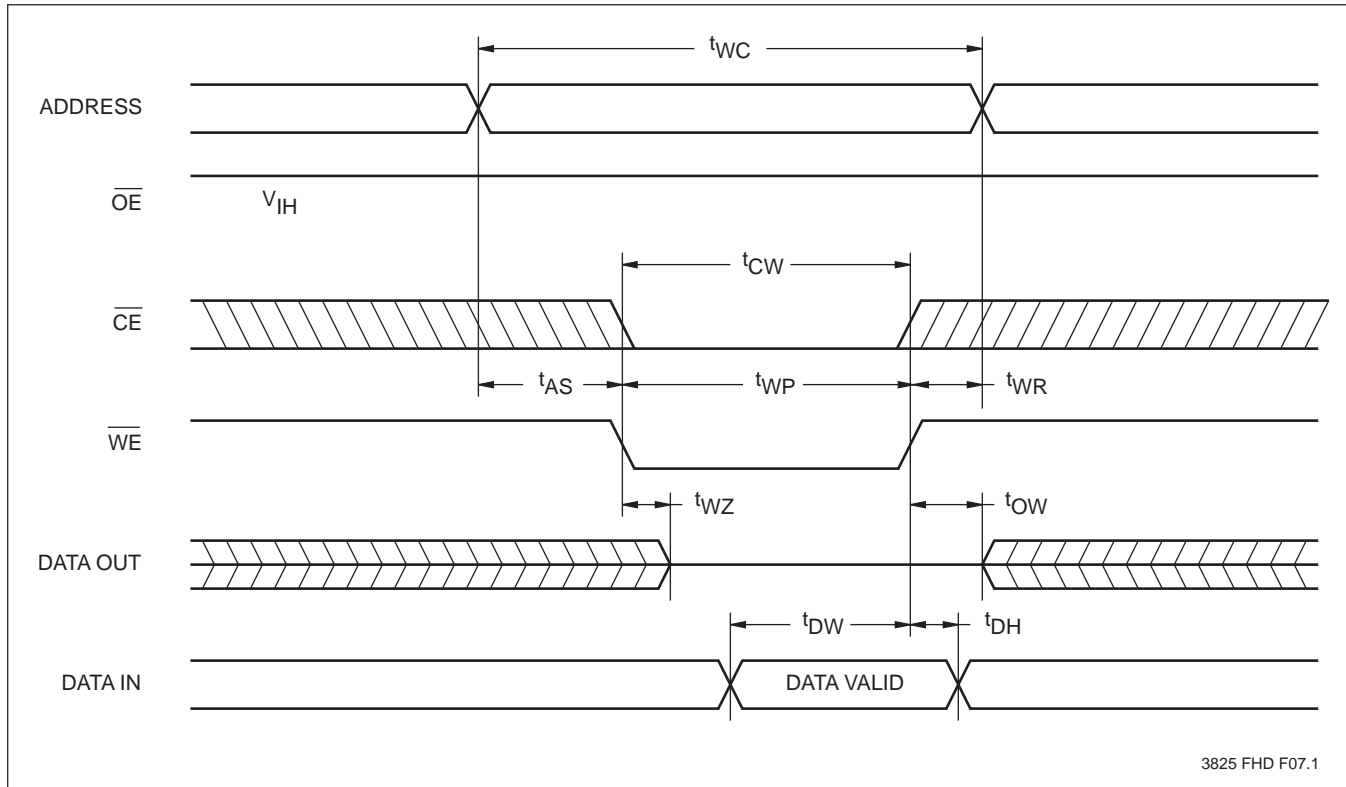


3825 FHD F06

**Note:** (4)  $t_{WZ}$ ,  $t_{OW}$ , and  $t_{OZ}$  are periodically sampled and not 100% tested.

# X20C04

## $\overline{CE}$ Controlled Write Cycle





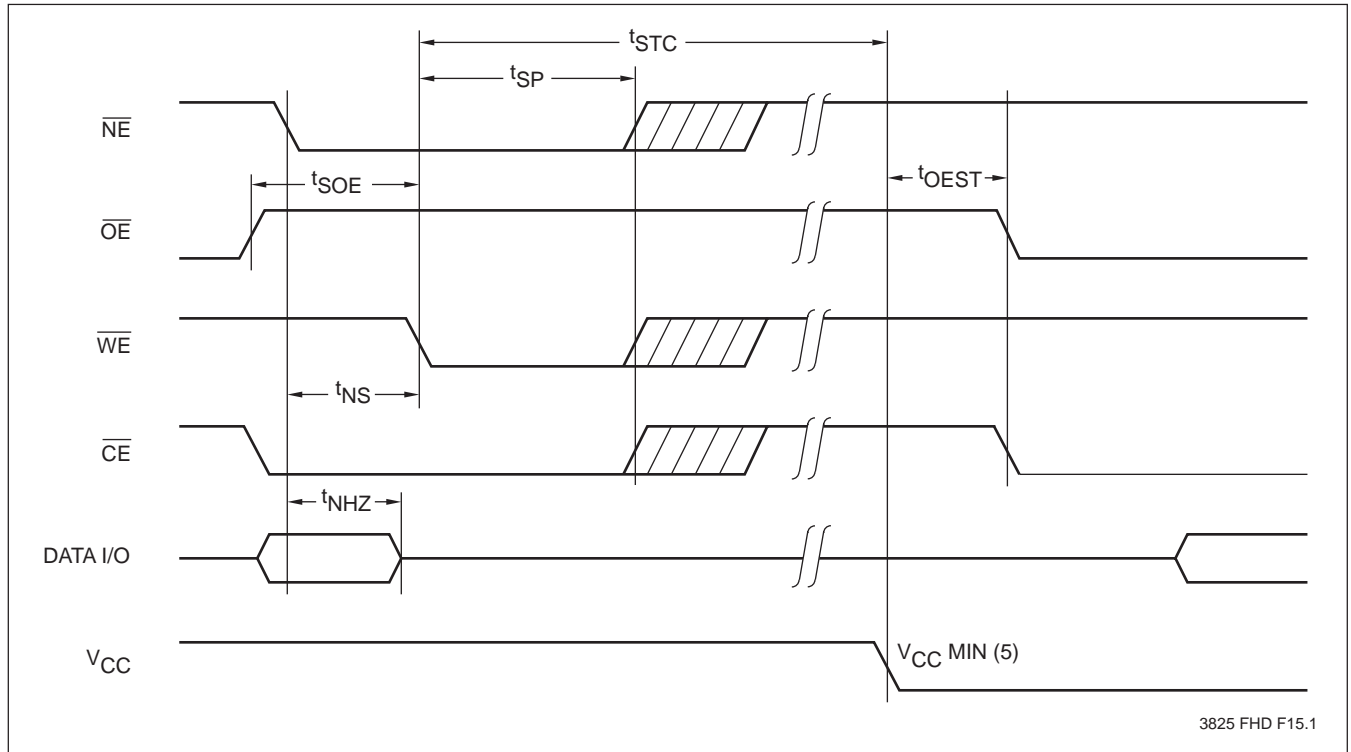
# X20C04

## STORE CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{STC}$	Store Cycle Time		5		5		5		5	ms
$t_{SP}$	Store Pulse Width	100		120		150		200		ns
$t_{NHZ}$	Nonvolatile Enable to Output in High Z		80		100		100		100	ns
$t_{OEST}$	Output Enable From End of Store	10		10		10		10		ns
$t_{SOE}$	$\overline{OE}$ Disable to Store Function	20		20		20		20		ns
$t_{NS}$	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		0		ns

3825 PGM T09

## Store Timing



3825 FHD F15.1

**Note:** (5) X20C04  $V_{CC}$  min. = 4.5V

The Store Pulse Width ( $t_{SP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{WE}$  and  $\overline{CE}$  must be LOW simultaneously.

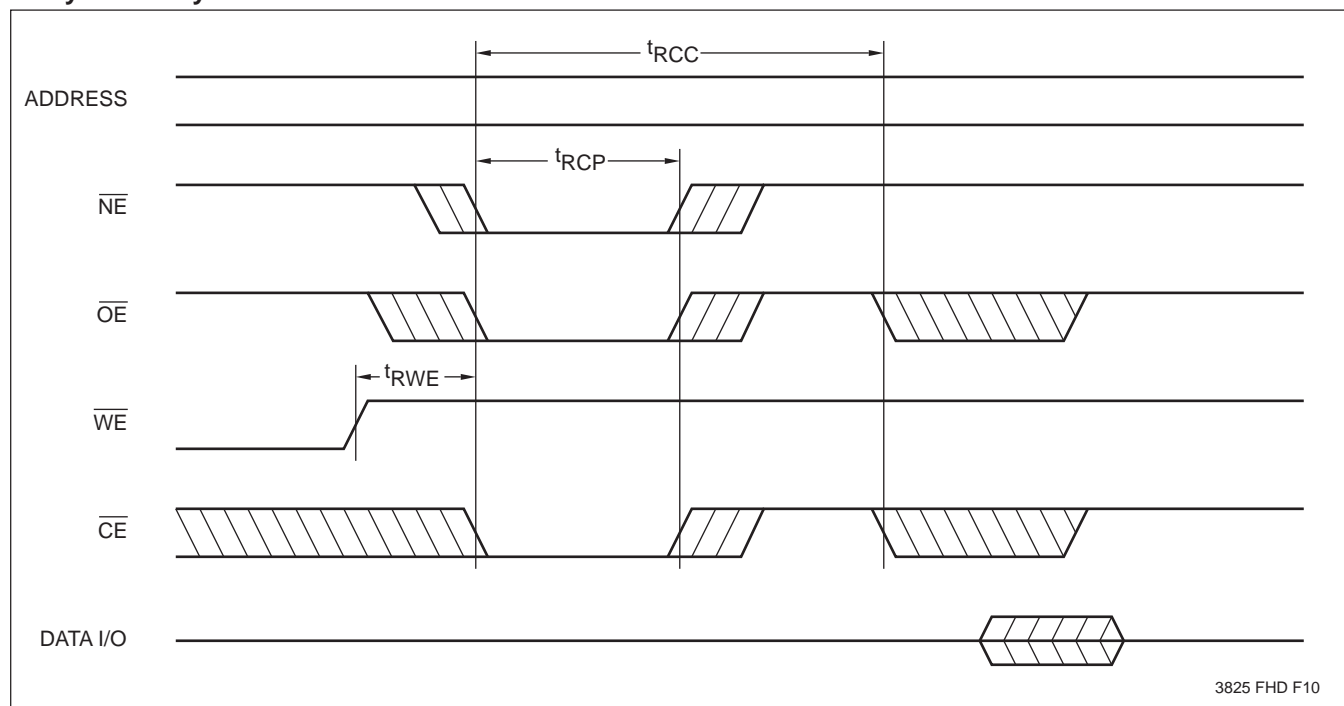
# X20C04

## ARRAY RECALL CYCLE LIMITS

Symbol	Parameter	X20C04-15		X20C04-20		X20C04-25		X20C04		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RCC}$	Array Recall Cycle Time		5		5		5		5	$\mu$ s
$t_{RCP}^{(6)}$	Recall Pulse Width to Initiate Recall	0.1	1	0.12	1	0.15	1	0.2	1	$\mu$ s
$t_{RWE}$	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		0		ns

3825 PGM T13.1

## Array Recall Cycle



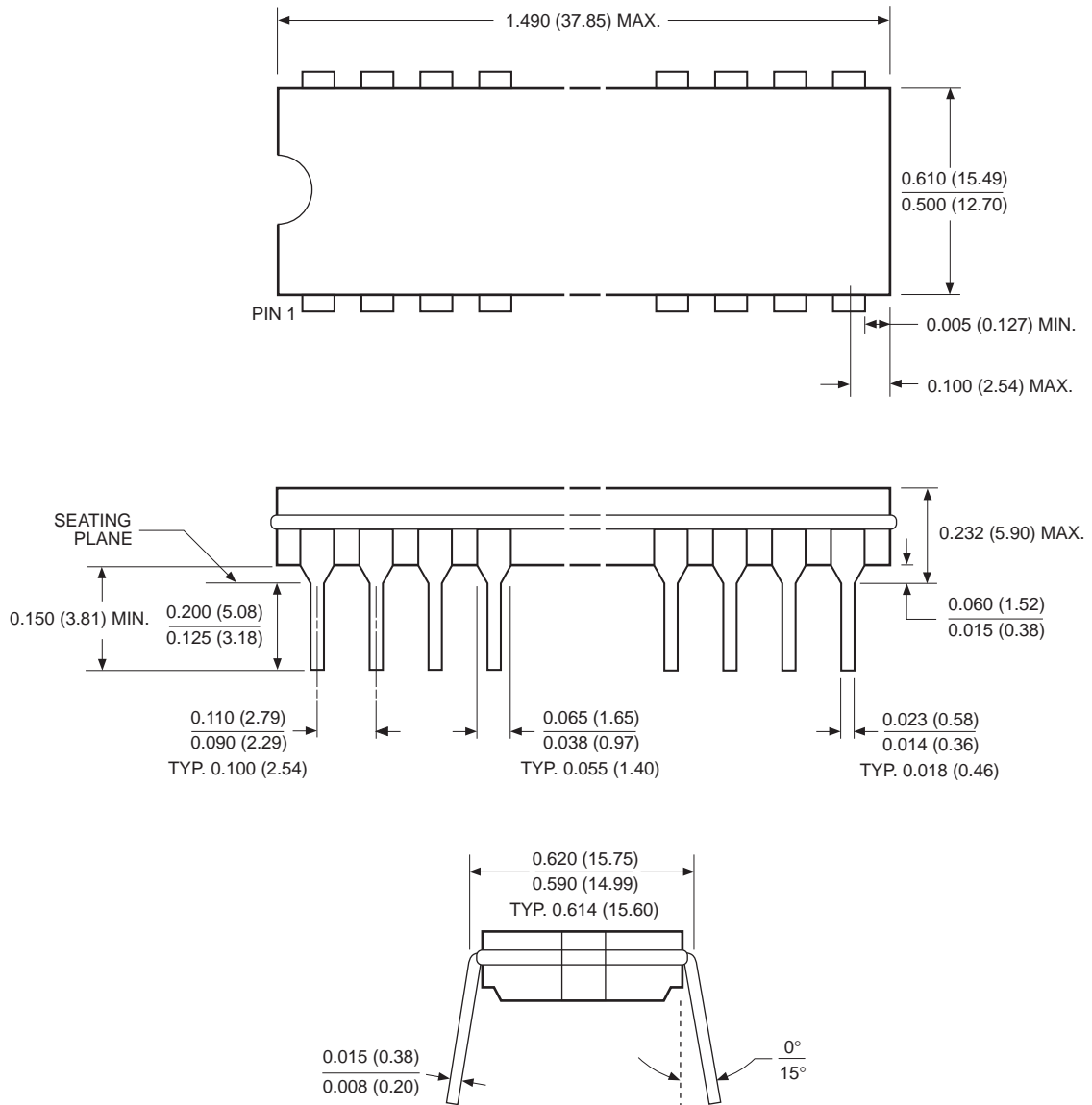
3825 FHD F10

**Note:** (6) The Recall Pulse Width ( $t_{RCP}$ ) is a minimum time that  $\overline{NE}$ ,  $\overline{OE}$  and  $\overline{CE}$  must be LOW simultaneously to insure data integrity,  $\overline{NE}$  and  $\overline{CE}$ .

# X20C04

## PACKAGING INFORMATION

### 28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



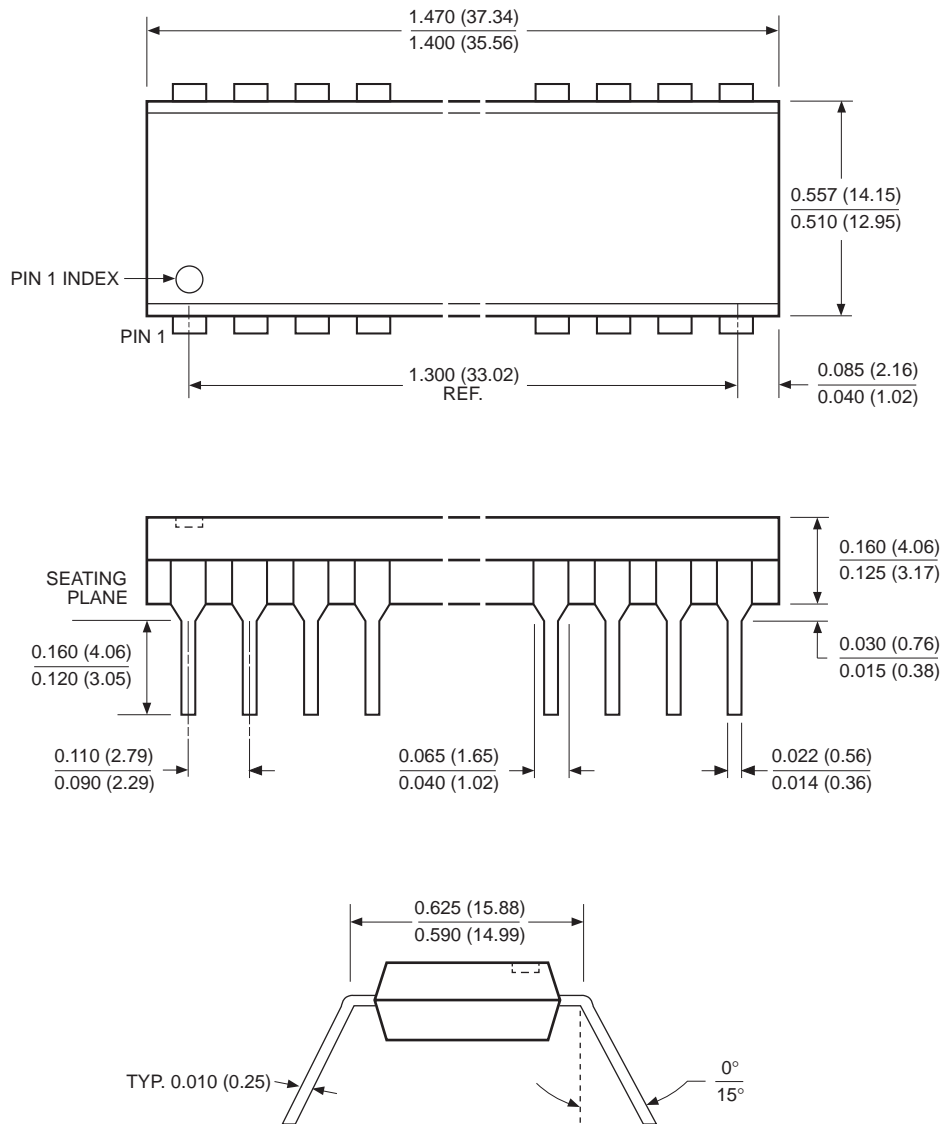
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F08

# X20C04

## PACKAGING INFORMATION

### 28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



**NOTE:**

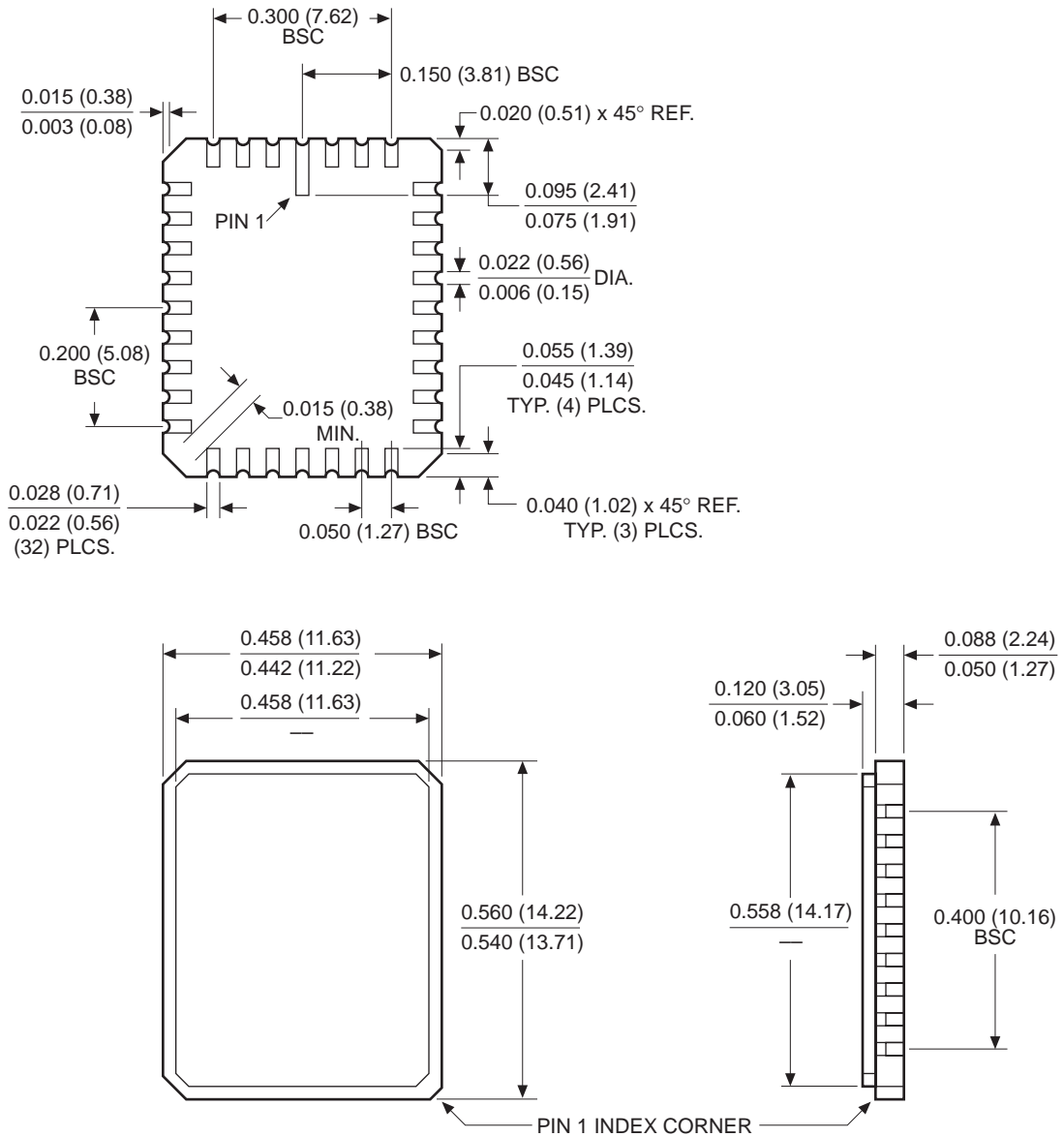
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

3926 FHD F04

# X20C04

## PACKAGING INFORMATION

### 32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

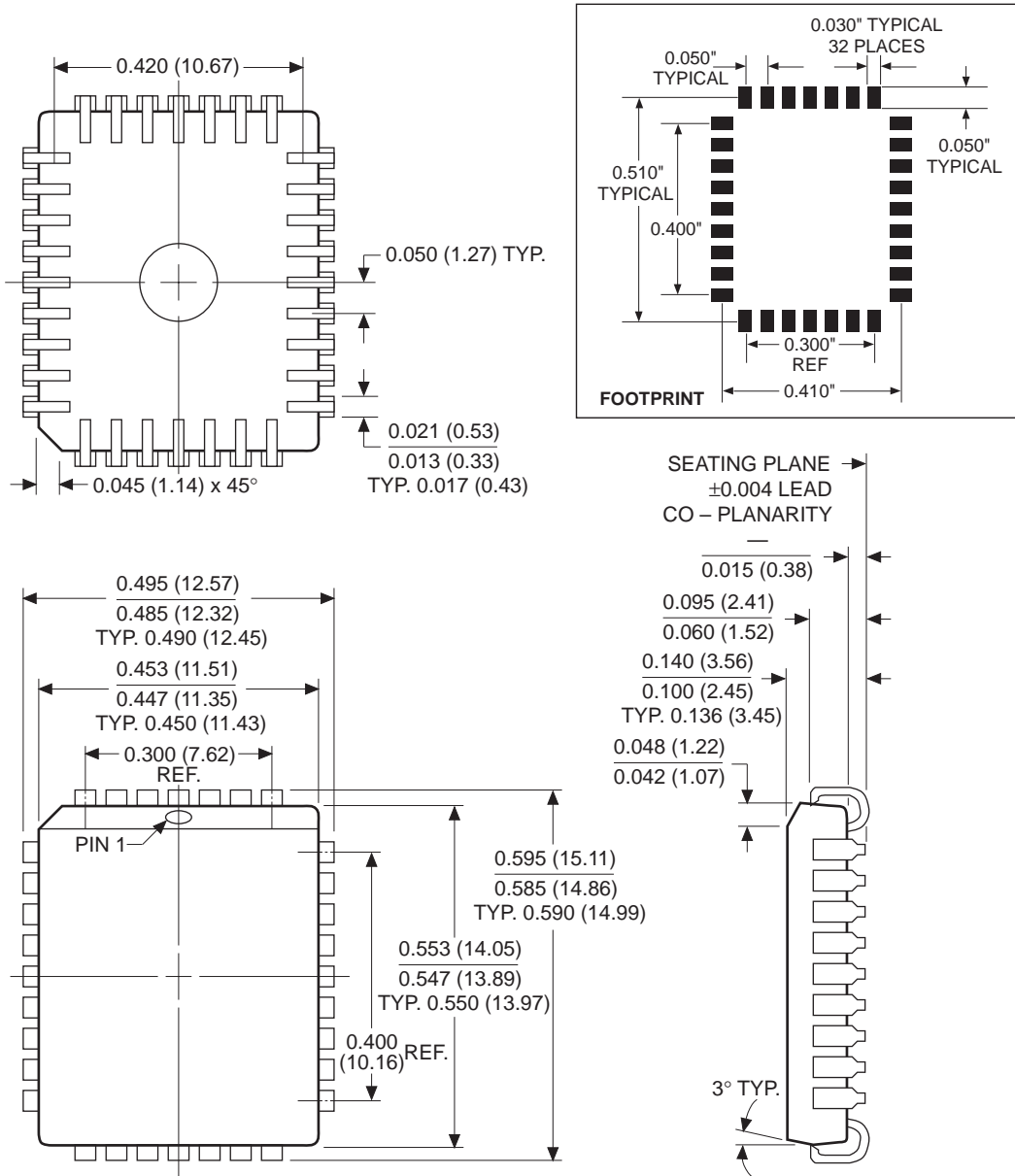


**NOTE:**

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE:  $\pm 1\%$  NLT  $\pm 0.005$  (0.127)

3926 FHD F14

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

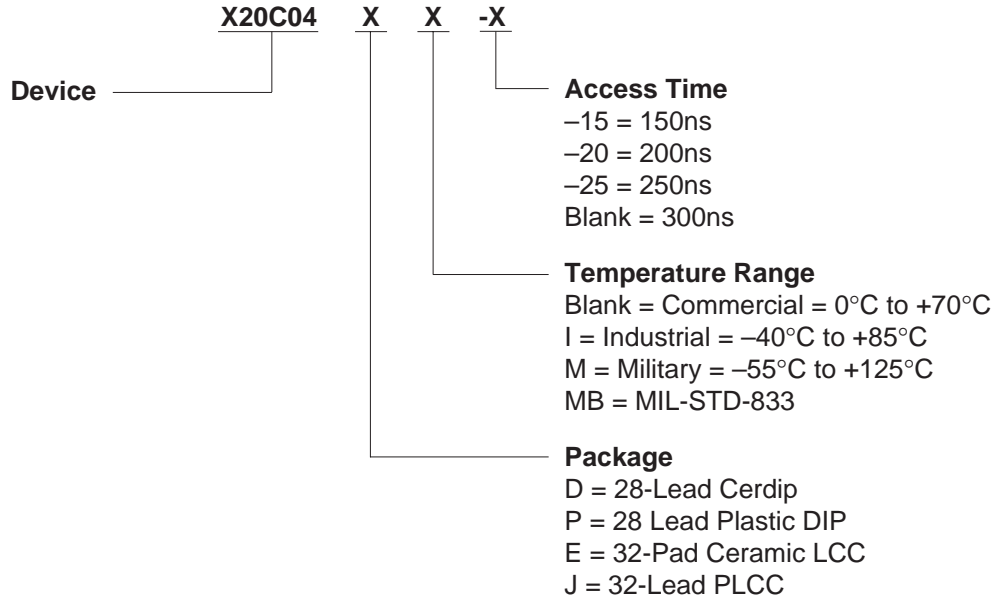


- NOTES:**
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
  2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

# X20C04

---

## ORDERING INFORMATION



---

### LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

### US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976. Foreign patents and additional patents pending.

### LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use as critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.