

Serial E²PROM

FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
 - Active Read Current Less Than 1 mA
 - Active Write Current Less Than 3 mA
 - Standby Current Less Than 50 μ A
- Internally Organized 2048 x 8
- 2 Wire Serial Interface
 - Bidirectional Data Transfer Protocol
- Sixteen Byte Page Write Mode
 - Minimizes Total Write Time Per Byte
- Self Timed Write Cycle
 - Typical Write Cycle Time of 5 ms
- High Reliability
 - Endurance: 100,000 Cycles
 - Data Retention: 100 Years
- Pin and Function Compatible with X24C16
- 8-Pin Plastic DIP and 8-Lead SOIC Packages

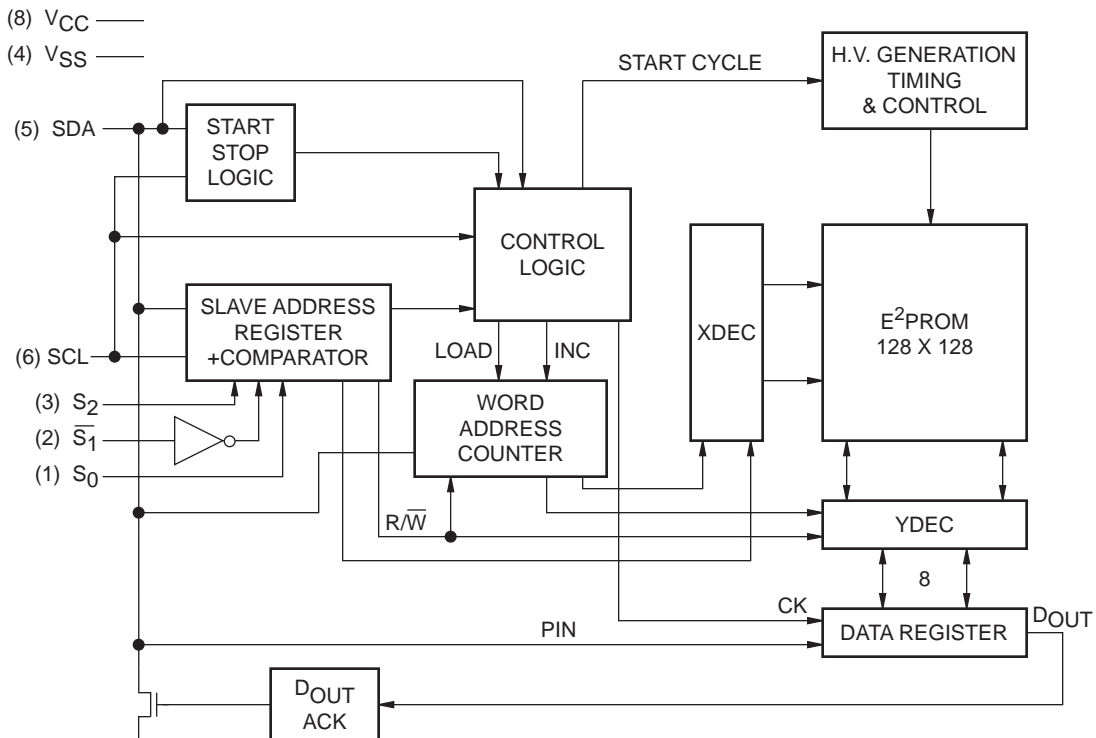
DESCRIPTION

The X24164 is a CMOS 16,384 bit serial E²PROM, internally organized 2048 x 8. The X24164 features a serial interface and software protocol allowing operation on a simple two wire bus.

Three device select inputs (S₀–S₂) allow up to eight devices to share a common two wire bus.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

FUNCTIONAL DIAGRAM



3846 FHD F01

X24164

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-Up Resistor selection graph at the end of this data sheet.

Device Select (S_0 , \bar{S}_1 , S_2)

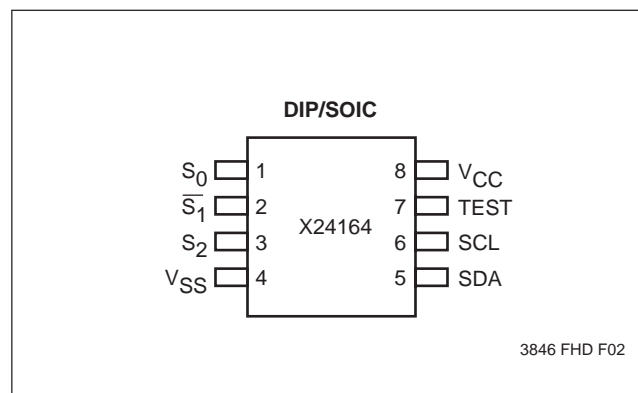
The device select inputs (S_0 , \bar{S}_1 , S_2) are used to set the second, third and fourth bits of the 8 bit slave address. This allows up to eight X24164's to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven to V_{SS} or V_{CC} . To be compatible with the X24C16 these pins must all be tied to V_{SS} .

Pin Names

Symbol	Description
S_0 – S_2	Device Select Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	Supply Voltage

3846 PGM T01

PIN CONFIGURATION



X24164

DEVICE OPERATION

The X24164 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24164 will be considered a slave in all applications.

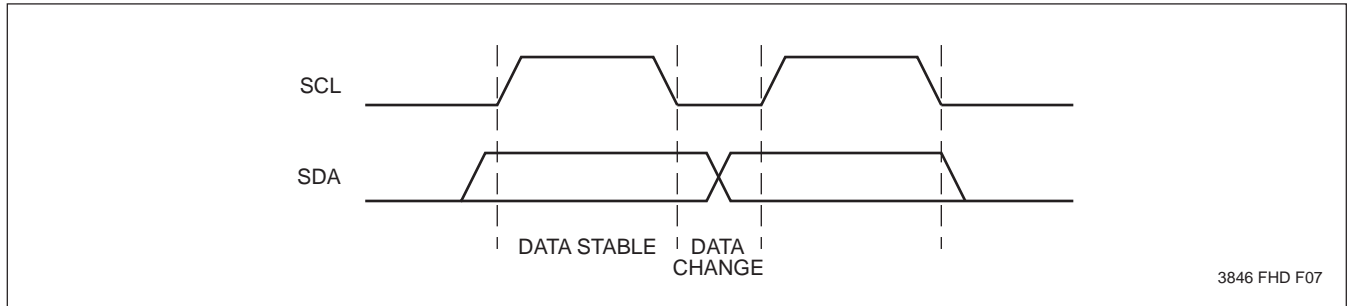
Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24164 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

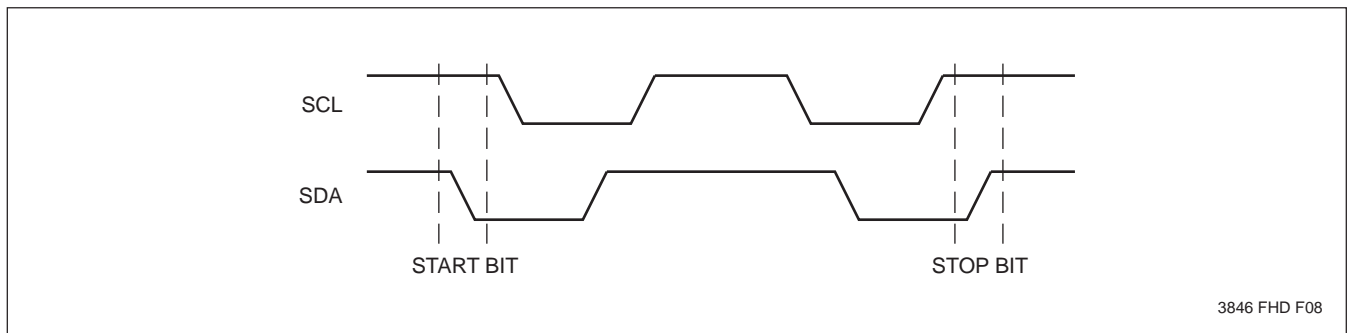
Figure 1. Data Validity



Notes: (5) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage (5V)

(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Figure 2. Definition of Start and Stop



X24164

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

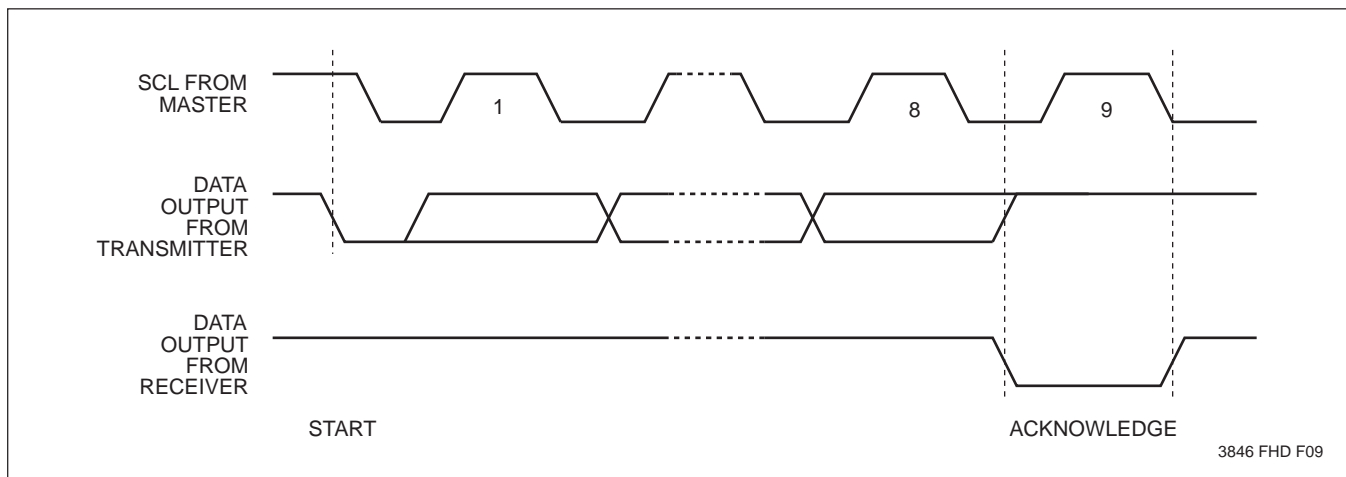
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24164 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24164 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24164 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24164 will continue to transmit data. If an acknowledge is not detected, the X24164 will terminate further data transmissions. The master must then issue a stop condition to return the X24164 to the standby power mode and place the device into a known state.

Figure 3. Acknowledge Response From Receiver

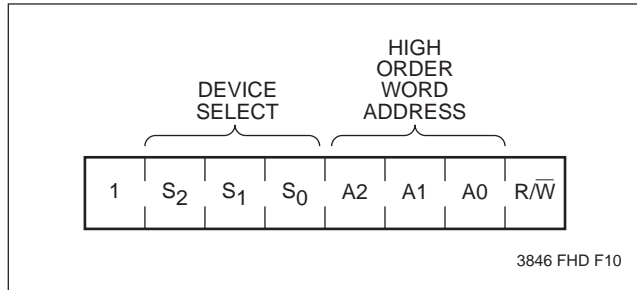


X24164

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant bit of the slave is a one (see Figure 4). The next three bits are the device select bits. A system could have up to eight X24164's on the bus. The eight addresses are defined by the state of the S_0 , S_1 , and S_2 inputs. S_1 of the slave address must be the inverse of the \overline{S}_1 input pin.

Figure 4. Slave Address



The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the whole 2048 x 8 array.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

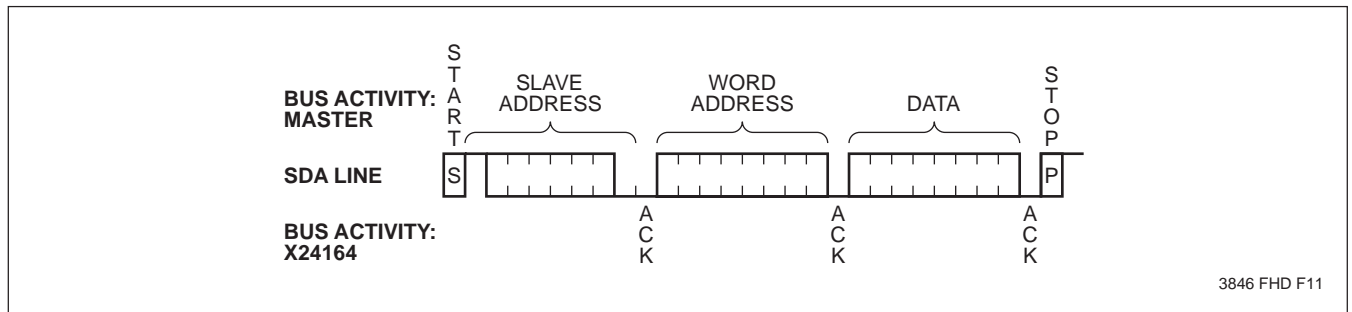
Following the start condition, the X24164 monitors the SDA bus comparing the slave address being transmitted with its slave address device type identifier. Upon a correct compare the X24164 outputs an acknowledge on the SDA line. Depending on the state of the R/\overline{W} bit, the X24164 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24164 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of 2048 words in the array. Upon receipt of the word address the X24164 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24164 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24164 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write



X24164

Page Write

The X24164 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24164 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24164 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a **write operation**. If the X24164 is still busy with the write operation no ACK will be returned. If the X24164 has completed the **write operation** an ACK will be returned and the host can then proceed with the next read or write operation. Refer to Flow 1.

Flow 1. ACK Polling Sequence

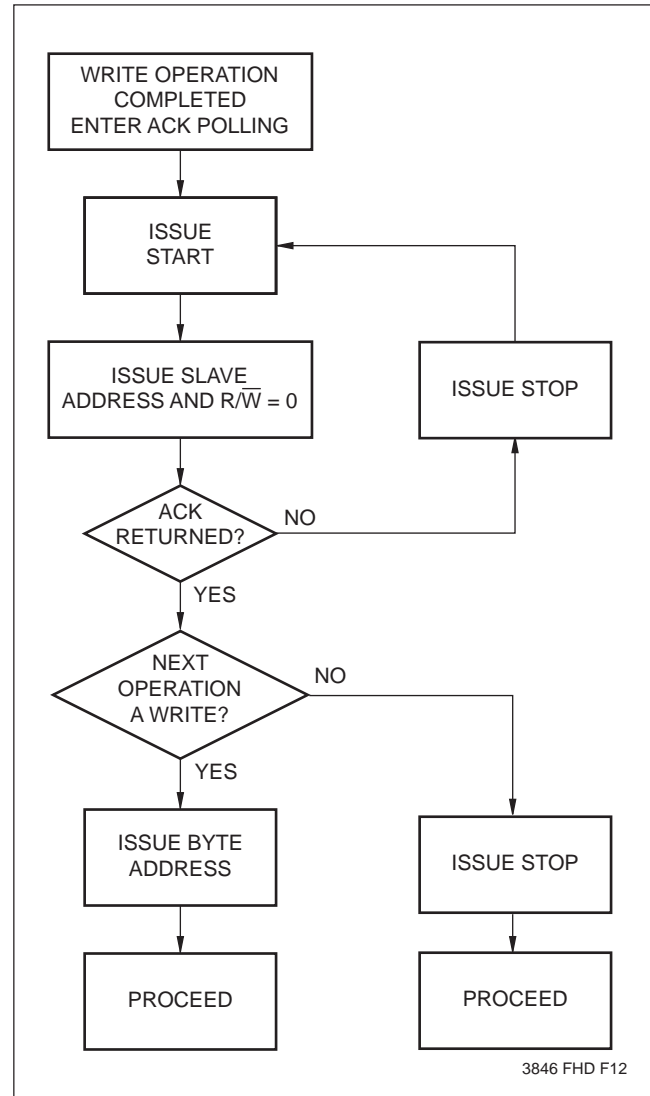
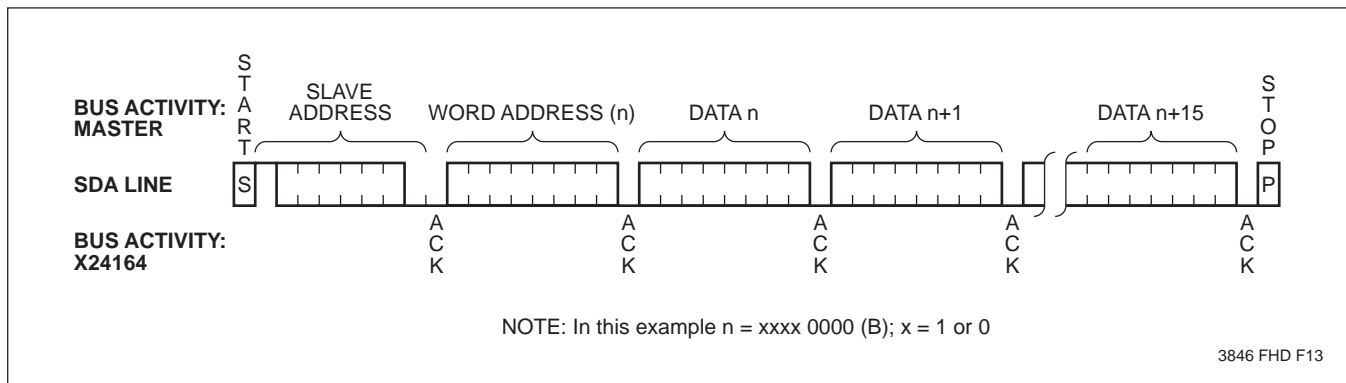


Figure 6. Page Write



X24164

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Current Address Read

Internally the X24164 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/W set to one, the X24164 issues an acknowledge and transmits the eight bit word.

The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24164 and then by the eight bit word. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read

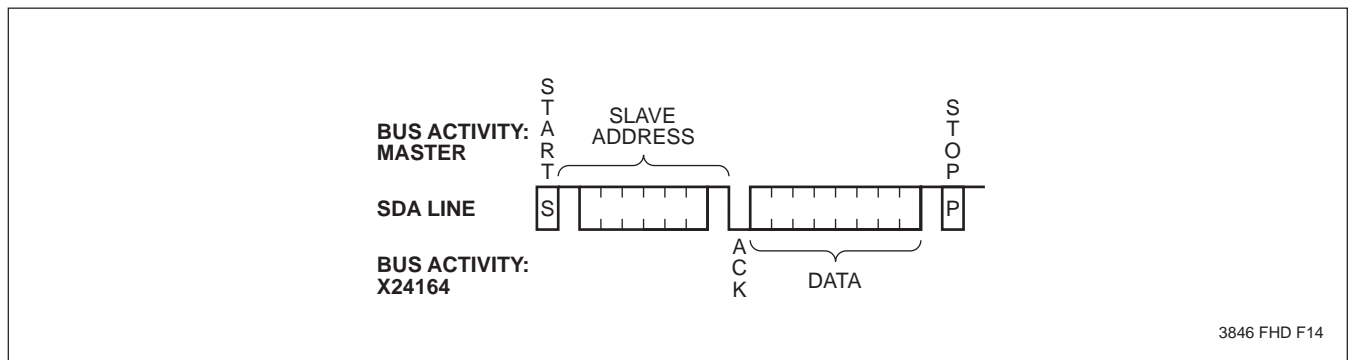
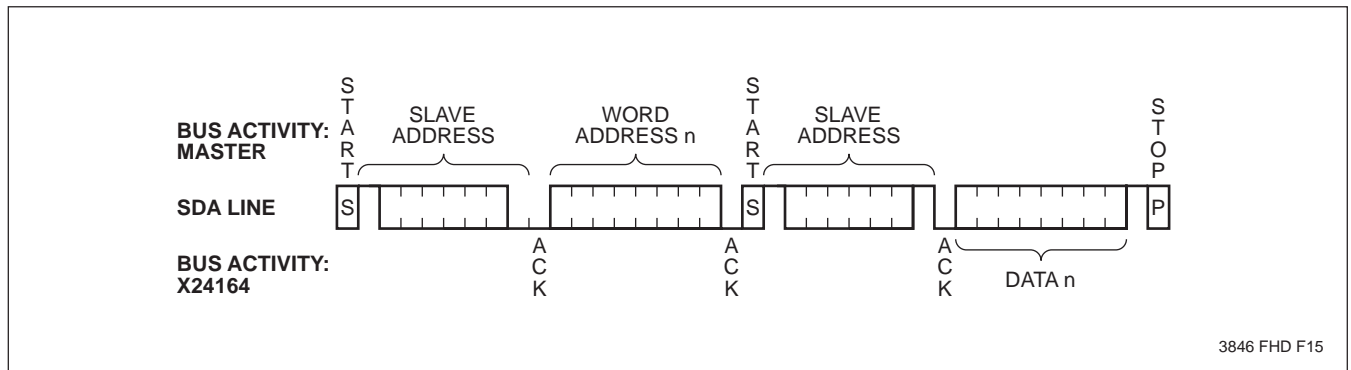


Figure 8. Random Read



X24164

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24164 continues to output data for each acknowledge received. The read operation is terminated by the master; by not responding with an acknowledge and by issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from $n + 1$. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 2047), the counter “rolls over” to 0 and the X24164 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

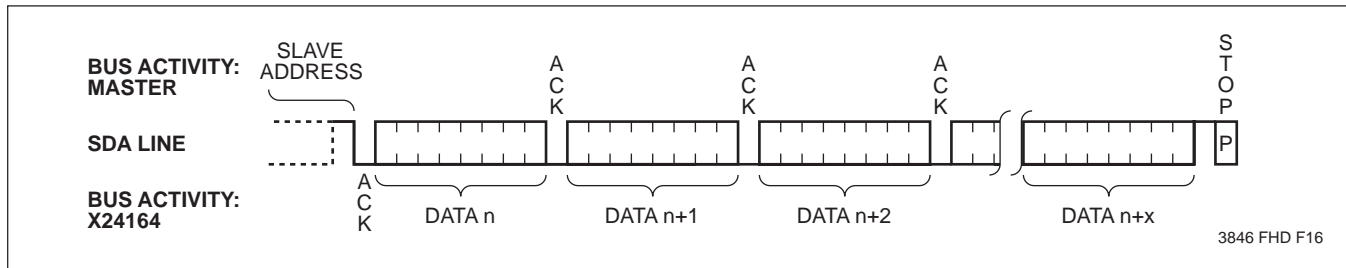
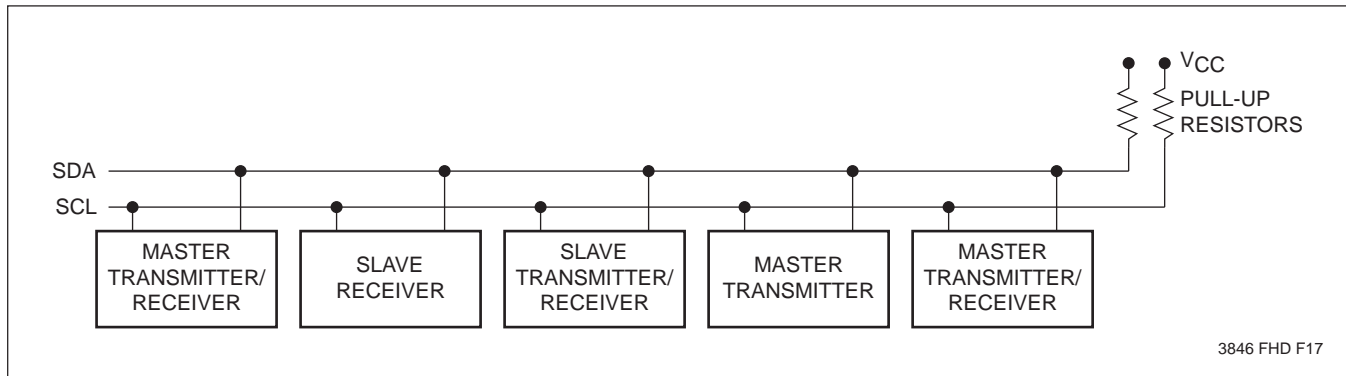


Figure 10. Typical System Configuration



X24164

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias

X24164 -65°C to +135°C

Storage Temperature -65°C to +150°C

Voltage on any Pin with

Respect to V_{SS} -1.0V to +7.0V

D.C. Output Current 5 mA

Lead Temperature (Soldering, 10 Seconds) 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

3846 PGM T02

Supply Voltage	Limits
X24164	4.5V to 5.5V
X24164-3	3V to 5.5V
X24164-2.7	2.7V to 5.5V

3846 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	SCL = $V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 100 KHz, SDA = Open, All
Other I_{CC2}	V_{CC} Supply Current (Write)		3	mA	
$I_{SB1}^{(1)}$	V_{CC} Standby Current		150	μA	SCL = SDA = V_{CC} , All Other Inputs = GND or $V_{CC} - 0.3V$, $V_{CC} = 5V \pm 10\%$
$I_{SB2}^{(1)}$	V_{CC} Standby Current		50	μA	SCL = SDA = V_{CC} , All Other Inputs = GND or $V_{CC} - 0.3V$, $V_{CC} = 3V$
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = GND$ to V_{CC}
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = GND$ to V_{CC}
$V_{IL}^{(2)}$	Input Low Voltage	-1.0	$V_{CC} \times 0.3$	V	
$V_{IH}^{(2)}$	Input High Voltage	$V_{CC} \times 0.7$	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 3$ mA

3846 PGM T04

CAPACITANCE $T_A = 25^\circ C$, $f = 1.0$ MHz, $V_{CC} = 5V$

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}^{(3)}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}^{(3)}$	Input Capacitance (S_0, S_1, S_2, SCL)	6	pF	$V_{IN} = 0V$

3846 PGM T05

- Notes: (1) Must perform a stop command prior to measurement.
 (2) V_{IL} min. and V_{IH} max. are for reference only and are not 100% tested.
 (3) This parameter is periodically sampled and not 100% tested.

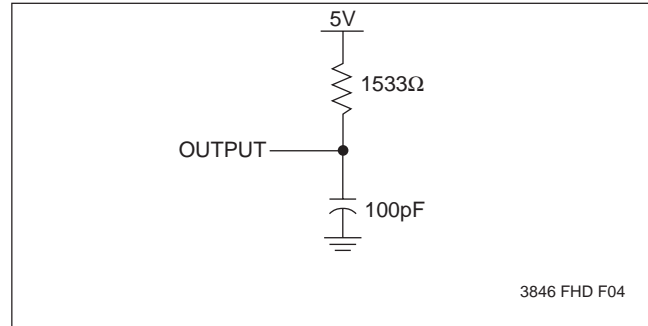
X24164

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$

3846 PGM T06

EQUIVALENT A.C. LOAD CIRCUIT



3846 FHD F04

A.C. CHARACTERISTICS (Over recommended operating range unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

3846 PGM T07

POWER-UP TIMING⁽⁴⁾

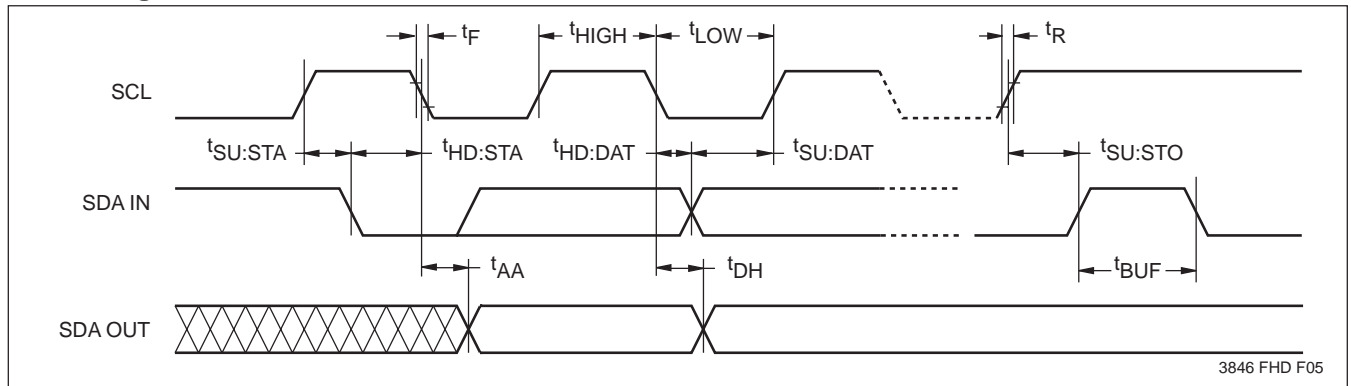
Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	5	ms

3846 PGM T08

Notes: (4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24164

Bus Timing



3846 FHD F05

Write Cycle Limits

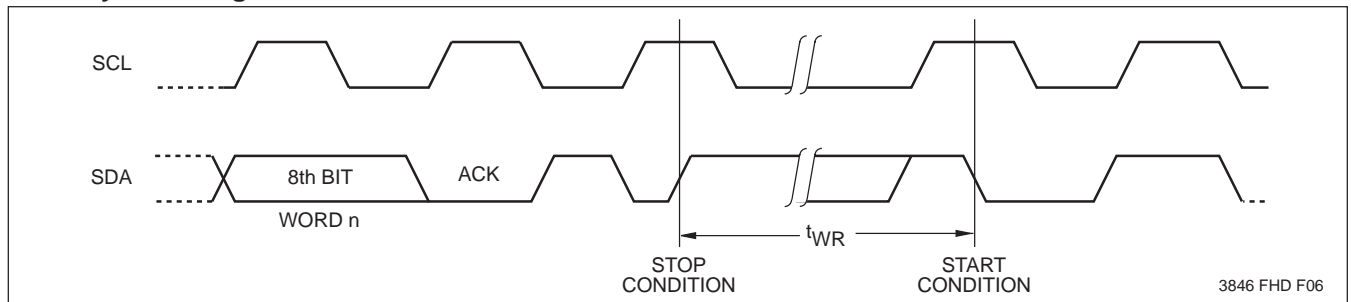
Symbol	Parameter	Min.	Typ. ⁽⁵⁾	Max.	Units
$T_{WR}^{(6)}$	Write Cycle Time		5	10	ms

3846 PGM T09

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24164

bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing

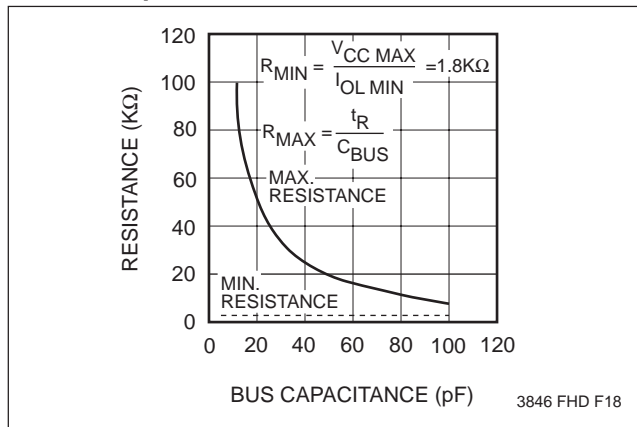


3846 FHD F06

Notes: (5) Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage (5V).

(6) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



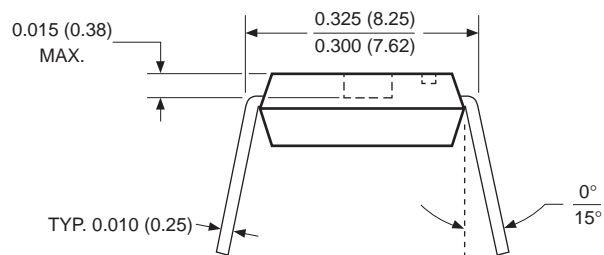
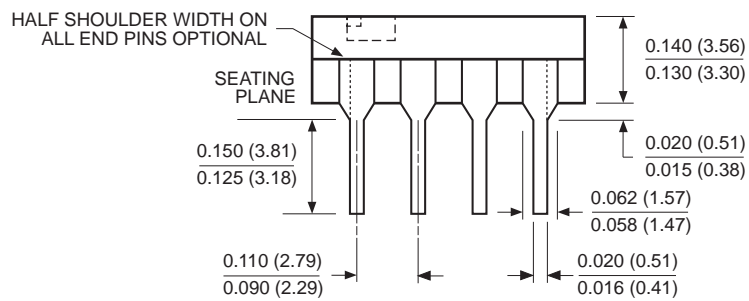
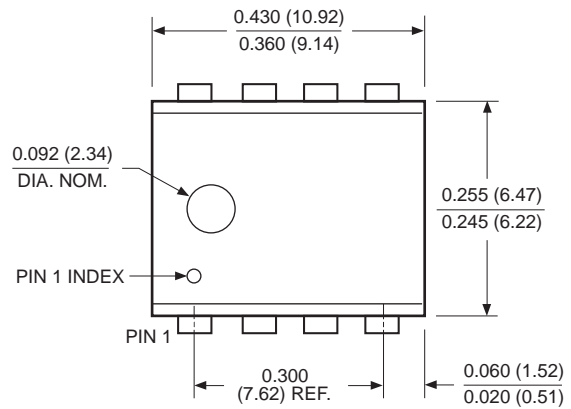
3846 FHD F18

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



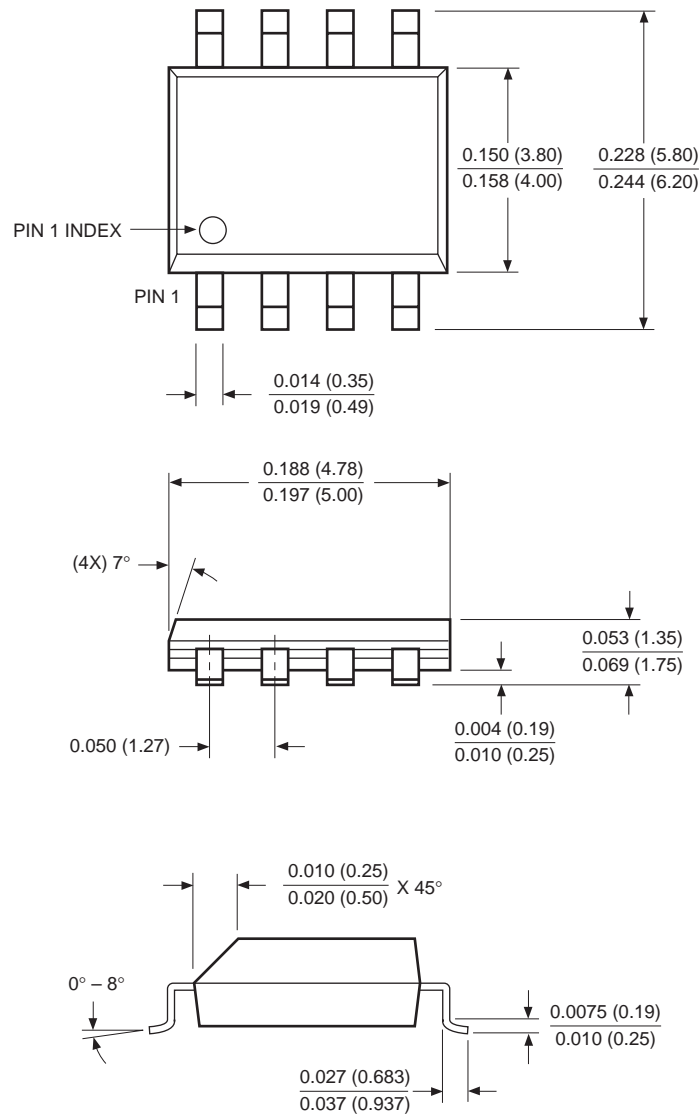
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F01

X24164

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

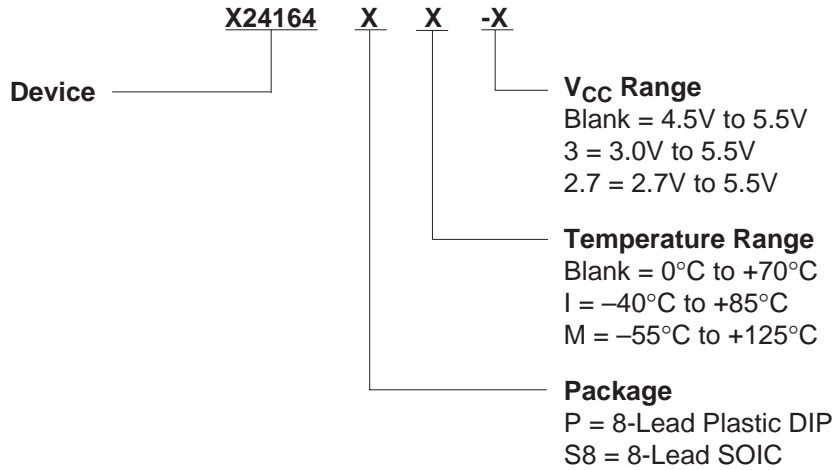


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESIS IN MILLIMETERS)

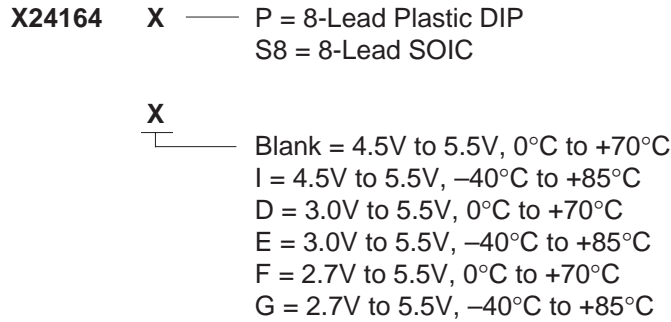
3926 FHD F22

X24164

ORDERING INFORMATION



Part Mark Convention



LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurrence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.