ICmic™
IC MICROSYSTEMS

2K	X24C02	256 x 8 Bit

Serial E^{2}PROM

FEATURES

- 2.7V to 5.5V Power Supply
- Low Power CMOS
  - —Active Current Less Than 1 mA
  - —Standby Current Less Than 50 ∝A
- Internally Organized 256 x 8
- Self Timed Write Cycle
  - —Typical Write Cycle Time of 5 ms
- 2 Wire Serial Interface
  - —Bidirectional Data Transfer Protocol
- Four Byte Page Write Operation
  - —Minimizes Total Write Time Per Byte
- High Reliability
  - —Endurance: 100,000 Cycles
  - —Data Retention: 100 Years
- New Hardwire—Write Control Function

DESCRIPTION

The X24C02 is CMOS a 2048 bit serial E^{2}PROM, internally organized 256 x 8. The X24C02 features a serial interface and software protocol allowing operation on a simple two wire bus. Three address inputs allow up to eight devices to share a common two wire bus.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years. Available in DIP, MSOP and SOIC packages.

FUNCTIONAL DIAGRAM

3838 FHD F01

1

Characteristics subject to change without notice
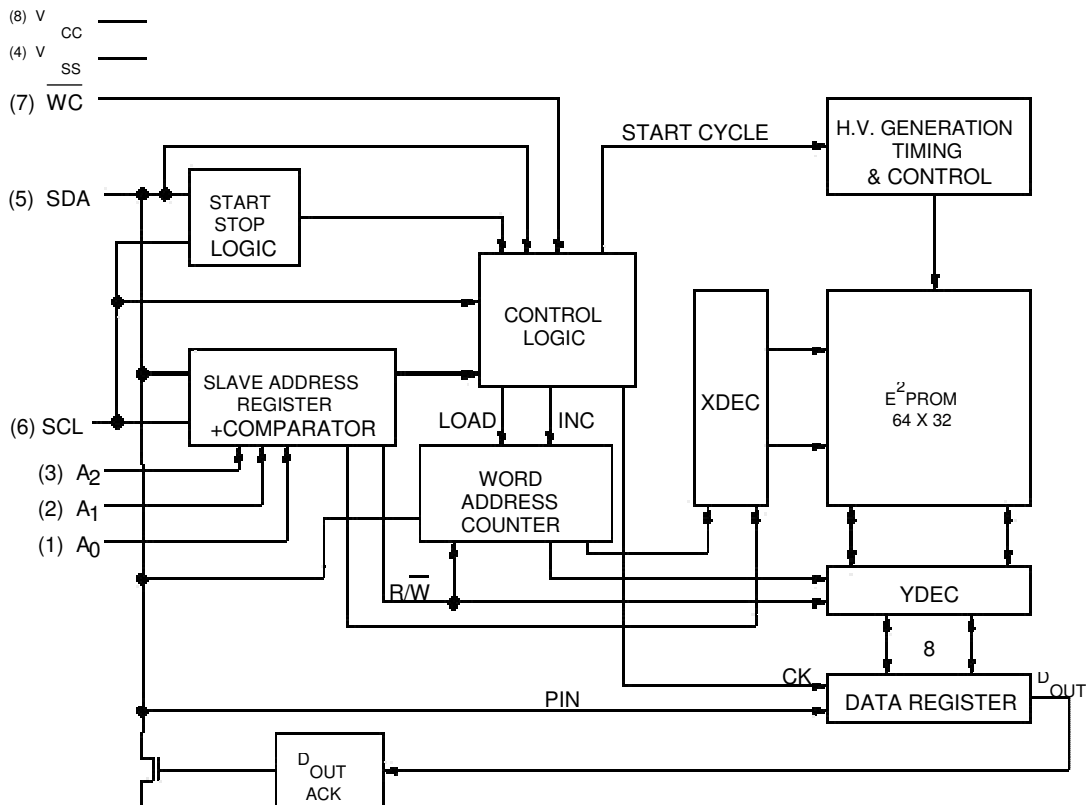
X24C02

PIN DESCRIPTIONS

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be

wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Guide-

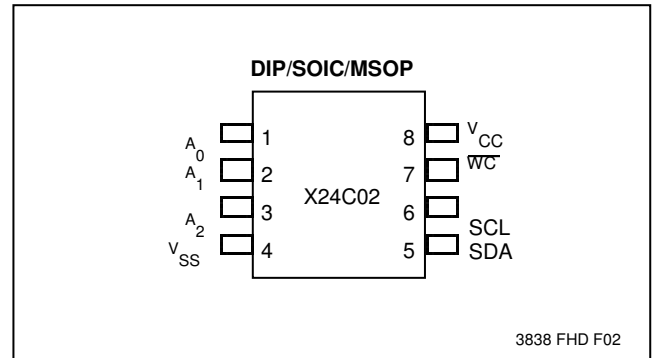lines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A_0, A_1, A_2)
The address inputs are used to set the least significant three bits of the seven bit slave address. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven to V_{SS} or to V_{CC}.

Write Control (WC)
The Write Control input controls the ability to write to the device. When WC is LOW (tied to V_{SS}) the X24C02 will be enabled to perform write operations. When WC is HIGH (tied to V_{CC}) the internal high voltage circuitry will be disabled and all writes will be disabled.

PIN CONFIGURATION

DIP/SOIC/MSOP

X24C02

Pin	Signal
1	A_0
2	A_1
3	A_2
4	V_{SS}
5	SDA
6	SCL
7	$\overline{WC}$
8	V_{CC}

3838 FHD F02

PIN DESCRIPTIONS

Symbol	Description
A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
WC	Write Control
V_{SS}	Ground
V_{CC}	+5V

3838 PGM T01

X24C02

DEVICE OPERATION

The X24C02 supports a bidirectional bus oriented protocol The protocol defines any device that sends data onto the

bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the

device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit

and receive operations. Therefore, the X24C02 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are re-

served for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is

HIGH. The X24C02 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 1. Data Validity
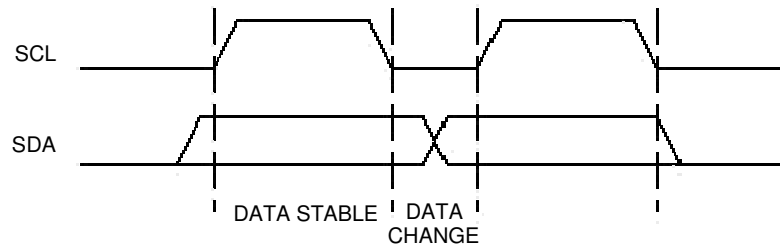
3838 FHD F06

X24C02

Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C02 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.
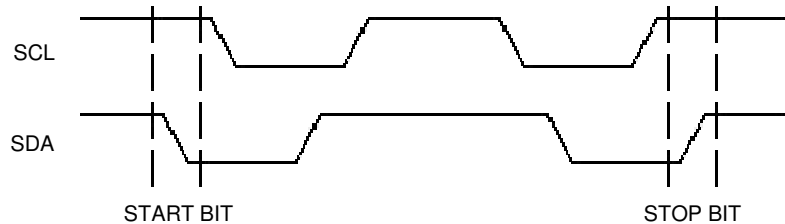
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C02 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24C02 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24C02 will transmit eight bits of data release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24C02 will continue to transmit data. If an acknowledge is not detected, the X24C02 will terminate further data transmissions. The master must then issue a stop condition to return the X24C02 to the standby power mode and place the device into a known state.

Figure 2. Definition of Start and Stop

3838 FHD F07

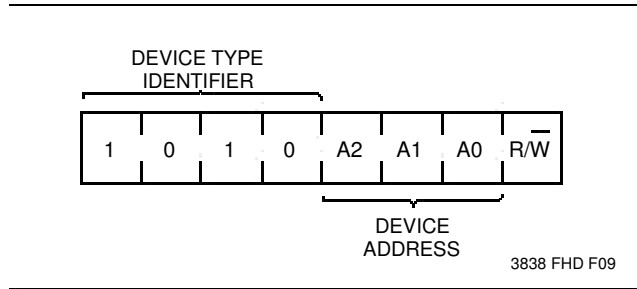## Figure 3. Acknowledge Response From Receiver
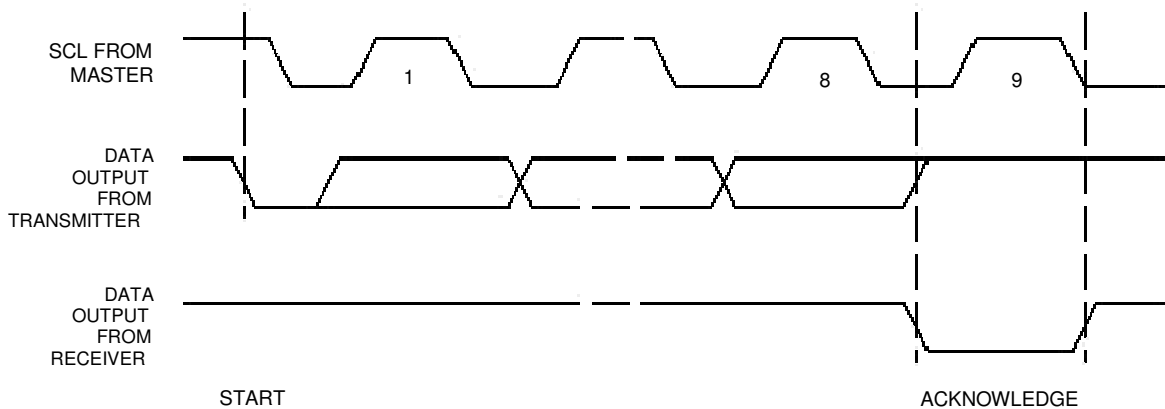
3838 FHD F08

X24C02

DEVICE ADDRESSING

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave are the device type identifier (see Figure 4). For the X24C02 this is fixed as 1010[B].

Figure 4. Slave Address

```
                DEVICE TYPE
                 IDENTIFIER
              ┌──────────────┐
          ┌───┬───┬───┬───┬───┬───┬───┬─────┐
          │ 1 │ 0 │ 1 │ 0 │A2 │A1 │A0 │ R/W │
          └───┴───┴───┴───┴───┴───┴───┴─────┘
                          └──────────┘
                            DEVICE
                            ADDRESS
                                    3838 FHD F09
```

The next three significant bits address a particular device. A system could have up to eight X24C02 devices on the bus (see Figure 10). The eight addresses are defined by the state of the A_0, A_1 and A_2 inputs.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operations is selected.

Following the start condition, the X24C02 monitors the SDA bus comparing the slave address being transmitted with its slave address (device type and state of A_0, A_1 and A_2 inputs). Upon a correct compare the X24C02 outputs an acknowledge on the SDA line. Depending on the state of the R/W bit, the X24C02 will execute a read or write operation.
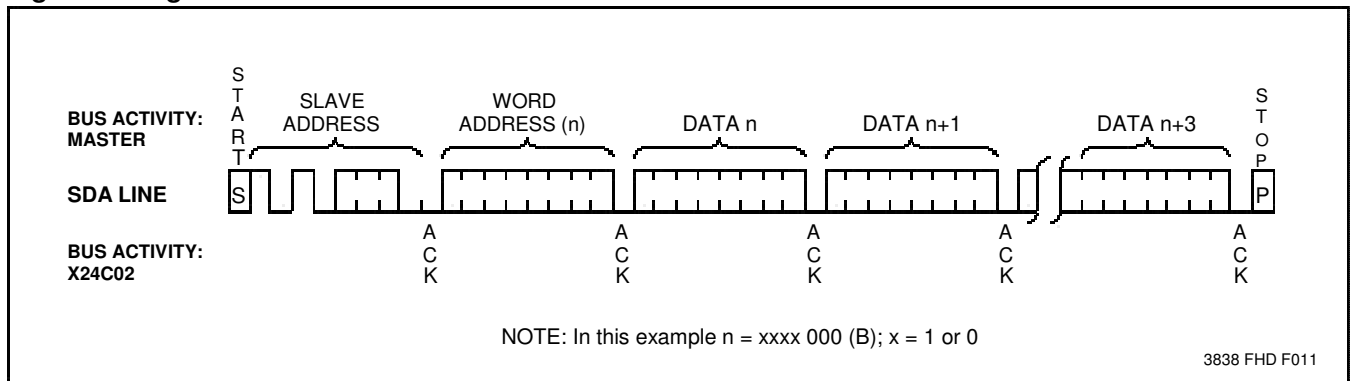
WRITE OPERATIONS

Byte Write
For a write operation, the X24C02 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24C02 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24C02 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24C02 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5. Byte Write

Figure 6. Page Write

NOTE: In this example n = xxxx 000 (B); x = 1 or 0
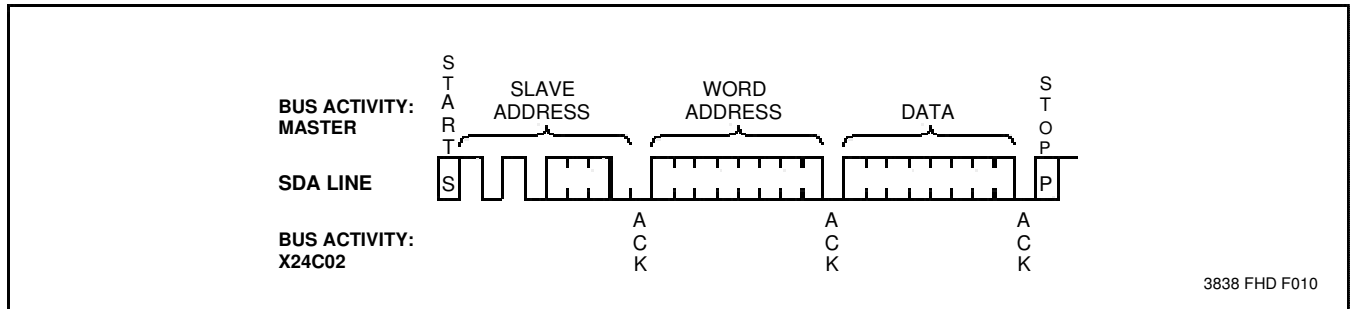
X24C02

Page Write

The X24C02 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to three more words. After the receipt of each word, the X24C02 will respond with an acknowledge.

After the receipt of each word, the two low order address bits are internally incremented by one. The high order six bits of the address remain constant. If the master should transmit more than four words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs, during the internal write operation, can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C02 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24C02 is still busy with the write operation no ACK will be returned. If the X24C02 has completed the write operation an ACK will be returned and the master can then proceed with the next read or write operation.

READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

It should be noted that the ninth clock cycle of the read operation is not a "don't care." To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

## Flow 1. ACK Polling Sequence
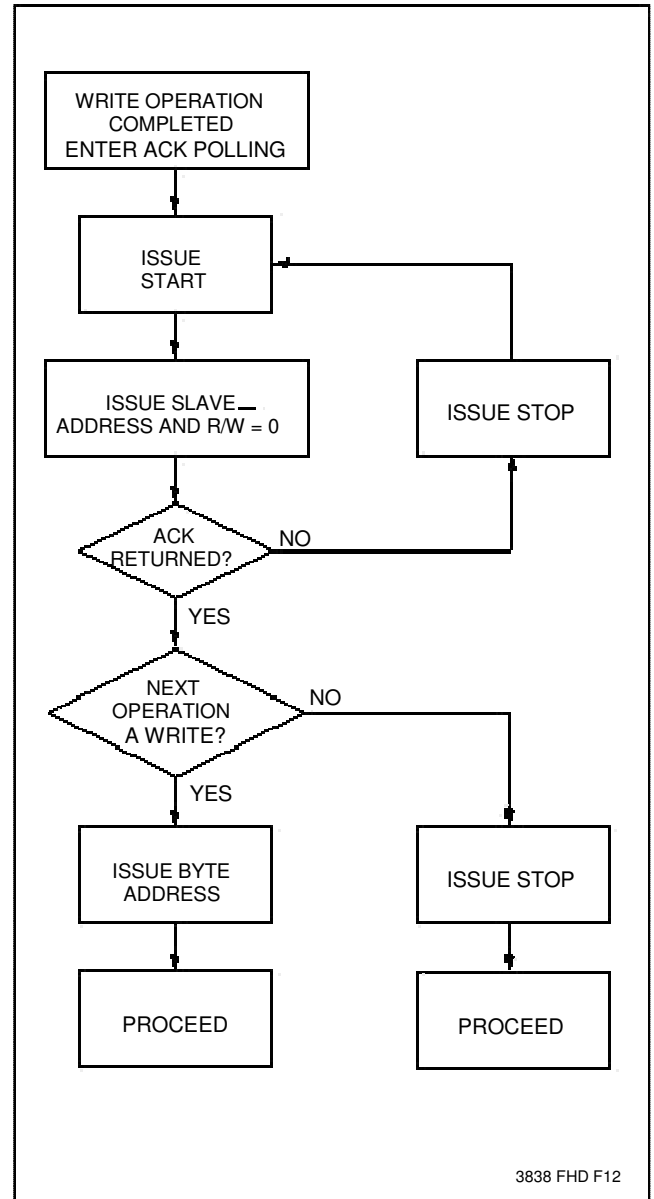
3838 FHD F12

X24C02

Current Address Read

Internally the X24C02 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with the R/W bit set to one, the X24C02 issues an acknowledge and transmits the eight bit word during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the X24C02 and then by the eight bit word. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Figure 7. Current Address Read
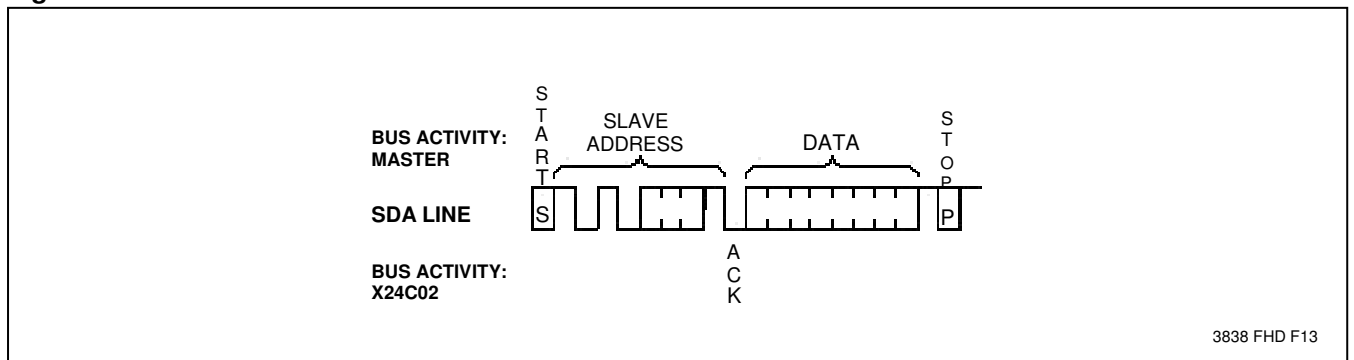
3838 FHD F13

Figure 8. Random Read
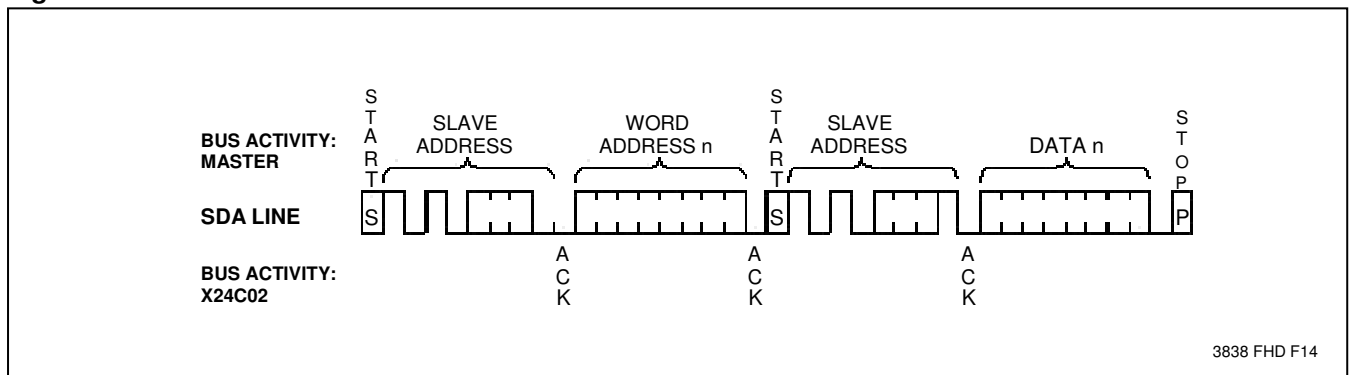
3838 FHD F14

X24C02

Sequential Read

Sequential Read can be initiated as either a current address read or random access read. The first word is transmitted as with the other modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24C02 continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge.

The data output is sequential, with the data from address and followed by the data from n + 1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255) the counter "rolls over" to address 0 and the X24C02 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 9. Sequential Read

3838 FHD F15
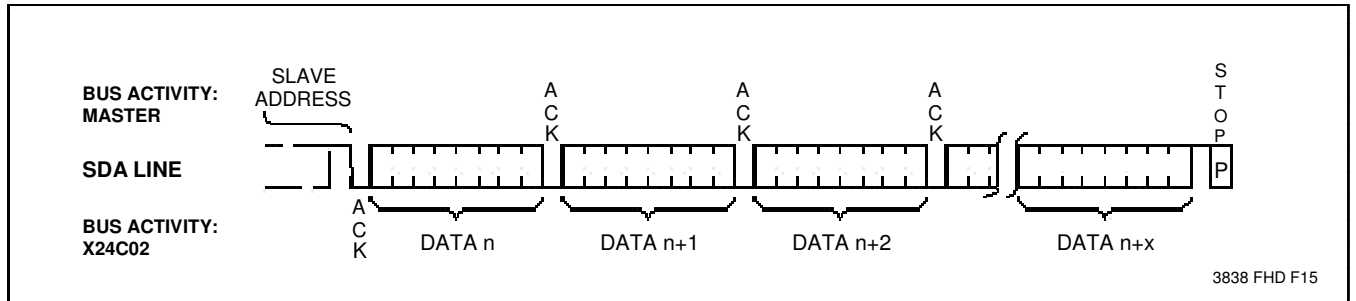
Figure 10. Typical System Configuration

3838 FHD F16
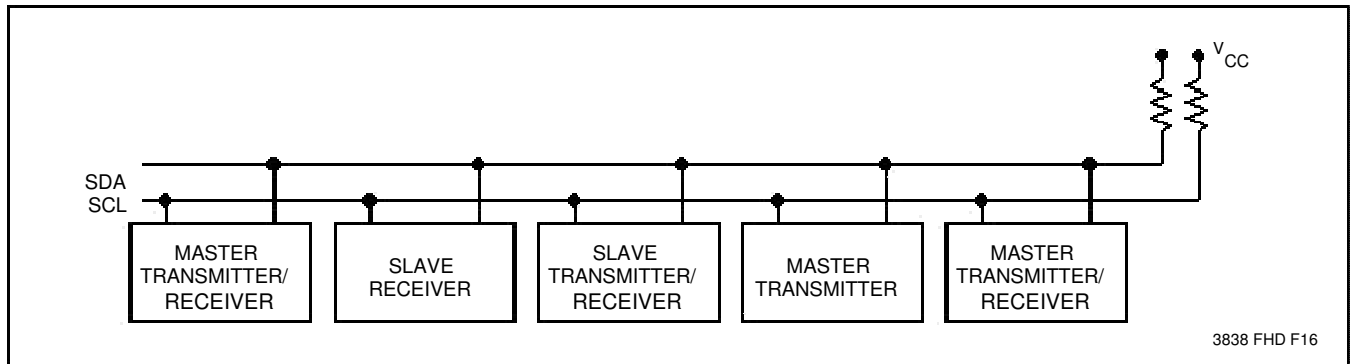
X24C02

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias   .... –65°C to +135°C
Storage Temperature .... –65°C to +150°C
Voltage on any Pin with
    Respect to V_{SS} .... –1.0V to +7.0V
D.C. Output Current .... 5 mA
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and the functional operation of the device at these or any other conditions above those

indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

3838 PGM T09

Supply Voltage	Limits
X24C02	4.5V to 5.5V
X24C02-3.5	3.5V to 5.5V
X24C02-3	3V to 5.5V
X24C02-2.7	2.7 to 5.5V

3838 PGM T10

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified).

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	Power Supply Current (read)		1	mA	SCL = V_{CC} x 0.1/V_{CC} x 0.9 Levels @ 100 KHz, SDA = Open, All Other Inputs = GND or V_{CC} – 0.3V
I_{CC2}	Power Supply Current (write)		2		
I_{SB}[1]	Standby Current		50	∝A	SCL = SDA = V_{CC} – 0.3V, All other Inputs = GND or V_{CC}, V_{CC} = 5.5V
I_{SB}[2]	Standby Current		30	∝A	SCL = SDA = V_{CC} – 0.3V, All Other Inputs = GND or V_{CC} = 3.3V + 10%
I_{LI}	Input Leakage Current		10	∝A	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	∝A	V_{OUT} = GND to V_{CC}
V_{IL}[2]	Input Low Voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}[2]	Input High Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 3 mA

3838 PGM T02

CAPACITANCE T_A = 25°C, f = 1 MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$[3]	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}[3]	Input Capacitance (A_0, A_1, A_2, SCL, WC)	6	pF	V_{IN} = 0V

3838 PGM T04

Notes: (1) Must perform a stop command prior to measurement.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested. (3) This parameter is periodically sampled and not 100% tested.
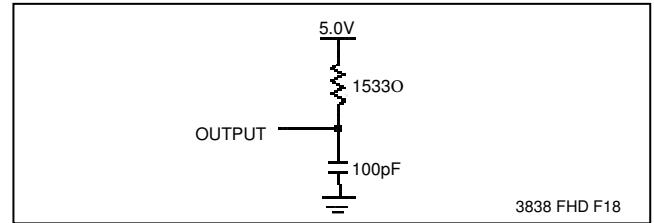
X24C02

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5

3838 PGM T05

EQUIVALENT A.C. LOAD CIRCUIT
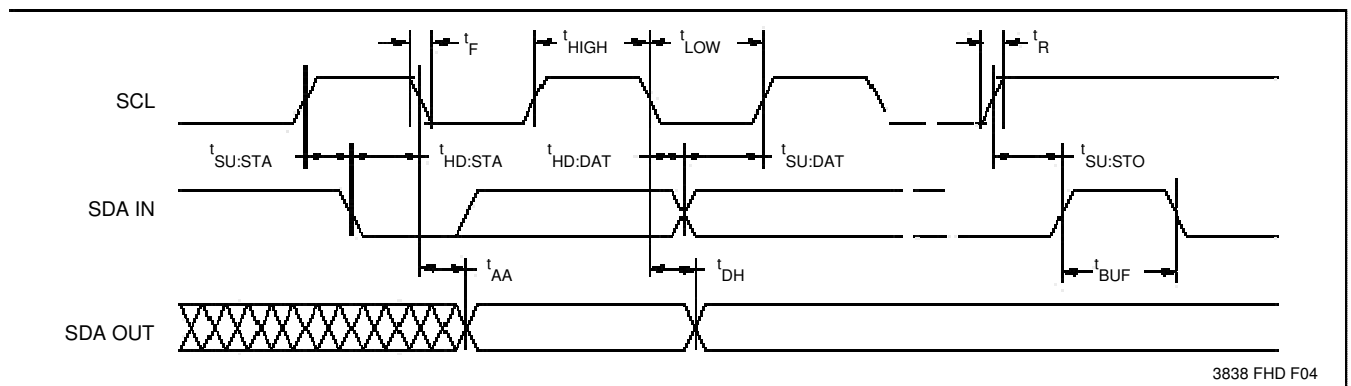

3838 FHD F18

A.C. CHARACTERISTICS (Over recommended operating conditions)
DATA INPUT TIMING

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	$\propto$S
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		$\propto$S
$t_{HD:STA}$	Start Condition Hold Time	4.0		$\propto$S
t_{LOW}	Clock Low Period	4.7		$\propto$S
t_{HIGH}	Clock High Period	4.0		$\propto$S
$t_{SU:STA}$	Start Condition Setup Time	4.7		$\propto$S
$t_{HD:DAT}$	Data In Hold Time	0		$\propto$S
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	$\propto$S
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		$\propto$S
t_{DH}	Data Out Hold Time	300		ns

3838 PGM T06

Bus Timing

3838 FHD F04

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}[4]	Power-up to Read Operation	1	ms
t_{PUW}[4]	Power-up to Write Operation	5	ms

3838 PGM T07

Notes:(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

X24C02

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.[5]	Max.	Units
t_{WR}[6]	Write Cycle Time		5	10	ms

3838 PGM T08

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C02 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.
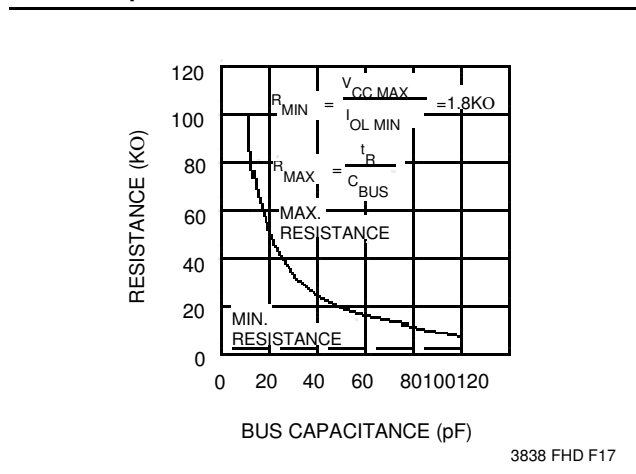
Write Cycle Timing
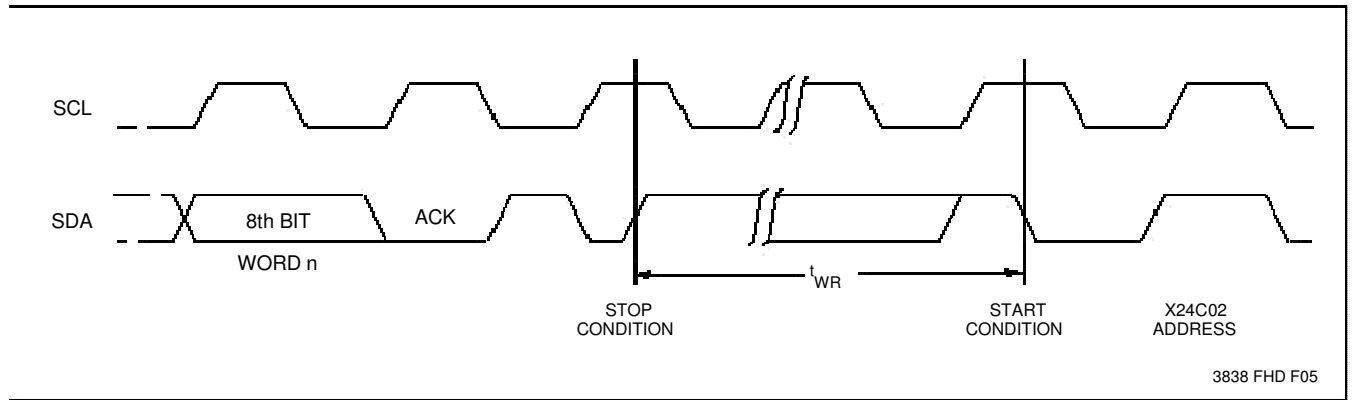
3838 FHD F05

Notes: (5) Typical values are for $T_A = 25$ C and nominal supply voltage (5V)

(6) t_{WR} is the minimum cycle time from the system perspective when polling techniques are not used. It is the maximum time the device requires to perform the internal write operation.

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors
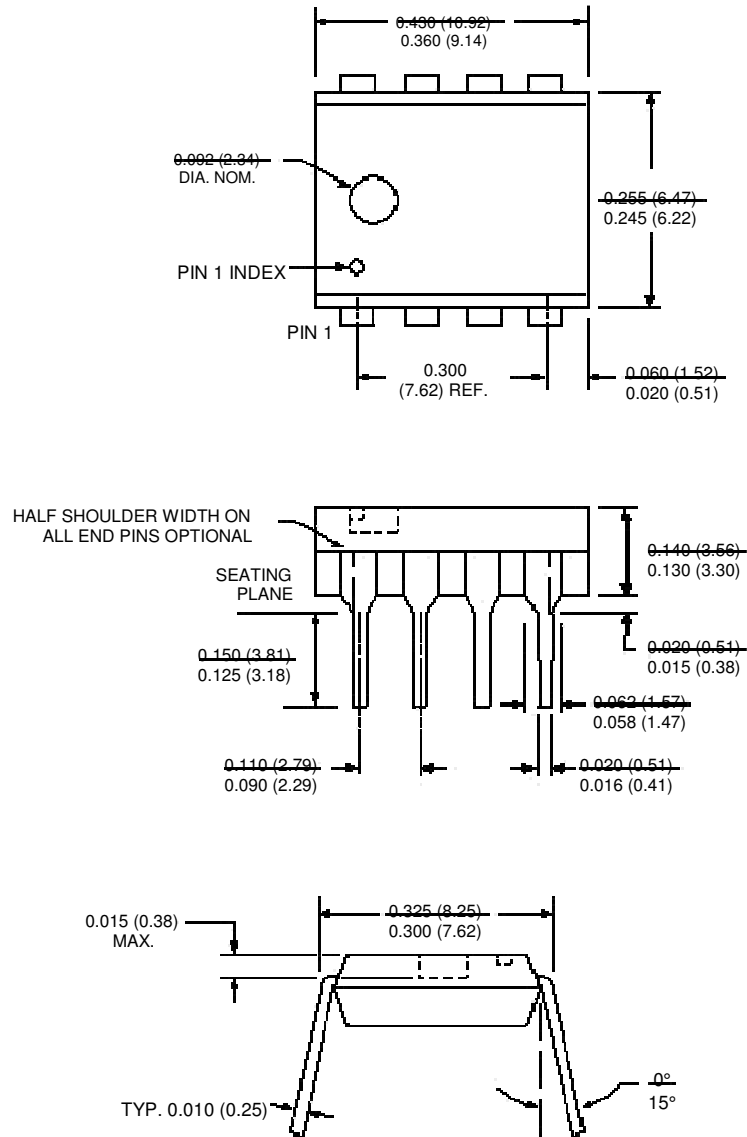

3838 FHD F17

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

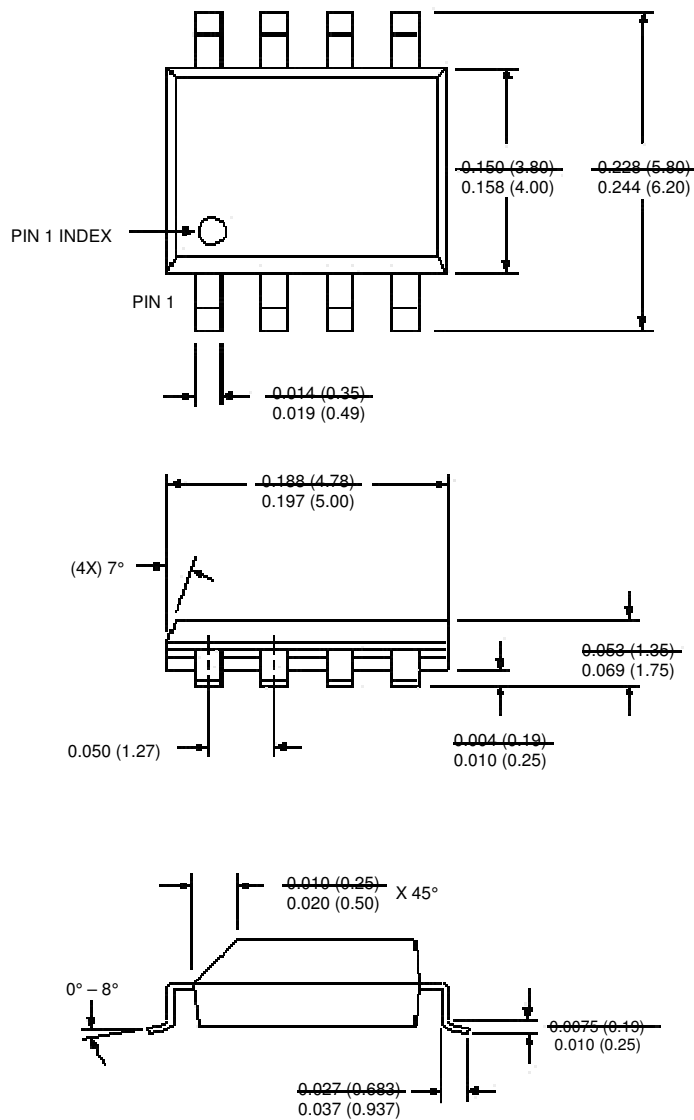0.430 (10.92)
0.360 (9.14)

0.092 (2.34)
DIA. NOM.

0.255 (6.47)
0.245 (6.22)

PIN 1 INDEX

PIN 1

0.300
(7.62) REF.

0.060 (1.52)
0.020 (0.51)

HALF SHOULDER WIDTH ON
ALL END PINS OPTIONAL

SEATING
PLANE

0.140 (3.56)
0.130 (3.30)

0.150 (3.81)
0.125 (3.18)

0.020 (0.51)
0.015 (0.38)

0.062 (1.57)
0.058 (1.47)

0.110 (2.79)
0.090 (2.29)

0.020 (0.51)
0.016 (0.41)

0.015 (0.38)
MAX.

0.325 (8.25)
0.300 (7.62)

0°
15°

TYP. 0.010 (0.25)

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

PIN 1 INDEX

PIN 1

0.150 (3.80)
0.158 (4.00)

0.228 (5.80)
0.244 (6.20)

0.014 (0.35)
0.019 (0.49)

0.188 (4.78)
0.197 (5.00)

(4X) 7°

0.053 (1.35)
0.069 (1.75)

0.050 (1.27)

0.004 (0.19)
0.010 (0.25)

0.010 (0.25)
0.020 (0.50)   X 45°

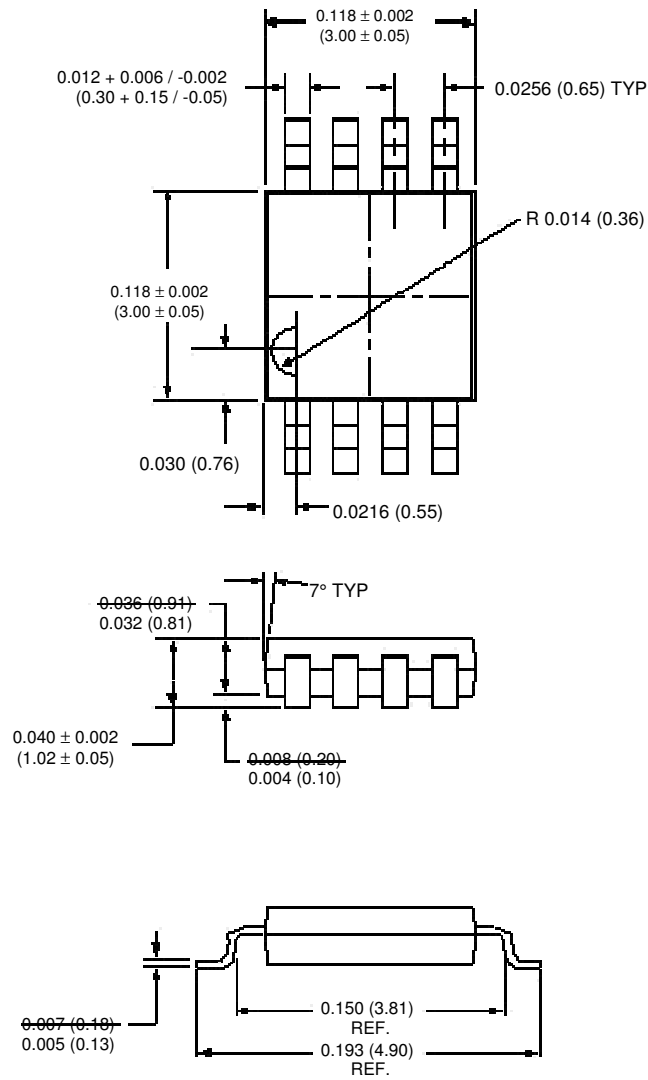0° – 8°

0.0075 (0.19)
0.010 (0.25)

0.027 (0.683)
0.037 (0.937)

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESIS IN MILLIMETERS)

PACKAGING INFORMATION

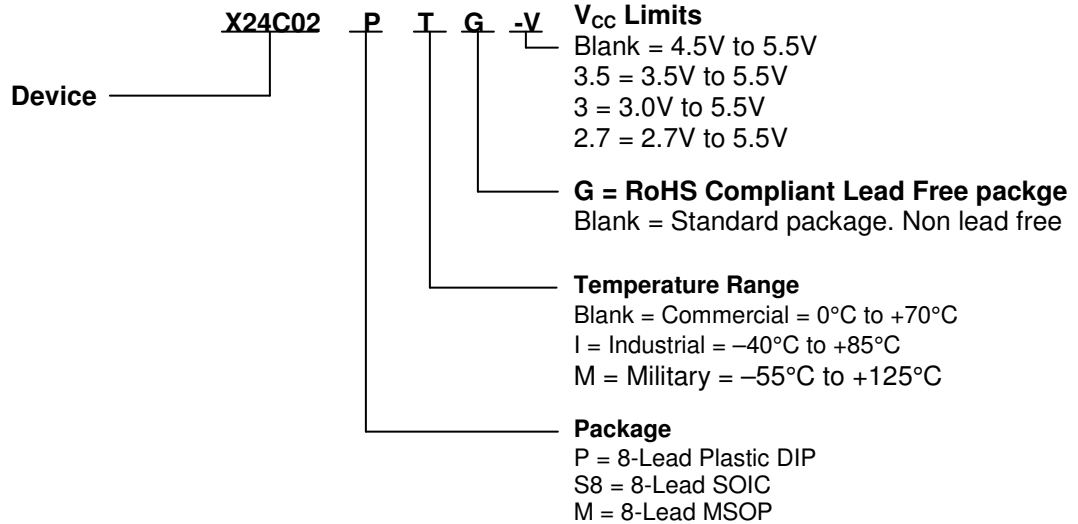### 8-LEAD MINIATURE SMALL OUTLINE GULL WING PACKAGE TYPE M

0.118 ± 0.002
(3.00 ± 0.05)

0.012 + 0.006 / -0.002
(0.30 + 0.15 / -0.05)

0.0256 (0.65) TYP

R 0.014 (0.36)

0.118 ± 0.002
(3.00 ± 0.05)

0.030 (0.76)

0.0216 (0.55)

7° TYP

0.036 (0.91)
0.032 (0.81)

0.040 ± 0.002
(1.02 ± 0.05)

0.008 (0.20)
0.004 (0.10)

0.007 (0.18)
0.005 (0.13)

0.150 (3.81)
REF.

0.193 (4.90)
REF.

NOTE:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS)

3003 ILL 01

NOTES

X24C02

ORDERING INFORMATION

```
X24C02   P   T   G   -V   Vcc Limits
                              Blank = 4.5V to 5.5V
Device ─────────┘            3.5 = 3.5V to 5.5V
                             3 = 3.0V to 5.5V
                             2.7 = 2.7V to 5.5V

                          G = RoHS Compliant Lead Free packge
                          Blank = Standard package. Non lead free

                          Temperature Range
                          Blank = Commercial = 0°C to +70°C
                          I = Industrial = −40°C to +85°C
                          M = Military = −55°C to +125°C

                          Package
                          P = 8-Lead Plastic DIP
                          S8 = 8-Lead SOIC
                          M = 8-Lead MSOP
```

Part Mark Convention

```
X24C02   X G ── Blank = 8-Lead SOIC
                P = 8-Lead Plastic DIP
                S8 = 8-Lead SOIC
                M = 8-Lead MSOP
            X   G= RoHS compliant lead free

                Blank = 4.5V to 5.5V, 0°C to +70°C
                I = 4.5V to 5.5V, −40°C to +85°C
                M = 4.5V to 5.5V, −55°C to 125°C
                B = 3.5V to 5.5V, 0°C to +70°C
                C = 3.5V to 5.5V, −40°C to +85°C
                D = 3.0V to 5.5V, 0°C to +70°C
                E = 3.0V to 5.5V, −40°C to +85°C
                F = 2.7V to 5.5V, 0°C to +70°C
                G = 2.7V to 5.5V, −40°C to +85°C
```