ISO 7816 Compatible

64K X76F641 8Kx8+32x8

Secure SerialFlash

FEATURES

- **64-bit Password Security**
  - **—Five 64-bit Passwords for Read, Program and Reset**
- **8192 Byte+32 Byte Password Protected Arrays**
  - **—Seperate Read Passwords**
  - **—Seperate Write Passwords**
  - **—Reset Password**
- **Programmable Passwords**
- **Retry Counter Register**
  - **—Allows 8 tries before clearing of both arrays**
  - **—Password Protected Reset**
- **32-bit Response to Reset (RST Input)**
- **32 byte Sector Program**
- **400kHz Clock Rate**
- **2 wire Serial Interface**
- **Low Power CMOS**
  - **—2.0 to 5.5V operation**
  - **—Standby current Less than 1µA**
  - **—Active current less than 3 mA**
- **High Reliability Endurance:**
  - **—100,000 Write Cycles**
- **Data Retention: 100 years**
- **Available in:**
  - **—8 lead EIAJ SOIC**
  - **—SmartCard Module**

DESCRIPTION

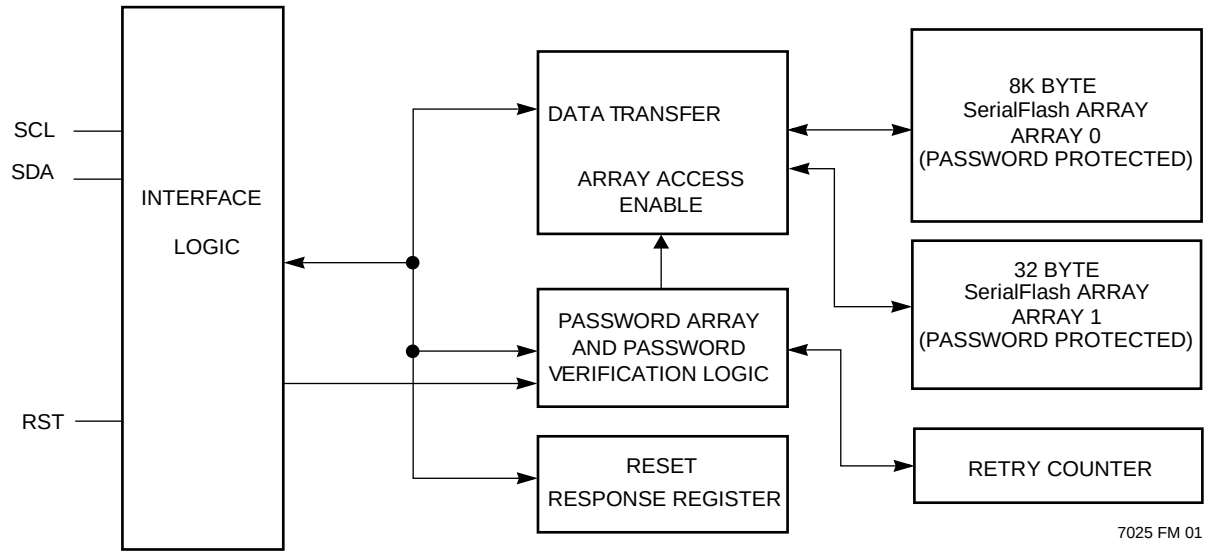
The X76F641 is a Password Access Security Supervisor, containing one 65536-bit Secure SerialFlash array and one 256-bit Secure SerialFlash array. Access to each memory array is controlled by five 64-bit passwords each. These passwords protect read and write operations of the memory array. A separate RESET password is used to reset the passwords and clear the memory arrays in the event the read and write passwords are lost.

The X76F641 features a serial interface and software protocol allowing operation on a popular two wire bus. The bus signals are a clock Input (SCL) and a bidirectional data input and output (SDA).

The X76F641 also features a synchronous response to reset providing an automatic output of a hard-wired 32-bit data stream conforming to the industry standard for memory cards.

The X76F641 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

Functional Diagram



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a true three state serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin. In all other cases, this pin is in a high impedance state.

Reset (RST)

RST is a device reset pin. When RST is pulsed high the X76F641 will output 32 bits of fixed data which conforms to the standard for “synchronous response to reset”. The part must not be in a write cycle for the response to reset to occur. See Figure 11. If there is power interrupted during the Response to Reset, the response to reset will be aborted and the part will return to the standby state. The response to reset is "mask programmable" only!

DEVICE OPERATION

There are two primary modes of operation for the X76F641; Protected READ and protected WRITE. Protected operations must be performed with one of four 8-byte passwords.

The basic method of communication for the device is generating a start condition, then transmitting a command, followed by the correct password. All parts will be shipped from the factory with all passwords equal to ‘0’. The user must perform ACK Polling to determine the validity of the password, before starting a data transfer (see Acknowledge Polling.) Only after the correct password is accepted and a ACK polling has been performed, can the data transfer occur.

To ensure the correct communication, RST must remain LOW under all conditions except when running a “Response to Reset sequence”.

Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

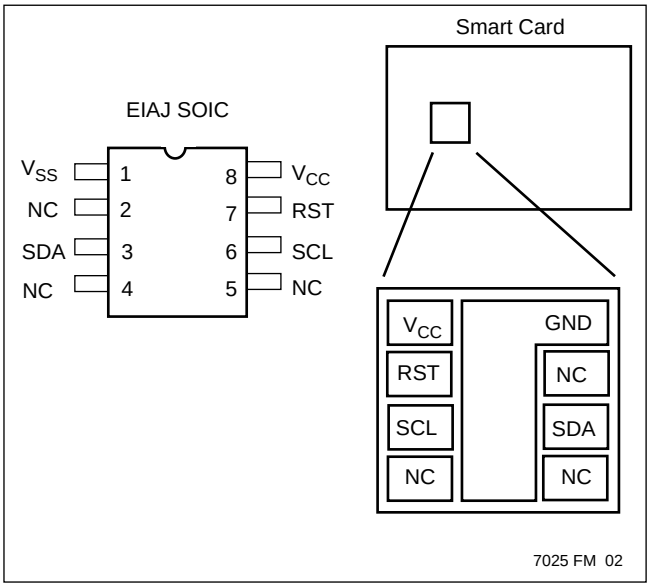
If the X76F641 is in a nonvolatile write cycle a “no ACK” (SDA=High) response will be issued in response to loading of the command byte. If a stop is issued prior to the nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

The basic sequence is illustrated in Figure 1.

PIN NAMES

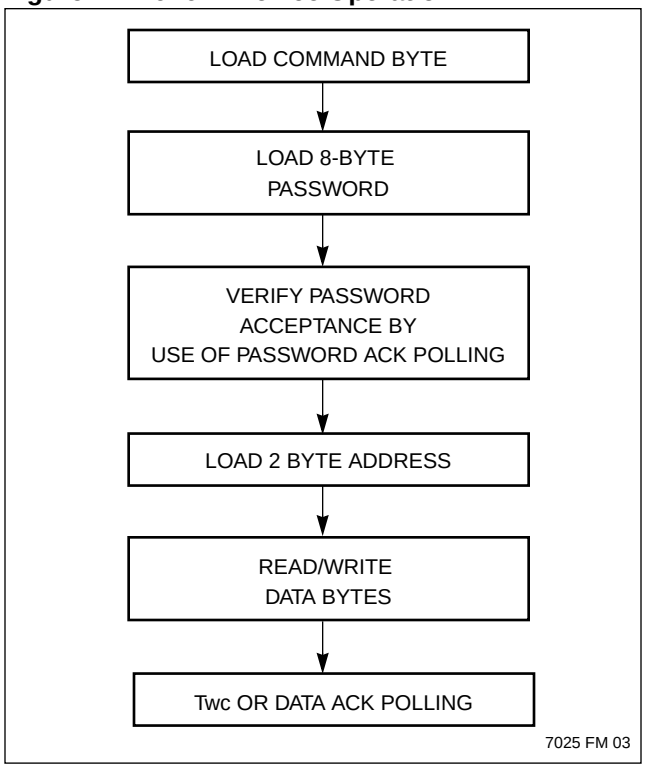
Symbol	Description
SDA	Serial Data Input/Output
SCL	Serial Clock Input
RST	Reset Input
Vcc	Supply Voltage
Vss	Ground
NC	No Connect

PIN CONFIGURATION



After each transaction is completed, the X76F641 will reset and enter into a standby mode. This will also be the response if an unsuccessful attempt is made to access a protected array.

Figure 1. X76F641 Device Operation



Retry Counter

The X76F641 contains a retry counter. The retry counter allows 8 accesses with an invalid password before any action is taken. The counter will increment with any combination of incorrect passwords. If the retry counter overflows, all memory areas are cleared and the device is locked by preventing any read or write array password matches. The passwords are unaffected. If a correct password is received prior to retry counter overflow, the retry counter is reset and access is granted. In order to reset the operation of a locked up device, a special reset command must be used with a RESET password.

Device Protocol

The X76F641 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as a receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X76F641 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figure 2 and Figure 3.

Start Condition

All commands are preceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X76F641 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

A start may be issued to terminate the input of a control byte or the input data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are inhibited while a write is in progress.

Stop Condition

All communications must be terminated by a stop condition. The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to reset the device during a command or data input sequence and will leave the device in the standby power mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

The X76F641 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write condition have been selected, the X76F641 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

Reset Device Command

The reset device command is used to clear the retry counter and reactivate the device. When the reset device command is used prior to the retry counter overflow, the retry counter is reset and no arrays or passwords are affected. If the retry counter has overflowed, all memory areas are cleared and all commands are blocked and the retry counter is disabled. Issuing a valid reset device command (with reset password) to the device resets and re-enables the retry counter and re-enables the other commands. Again, the passwords are not affected.

Reset Password Command

A reset password command will clear both arrays and set all passwords to all zero.

Figure 2. Data Validity

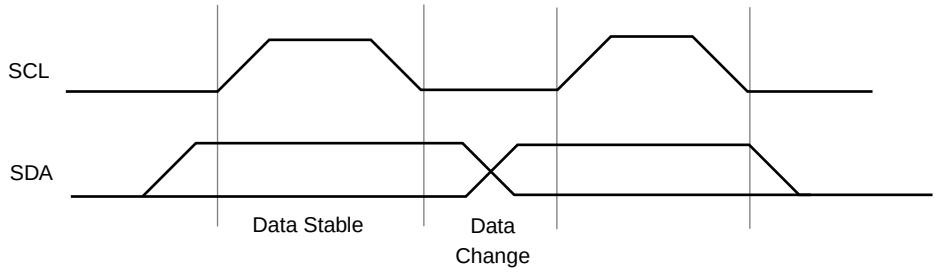


Figure 3. Definition of Start and Stop Conditions

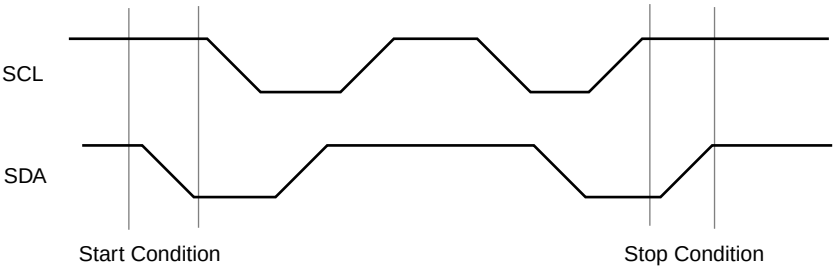


Table 1. X76F641 Instruction Set

1st Byte after Start	1st Byte after Password	2nd Byte after Password	Command Description	Password used
1000 0000	High Address	Low address	Read (Array 0)	Read 0
1000 1000	High Address	Low address	Read (Array 1)	Read 1
1001 0000	High Address	Low address	Sector Write (Array 0)	Write 0
1001 1000	High Address	Low address	Sector Write (Array 1)	Write 1
1010 0000	0000 0000	0000 0000	Change Read 0 Password	Read 0
1010 1000	0000 0000	0000 0000	Change Read 1 Password	Read 1
1011 0000	0000 0000	0000 0000	Change Write 0 Password	Write 0
1011 1000	0000 0000	0000 0000	Change Write 1 Password	Write 1
1100 0000	0000 0000	0000 0000	Change Reset Password	Reset
1110 0000	not used	not used	Reset Password Command	Reset
1110 1000	not used	not used	Reset Device Command	Reset
1111 0000	not used	not used	ACK Polling command (Ends Password operation)	None
All the rest			Reserved	

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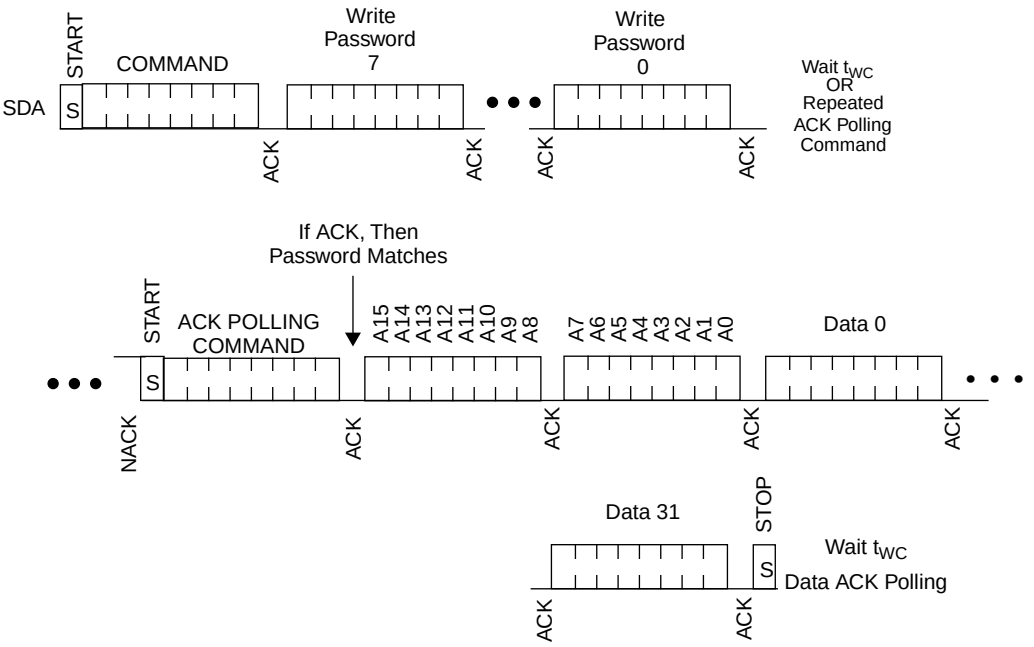
Notes: Illegal command codes will be disregarded. The part will respond with a “no-ACK” to the illegal byte and then return to the standby mode. All write/read operations require a password.

PROGRAM OPERATIONS

Sector Programming

The sector program mode requires issuing the 8-bit write command followed by the password, password Ack command, the address and then the data bytes transferred as illustrated in figure 4. Up to 32 bytes may be transferred. After the last byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle.

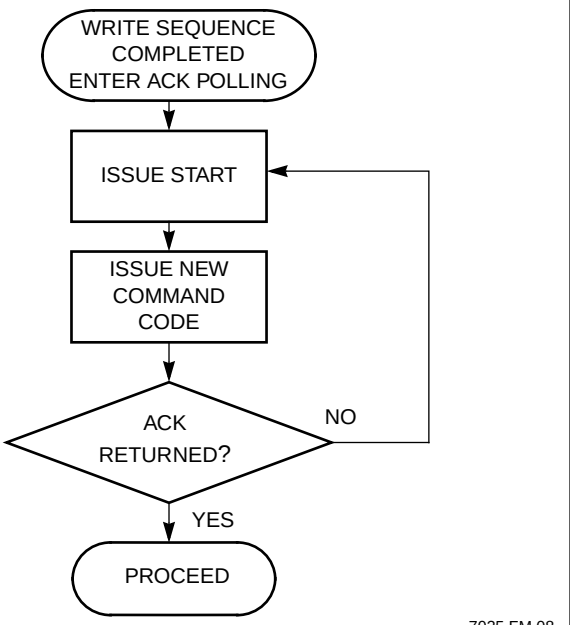
Figure 4. Sector Programming



ACK Polling

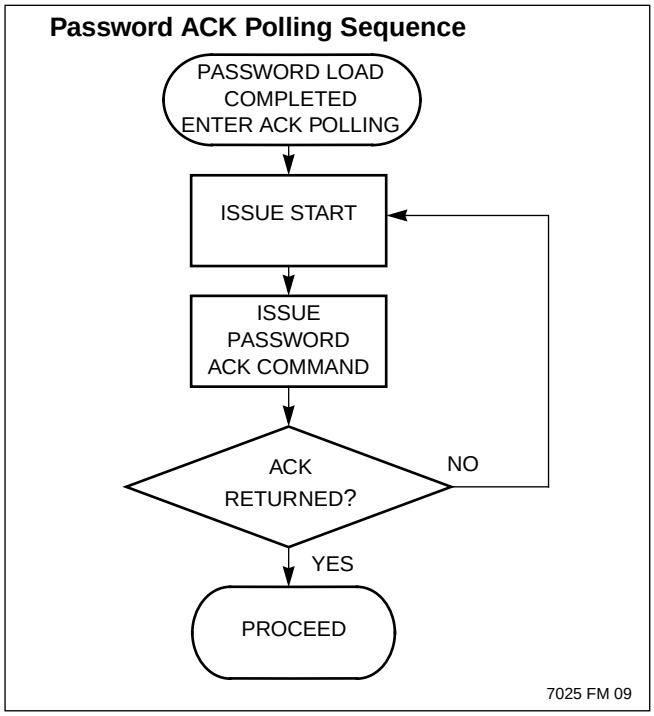
Once a stop condition is issued to indicate the end of the host's write sequence, the X76F641 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can begin immediately. This involves issuing the start condition followed by the new command code of 8 bits (1st byte of the protocol.) If the X76F641 is still busy with the nonvolatile write operation, it will issue a "no-ACK" in response. If the nonvolatile write operation has completed, an "ACK" will be returned and the host can then proceed with the rest of the protocol.

Data ACK Polling Sequence



After the password sequence, there is always a nonvolatile write cycle. This is done to discourage random guesses of the password if the device is being tampered with. In order to continue the transaction, the X76F641 requires the master to perform an ACK polling with the specific code of F0h. As with regular Acknowledge polling the user can either time out for 10ms, and then issue the ACK polling once, or continuously loop as described in the flow.

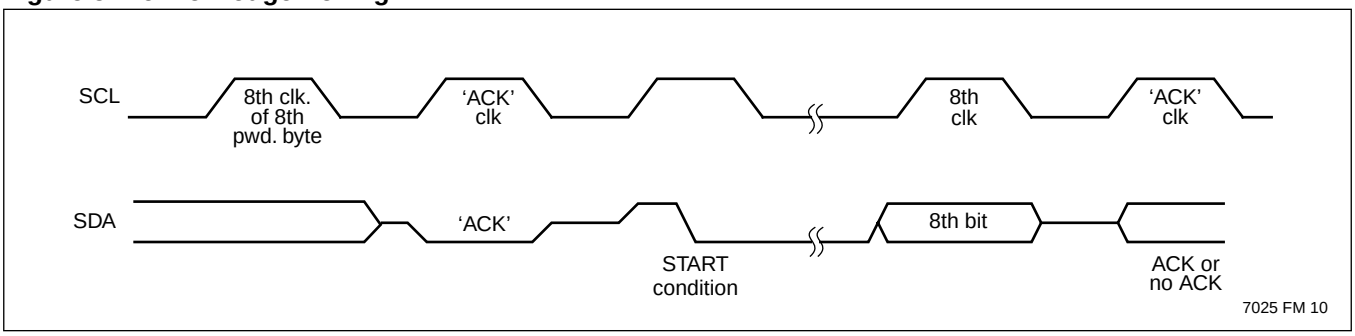
Password ACK Polling Sequence



If the password that was inserted was correct, then an "ACK" will be returned once the nonvolatile cycle is over, in response to the ACK polling cycle immediately following it.

If the password that was inserted was incorrect, then a "no ACK" will be returned even if the nonvolatile cycle is over. Therefore, the user cannot be certain that the password is incorrect until the 10ms write cycle time has elapsed.

Figure 5. Acknowledge Polling



READ OPERATIONS

Read operations are initiated in the same manner as write operations but with a different command code.

Random Read

The master issues the start condition and a Read instruction and password, performs a Password Ack Polling, then issues the word address. Once the password has been acknowledged and first byte has been read, another start can be issued followed by a new 8-bit address. Random reads are allowed, but only the low order 8 bits can change. This limits random reads to a 256 byte block. Therefore, with a single password cycle only a 256 byte block of array 0 may be accessed randomly. To randomly access another block of array 0, a stop must be issued followed by a new command/address/password sequence. A random read of the array 1 can access all locations without another password command sequence.

Sequential Read

The host can read sequentially within an array after the password acceptance sequence. The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory array contents to be serially read during one operation. At the end of the address space (address 1FFFh for array 0, 1Fh for array 1), the counter "rolls over" to address 0 and the X76F641 continues to output data for each acknowledge received. Refer to figure 7 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, a stop condition is generated without a preceding acknowledge.

Figure 6. Random Read

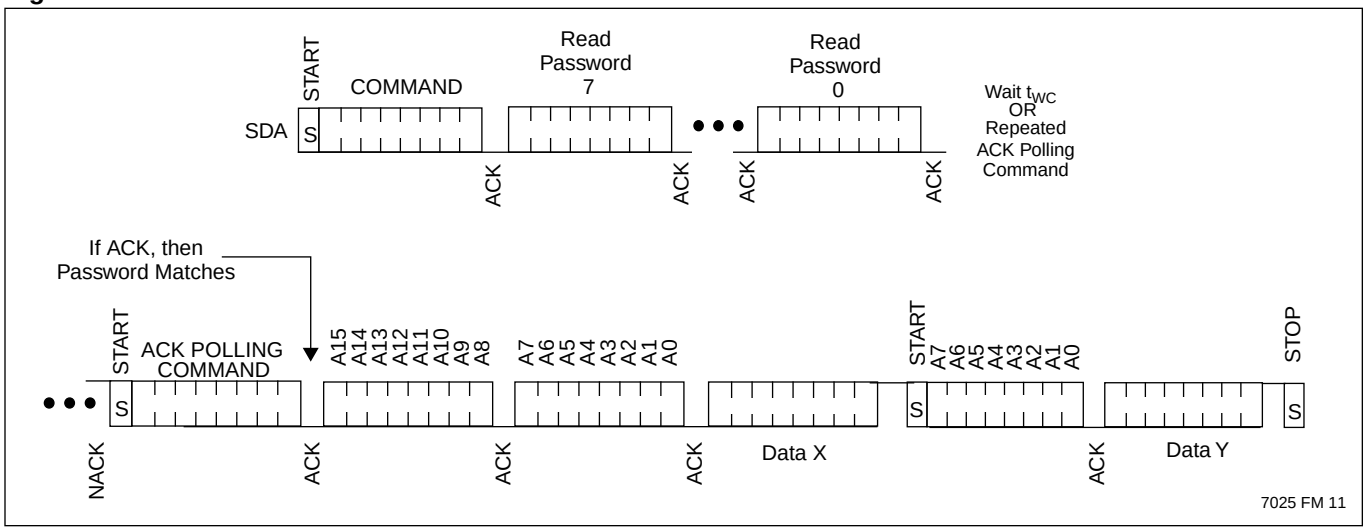
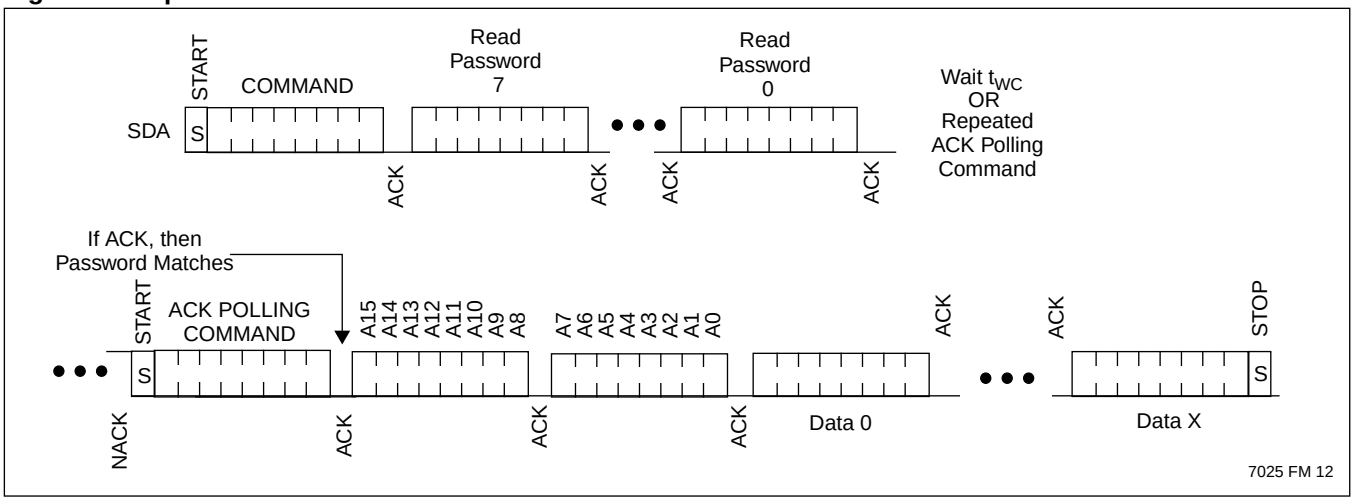


Figure 7. Sequential Read



PASSWORDS

The sequence in Figure 8 shows how to change (program) the passwords. The programming of passwords is done twice prior to the nonvolatile write cycle in order to verify that the new password is consistent. After the eight bytes are entered in the second pass, a comparison takes place. A mismatch will cause the part to reset and enter into the standby mode.

Data ACK polling can be used to determine if a password has been loaded correctly, however the data ACK command must be issued less than 2ms after the stop bit. After this time, it cannot be determined if the password has been loaded correctly, without trying the new password. To determine if the new password has been loaded correctly the data ACK polling command is issued immediately following the stop bit. If it returns an ACK, then the two passes of the new password entry do not match. If it returns a "no ACK" then the passwords match and a high voltage cycle is in progress. The high voltage cycle is complete when a subsequent data ACK command returns an "ACK".

There is no way to read any of the passwords.

Figure 8. Change Passwords

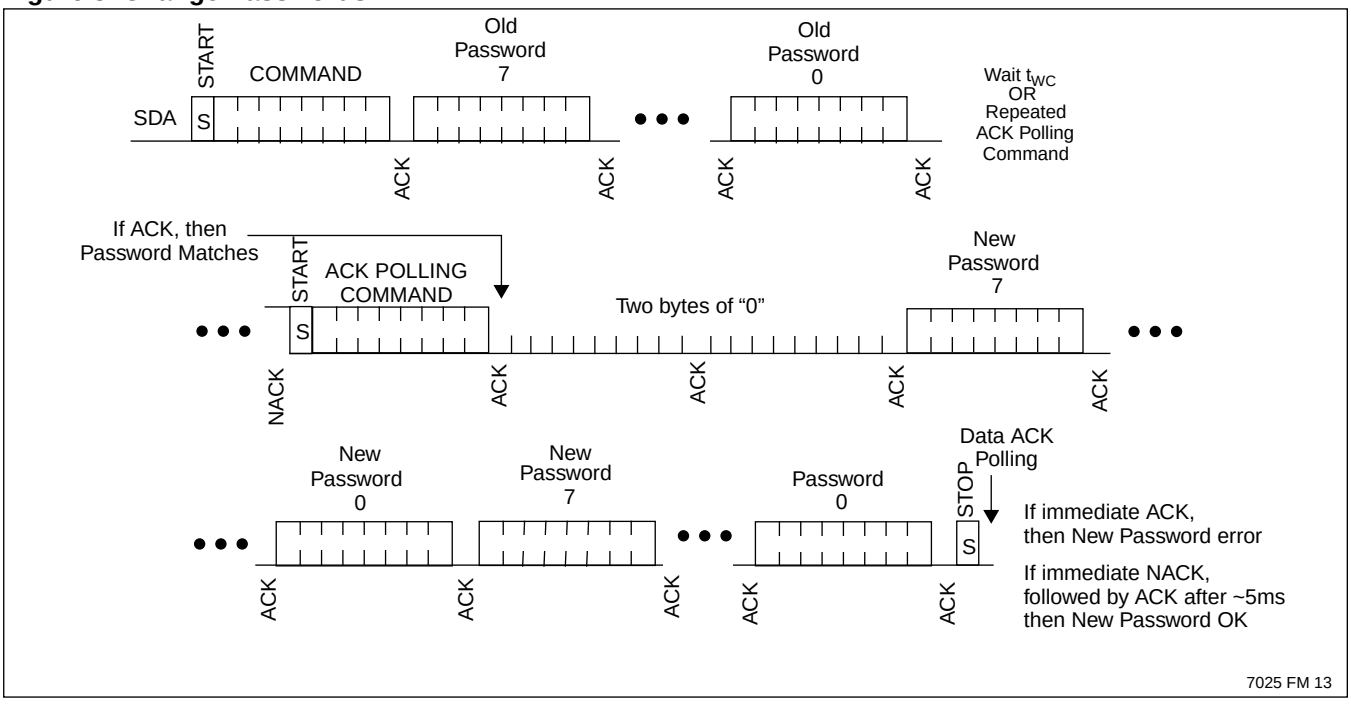


Figure 9. Reset Password

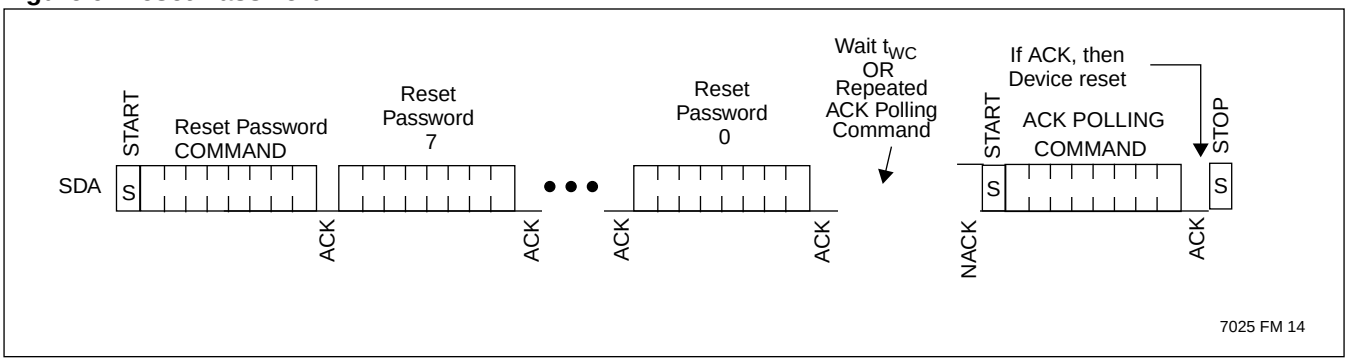
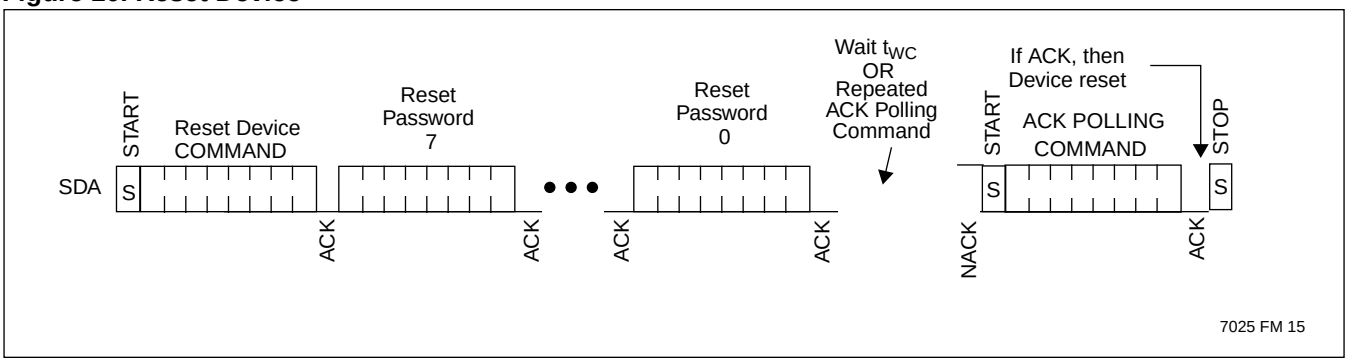


Figure 10. Reset Device



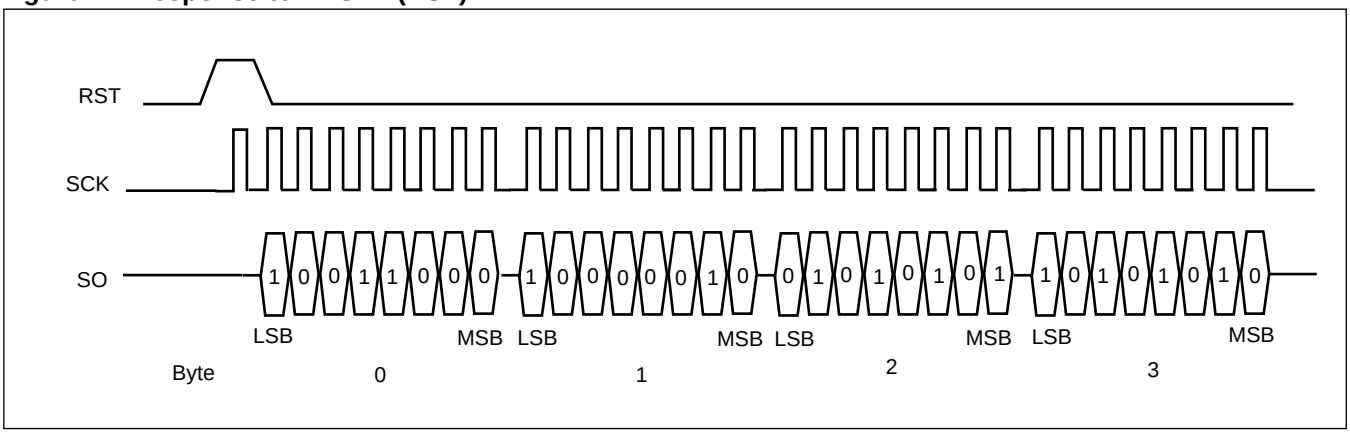
RESPONSE TO RESET (DEFAULT = 19 41 AA 55)

The ISO Response to reset is controlled by the RST and CLK pins. When RST is pulsed high during a clock pulse, the device will output 32 bits of data, one bit per clock, and it resets to the standby state. This conforms to the ISO standard for “synchronous response to reset”. The part must not be in a write cycle for the response to reset to occur.

After initiating a nonvolatile write cycle the RST pin must not be pulsed until the nonvolatile write cycle is complete. If not, the ISO response will not be activated. If the RST is pulsed HIGH and the CLK is within the RST pulse (meet the t_{NOL} spec.) in the middle of an ISO transaction, it will output the 32 bit sequence again (starting at bit 0). Otherwise, this aborts the ISO operation and the part returns to standby state. If the RST is pulsed HIGH and the CLK is outside the RST pulse (in the middle of an ISO transaction), this aborts the ISO operation and the part returns to standby state.

If there is power interrupted during the Response to Reset, the response to reset will be aborted and the part will return to the standby state. A Response to Reset is not available during a nonvolatile write cycle.

Figure 11. Response to RESET (RST)



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS}.....–1V to +7V
D.C. Output Current.....5mA
Lead Temperature
(Soldering, 10 seconds)..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C

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Supply Voltage	Limits
X76F641	4.5V to 5.5V
X76F641 – 2.0	2.0V to 3.6V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$f_{SCL} = V_{CC}$ x 0.1/V_{CC} x 0.9 Levels @ 400 KHz, SDA = Open RST = V_{SS}
I_{CC2}(3)	V_{CC} Supply Current (Write)		3	mA	$f_{SCL} = V_{CC}$ x 0.1/V_{CC} x 0.9 Levels @ 400 KHz, SDA = Open RST = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		50	µA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9 f_{SCL} = 400 KHz, f_{SDA} = 400 KHz
I_{SB2}(1)	V_{CC} Supply Current (Standby)		1	µA	$V_{SDA} = V_{SCC} = V_{CC}$ Other = GND or V_{CC}–0.3V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IL1}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	V_{CC} = 5.5V
V_{IH1}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	V_{CC} = 5.5V
V_{IL2}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.1	V	V_{CC} = 2.0V
V_{IH2}(2)	Input HIGH Voltage	V_{CC} x 0.9	V_{CC} + 0.5	V	V_{CC} = 2.0V
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

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CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (RST, SCL)	6	pF	V_{IN} = 0V

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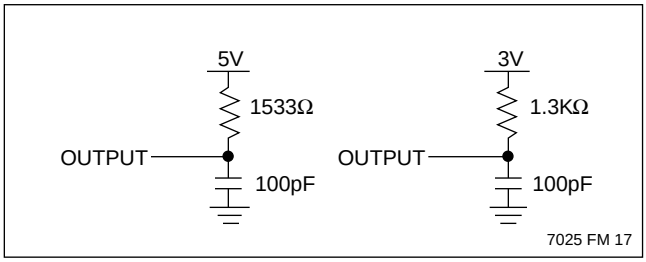
NOTES: (1) Must perform a stop command after a read command prior to measurement

(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5
Output Load	100pF

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AC CHARACTERISTICS

AC Specifications (Over the recommended operating conditions)

Symbol	Parameter	Min	Typ(1)	Max	Units
f_{SCL}	SCL Clock Frequency	0		400	KHz
t_{IN}(1)	Pulse width of spikes which must be suppressed by the input filter	50	100		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.3	0.9	µs
t_{BUF}	Time the bus must be free before a new transmit can start	1.3			µs
t_{LOW}	Clock LOW Time	1.3			µs
t_{HIGH}	Clock HIGH Time	0.6			µs
$t_{SU:STA}$	Start Condition Setup Time	0.6			µs
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs
$t_{SU:DAT}$	Data In Setup Time	100			ns
$t_{HD:DAT}$	Data In Hold Time	0			µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs
t_{DH}	Data Output Hold Time	50	300		ns
t_R	SDA and SCL Rise Time	20 + 0.1 x C_b(2)		300	ns
t_F	SDA and SCL Fall Time	20 + 0.1 x C_b(2)		300	ns
f_{SCL_RST}	SCL Clock Frequency during Response to Reset			400	kHz
t_{SR}	Device Select to RST active	200			ns
t_{NOL}	RST to SCL Non-Overlap	500			ns
t_{RST}	RST High Time	2.25			µs
$t_{SU:RST}$	Response to Reset Setup Time	1.25			µs
t_{LOW_RST}	Clock LOW during Response to Reset	1.25			µs
t_{HIGH_RST}	Clock HIGH during Response to Reset	1.25			µs
t_{RDV}	RST LOW to SDA Valid During Response to Reset	0		500	ns
t_{CDV}	CLK LOW to SDA Valid During Response to Reset	0		500	ns
t_{DHZ}	Device Deselect to SDA high impedance	0		500	ns

Notes: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V

Notes: 2. C_b = Total Capacitance of one bus line in pf.

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RESET AC SPECIFICATIONS

Power Up Timing

Symbol	Parameter	Min.	Typ(2)	Max.	Units
t_{PUR}(1)	Time from Power Up to Read			1	mS
t_{PUW}(1)	Time from Power Up to Write			5	mS

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Notes: 1. Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.
2. Typical values are for T_A = 25˚C and V_{CC} = 5.0V

Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(1)	Write Cycle Time		5	10	mS

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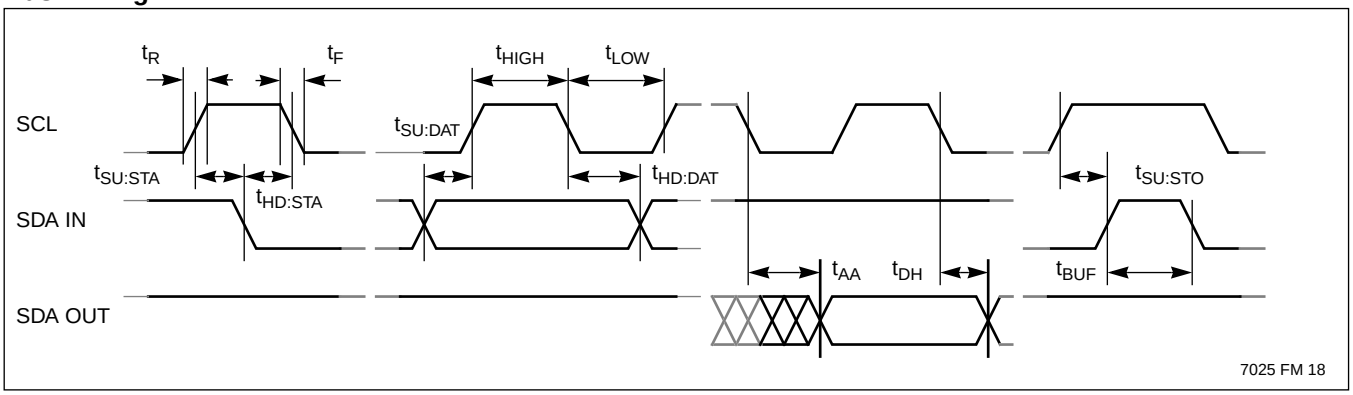
Notes: 1. t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

TIMING DIAGRAMS

Bus Timing



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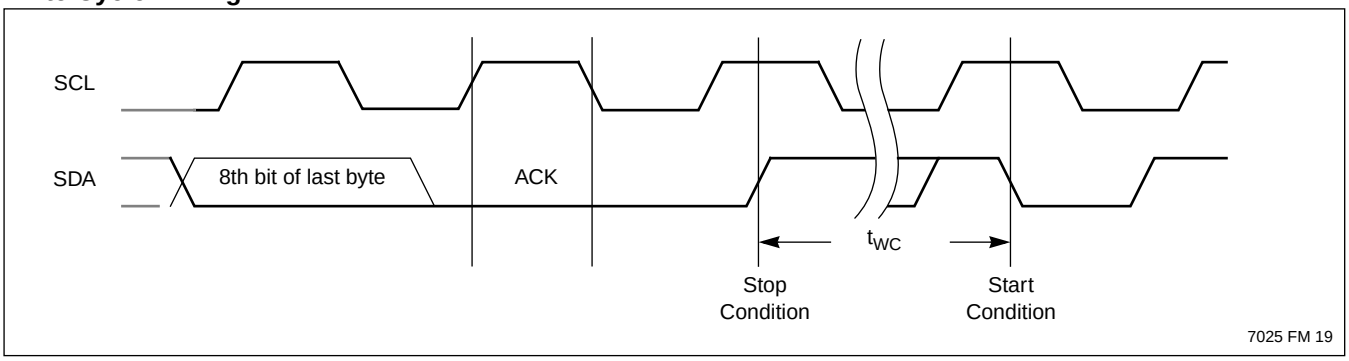
Write Cycle Timing



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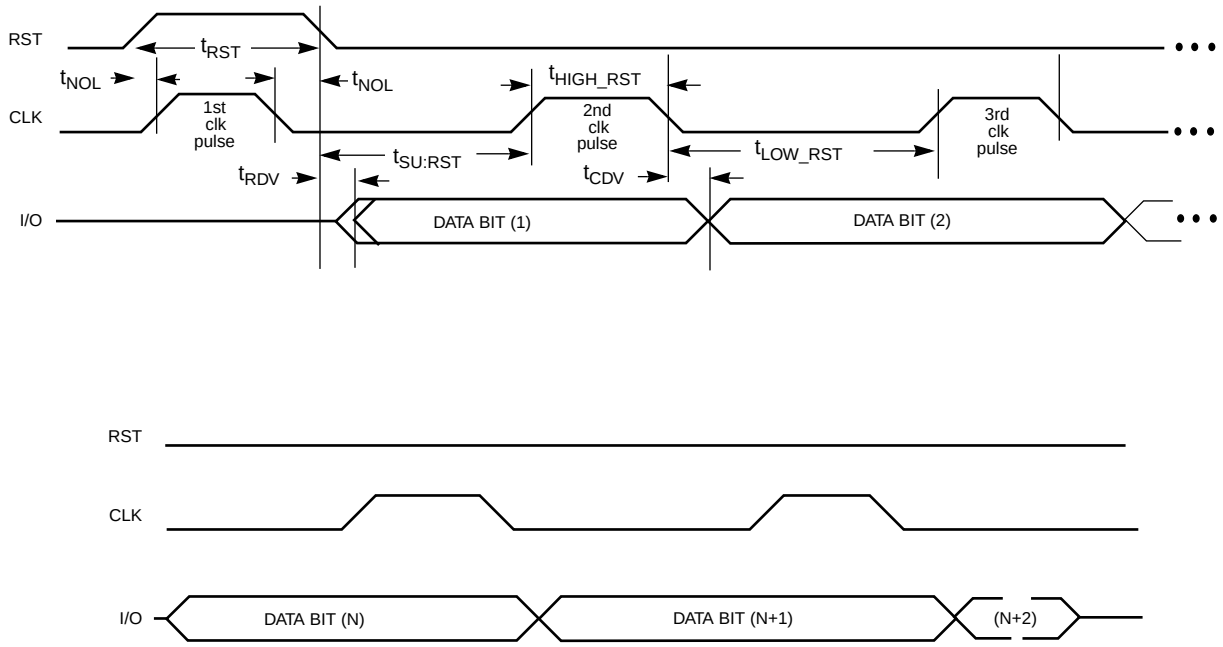
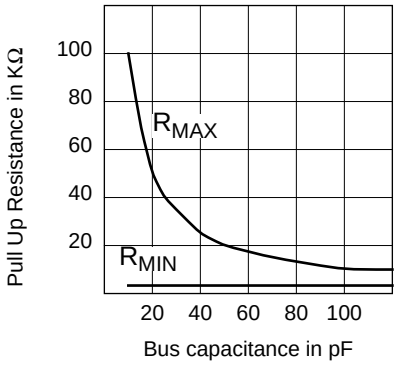
RST Timing Diagram – Response to a Synchronous Reset



7025 FM 21

GUIDELINES FOR CALCULATING TYPICAL VALUES OF BUS PULL UP RESISTORS



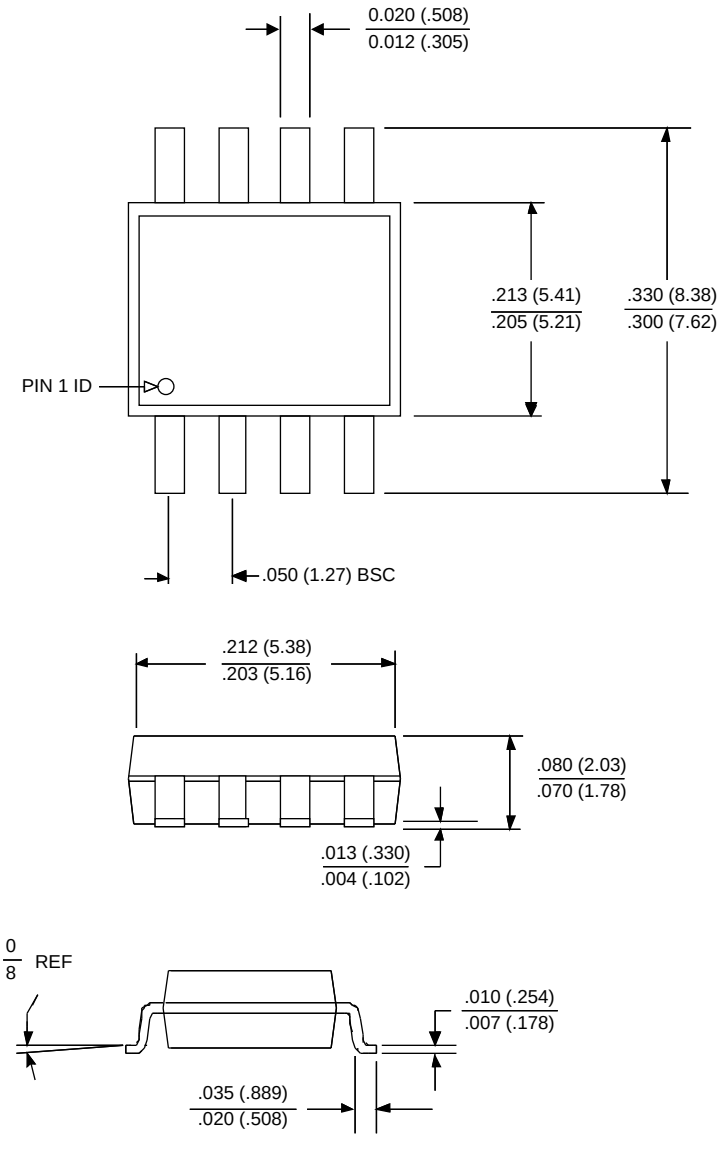
$$R_{MIN} = \frac{V_{CCMAX}}{I_{OLMIN}} = 1.8K\Omega$$

$$R_{MAX} = \frac{t_R}{C_{BUS}}$$

t_R = maximum allowable SDA rise time

7025 FM 22

8-LEAD PLASTIC, 0.200” WIDE SMALL OUTLINE GULLWING PACKAGE TYP “A” (EIAJ SOIC)



NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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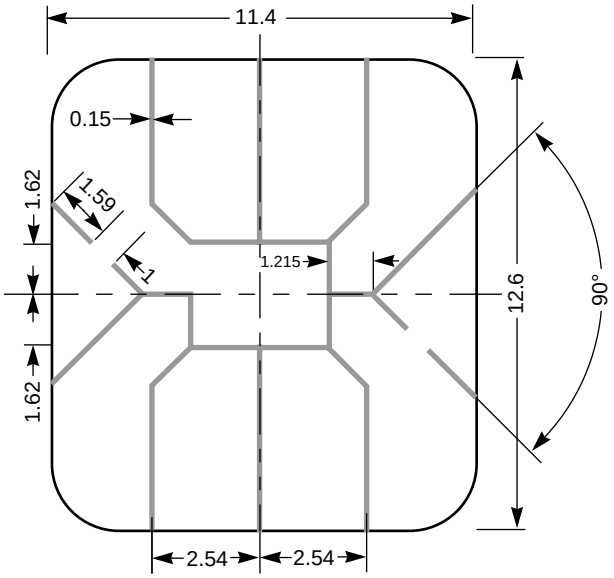
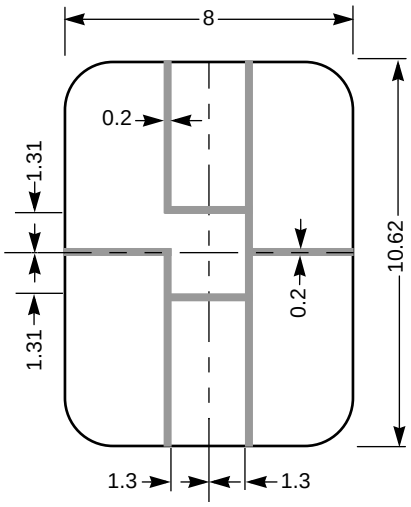
8 PAD CHIP ON BOARD SMART CARD MODULE TYPE X

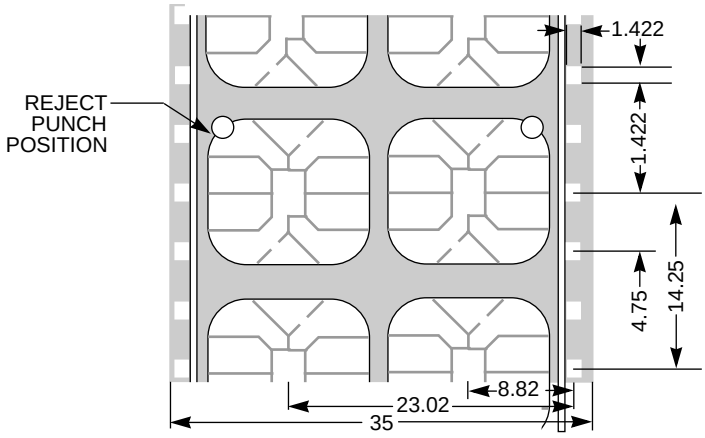
8 CONTACT MODULE



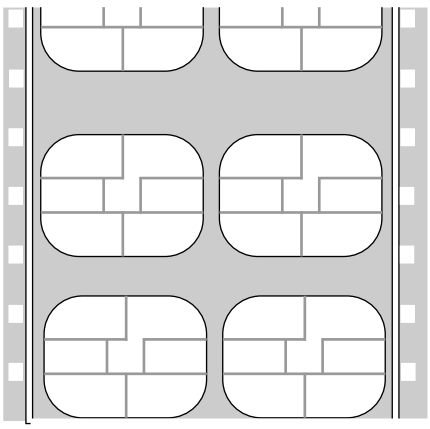
6 CONTACT MODULE



35mm TAPE



35mm TAPE



NOTE: ALL MEASUREMENTS IN MILLIMETERS

ORDERING INFORMATION