Data Sheet, V0.1, June 2007

XC236x

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance

Microcontrollers

Never stop thinking

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None

Page	Subjects (major changes since last revision)

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Preliminary

16/32-Bit Single-Chip Microcontroller with 32-Bit Performance **XC236x**
XC2000 Family

1 Summary of Features

For a quick overview or reference, the XC236x's properties are listed here in a condensed way.

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 15 ns Instruction Cycle Time at 66 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle 32-bit Addition and Subtraction with 40-bit result
  - 1-Cycle Multiplication (16 × 16 bit)
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Background Division (32 / 16 bit) in 21 Cycles
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with up to 79 Sources, Selectable External Inputs for Interrupt Generation and Wake-Up, Sample-Rate down to 15 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation from Internal or External Clock Sources, via on-chip PLL or via Prescaler
- On-Chip Memory Modules
  - 1 Kbyte On-Chip Stand-By RAM (SBRAM)
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 16 Kbytes On-Chip Data SRAM (DSRAM)
  - Up to 32 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - Up to 576 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - Two Synchronizable A/D Converters with a total of 16 Channels, 10-bit Resolution, Conversion Time down to 1.2 μs, Optional Data Preprocessing (Data Reduction, Range Check)
  - 16-Channel General Purpose Capture/Compare Unit (CAPCOM2)
  - Two Capture/Compare Units for flexible PWM Signal Generation (CCU6x)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Six Serial Interface Channels to be used as UART, LIN, High-Speed Synchronous Channel (SPI/QSPI), IIC Bus Interface (10-bit addressing, 400 kbit/s), IIS Interface

  - On-Chip MultiCAN Interface (Rev. 2.0B active) with 64 Message Objects (Full CAN/Basic CAN) on 3 CAN Nodes and Gateway Functionality
  - On-Chip Real Time Clock
- Up to 12 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses
  - Selectable Address Bus Width
  - 16-Bit or 8-Bit Data Bus Width
  - Four Programmable Chip-Select Signals
- Single Power Supply from 3.0 V to 5.5 V
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 75 General Purpose I/O Lines
- On-Chip Bootstrap Loader
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Debug Support via JTAG Interface
- 100-Pin Green LQFP Package, 0.5 mm (19.7 mil) pitch

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the XC236x please refer to your responsible sales representative or your local distributor.

This document describes several derivatives of the XC236x group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **XC236x** throughout this document.

Table 1 XC236x Derivative Synopsis

Derivative[1]	Temp. Range	Program Memory	PSRAM[2]	CCU6 Mod.	ADC[3] Chan.	Interfaces
SAK-XC2365-72F66L	-40 °C to 125 °C	576 Kbytes Flash	32 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.
SAF-XC2365-72F66L	-40 °C to 85 °C	576 Kbytes Flash	32 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.
SAK-XC2365-56F66L	-40 °C to 125 °C	448 Kbytes Flash	16 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.
SAF-XC2365-56F66L	-40 °C to 85 °C	448 Kbytes Flash	16 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.
SAK-XC2365-48F66L	-40 °C to 125 °C	384 Kbytes Flash	8 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.
SAF-XC2365-48F66L	-40 °C to 85 °C	384 Kbytes Flash	8 Kbytes	0, 1	11 + 5	3 CAN Nodes, 6 Serial Chan.

1) This Data Sheet is valid for devices starting with and including design step AA.

2) All derivatives additionally provide 1 Kbyte SBRAM, 2 Kbytes DPRAM, and 16 Kbytes DSRAM.

3) Analog input channels are listed for each Analog/Digital Converter module separately.

2 General Device Information

The XC236x derivatives are high-performance members of the Infineon XC2000 Family of full featured single-chip CMOS microcontrollers. These devices extend the functionality and performance of the C166 Family in terms of instructions (MAC unit), peripherals, and speed. They combine high CPU performance (up to 66 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. Optimized peripherals can be adapted to the application's requirements in a flexible way. These derivatives also provide clock generation via PLL and internal or external clock sources, and various on-chip memory modules such as program Flash, program RAM, and data RAM.

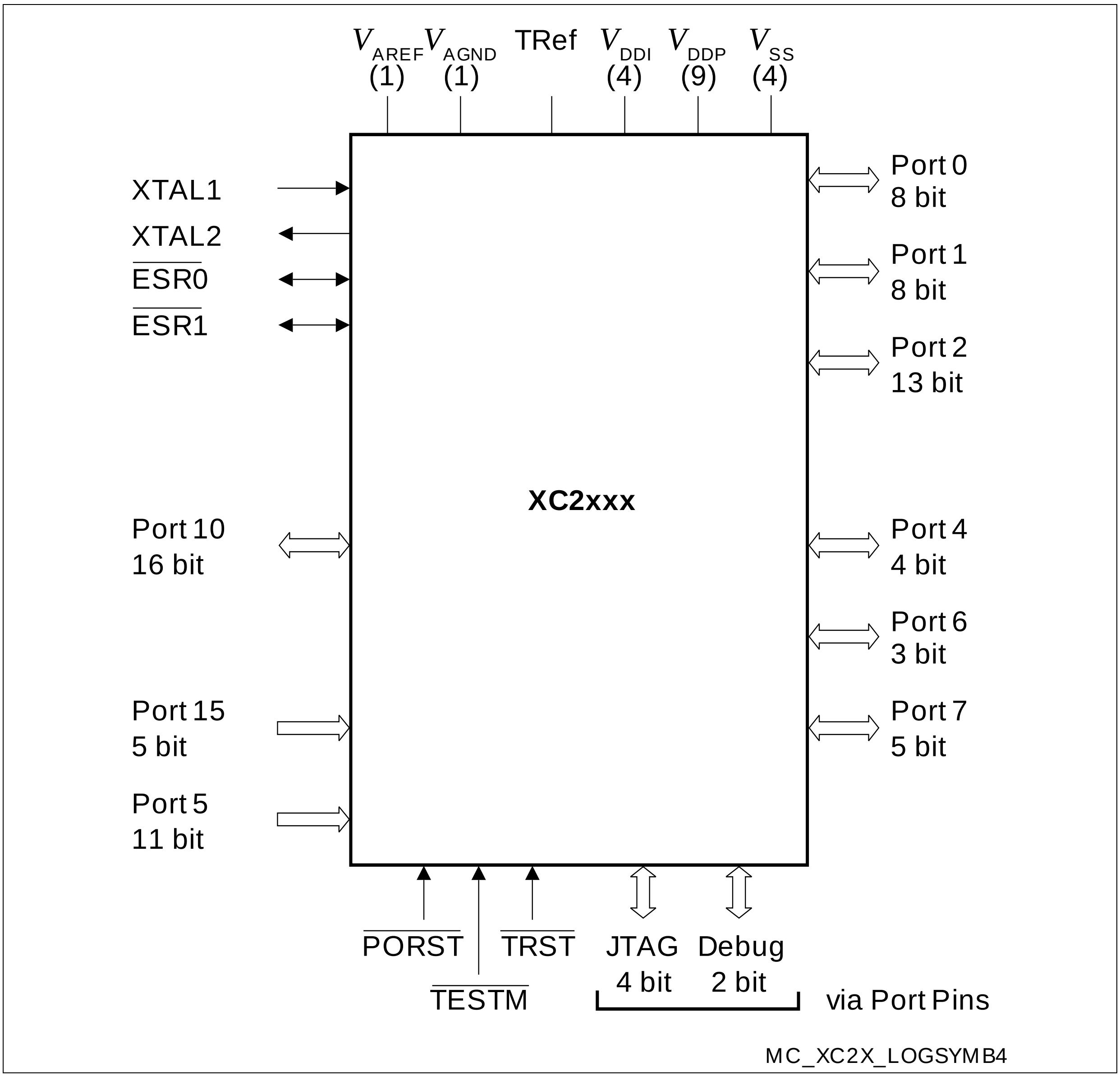

Figure 1 Logic Symbol

2.1 Pin Configuration and Definition

The pins of the XC236x are described in detail in **Table 2**, including all their alternate functions. For explanations, please refer to the footnotes at the table's end. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package.

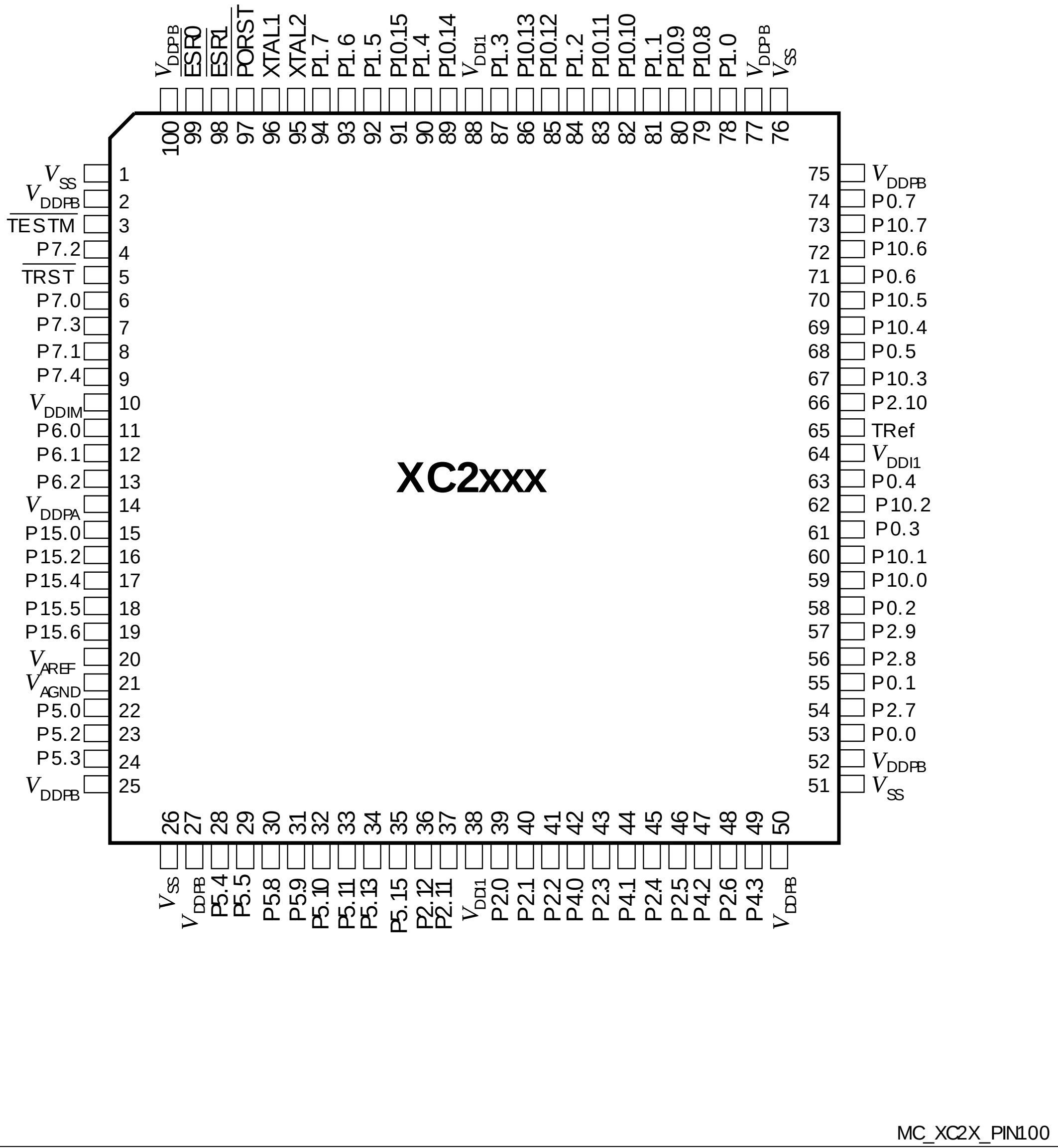

Figure 2 Pin Configuration (top view)

Notes to Pin Definitions

1. ***Ctrl.**: The output signal for a port pin is selected via bitfield PC in the associated register Px_IOCRy. Output O0 is selected by setting the respective bitfield PC to $1x00_B$, output O1 is selected by $1x01_B$, etc.*
   Output signal OH is controlled by hardware.
2. ***Type**: Indicates the employed pad type (St=standard pad, Sp=special pad, DP=double pad, In=input pad, PS=power supply) and its power supply domain (A, B, M, 1).*

Table 2 Pin Definitions and Functions

Pin	Symbol	Ctrl.	Type	Function
3	$\overline{\text{TESTM}}$	I	In/B	**Testmode Enable** Enables factory test modes, must be held HIGH for normal operation (connect to V_{DDPB}).
4	P7.2	O0 / I	St/B	**Bit 2 of Port 7, General Purpose Input/Output**
	EMUX0	O1	St/B	**External Analog MUX Control Output 0**
	TDI_C	I	St/B	**JTAG Test Data Input**
5	$\overline{\text{TRST}}$	I	In/B	**Test-System Reset Input** For normal system operation, pin $\overline{\text{TRST}}$ should be held low. A high level at this pin at the rising edge of $\overline{\text{PORST}}$ activates the XC236x's debug system. In this case, pin $\overline{\text{TRST}}$ must be driven low once to reset the debug system.
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT1 Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT2 Timer T6 Toggle Latch Output**
	TDO	OH	St/B	**JTAG Test Data Output**
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	TMS_C	I	St/B	**JTAG Test Mode Selection Input**
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**
9	P7.4	O0 / I	St/B	**Bit 4 of Port 7, General Purpose Input/Output**
	EMUX2	O1	St/B	**External Analog MUX Control Output 2**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C1_SCLK	O3	St/B	**USIC0 Channel 1 Shift Clock Output**
	TCK_C	I	St/B	**JTAG Clock Input**
	U0C0_DX0D	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX1E	I	St/B	**USIC0 Channel 1 Shift Clock Input**
11	P6.0	O0 / I	St/A	**Bit 0 of Port 6, General Purpose Input/Output**
	EMUX0	O1	St/A	**External Analog MUX Control Output 0**
	U1C1_DOUT	O2	St/A	**USIC1 Channel 1 Shift Data Output**
	$\overline{\text{BRKOUT}}$	O3	St/A	**OCDS Break Signal Output**
	ADCx_ REQGTyC	I	St/A	**External Request Gate Input for ADC0/1**
	U1C1_DX0E	I	St/A	**USIC1 Channel 1 Shift Data Input**
12	P6.1	O0 / I	St/A	**Bit 1 of Port 6, General Purpose Input/Output**
	EMUX1	O1	St/A	**External Analog MUX Control Output 1**
	T3OUT	O2	St/A	**GPT1 Timer T3 Toggle Latch Output**
	U1C1_DOUT	O3	St/A	**USIC1 Channel 1 Shift Data Output**
	ADCx_ REQTRyC	I	St/A	**External Request Trigger Input for ADC0/1**
13	P6.2	O0 / I	St/A	**Bit 2 of Port 6, General Purpose Input/Output**
	EMUX2	O1	St/A	**External Analog MUX Control Output 2**
	T6OUT	O2	St/A	**GPT2 Timer T6 Toggle Latch Output**
	U1C1_SCLK	O3	St/A	**USIC1 Channel 1 Shift Clock Output**
	U1C1_DX1C	I	St/A	**USIC1 Channel 1 Shift Clock Input**
15	P15.0	I	In/A	**Bit 0 of Port 15, General Purpose Input**
	ADC1_CH0	I	In/A	**Analog Input Channel 0 for ADC1**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
16	P15.2	I	In/A	**Bit 2 of Port 15, General Purpose Input**
	ADC1_CH2	I	In/A	**Analog Input Channel 2 for ADC1**
	T5IN	I	In/A	**GPT2 Timer T5 Count/Gate Input**
17	P15.4	I	In/A	**Bit 4 of Port 15, General Purpose Input**
	ADC1_CH4	I	In/A	**Analog Input Channel 4 for ADC1**
	T6IN	I	In/A	**GPT2 Timer T6 Count/Gate Input**
18	P15.5	I	In/A	**Bit 5 of Port 15, General Purpose Input**
	ADC1_CH5	I	In/A	**Analog Input Channel 5 for ADC1**
	T6EUD	I	In/A	**GPT2 Timer T6 External Up/Down Control Input**
19	P15.6	I	In/A	**Bit 6 of Port 15, General Purpose Input**
	ADC1_CH6	I	In/A	**Analog Input Channel 6 for ADC1**
20	V_{AREF}	-	PS/A	**Reference Voltage for A/D Converters ADC0/1**
21	V_{AGND}	-	PS/A	**Reference Ground for A/D Converters ADC0/1**
22	P5.0	I	In/A	**Bit 0 of Port 5, General Purpose Input**
	ADC0_CH0	I	In/A	**Analog Input Channel 0 for ADC0**
23	P5.2	I	In/A	**Bit 2 of Port 5, General Purpose Input**
	ADC0_CH2	I	In/A	**Analog Input Channel 2 for ADC0**
	TDI_A	I	In/A	**JTAG Test Data Input**
24	P5.3	I	In/A	**Bit 3 of Port 5, General Purpose Input**
	ADC0_CH3	I	In/A	**Analog Input Channel 3 for ADC0**
	T3IN	I	In/A	**GPT1 Timer T3 Count/Gate Input**
28	P5.4	I	In/A	**Bit 4 of Port 5, General Purpose Input**
	ADC0_CH4	I	In/A	**Analog Input Channel 4 for ADC0**
	T3EUD	I	In/A	**GPT1 Timer T3 External Up/Down Control Input**
	TMS_A	I	In/A	**JTAG Test Mode Selection Input**
29	P5.5	I	In/A	**Bit 5 of Port 5, General Purpose Input**
	ADC0_CH5	I	In/A	**Analog Input Channel 5 for ADC0**
	CCU60_ T12HRB	I	In/A	**External Run Control Input for T12 of CCU60**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
30	P5.8	I	In/A	**Bit 8 of Port 5, General Purpose Input**
	ADC0_CH8	I	In/A	**Analog Input Channel 8 for ADC0**
	CCU6x_T12HRC	I	In/A	**External Run Control Input for T12 of CCU60/1**
	CCU6x_T13HRC	I	In/A	**External Run Control Input for T13 of CCU60/1**
31	P5.9	I	In/A	**Bit 9 of Port 5, General Purpose Input**
	ADC0_CH9	I	In/A	**Analog Input Channel 9 for ADC0**
	CC2_T7IN	I	In/A	**CAPCOM2 Timer T7 Count Input**
32	P5.10	I	In/A	**Bit 10 of Port 5, General Purpose Input**
	ADC0_CH10	I	In/A	**Analog Input Channel 10 for ADC0**
	$\overline{\text{BRKIN\_A}}$	I	In/A	**OCDS Break Signal Input**
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
	EX0BINB	I	In/A	**External Interrupt Trigger Input**
35	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
36	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	READY	I	St/B	**External Bus Interface READY Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
37	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_ SELO2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_ SELO2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$).
39	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	AD13	OH / I	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
40	P2.1	O0 / I	St/B	**Bit 1 of Port 2, General Purpose Input/Output**
	TxDC0	O1	St/B	**CAN Node 0 Transmit Data Output**
	AD14	OH / I	St/B	**External Bus Interface Address/Data Line 14**
	ESR1_5	I	St/B	**ESR1 Trigger Input 5**
	EX0AINA	I	St/B	**External Interrupt Trigger Input**
41	P2.2	O0 / I	St/B	**Bit 2 of Port 2, General Purpose Input/Output**
	TxDC1	O1	St/B	**CAN Node 1 Transmit Data Output**
	AD15	OH / I	St/B	**External Bus Interface Address/Data Line 15**
	ESR2_5	I	St/B	**ESR2 Trigger Input 5**
	EX1AINA	I	St/B	**External Interrupt Trigger Input**
42	P4.0	O0 / I	St/B	**Bit 0 of Port 4, General Purpose Input/Output**
	CC2_24	O3 / I	St/B	**CAPCOM2 CC24IO Capture Inp./ Compare Out.**
	$\overline{\text{CS0}}$	OH	St/B	**External Bus Interface Chip Select 0 Output**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
43	P2.3	O0 / I	St/B	**Bit 3 of Port 2, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CC2_16	O3 / I	St/B	**CAPCOM2 CC16IO Capture Inp./ Compare Out.**
	A16	OH	St/B	**External Bus Interface Address Line 16**
	ESR2_0	I	St/B	**ESR2 Trigger Input 0**
	U0C0_DX0E	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0D	I	St/B	**USIC0 Channel 1 Shift Data Input** *Note: Not available in step AA.*
	RxDC0A	I	St/B	**CAN Node 0 Receive Data Input**
44	P4.1	O0 / I	St/B	**Bit 1 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_25	O3 / I	St/B	**CAPCOM2 CC25IO Capture Inp./ Compare Out.**
	$\overline{\text{CS1}}$	OH	St/B	**External Bus Interface Chip Select 1 Output**
45	P2.4	O0 / I	St/B	**Bit 4 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output** *Note: Not available in step AA.*
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_17	O3 / I	St/B	**CAPCOM2 CC17IO Capture Inp./ Compare Out.**
	A17	OH	St/B	**External Bus Interface Address Line 17**
	ESR1_0	I	St/B	**ESR1 Trigger Input 0**
	U0C0_DX0F	I	St/B	**USIC0 Channel 0 Shift Data Input**
	RxDC1A	I	St/B	**CAN Node 1 Receive Data Input**
46	P2.5	O0 / I	St/B	**Bit 5 of Port 2, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CC2_18	O3 / I	St/B	**CAPCOM2 CC18IO Capture Inp./ Compare Out.**
	A18	OH	St/B	**External Bus Interface Address Line 18**
	U0C0_DX1D	I	St/B	**USIC0 Channel 0 Shift Clock Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
47	P4.2	O0 / I	St/B	**Bit 2 of Port 4, General Purpose Input/Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	CC2_26	O3 / I	St/B	**CAPCOM2 CC26IO Capture Inp./ Compare Out.**
	$\overline{\text{CS2}}$	OH	St/B	**External Bus Interface Chip Select 2 Output**
	T2IN	I	St/B	**GPT1 Timer T2 Count/Gate Input**
48	P2.6	O0 / I	St/B	**Bit 6 of Port 2, General Purpose Input/Output**
	U0C0_ SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	U0C1_ SELO1	O2	St/B	**USIC0 Channel 1 Select/Control 1 Output**
	CC2_19	O3 / I	St/B	**CAPCOM2 CC19IO Capture Inp./ Compare Out.**
	A19	OH	St/B	**External Bus Interface Address Line 19**
	U0C0_DX2D	I	St/B	**USIC0 Channel 0 Shift Control Input**
	RxDC0D	I	St/B	**CAN Node 0 Receive Data Input**
49	P4.3	O0 / I	St/B	**Bit 3 of Port 4, General Purpose Input/Output**
	CC2_27	O3 / I	St/B	**CAPCOM2 CC27IO Capture Inp./ Compare Out.**
	$\overline{\text{CS3}}$	OH	St/B	**External Bus Interface Chip Select 3 Output**
	RxDC2A	I	St/B	**CAN Node 2 Receive Data Input**
	T2EUD	I	St/B	**GPT1 Timer T2 External Up/Down Control Input**
53	P0.0	O0 / I	St/B	**Bit 0 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	CCU61_ CC60	O3 / I	St/B	**CCU61 Channel 0 Input/Output**
	A0	OH	St/B	**External Bus Interface Address Line 0**
	U1C0_DX0A	I	St/B	**USIC1 Channel 0 Shift Data Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
54	P2.7	O0 / I	St/B	**Bit 7 of Port 2, General Purpose Input/Output**
	U0C1_ SELO0	O1	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	U0C0_ SELO1	O2	St/B	**USIC0 Channel 0 Select/Control 1 Output**
	CC2_20	O3 / I	St/B	**CAPCOM2 CC20IO Capture Inp./ Compare Out.**
	A20	OH	St/B	**External Bus Interface Address Line 20**
	U0C1_DX2C	I	St/B	**USIC0 Channel 1 Shift Control Input**
	RxDC1C	I	St/B	**CAN Node 1 Receive Data Input**
55	P0.1	O0 / I	St/B	**Bit 1 of Port 0, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC61	O3 / I	St/B	**CCU61 Channel 1 Input/Output**
	A1	OH	St/B	**External Bus Interface Address Line 1**
	U1C0_DX0B	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1A	I	St/B	**USIC1 Channel 0 Shift Clock Input**
56	P2.8	O0 / I	DP/B	**Bit 8 of Port 2, General Purpose Input/Output**
	U0C1_ SCLKOUT	O1	DP/B	**USIC0 Channel 1 Shift Clock Output**
	EXTCLK	O2	DP/B	**Programmable Clock Signal Output** [1]
	CC2_21	O3 / I	DP/B	**CAPCOM2 CC21IO Capture Inp./ Compare Out.**
	A21	OH	DP/B	**External Bus Interface Address Line 21**
	U0C1_DX1D	I	DP/B	**USIC0 Channel 1 Shift Clock Input**
57	P2.9	O0 / I	St/B	**Bit 9 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CC2_22	O3 / I	St/B	**CAPCOM2 CC22IO Capture Inp./ Compare Out.**
	A22	OH	St/B	**External Bus Interface Address Line 22**
	DIRIN	I	St/B	**Clock Signal Input**
	TCK_A	I	St/B	**JTAG Clock Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
58	P0.2	O0 / I	St/B	**Bit 2 of Port 0, General Purpose Input/Output**
	U1C0_ SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	TxDC0	O2	St/B	**CAN Node 0 Transmit Data Output**
	CCU61_ CC62	O3 / I	St/B	**CCU61 Channel 2 Input/Output**
	A2	OH	St/B	**External Bus Interface Address Line 2**
	U1C0_DX1B	I	St/B	**USIC1 Channel 0 Shift Clock Input**
59	P10.0	O0 / I	St/B	**Bit 0 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ CC60	O2 / I	St/B	**CCU60 Channel 0 Input/Output**
	AD0	OH / I	St/B	**External Bus Interface Address/Data Line 0**
	U0C0_DX0A	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C1_DX0A	I	St/B	**USIC0 Channel 1 Shift Data Input**
60	P10.1	O0 / I	St/B	**Bit 1 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	CCU60_ CC61	O2 / I	St/B	**CCU60 Channel 1 Input/Output**
	AD1	OH / I	St/B	**External Bus Interface Address/Data Line 1**
	U0C0_DX0B	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U0C0_DX1A	I	St/B	**USIC0 Channel 0 Shift Clock Input**
61	P0.3	O0 / I	St/B	**Bit 3 of Port 0, General Purpose Input/Output**
	U1C0_ SELO0	O1	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	U1C1_ SELO1	O2	St/B	**USIC1 Channel 1 Select/Control 1 Output**
	CCU61_ COUT60	O3	St/B	**CCU61 Channel 0 Output**
	A3	OH	St/B	**External Bus Interface Address Line 3**
	U1C0_DX2A	I	St/B	**USIC1 Channel 0 Shift Control Input**
	RxDC0B	I	St/B	**CAN Node 0 Receive Data Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
62	P10.2	O0 / I	St/B	**Bit 2 of Port 10, General Purpose Input/Output**
	U0C0_SCLKOUT	O1	St/B	**USIC0 Channel 0 Shift Clock Output**
	CCU60_CC62	O2 / I	St/B	**CCU60 Channel 2 Input/Output**
	AD2	OH / I	St/B	**External Bus Interface Address/Data Line 2**
	U0C0_DX1B	I	St/B	**USIC0 Channel 0 Shift Clock Input**
63	P0.4	O0 / I	St/B	**Bit 4 of Port 0, General Purpose Input/Output**
	U1C1_SELO0	O1	St/B	**USIC1 Channel 1 Select/Control 0 Output**
	U1C0_SELO1	O2	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	CCU61_COUT61	O3	St/B	**CCU61 Channel 1 Output**
	A4	OH	St/B	**External Bus Interface Address Line 4**
	U1C1_DX2A	I	St/B	**USIC1 Channel 1 Shift Control Input**
	RxDC1B	I	St/B	**CAN Node 1 Receive Data Input**
65	TRef	IO	Sp/1	**Control Pin for Core Voltage Generation** Connect TRef to V_{DDPB} to use the on-chip EVRs. Connect TRef to V_{DDI1} for external core voltage supply (on-chip EVRs off).
66	P2.10	O0 / I	St/B	**Bit 10 of Port 2, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_SELO3	O2	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CC2_23	O3 / I	St/B	**CAPCOM2 CC23IO Capture Inp./ Compare Out.**
	A23	OH	St/B	**External Bus Interface Address Line 23**
	U0C1_DX0E	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CAPIN	I	St/B	**GPT2 Register CAPREL Capture Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
67	P10.3	O0 / I	St/B	**Bit 3 of Port 10, General Purpose Input/Output**
	CCU60_COUT60	O2	St/B	**CCU60 Channel 0 Output**
	AD3	OH / I	St/B	**External Bus Interface Address/Data Line 3**
	U0C0_DX2A	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2A	I	St/B	**USIC0 Channel 1 Shift Control Input**
68	P0.5	O0 / I	St/B	**Bit 5 of Port 0, General Purpose Input/Output**
	U1C1_SCLKOUT	O1	St/B	**USIC1 Channel 1 Shift Clock Output**
	U1C0_SELO2	O2	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	CCU61_COUT62	O3	St/B	**CCU61 Channel 2 Output**
	A5	OH	St/B	**External Bus Interface Address Line 5**
	U1C1_DX1A	I	St/B	**USIC1 Channel 1 Shift Clock Input**
	U1C0_DX1C	I	St/B	**USIC1 Channel 0 Shift Clock Input**
69	P10.4	O0 / I	St/B	**Bit 4 of Port 10, General Purpose Input/Output**
	U0C0_SELO3	O1	St/B	**USIC0 Channel 0 Select/Control 3 Output**
	CCU60_COUT61	O2	St/B	**CCU60 Channel 1 Output**
	AD4	OH / I	St/B	**External Bus Interface Address/Data Line 4**
	U0C0_DX2B	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX2B	I	St/B	**USIC0 Channel 1 Shift Control Input**
70	P10.5	O0 / I	St/B	**Bit 5 of Port 10, General Purpose Input/Output**
	U0C1_SCLKOUT	O1	St/B	**USIC0 Channel 1 Shift Clock Output**
	CCU60_COUT62	O2	St/B	**CCU60 Channel 2 Output**
	AD5	OH / I	St/B	**External Bus Interface Address/Data Line 5**
	U0C1_DX1B	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
71	P0.6	O0 / I	St/B	**Bit 6 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	TxDC1	O2	St/B	**CAN Node 1 Transmit Data Output**
	CCU61_ COUT63	O3	St/B	**CCU61 Channel 3 Output**
	A6	OH	St/B	**External Bus Interface Address Line 6**
	U1C1_DX0A	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_ CTRAPA	I	St/B	**CCU61 Emergency Trap Input**
	U1C1_DX1B	I	St/B	**USIC1 Channel 1 Shift Clock Input**
72	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	U1C0_ SELO0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	AD6	OH / I	St/B	**External Bus Interface Address/Data Line 6**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_ CTRAPA	I	St/B	**CCU60 Emergency Trap Input**
73	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_ COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / I	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_ CCPOS0A	I	St/B	**CCU60 Position Input 0**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
74	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_ SELO3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_ CTRAPB	I	St/B	**CCU61 Emergency Trap Input**
78	P1.0	O0 / I	St/B	**Bit 0 of Port 1, General Purpose Input/Output**
	U1C0_ MCLKOUT	O1	St/B	**USIC1 Channel 0 Master Clock Output**
	U1C0_ SELO4	O2	St/B	**USIC1 Channel 0 Select/Control 4 Output**
	A8	OH	St/B	**External Bus Interface Address Line 8**
	ESR1_3	I	St/B	**ESR1 Trigger Input 3**
	EX0BINA	I	St/B	**External Interrupt Trigger Input**
79	P10.8	O0 / I	St/B	**Bit 8 of Port 10, General Purpose Input/Output**
	U0C0_ MCLKOUT	O1	St/B	**USIC0 Channel 0 Master Clock Output**
	U0C1_ SELO0	O2	St/B	**USIC0 Channel 1 Select/Control 0 Output**
	AD8	OH / I	St/B	**External Bus Interface Address/Data Line 8**
	CCU60_ CCPOS1A	I	St/B	**CCU60 Position Input 1**
	U0C0_DX1C	I	St/B	**USIC0 Channel 0 Shift Clock Input**
	$\overline{\text{BRKIN}}$_B	I	St/B	**OCDS Break Signal Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
80	P10.9	O0 / I	St/B	**Bit 9 of Port 10, General Purpose Input/Output**
	U0C0_ SELO4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_ MCLKOUT	O2	St/B	**USIC0 Channel 1 Master Clock Output**
	AD9	OH / I	St/B	**External Bus Interface Address/Data Line 9**
	CCU60_ CCPOS2A	I	St/B	**CCU60 Position Input 2**
	TCK_B	I	St/B	**JTAG Clock Input**
81	P1.1	O0 / I	St/B	**Bit 1 of Port 1, General Purpose Input/Output**
	U1C0_ SELO5	O2	St/B	**USIC1 Channel 0 Select/Control 5 Output**
	U2C1_DOUT	O3	St/B	**USIC2 Channel 1 Shift Data Output**
	A9	OH	St/B	**External Bus Interface Address Line 9**
	ESR2_3	I	St/B	**ESR2 Trigger Input 3**
	EX1BINA	I	St/B	**External Interrupt Trigger Input**
	U2C1_DX0C	I	St/B	**USIC2 Channel 1 Shift Data Input**
82	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_ SELO0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_ COUT63	O2	St/B	**CCU60 Channel 3 Output**
	AD10	OH / I	St/B	**External Bus Interface Address/Data Line 10**
	ESR1_2	I	St/B	**ESR1 Trigger Input 2**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	TDI_B	I	St/B	**JTAG Test Data Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
83	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLKOUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	AD11	OH / I	St/B	**External Bus Interface Address/Data Line 11**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RxDC2B	I	St/B	**CAN Node 2 Receive Data Input**
	TMS_B	I	St/B	**JTAG Test Mode Selection Input**
84	P1.2	O0 / I	St/B	**Bit 2 of Port 1, General Purpose Input/Output**
	U1C0_SELO6	O2	St/B	**USIC1 Channel 0 Select/Control 6 Output**
	U2C1_SCLKOUT	O3	St/B	**USIC2 Channel 1 Shift Clock Output**
	A10	OH	St/B	**External Bus Interface Address Line 10**
	ESR1_4	I	St/B	**ESR1 Trigger Input 4**
	CCU61_T12HRB	I	St/B	**External Run Control Input for T12 of CCU61**
	EX2AINA	I	St/B	**External Interrupt Trigger Input**
	U2C1_DX0D	I	St/B	**USIC2 Channel 1 Shift Data Input**
	U2C1_DX1C	I	St/B	**USIC2 Channel 1 Shift Clock Input**
85	P10.12	O0 / I	St/B	**Bit 12 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	TxDC2	O2	St/B	**CAN Node 2 Transmit Data Output**
	TDO	O3	St/B	**JTAG Test Data Output**
	AD12	OH / I	St/B	**External Bus Interface Address/Data Line 12**
	U1C0_DX0C	I	St/B	**USIC1 Channel 0 Shift Data Input**
	U1C0_DX1E	I	St/B	**USIC1 Channel 0 Shift Clock Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
86	P10.13	O0 / I	St/B	**Bit 13 of Port 10, General Purpose Input/Output**
	U1C0_DOUT	O1	St/B	**USIC1 Channel 0 Shift Data Output**
	U1C0_ SELO3	O3	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	$\overline{\text{WR}}$/$\overline{\text{WRL}}$	OH	St/B	**External Bus Interface Write Strobe Output** Active for each external write access, when $\overline{\text{WR}}$, active for ext. writes to the low byte, when $\overline{\text{WRL}}$.
	U1C0_DX0D	I	St/B	**USIC1 Channel 0 Shift Data Input**
87	P1.3	O0 / I	St/B	**Bit 3 of Port 1, General Purpose Input/Output**
	U1C0_ SELO7	O2	St/B	**USIC1 Channel 0 Select/Control 7 Output**
	U2C0_ SELO4	O3	St/B	**USIC2 Channel 0 Select/Control 4 Output**
	A11	OH	St/B	**External Bus Interface Address Line 11**
	ESR2_4	I	St/B	**ESR2 Trigger Input 4**
	EX3AINA	I	St/B	**External Interrupt Trigger Input**
89	P10.14	O0 / I	St/B	**Bit 14 of Port 10, General Purpose Input/Output**
	U1C0_ SELO1	O1	St/B	**USIC1 Channel 0 Select/Control 1 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	$\overline{\text{RD}}$	OH	St/B	**External Bus Interface Read Strobe Output**
	ESR2_2	I	St/B	**ESR2 Trigger Input 2**
	U0C1_DX0C	I	St/B	**USIC0 Channel 1 Shift Data Input**
	RxDC3C	I	St/B	**CAN Node 3 Receive Data Input**
90	P1.4	O0 / I	St/B	**Bit 4 of Port 1, General Purpose Input/Output**
	U1C1_ SELO4	O2	St/B	**USIC1 Channel 1 Select/Control 4 Output**
	U2C0_ SELO5	O3	St/B	**USIC2 Channel 0 Select/Control 5 Output**
	A12	OH	St/B	**External Bus Interface Address Line 12**
	U2C0_DX2B	I	St/B	**USIC2 Channel 0 Shift Control Input**

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
91	P10.15	O0 / I	St/B	**Bit 15 of Port 10, General Purpose Input/Output**
	U1C0_ SELO2	O1	St/B	**USIC1 Channel 0 Select/Control 2 Output**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U1C0_DOUT	O3	St/B	**USIC1 Channel 0 Shift Data Output**
	ALE	OH	St/B	**External Bus Interf. Addr. Latch Enable Output**
	U0C1_DX1C	I	St/B	**USIC0 Channel 1 Shift Clock Input**
92	P1.5	O0 / I	St/B	**Bit 5 of Port 1, General Purpose Input/Output**
	U1C1_ SELO3	O2	St/B	**USIC1 Channel 1 Select/Control 3 Output**
	$\overline{\mathrm{BRKOUT}}$	O3	St/B	**OCDS Break Signal Output**
	A13	OH	St/B	**External Bus Interface Address Line 13**
	U2C0_DX0C	I	St/B	**USIC2 Channel 0 Shift Data Input**
93	P1.6	O0 / I	St/B	**Bit 6 of Port 1, General Purpose Input/Output**
	U1C1_ SELO2	O2	St/B	**USIC1 Channel 1 Select/Control 2 Output**
	U2C0_DOUT	O3	St/B	**USIC2 Channel 0 Shift Data Output**
	A14	OH	St/B	**External Bus Interface Address Line 14**
	U2C0_DX0D	I	St/B	**USIC2 Channel 0 Shift Data Input**
94	P1.7	O0 / I	St/B	**Bit 7 of Port 1, General Purpose Input/Output**
	U1C1_ MCLKOUT	O2	St/B	**USIC1 Channel 1 Master Clock Output**
	U2C0_ SCLKOUT	O3	St/B	**USIC2 Channel 0 Shift Clock Output**
	A15	OH	St/B	**External Bus Interface Address Line 15**
	U2C0_DX1C	I	St/B	**USIC2 Channel 0 Shift Clock Input**
95	XTAL2	O	Sp/1	**Crystal Oscillator Amplifier Output**
96	XTAL1	I	Sp/1	**Crystal Oscillator Amplifier Input** To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.

Table 2 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	$\overline{\text{PORST}}$	I	In/B	**Power On Reset Input** A low level at this pin resets the XC236x completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns.
98	$\overline{\text{ESR1}}$	O0 / I	St/B	**External Service Request 1**
	EX0AINB	I	St/B	**External Interrupt Trigger Input**
99	$\overline{\text{ESR0}}$	O0 / I	St/B	**External Service Request 0** *Note: After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.*
10	V_{DDIM}	-	PS/M	**Digital Core Supply Voltage for Domain M** Decouple with a 680 nF ceramic capacitor.
38, 64, 88	V_{DDI1}	-	PS/1	**Digital Core Supply Voltage for Domain 1** Decouple each with a 220 nF ceramic capacitor. All V_{DDI1} pins must be connected to each other.
14	V_{DDPA}	-	PS/A	**Digital Pad Supply Voltage for Domain A** Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. *Note: The A/D_Converters and ports P5, P6, and P15 are fed from supply voltage V_{DDPA}.*
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent $V_{\text{DDP}}/V_{\text{SS}}$ pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6, and P15 are fed from supply voltage V_{DDPB}.*
1, 26, 51, 76	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane.

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1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

3 Functional Description

The architecture of the XC236x combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a very well-balanced way. In addition, the on-chip memory blocks allow the design of compact systems-on-silicon with maximum performance (computing, control, communication).

The on-chip memory blocks (program code-memory and SRAM, dual-port RAM, data SRAM) and the set of generic peripherals are connected to the CPU via separate buses. Another bus, the LXBus, connects additional on-chip resources as well as external resources (see **Figure 3**). This bus structure enhances the overall system performance by enabling the concurrent operation of several subsystems of the XC236x.

The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the XC236x.

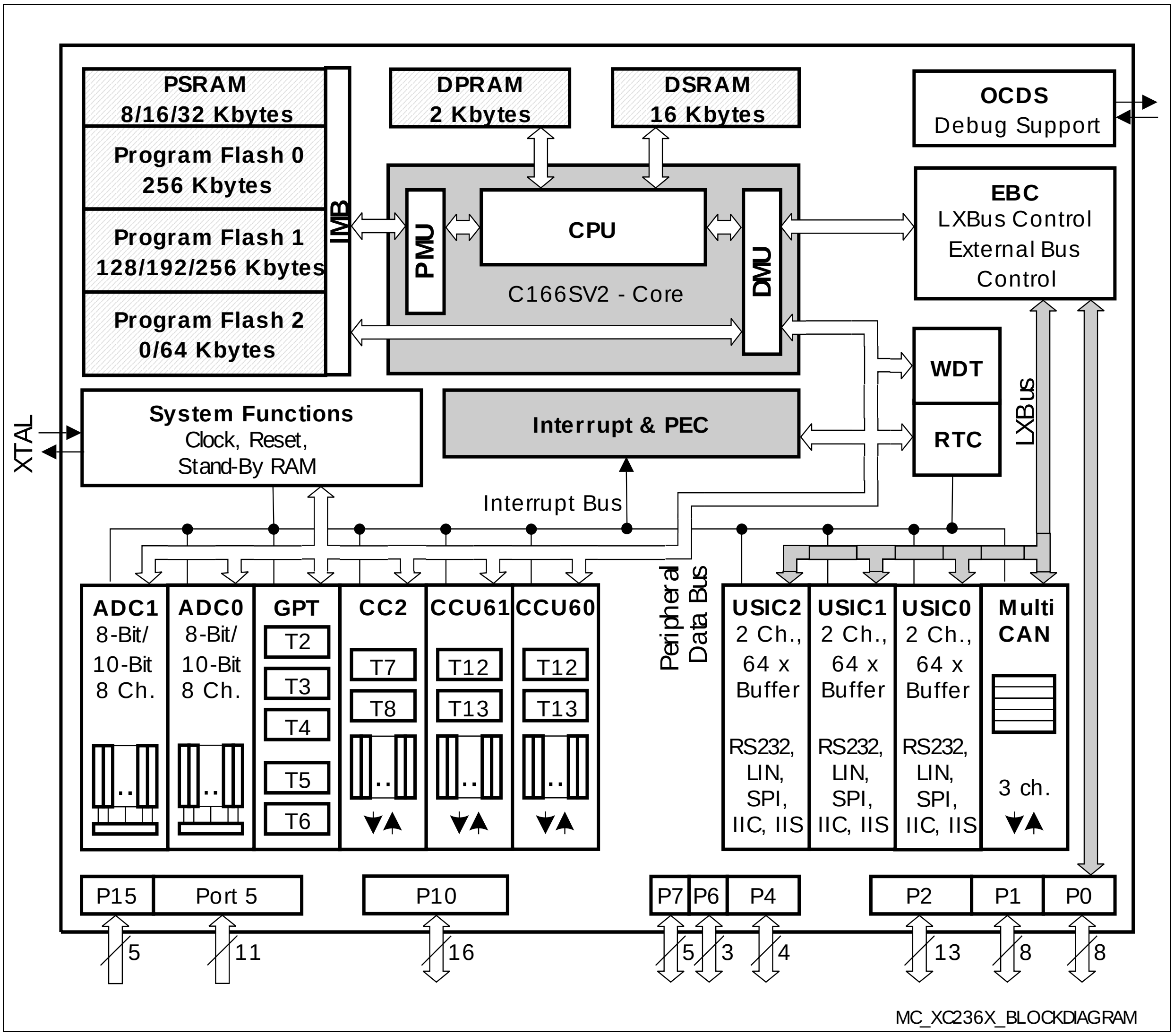

Figure 3 Block Diagram

3.1 Memory Subsystem and Organization

The memory space of the XC236x is configured in a von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space.

Table 3 XC236x Memory Map

Address Area	Start Loc.	End Loc.	Area Size[1]	Notes
IMB register space	$FF'FF00_H$	$FF'FFFF_H$	256 Bytes	–
Reserved (Access trap)	$F0'0000_H$	$FF'FEFF_H$	<1 Mbyte	Minus IMB reg.
Reserved for EPSRAM	$E8'8000_H$	$EF'FFFF_H$	480 Kbytes	Mirrors EPSRAM
Emulated PSRAM	$E8'0000_H$	$E8'7FFF_H$	32 Kbytes	Flash timing
Reserved for PSRAM	$E0'8000_H$	$E7'FFFF_H$	480 Kbytes	Mirrors PSRAM
Program SRAM	$E0'0000_H$	$E0'7FFF_H$	32 Kbytes	Maximum speed
Reserved for pr. mem.	$C9'0000_H$	$DF'FFFF_H$	<1.25 Mbytes	–
Program Flash 2	$C8'0000_H$	$C8'FFFF_H$	64 Kbytes	–
Program Flash 1	$C4'0000_H$	$C7'FFFF_H$	256 Kbytes	–
Program Flash 0	$C0'0000_H$	$C3'FFFF_H$	256 Kbytes	[2]
External memory area	$40'0000_H$	$BF'FFFF_H$	8 Mbytes	–
Available Ext. IO area[3]	$20'5800_H$	$3F'FFFF_H$	< 2 Mbytes	Minus USIC/CAN
USIC registers	$20'4000_H$	$20'57FF_H$	6 Kbytes	Accessed via EBC
MultiCAN registers	$20'0000_H$	$20'3FFF_H$	16 Kbytes	Accessed via EBC
External memory area	$01'0000_H$	$1F'FFFF_H$	< 2 Mbytes	Minus segment 0
SFR area	$00'FE00_H$	$00'FFFF_H$	0.5 Kbyte	–
Dual-Port RAM	$00'F600_H$	$00'FDFF_H$	2 Kbytes	–
Reserved for DPRAM	$00'F200_H$	$00'F5FF_H$	1 Kbyte	–
ESFR area	$00'F000_H$	$00'F1FF_H$	0.5 Kbyte	–
XSFR area	$00'E000_H$	$00'EFFF_H$	4 Kbytes	–
Data SRAM	$00'A000_H$	$00'DFFF_H$	16 Kbytes	–
Reserved for DSRAM	$00'8000_H$	$00'9FFF_H$	8 Kbytes	–
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	–

1) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

2) The uppermost 4-Kbyte sector is reserved for internal use.

3) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed byte wise or word wise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) have additionally been made directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as USIC or MultiCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 32 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the chosen derivative (see ***Table 1****).*

16 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via a separate interface and is, therefore, optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks. A register bank can consist of up to 16 word wide (R0 to R15) and/or byte wide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).
The upper 256 bytes of the DPRAM are directly bit addressable. When used by a GPR, any location in the DPRAM is bit addressable.

1 Kbyte of on-chip Stand-By SRAM (SBRAM) is provided as a storage for system-relevant user data that must be preserved while the major part of the device is powered down. The SBRAM is accessed via a specific interface and is powered via domain M.

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are word wide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the XC2000 Family. Therefore, they should either not be accessed, or written with zeros, to ensure upward compatibility.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 12 Mbytes (approximately, see **Table 3**) of external RAM and/or ROM can be connected to the microcontroller. The External Bus Interface also provides access to external peripherals.

Up to 576 Kbytes of on-chip Flash memory store code, constant data, and control data. The on-chip Flash memory consists of up to 3 modules with a maximum capacity of 256 Kbytes each. Each module is organized in 4-Kbyte sectors. One 4-Kbyte sector of Flash module 0 is used internally to store operation control parameters and protection information.

Note: The actual size of the Flash memory depends on the chosen derivative (see ***Table 1****).*

Each sector can be separately write protected1), erased and programmed (in blocks of 128 Bytes). The complete Flash area can be read-protected. A user-defined password sequence temporarily unlocks protected areas. The Flash modules combine 128-bit read accesses with protected and efficient writing algorithms for programming and erasing. Dynamic error correction provides extremely high read data security for all read accesses. Accesses to different Flash modules can be executed in parallel.
For timing characteristics, please refer to **Section 4.4.2**, for further Flash parameters, please refer to **Section 5.3**.

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1) To save control bits, sectors are clustered for protection purposes, they remain separate for programming/erasing.

3.2 External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). The EBC also controls accesses to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus and allows accessing integrated peripherals and modules in the same way as external components.

The EBC can be programmed either to Single Chip Mode when no external memory is required, or to an external bus mode with the following possible selections1):

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are separately output on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

Up to 4 external $\overline{\text{CS}}$ signals (3 windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can directly be connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface have been made programmable (via registers TCONCSx/FCONCSx) to allow the user the adaption of a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported via a particular 'Ready' function. The active level of the control input signal is selectable.

In addition, up to 4 independent address windows may be defined (via registers ADDRSELx) which control accesses to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these 4 address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is related to the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

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1) Bus modes are switched dynamically if several address windows with different mode settings are used.

3.3 Central Processing Unit (CPU)

The main core of the CPU consists of a 5-stage execution pipeline with a 2-stage instruction-fetch pipeline, a 16-bit arithmetic and logic unit (ALU), a 32-bit/40-bit multiply and accumulate unit (MAC), a register-file providing three register banks, and dedicated SFRs. The ALU features a multiply and divide unit, a bit-mask generator, and a barrel shifter.

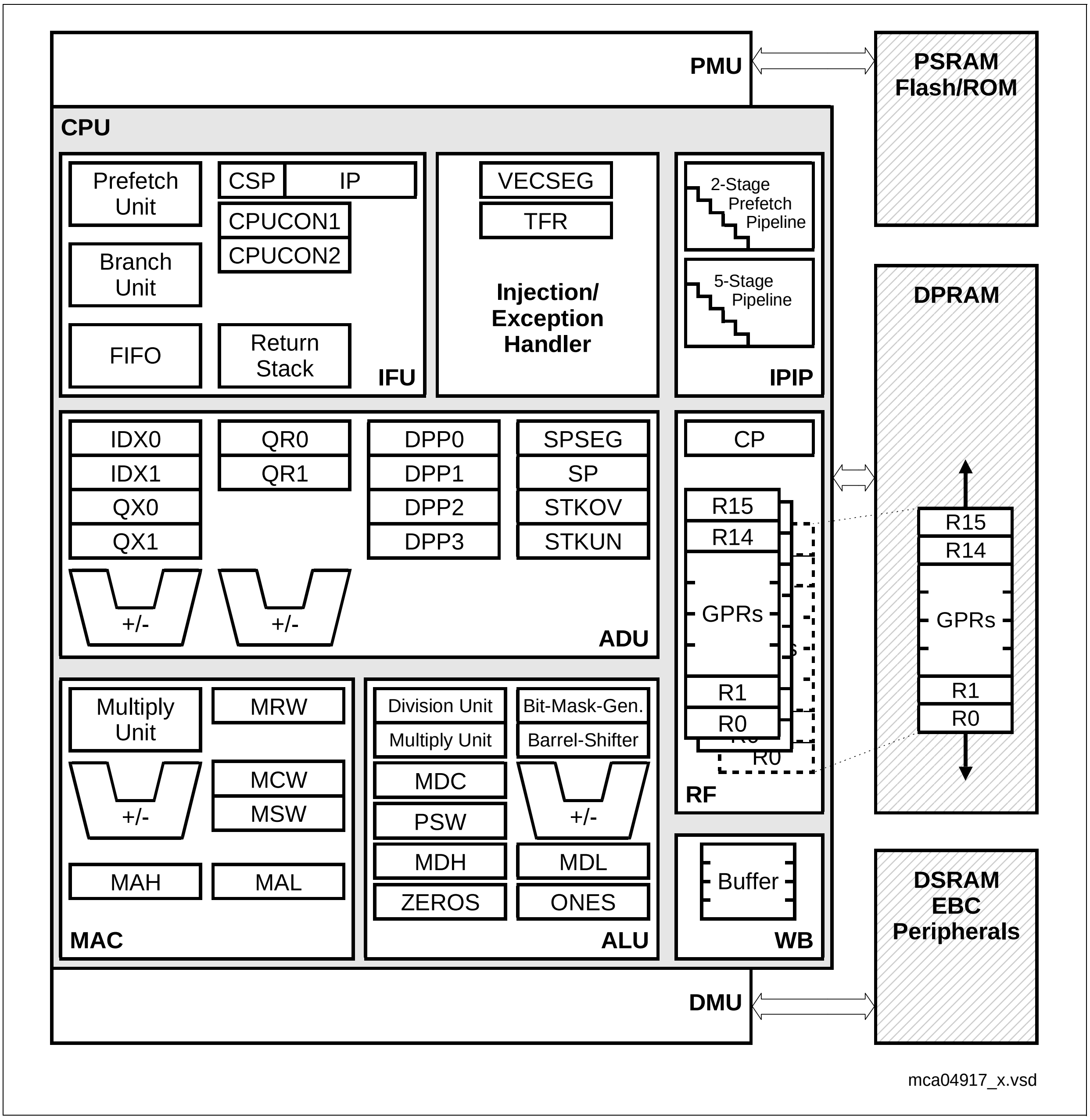


Figure 4 CPU Block Diagram

Based on these hardware provisions, most of the XC236x's instructions can be executed in just one machine cycle which requires 15 ns at 66 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. Also multiplication and most MAC instructions execute in one single cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: for example, a 32-/16-bit division is started within 4 cycles, while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, allows eliminating the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided as a storage for temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area), and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient XC236x instruction set which includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

3.4 Interrupt System

With an interrupt response time of typically 8 CPU clocks (in case of internal program execution), the XC236x is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the XC236x supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source, or the destination pointer, or both. An individual PEC transfer counter is implicitly decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The XC236x has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bit field exists for each of the possible interrupt nodes. Via its related register, each node can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt nodes has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge, or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 4 shows all of the possible XC236x interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not assigned to peripherals (unassigned nodes), may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 4 XC236x Interrupt Nodes

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1]	Trap Number
CAPCOM Register 16, or ERU Request 0	CC2_CC16IC	xx'0040$_H$	10$_H$ / 16$_D$
CAPCOM Register 17, or ERU Request 1	CC2_CC17IC	xx'0044$_H$	11$_H$ / 17$_D$
CAPCOM Register 18, or ERU Request 2	CC2_CC18IC	xx'0048$_H$	12$_H$ / 18$_D$
CAPCOM Register 19, or ERU Request 3	CC2_CC19IC	xx'004C$_H$	13$_H$ / 19$_D$
CAPCOM Register 20, or USIC0 Request 6	CC2_CC20IC	xx'0050$_H$	14$_H$ / 20$_D$
CAPCOM Register 21, or USIC0 Request 7	CC2_CC21IC	xx'0054$_H$	15$_H$ / 21$_D$
CAPCOM Register 22, or USIC1 Request 6	CC2_CC22IC	xx'0058$_H$	16$_H$ / 22$_D$
CAPCOM Register 23, or USIC1 Request 7	CC2_CC23IC	xx'005C$_H$	17$_H$ / 23$_D$
CAPCOM Register 24, or ERU Request 0	CC2_CC24IC	xx'0060$_H$	18$_H$ / 24$_D$
CAPCOM Register 25, or ERU Request 1	CC2_CC25IC	xx'0064$_H$	19$_H$ / 25$_D$
CAPCOM Register 26, or ERU Request 2	CC2_CC26IC	xx'0068$_H$	1A$_H$ / 26$_D$
CAPCOM Register 27, or ERU Request 3	CC2_CC27IC	xx'006C$_H$	1B$_H$ / 27$_D$
CAPCOM Register 28, or USIC2 Request 6	CC2_CC28IC	xx'0070$_H$	1C$_H$ / 28$_D$
CAPCOM Register 29, or USIC2 Request 7	CC2_CC29IC	xx'0074$_H$	1D$_H$ / 29$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0078$_H$	1E$_H$ / 30$_D$
CAPCOM Register 31	CC2_CC31IC	xx'007C$_H$	1F$_H$ / 31$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0080$_H$	20$_H$ / 32$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'0084$_H$	21$_H$ / 33$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0088$_H$	22$_H$ / 34$_D$

Table 4 XC236x Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	**Control Register**	**Vector Location**[1]	**Trap Number**
GPT2 Timer 5	GPT12E_T5IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'0094$_H$	25$_H$ / 37$_D$
CAPCOM Timer 7	CC2_T7IC	xx'0098$_H$	26$_H$ / 38$_D$
CAPCOM Timer 8	CC2_T8IC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Converter Request 0	ADC_0IC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Converter Request 1	ADC_1IC	xx'00A4$_H$	29$_H$ / 41$_D$
A/D Converter Request 2	ADC_2IC	xx'00A8$_H$	2A$_H$ / 42$_D$
A/D Converter Request 3	ADC_3IC	xx'00AC$_H$	2B$_H$ / 43$_D$
A/D Converter Request 4	ADC_4IC	xx'00B0$_H$	2C$_H$ / 44$_D$
A/D Converter Request 5	ADC_5IC	xx'00B4$_H$	2D$_H$ / 45$_D$
A/D Converter Request 6	ADC_6IC	xx'00B8$_H$	2E$_H$ / 46$_D$
A/D Converter Request 7	ADC_7IC	xx'00BC$_H$	2F$_H$ / 47$_D$
CCU60 Request 0	CCU60_0IC	xx'00C0$_H$	30$_H$ / 48$_D$
CCU60 Request 1	CCU60_1IC	xx'00C4$_H$	31$_H$ / 49$_D$
CCU60 Request 2	CCU60_2IC	xx'00C8$_H$	32$_H$ / 50$_D$
CCU60 Request 3	CCU60_3IC	xx'00CC$_H$	33$_H$ / 51$_D$
CCU61 Request 0	CCU61_0IC	xx'00D0$_H$	34$_H$ / 52$_D$
CCU61 Request 1	CCU61_1IC	xx'00D4$_H$	35$_H$ / 53$_D$
CCU61 Request 2	CCU61_2IC	xx'00D8$_H$	36$_H$ / 54$_D$
CCU61 Request 3	CCU61_3IC	xx'00DC$_H$	37$_H$ / 55$_D$
Unassigned node	–	xx'00E0$_H$	38$_H$ / 56$_D$
Unassigned node	–	xx'00E4$_H$	39$_H$ / 57$_D$
Unassigned node	–	xx'00E8$_H$	3A$_H$ / 58$_D$
Unassigned node	–	xx'00EC$_H$	3B$_H$ / 59$_D$
Unassigned node	–	xx'00F0$_H$	3C$_H$ / 60$_D$
Unassigned node	–	xx'00F4$_H$	3D$_H$ / 61$_D$
Unassigned node	–	xx'00F8$_H$	3E$_H$ / 62$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
CAN Request 0	CAN_0IC	xx'0100$_H$	40$_H$ / 64$_D$

Table 4 XC236x Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1]	Trap Number
CAN Request 1	CAN_1IC	xx'0104$_H$	41$_H$ / 65$_D$
CAN Request 2	CAN_2IC	xx'0108$_H$	42$_H$ / 66$_D$
CAN Request 3	CAN_3IC	xx'010C$_H$	43$_H$ / 67$_D$
CAN Request 4	CAN_4IC	xx'0110$_H$	44$_H$ / 68$_D$
CAN Request 5	CAN_5IC	xx'0114$_H$	45$_H$ / 69$_D$
CAN Request 6	CAN_6IC	xx'0118$_H$	46$_H$ / 70$_D$
CAN Request 7	CAN_7IC	xx'011C$_H$	47$_H$ / 71$_D$
CAN Request 8	CAN_8IC	xx'0120$_H$	48$_H$ / 72$_D$
CAN Request 9	CAN_9IC	xx'0124$_H$	49$_H$ / 73$_D$
CAN Request 10	CAN_10IC	xx'0128$_H$	4A$_H$ / 74$_D$
CAN Request 11	CAN_11IC	xx'012C$_H$	4B$_H$ / 75$_D$
CAN Request 12	CAN_12IC	xx'0130$_H$	4C$_H$ / 76$_D$
CAN Request 13	CAN_13IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAN Request 14	CAN_14IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAN Request 15	CAN_15IC	xx'013C$_H$	4F$_H$ / 79$_D$
USIC0 Request 0	U0C0_0IC	xx'0140$_H$	50$_H$ / 80$_D$
USIC0 Request 1	U0C0_1IC	xx'0144$_H$	51$_H$ / 81$_D$
USIC0 Request 2	U0C0_2IC	xx'0148$_H$	52$_H$ / 82$_D$
USIC0 Request 3	U0C1_0IC	xx'014C$_H$	53$_H$ / 83$_D$
USIC0 Request 4	U0C1_1IC	xx'0150$_H$	54$_H$ / 84$_D$
USIC0 Request 5	U0C1_2IC	xx'0154$_H$	55$_H$ / 85$_D$
USIC1 Request 0	U1C0_0IC	xx'0158$_H$	56$_H$ / 86$_D$
USIC1 Request 1	U1C0_1IC	xx'015C$_H$	57$_H$ / 87$_D$
USIC1 Request 2	U1C0_2IC	xx'0160$_H$	58$_H$ / 88$_D$
USIC1 Request 3	U1C1_0IC	xx'0164$_H$	59$_H$ / 89$_D$
USIC1 Request 4	U1C1_1IC	xx'0168$_H$	5A$_H$ / 90$_D$
USIC1 Request 5	U1C1_2IC	xx'016C$_H$	5B$_H$ / 91$_D$
USIC2 Request 0	U2C0_0IC	xx'0170$_H$	5C$_H$ / 92$_D$
USIC2 Request 1	U2C0_1IC	xx'0174$_H$	5D$_H$ / 93$_D$
USIC2 Request 2	U2C0_2IC	xx'0178$_H$	5E$_H$ / 94$_D$

Table 4 XC236x Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1]	Trap Number
USIC2 Request 3	U2C1_0IC	xx'017C$_H$	5F$_H$ / 95$_D$
USIC2 Request 4	U2C1_1IC	xx'0180$_H$	60$_H$ / 96$_D$
USIC2 Request 5	U2C1_2IC	xx'0184$_H$	61$_H$ / 97$_D$
Unassigned node	–	xx'0188$_H$	62$_H$ / 98$_D$
Unassigned node	–	xx'018C$_H$	63$_H$ / 99$_D$
Unassigned node	–	xx'0190$_H$	64$_H$ / 100$_D$
Unassigned node	–	xx'0194$_H$	65$_H$ / 101$_D$
Unassigned node	–	xx'0198$_H$	66$_H$ / 102$_D$
Unassigned node	–	xx'019C$_H$	67$_H$ / 103$_D$
Unassigned node	–	xx'01A0$_H$	68$_H$ / 104$_D$
Unassigned node	–	xx'01A4$_H$	69$_H$ / 105$_D$
Unassigned node	–	xx'01A8$_H$	6A$_H$ / 106$_D$
SCU Request 1	SCU_1IC	xx'01AC$_H$	6B$_H$ / 107$_D$
SCU Request 0	SCU_0IC	xx'01B0$_H$	6C$_H$ / 108$_D$
Program Flash Modules	PFM_IC	xx'01B4$_H$	6D$_H$ / 109$_D$
RTC	RTC_IC	xx'01B8$_H$	6E$_H$ / 110$_D$
End of PEC Subchannel	EOPIC	xx'01BC$_H$	6F$_H$ / 111$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC236x also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called 'Hardware Traps'. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1]	Trap Number	Trap Priority
Reset Functions	–	RESET	xx'0000$_H$	00$_H$	III
Class A Hardware Traps:					
• System Request 0	SR0	SR0TRAP	xx'0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx'0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx'0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx'0020$_H$	08$_H$	II
Class B Hardware Traps:					
• System Request 1	SR1	BTRAP	xx'0028$_H$	0A$_H$	I
• Undefined Opcode	UNDOPC	BTRAP	xx'0028$_H$	0A$_H$	I
• Memory Access Error	ACER	BTRAP	xx'0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx'0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx'0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps: • TRAP Instruction	–	–	Any [xx'0000$_H$ - xx'01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

[1] Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC236x. The user software running on the XC236x can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface or via the external bus interface for increased performance.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 optional break lines) to communicate with external circuitry.

3.6 Capture/Compare Unit (CAPCOM2)

The CAPCOM2 unit supports generation and control of timing sequences on up to 16 channels with a maximum resolution of 1 system clock cycle (8 cycles in staggered mode). The CAPCOM2 unit is typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PWM), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Two 16-bit timers (T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2. This provides a wide range of variation for the timer period and resolution and allows precise adjustments to the application specific requirements. In addition, an external count input for CAPCOM2 timer T7 allows event scheduling for the capture/compare registers relative to external events.

The capture/compare register array contains 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM2 timer T7 or T8 and programmed for capture or compare function.
12 registers of the CAPCOM2 module have each one port pin associated with it which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

Table 6 Compare Modes (CAPCOM2)

Compare Modes	Function
Mode 0	Interrupt-only compare mode; Several compare interrupts per timer period are possible
Mode 1	Pin toggles on each compare match; Several compare events per timer period are possible
Mode 2	Interrupt-only compare mode; Only one compare interrupt per timer period is generated
Mode 3	Pin set ‘1’ on match; pin reset ‘0’ on compare timer overflow; Only one compare event per timer period is generated
Double Register Mode	Two registers operate on one pin; Pin toggles on each compare match; Several compare events per timer period are possible
Single Event Mode	Generates single edges or pulses; Can be used with any compare mode

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (‘captured’) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated. Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event.

The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture/compare register, specific actions will be taken based on the selected compare mode.

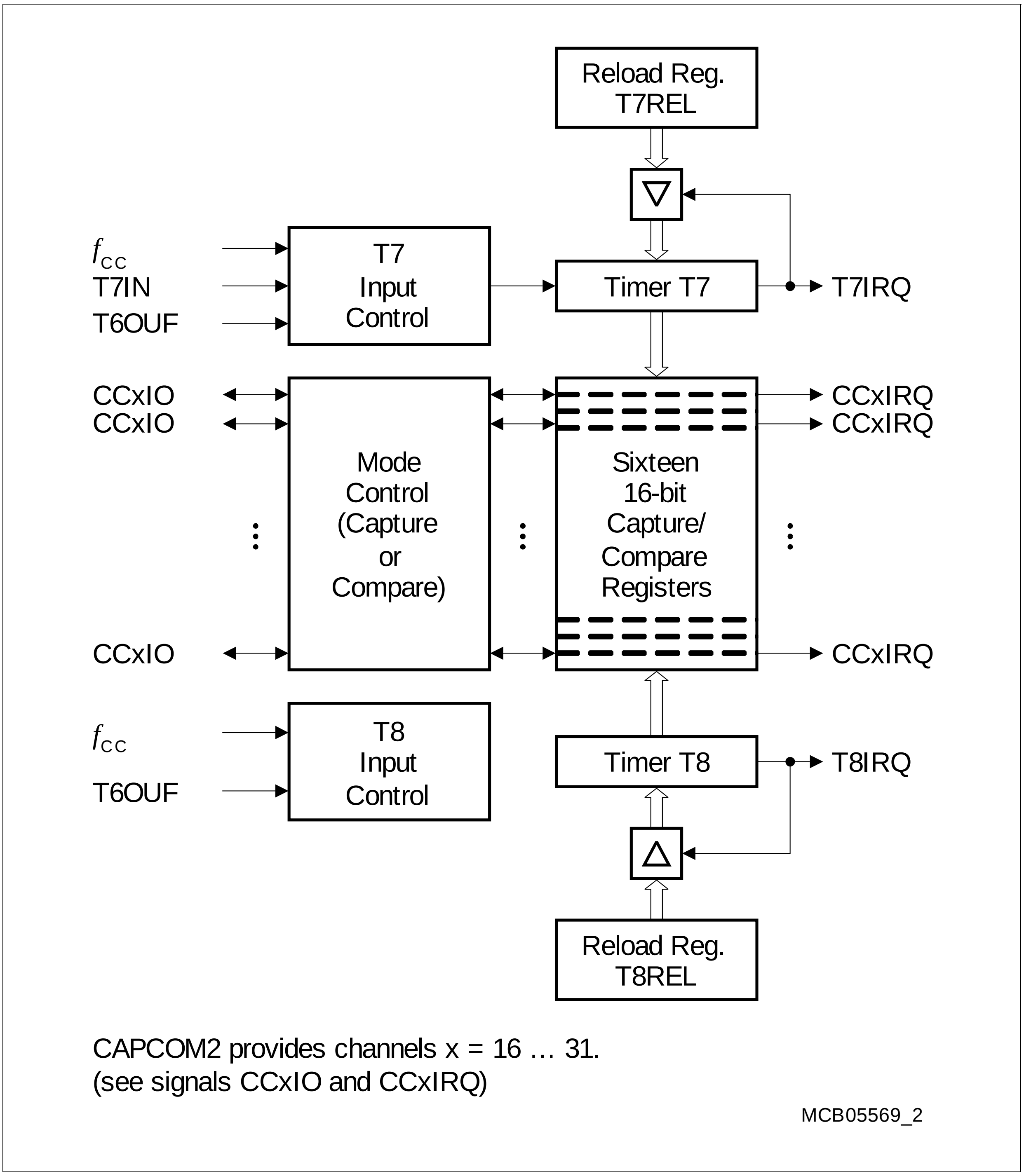


Figure 5 CAPCOM2 Unit Block Diagram

3.7 Capture/Compare Units CCU6x

The XC236x features two CCU6 units (CCU60, CCU61).

The CCU6 is a high-resolution capture and compare unit with application specific modes. It provides inputs to start the timers synchronously, an important feature in devices with several CCU6 modules.

The module provides two independent timers (T12, T13), that can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel.
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16 bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Automatic start on an HW event (T12HR, for synchronization purposes)

Timer 13 Features

- One independent compare channel with one output
- 16 bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Automatic start on an HW event (T13HR, for synchronization purposes)

Additional Features

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

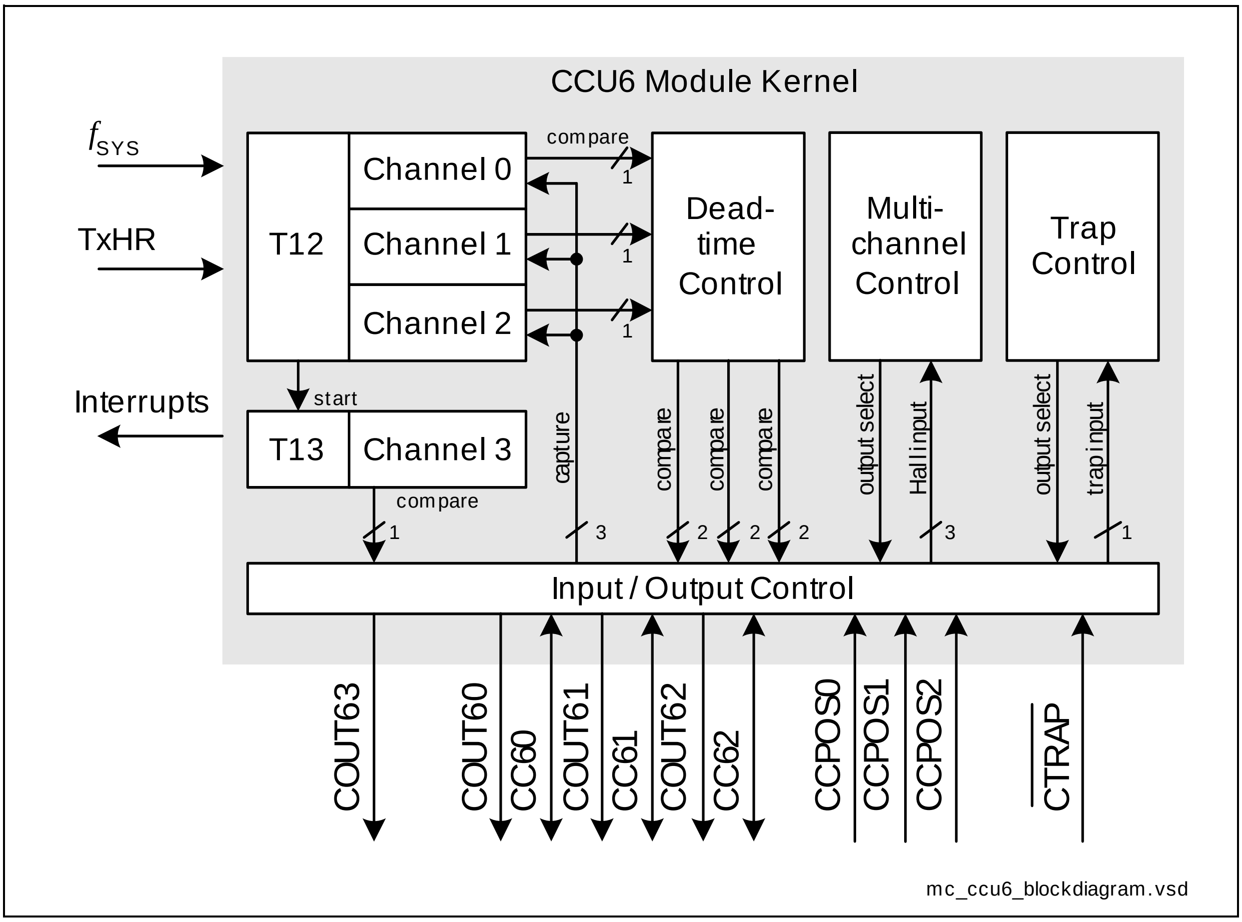


Figure 6 **CCU6 Block Diagram**

Timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. Timer T13 can work in compare mode only. The multi-channel control unit generates output patterns that can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for the signal modulation.

3.8 General Purpose Timer (GPT12E) Unit

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT12E unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the system clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.

Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the ‘gate’ level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 4 system clock cycles.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components. It may also be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

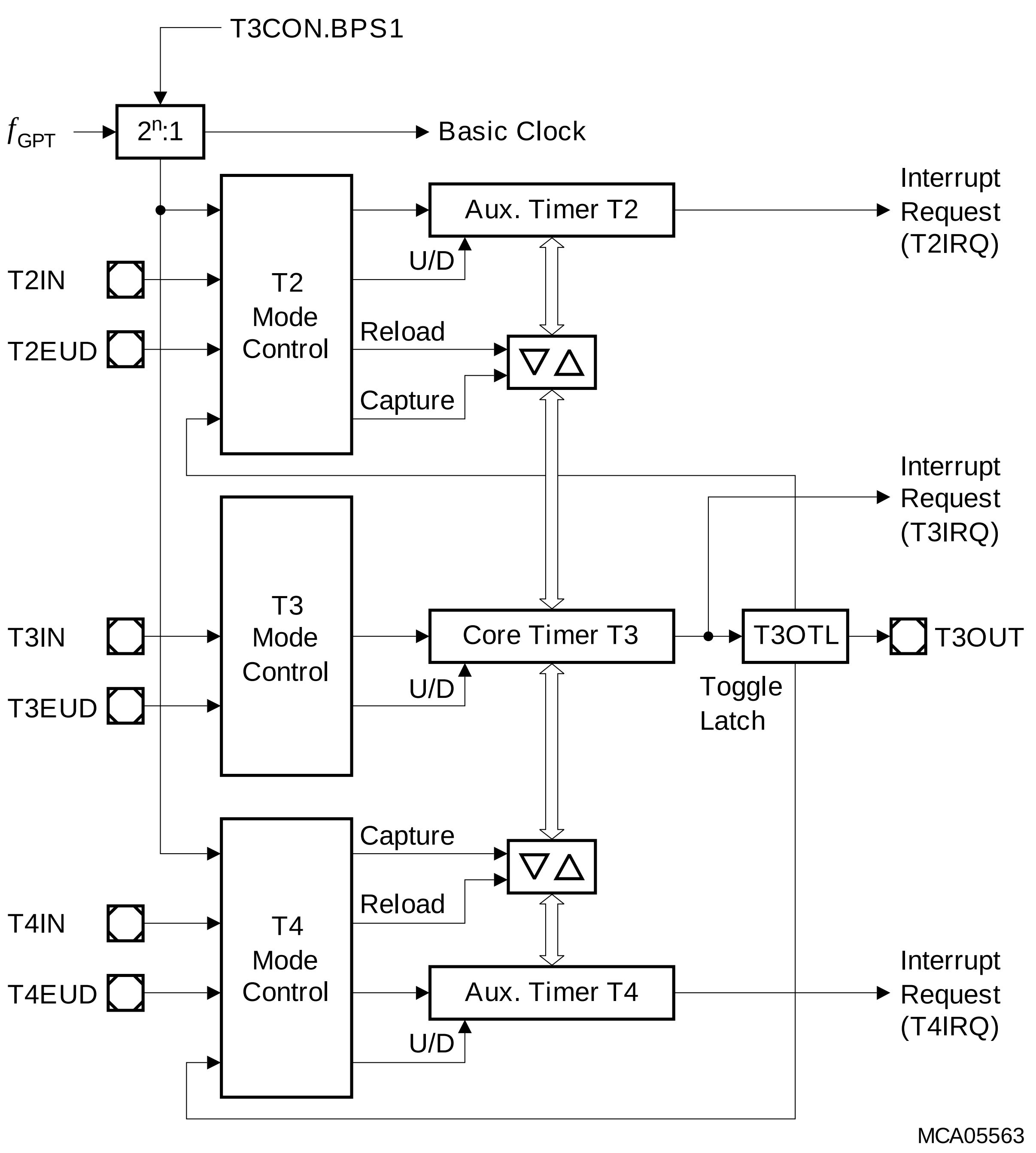


Figure 7 Block Diagram of GPT1

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC236x to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

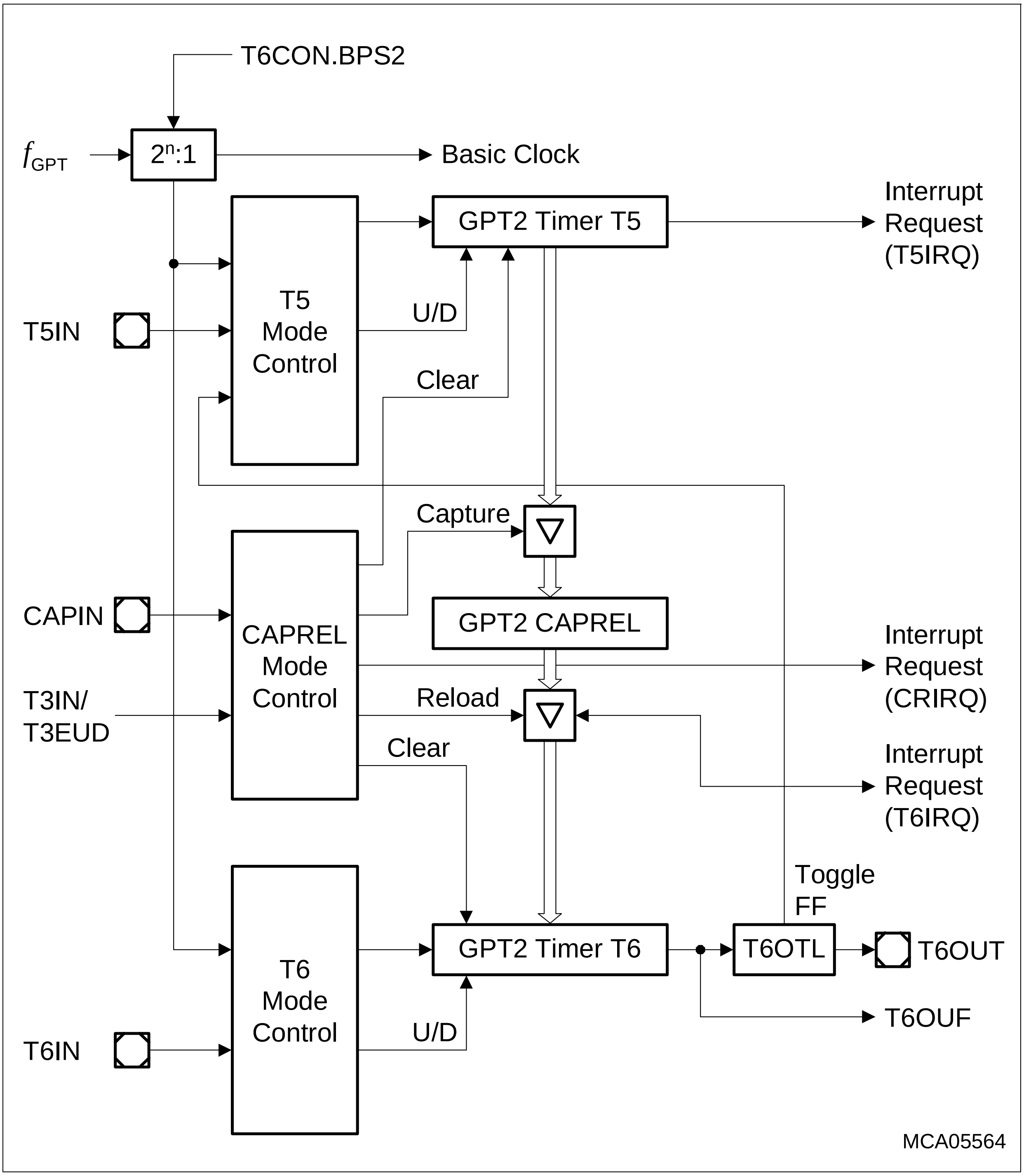


Figure 8 Block Diagram of GPT2

3.9 Real Time Clock

The Real Time Clock (RTC) module of the XC236x can be clocked with a selectable clock signal from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL), made of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

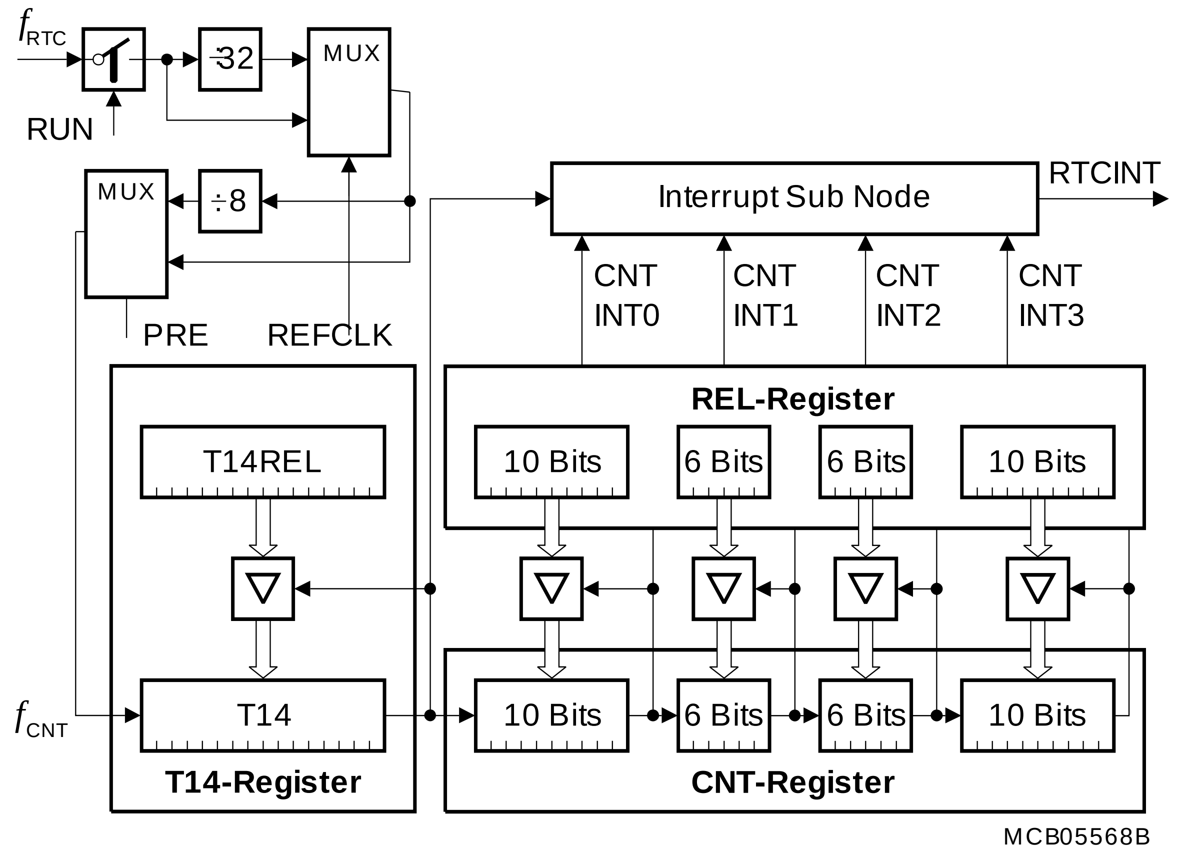


Figure 9 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

The RTC module can be used for different purposes:

- System clock to determine the current time and date
- Cyclic time based interrupt, to provide a system time tick independent of CPU frequency and other resources
- 48-bit timer for long term measurements
- Alarm interrupt upon a defined time

3.10 A/D Converters

For analog signal measurement, up to two 10-bit A/D converters (ADC0, ADC1) with 8 multiplexed input channels including a sample and hold circuit have been integrated on-chip. They use the method of successive approximation. The sample time (for loading the capacitors) and the conversion time are programmable and can thus be adjusted to the external circuitry. The A/D converters can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Several independent conversion result registers, selectable interrupt requests, and highly flexible conversion sequences provide a high degree of programmability to fulfill the requirements of the respective application. Both modules can be synchronized to allow parallel sampling of two input channels.

For applications that require more analog input channels, external analog multiplexers can be controlled automatically.

For applications that require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converters of the XC236x support two types of request sources which can be triggered by several internal and external events.

- Parallel requests are activated at the same time and then executed in a predefined sequence.
- Queued requests are executed in a user-defined sequence.

In addition, the conversion of a specific channel can be inserted into a running sequence without disturbing this sequence. All requests are arbitrated according to the priority level that has been assigned to them.

Data reduction features, such as limit checking or result accumulation, reduce the number of required CPU accesses and so allow the precise evaluation of analog inputs (high conversion rate) even at low CPU speed.

The Peripheral Event Controller (PEC) may be used to control the A/D converters or to automatically store conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer. Therefore, each A/D converter contains 8 result registers which can be concatenated to build a result FIFO. Wait-for-read mode can be enabled for each result register to prevent loss of conversion data.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital input stages under software control. This can be selected for each pin separately via registers P5_DIDIS and P15_DIDIS (Port x Digital Input Disable).

The Auto-Power-Down feature of the A/D converters minimizes the power consumption when no conversion is in progress.

3.11 Universal Serial Interface Channel Modules (USIC)

The XC236x features three USIC modules (USIC0, USIC1, USIC2), each providing two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent from the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit, so the inputs and outputs of each USIC channel can be assigned to different interface pins providing great flexibility to the application software. All assignments can be done during runtime.

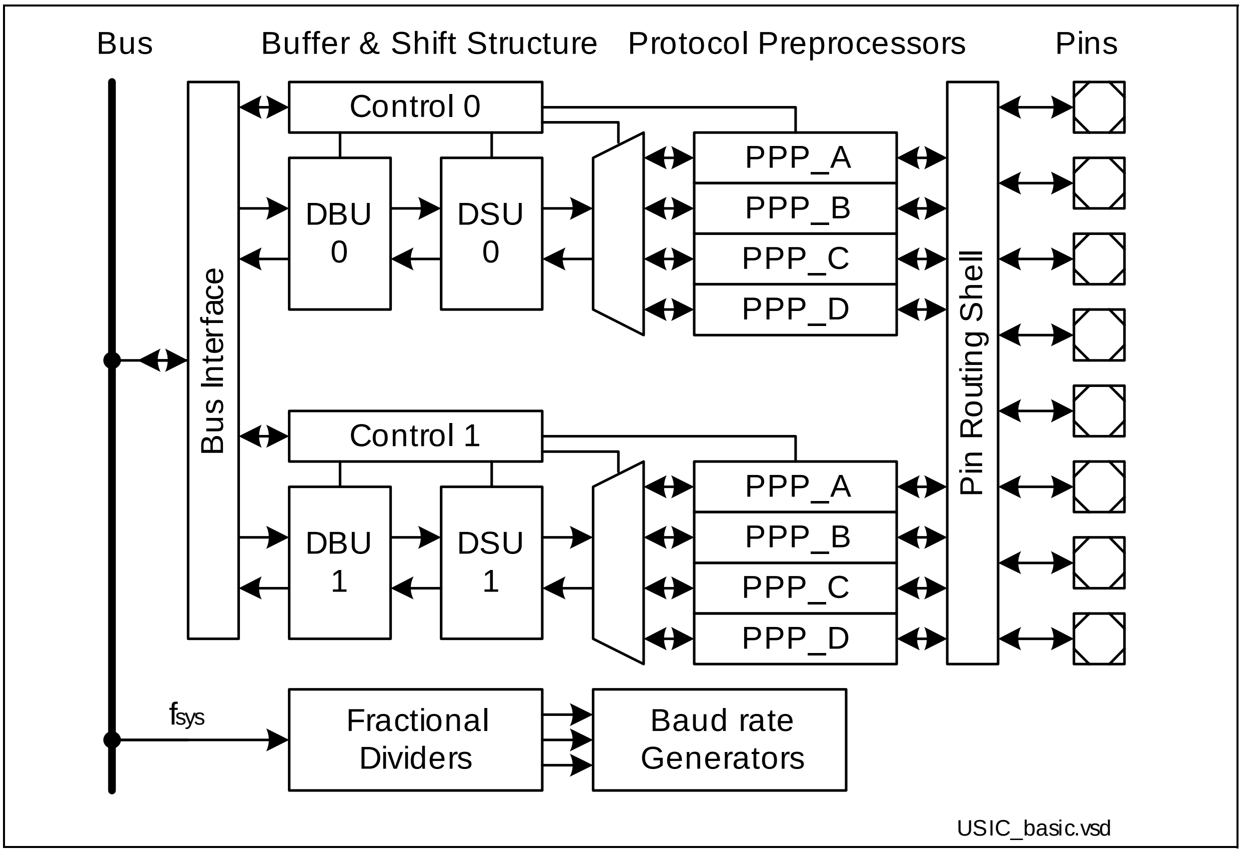


Figure 10 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols, but improved performances (baud rate, buffer handling)

Target Protocols

Each USIC channel can receive and transmit data frames with a selectable data word width from 1 to 16 bits in each of the following protocols:

- **UART** (asynchronous serial channel)
  - maximum baud rate: f_{SYS} / 4
  - data frame length programmable from 1 to 63 bits
  - MSB or LSB first
- **LIN** Support (Local Interconnect Network)
  - maximum baud rate: f_{SYS} / 16
  - checksum generation under software control
  - baud rate detection possible by built-in capture event of baud rate generator
- **SSC/SPI/QSPI** (synchronous serial channel with or without data buffer)
  - maximum baud rate in slave mode: f_{SYS}
  - maximum baud rate in master mode: f_{SYS} / 2
  - number of data bits programmable from 1 to 63, more with explicit stop condition
  - MSB or LSB first
  - optional control of slave select signals
- **IIC** (Inter-IC Bus)
  - supports baud rates of 100 kbit/s and 400 kbit/s
- **IIS** (Inter-IC Sound Bus)
  - maximum baud rate: f_{SYS} / 2 for transmitter, f_{SYS} for receiver

Note: Depending on the selected functions (such as digital filters, input synchronization stages, sample point adjustment, etc.), the maximum reachable baud rate can be limited. Please also take care about additional delays, such as internal or external propagation delays and driver delays (e.g. for collision detection in UART mode, for IIC, etc.).

3.12 MultiCAN Module

The MultiCAN module contains three independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of up to 64 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

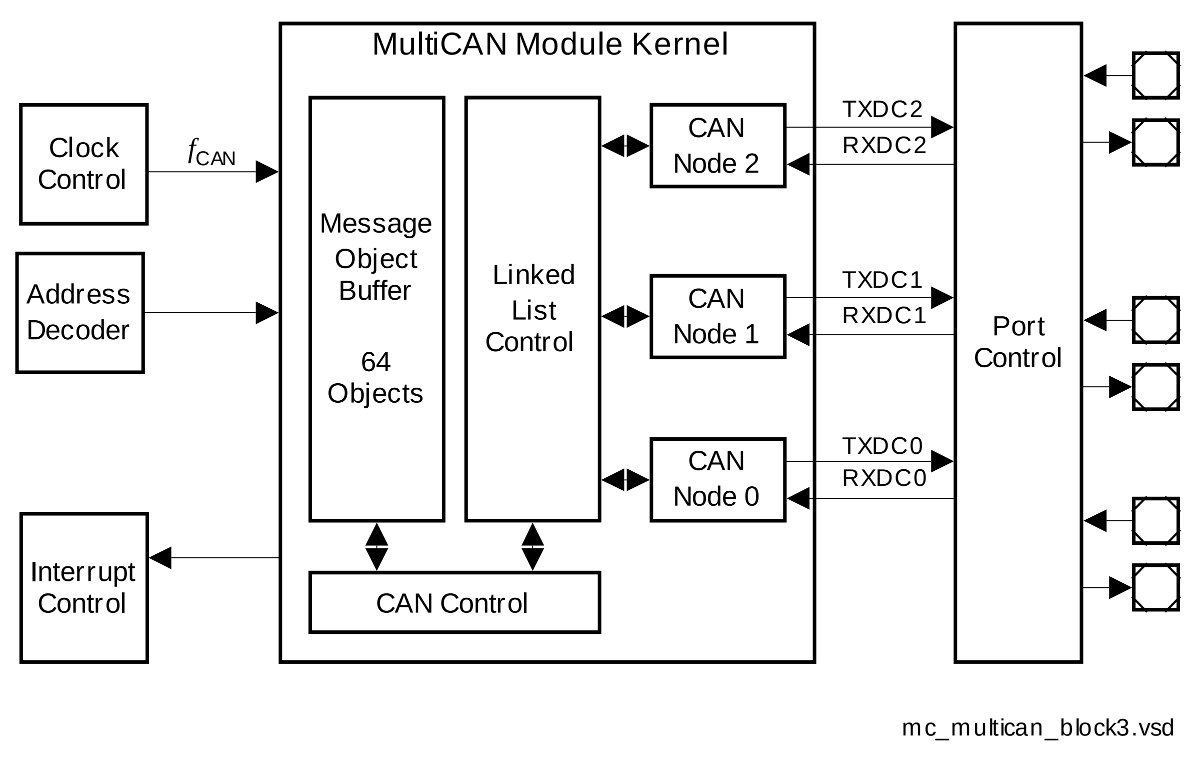


Figure 11 Block Diagram of MultiCAN Module

MultiCAN Features

- CAN functionality conforms to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Three independent CAN nodes
- 64 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.13 Watchdog Timer

The Watchdog Timer represents one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip, and can be disabled and enabled at any time by executing instructions DISWDT and ENWDT. The software has to be designed to service the Watchdog Timer before it overflows. If, due to hardware or software related failures, the software fails to do so, the Watchdog Timer overflows and generates a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer, clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Thus, time intervals between 3.9 μs and 16.3 s can be monitored (@ 66 MHz).
The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.14 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC236x with high flexibility from several external or internal clock sources.

- External clock signals on pad- or core-voltage level
- External crystal controlled by on-chip oscillator
- On-chip clock source for operation without crystal
- Wake-up clock (ultra-low power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals or from the on-chip clock source. See also **Section 4.4.1**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can also be output on one of two selectable pins.

3.15 Parallel Ports

The XC236x provides up to 75 I/O lines which are organized into 7 input/output ports and 2 input ports. All port lines are bit-addressable, and all input/output lines can be individually (bit-wise) configured via port control registers. This configuration selects the direction (input/output), push/pull or open-drain operation, activation of pull devices, and edge characteristics (shape) and driver characteristics (output current) of the port drivers. The I/O ports are true bidirectional ports which are switched to high impedance state when configured as inputs. During the internal reset, all port pins are configured as inputs without pull devices active.

All port lines have programmable alternate input or output functions associated with them. These alternate functions can be assigned to various port pins to support the optimal utilization for a given application. For this reason, certain functions appear several times in **Table 7**.

All port lines that are not used for these alternate functions may be used as general purpose I/O lines.

Table 7 Summary of the XC236x's Parallel Ports

Port	Width	Alternate Functions
Port 0	8	Address lines, Serial interface lines of USIC1, CAN0, and CAN1, Input/Output lines for CCU61
Port 1	8	Address lines, Serial interface lines of USIC1 and USIC2, OCDS control, interrupts
Port 2	13	Address and/or data lines, bus control, Serial interface lines of USIC0, CAN0, and CAN1, Input/Output lines for CCU60 and CAPCOM2, Timer control signals, JTAG, interrupts, system clock output
Port 4	4	Chip select signals, Serial interface lines of CAN2, Input/Output lines for CAPCOM2, Timer control signals
Port 5	11	Analog input channels to ADC0, Input/Output lines for CCU6x, Timer control signals, JTAG, OCDS control, interrupts

Table 7 Summary of the XC236x's Parallel Ports (cont'd)

Port	**Width**	**Alternate Functions**
Port 6	3	ADC control lines, Serial interface lines of USIC1, Timer control signals, OCDS control
Port 7	5	ADC control lines, Serial interface lines of USIC0, Timer control signals, JTAG, OCDS control,system clock output
Port 10	16	Address and/or data lines, bus control, Serial interface lines of USIC0, USIC1 and CAN2, Input/Output lines for CCU60, JTAG, OCDS control
Port 15	5	Analog input channels to ADC1, Timer control signals

3.16 Instruction Set Summary

Table 8 lists the instructions of the XC236x in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
ROL/ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS/Z	Move byte operand to word op. with sign/zero extension	2 / 4
JMPA/I/R	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4
JB(C)	Jump relative if direct bit is set (and clear bit)	4
JNB(S)	Jump relative if direct bit is not set (and set bit)	4
CALLA/I/R	Call absolute/indirect/relative subroutine if condition is met	4
CALLS	Call absolute subroutine in any code segment	4
PCALL	Push direct word register onto system stack and call absolute subroutine	4
TRAP	Call interrupt service routine via immediate trap number	2
PUSH/POP	Push/pop direct word register onto/from system stack	2
SCXT	Push direct word register onto system stack and update register with word operand	4
RET(P)	Return from intra-segment subroutine (and pop direct word register from system stack)	2
RETS	Return from inter-segment subroutine	2
RETI	Return from interrupt service subroutine	2
SBRK	Software Break	2
SRST	Software Reset	4
IDLE	Enter Idle Mode	4
PWRDN	Unused instruction1)	4
SRVWDT	Service Watchdog Timer	4
DISWDT/ENWDT	Disable/Enable Watchdog Timer	4
EINIT	End-of-Initialization Register Lock	4
ATOMIC	Begin ATOMIC sequence	2
EXTR	Begin EXTended Register sequence	2
EXTP(R)	Begin EXTended Page (and Register) sequence	2 / 4
EXTS(R)	Begin EXTended Segment (and Register) sequence	2 / 4

Table 8 Instruction Set Summary (cont'd)

Mnemonic	**Description**	**Bytes**
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

1) The Enter Power Down Mode instruction is not used in the XC236x, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

4 Electrical Parameters

The operating range for the XC236x is defined by its electrical parameters. For proper operation the indicated limitations must be respected when designing a system.

Attention:** **The parameters and values listed in the following sections of this Preliminary Data Sheet are preliminary and will be adjusted and amended after the complete device characterization has been completed.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 9 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST}	-65	–	150	°C	–
Junction temperature	T_J	-40	–	150	°C	under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDIM}, V_{DDI1}	-0.5	–	1.65	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDPA}, V_{DDPB}	-0.5	–	6.0	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} < V_{DDPmax}$
Input current on any pin during overload condition	–	-10	–	10	mA	–
Absolute sum of all input currents during overload condition	–	–	–	|100|	mA	–

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC236x. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital core supply voltage (if supplied externally)	V_{DDI}	1.4	–	1.6	V	
Core Supply Voltage Difference	ΔVDDI	-10	–	+10	mV	V_{DDIM} - V_{DDI1} [1]
Digital supply voltage for IO pads and voltage regulators, upper voltage range	V_{DDPA}, V_{DDPB}	4.5	–	5.5	V	[2]
Digital supply voltage for IO pads and voltage regulators, lower voltage range	V_{DDPA}, V_{DDPB}	3.0	–	4.5	V	[2]
Supply Voltage Difference	ΔVDD	-0.5	–	–	V	V_{DDP} - V_{DDI}[3]
Digital ground voltage	V_{SS}	0	–	0	V	Reference voltage
Overload current	I_{OV}	-5	–	5	mA	Per IO pin[4][5]
		-2	–	5	mA	Per analog input pin[4][5]
Overload positive current coupling factor for analog inputs[6]	K_{OVA}	–	–	1.0×10^{-4}	–	$I_{\text{OV}} > 0$
Overload negative current coupling factor for analog inputs[6]	K_{OVA}	–	–	1.5×10^{-3}	–	$I_{\text{OV}} < 0$
Overload positive current coupling factor for digital I/O pins[6]	K_{OVD}	–	–	5.0×10^{-3}	–	$I_{\text{OV}} > 0$
Overload negative current coupling factor for digital I/O pins[6]	K_{OVD}	–	–	1.0×10^{-2}	–	$I_{\text{OV}} < 0$

Table 10 Operating Condition Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute sum of overload currents	Σ|IOV|	–	–	50	mA	[5]
External Pin Load Capacitance	C_L	–	20	–	pF	Pin drivers in **default** mode[7]
Voltage Regulator Buffer Capacitance for DMP_M	C_{EVRM}	1.0	–	4.7	μF	[8]
Voltage Regulator Buffer Capacitance for DMP_1	C_{EVR1}	470	–	2200	nF	One for each supply pin[8]
Ambient temperature	T_A	–	–	–	°C	See **Table 1**

1) In case both core power domains are clocked, the difference between the power supply voltages must be less than 10mV. This condition imposes additional constraints when using external power supplies. In order to supply both core power domains, two independent external voltage regulators may not be used. The simplest possibility is to supply both power domains directly via a single external power supply.

2) Performance of pad drivers, A/D Converter, and Flash module depends on V_{DDP}.

3) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes, if V_{DDI} is supplied externally.

4) Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range: $V_{OV} > V_{IHmax}$ ($I_{OV} > 0$) or $V_{OV} < V_{ILmin}$ ($I_{OV} < 0$). The absolute sum of input overload currents on all pins may not exceed **50 mA**. The supply voltages must remain within the specified limits. Proper operation under overload conditions depends on the application.
Overload conditions must not occur on pin XTAL1 (powered by V_{DDI}).

5) Not subject to production test - verified by design/characterization.

6) An overload current (I_{OV}) through a pin injects a certain error current (I_{INJ}) into the adjacent pins. This error current adds to the respective pin's leakage current (I_{OZ}). The amount of error current depends on the overload current and is defined by the overload coupling factor K_{OV}. The polarity of the injected error current is inverse compared to the polarity of the overload current that produces it.
The total current through a pin is $|I_{TOT}| = |I_{OZ}| + (|I_{OV}| \times K_{OV})$. The additional error current may distort the input voltage on analog inputs.

7) The timing is valid for pin drivers operating in default current mode (selected after reset). Reducing the output current may lead to increased delays or reduced driving capability (C_L).

8) To ensure the stability of the voltage regulators the EVRs must be buffered with ceramic capacitors. Separate buffer capacitors with the recomended values shall be connected to each V_{DDI} pin as close as possible to the pins to keep the resistance of the board tracks below 2 Ω.
The minimum capacitance value is required for proper operation under all conditions (e.g. temperature). Higher values slightly increase the startup time. The maximum values are recommended to prevent overload conditions during charging phases.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the XC236x and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column "Symbol":

CC (**C**ontroller **C**haracteristics):
The logic of the XC236x will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):
The external system must provide signals with the respective characteristics to the XC236x.

4.2 DC Parameters

These parameters are static or average values, which may be exceeded during switching transitions (e.g. output current).

The XC236x can operate within a wide supply voltage range from 3.0 V to 5.5 V. However, during operation this supply voltage must not vary within the complete operating voltage range, but must remain within a certain band of 10% of the chosen nominal supply voltage.

For this reason and because the electrical behaviour partly depends on the supply voltage, the parameters are specified twice for the upper and the lower voltage area.

During operation, the supply voltages may only change with a maximum speed of dV/dt < 1 V/ms.

The leakage currents strongly depend on the operating temperature and the actual voltage level at the respective pin. The maximum values given in the following tables apply under worst case conditions, i.e. maximum temperature and an input level equal to the supply voltage.
The actual value for the leakage current can be determined by evaluating the respective leakage derating formula (see tables) using values from the actual application.

The pads of the XC236x are designed to operate in various driver modes. The DC parameter specifications refer to the current limits given in **Table 11**.

Table 11 Current Limits for Port Output Drivers

Port Output Driver Mode	**Maximum Output Current (I_{OLmax}, $-I_{OHmax}$)**[1]		**Nominal Output Current (I_{OLnom}, $-I_{OHnom}$)**	
	$V_{DDP} \geq 4.5$ **V**	$V_{DDP} < 4.5$ **V**	$V_{DDP} \geq 4.5$ **V**	$V_{DDP} < 4.5$ **V**
Strong driver	10 mA	10 mA	2.5 mA	2.5 mA
Medium driver	4.0 mA	2.5 mA	1.0 mA	1.0 mA
Weak driver	0.5 mA	0.5 mA	0.1 mA	0.1 mA

[1] An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time.
For any group of 16 neighboring output pins the total output current in each direction (ΣIOL and Σ-IOH) must remain below 50 mA.

4.2.1 DC Parameters for Upper Voltage Area

These parameters apply to the upper IO voltage area of 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Table 12 DC Characteristics for 4.5 V ≤ V_{DDP} ≤ 5.5 V (Operating Conditions apply)[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input low voltage for XTAL1	V_{ILC} SR	-1.7 + V_{DDI}	–	0.3 × V_{DDI}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input high voltage for XTAL1	V_{IHC} SR	0.7 × V_{DDI}	–	1.7	V	[2]
Input Hysteresis[3]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DD} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \leq I_{OLmax}$[4]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$[4] [5]
Output high voltage[6]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$[4]
Output high voltage[6]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$[4] [5]
Input leakage current (Port 5, Port 15)[7]	I_{OZ1} CC	–	±200	–	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[7][8]	I_{OZ2} CC	–	±2	±5	µA	$T_J \leq$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Input leakage current (all other)[7][8]	I_{OZ2} CC	–	±10	±30	µA	$T_J \leq$ 150°C, 0.45 V < V_{IN} < V_{DDP}
Level inactive hold current	I_{LHI}	–	–	-30	µA	$V_{OUT} \geq V_{IHmin}$
Level active hold current	I_{LHA}	-220	–	–	µA	$V_{OUT} \leq V_{ILmax}$

Table 12 DC Characteristics for 4.5 V ≤ V_{DDP} ≤ 5.5 V (cont'd) **(Operating Conditions apply)**[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XTAL1 input current	I_{IL} CC	–	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[9] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Overload conditions must not occur on pin XTAL1.

3) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 11**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

8) The given values are worst-case values. In the production test, this leakage current value is only tested at 125°C, other values are ensured via correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.009 \times e^{(0.054 \times TJ)}$ [µA]. For example, at a temperature of 130°C the resulting leakage current is 10.07 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax} - (1.6 \times DV)$ [µA]
The shown voltage derating formula is an approximation which applies for maximum temperature.
Pin P2.8 is connected to two pads (additionally the high-speed clock pad), so it sees twice the normal leakage.

9) Not subject to production test - verified by design/characterization.
Pin P2.8 is connected to two pads (additionally the high-speed clock pad), so it sees twice the normal capacitance.

4.2.2 DC Parameters for Lower Voltage Area

These parameters apply to the lower IO voltage area of 3.0 V ≤ V_{DDP} ≤ 4.5 V.

Table 13 DC Characteristics for 3.0 V ≤ V_{DDP} ≤ 4.5 V (Operating Conditions apply)[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage (all except XTAL1)	V_{IL} SR	-0.3	–	0.3 × V_{DDP}	V	–
Input low voltage for XTAL1	V_{ILC} SR	-1.7 + V_{DDI}	–	0.3 × V_{DDI}	V	–
Input high voltage (all except XTAL1)	V_{IH} SR	0.7 × V_{DDP}	–	V_{DDP} + 0.3	V	–
Input high voltage for XTAL1	V_{IHC} SR	0.7 × V_{DDI}	–	1.7	V	[2]
Input Hysteresis[3]	HYS CC	0.11 × V_{DDP}	–	–	V	V_{DD} in [V], Series resistance = 0 Ω
Output low voltage	V_{OL} CC	–	–	1.0	V	$I_{OL} \leq I_{OLmax}$[4]
Output low voltage	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$[4] [5]
Output high voltage[6]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$[4]
Output high voltage[6]	V_{OH} CC	V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$[4] [5]
Input leakage current (Port 5, Port 15)[7]	I_{OZ1} CC	–	±100	–	nA	0 V < V_{IN} < V_{DDP}
Input leakage current (all other)[7][8]	I_{OZ2} CC	–	±1	±2.5	µA	$T_J \leq$ 110°C, 0.45 V < V_{IN} < V_{DDP}
Input leakage current (all other)[7][8]	I_{OZ2} CC	–	±5	±15	µA	$T_J \leq$ 150°C, 0.45 V < V_{IN} < V_{DDP}
Level inactive hold current	I_{LHI}	–	–	-10	µA	$V_{OUT} \geq V_{IHmin}$
Level active hold current	I_{LHA}	-150	–	–	µA	$V_{OUT} \leq V_{ILmax}$

Table 13 DC Characteristics for 3.0 V ≤ V_{DDP} ≤ 4.5 V (cont'd)
(Operating Conditions apply)[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XTAL1 input current	I_{IL} CC	–	–	±20	μA	0 V < V_{IN} < V_{DDI}
Pin capacitance[9] (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) Overload conditions must not occur on pin XTAL1.

3) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

4) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 11**, **Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are verified.

6) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

7) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.
The leakage current value is not tested in the lower voltage range, but only in the upper voltage range. This parameter is ensured via correlation.

8) The given values are worst-case values. In the production test, this leakage current value is only tested at 125°C, other values are ensured via correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.005 \times e^{(0.054 \times TJ)}$ [μA]. For example, at a temperature of 130°C the resulting leakage current is 5.6 μA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax} - (1.3 \times DV)$ [μA]
The shown voltage derating formula is an approximation which applies for maximum temperature.
Pin P2.8 is connected to two pads (additionally the high-speed clock pad), so it sees twice the normal leakage.

9) Not subject to production test - verified by design/characterization.
Pin P2.8 is connected to two pads (additionally the high-speed clock pad), so it sees twice the normal capacitance.

4.2.3 Power Consumption

The amount of power that is consumed by the XC236x depends on several factors, such as supply voltage, operating frequency, amount of active circuitry, and operating temperature. Part of this depends on the device's activity (switching current), part of this is independent (leakage current). Therefore, the leakage current must be added to all other (frequency-dependent) parameters.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Table 14 Power Consumption XC236x (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current caused by leakage[1] (DMP_1 powered)	I_{DDL}	–	600,000 $\times$ e$^{-\alpha}$	tbd	mA	$V_{DDP} = V_{DDPmax}$[2] α = 5000 / (273 + T_J), T_J in [°C]
Supply current caused by leakage[1] (DMP_1 off)	I_{DDL}	–	500,000 $\times$ e$^{-\alpha}$	tbd	µA	$V_{DDP} = V_{DDPmax}$[2] α = 3000 / (273 + T_J), T_J in [°C]
Power supply current (active) with all peripherals active and EVVRs on	I_{DDP}	–	10 + 0.6$\times f_{SYS}$	tbd	mA	Active Mode[3] f_{SYS}in [MHz]

1) The supply current caused by leakage mainly depends on the junction temperature (see **Figure 12**) and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on the device's activity, it must be added to each other power consumption parameter.

2) All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP}, all outputs (including pins configured as outputs) disconnected. This parameter is tested at 25 °C and is valid for $T_J \geq 25$ °C.

3) The pad supply voltage pins (V_{DDP}) provide the input current for the on-chip EVVRs and the current consumed by the pin output drivers. A small amount of current is consumed because the drivers' input stages are switched.

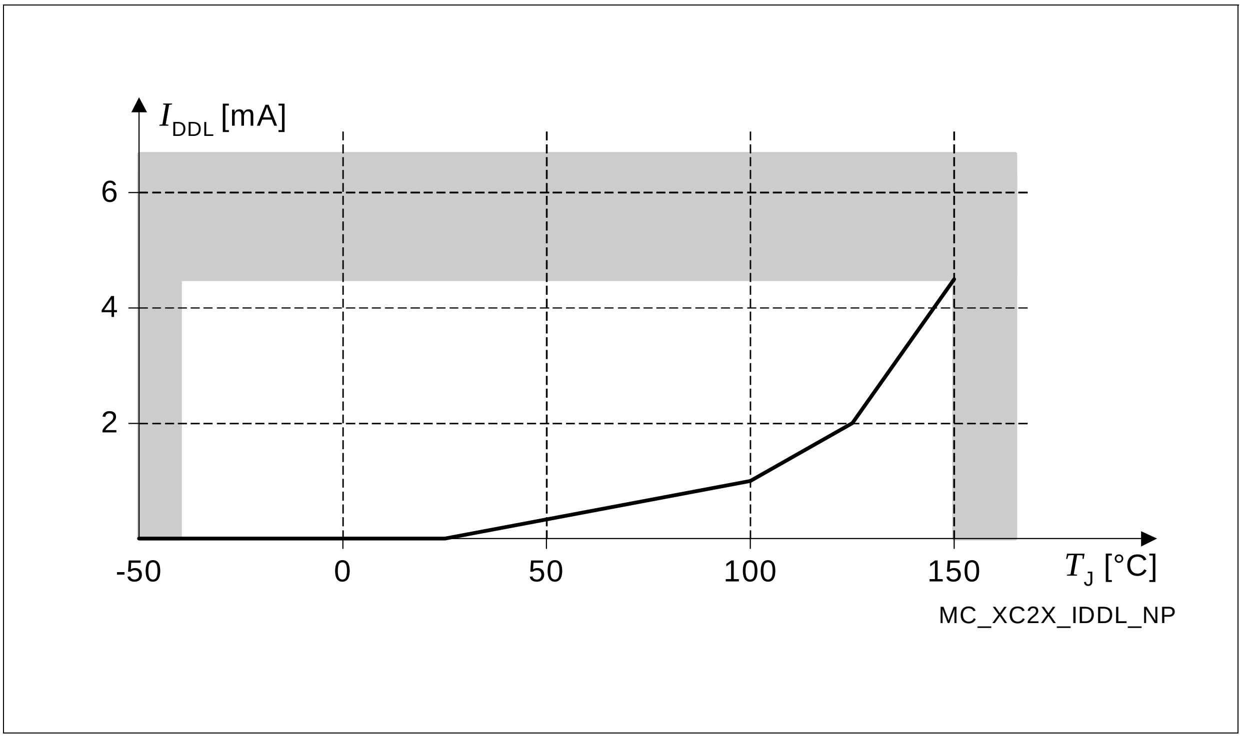


Figure 12 Leakage Supply Current as a Function of Temperature

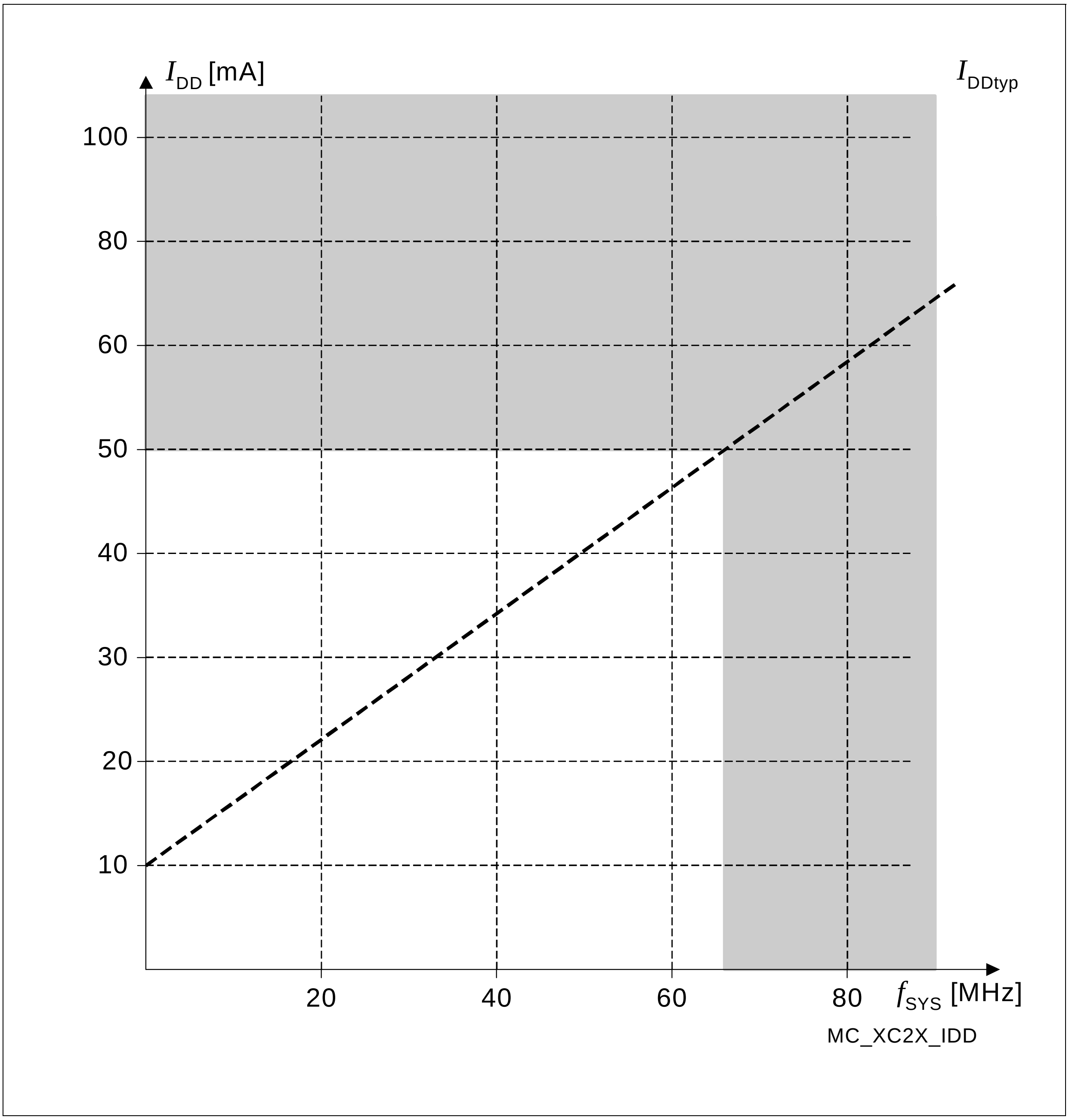


Figure 13 Supply Current in Active Mode as a Function of Frequency

4.3 Analog/Digital Converter Parameters

These parameters describe how the optimum ADC performance can be reached.

Table 15 A/D Converter Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		Min.	Max.		
Analog reference supply	V_{AREF} SR	V_{AGND} + 1.0	V_{DDPA} + 0.05	V	[1]
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	V_{AREF} - 1.0	V	–
Analog input voltage range	V_{AIN} SR	V_{AGND}	V_{AREF}	V	[2]
Basic clock frequency	f_{ADCI}	0.5	16.5	MHz	[3]
Conversion time for 10-bit result[4]	t_{C10} CC	(17 + STC) × t_{ADCI}		–	–
Conversion time for 8-bit result[4]	t_{C8} CC	(15 + STC) × t_{ADCI}		–	–
Total unadjusted error	TUE CC	–	±2	LSB	[1]
Total capacitance of an analog input	C_{AINT} CC	–	15	pF	[5]
Switched capacitance of an analog input	C_{AINS} CC	–	7	pF	[5]
Resistance of the analog input path	R_{AIN} CC	–	1.5	kΩ	[5]
Total capacitance of the reference input	C_{AREFT} CC	–	20	pF	[5]
Switched capacitance of the reference input	C_{AREFS} CC	–	20	pF	[5]
Resistance of the reference input path	R_{AREF} CC	–	2	kΩ	[5]

1) TUE is tested at $V_{\text{AREFx}} = V_{\text{DDPA}}$, $V_{\text{AGND}} = 0$ V. It is verified by design for all other voltages within the defined voltage range.
The specified TUE is valid only, if the absolute sum of input overload currents on Port 5 or Port 15 pins (see I_{OV} specification) does not exceed 10 mA, and if V_{AREF} and V_{AGND} remain stable during the respective period of time.

2) V_{AIN} may exceed V_{AGND} or V_{AREFx} up to the absolute maximum ratings. However, the conversion result in these cases will be X000$_{\text{H}}$ or X3FF$_{\text{H}}$, respectively.

3) The limit values for f_{ADCI} must not be exceeded when selecting the peripheral frequency and the prescaler setting.

4) This parameter includes the sample time (also the additional sample time specified by STC), the time for determining the digital result and the time to load the result register with the conversion result.
Values for the basic clock t_{ADCI} depend on programming and can be taken from **Table 16**.

5) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
C_{AINTtyp} = 12 pF, C_{AINStyp} = 5 pF, R_{AINtyp} = 1.0 kΩ, C_{AREFTtyp} = 15 pF, C_{AREFStyp} = 10 pF, R_{AREFtyp} = 1.0 kΩ.

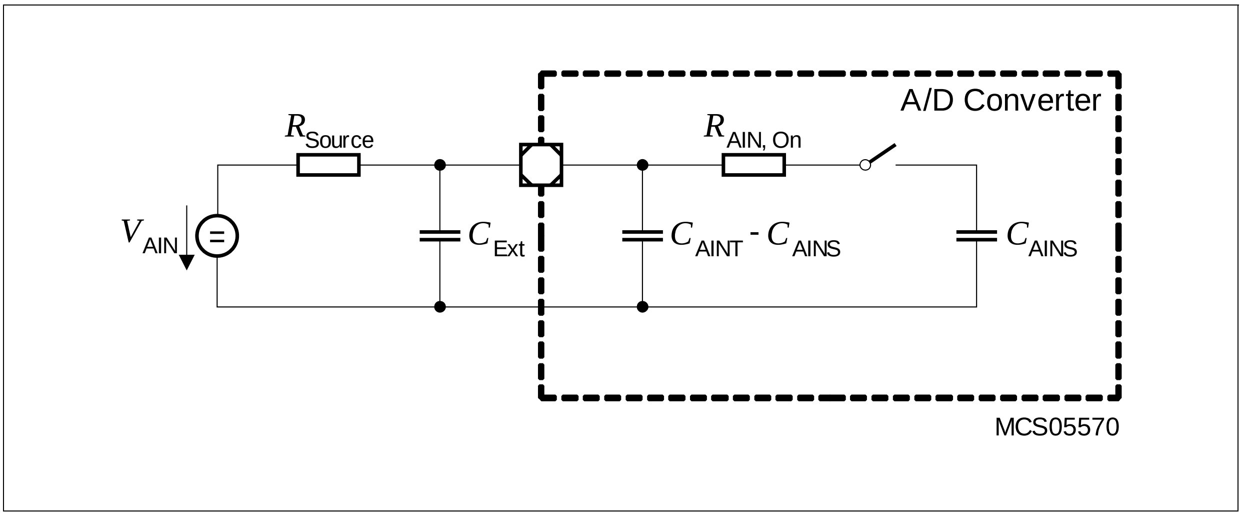


Figure 14 Equivalent Circuitry for Analog Inputs

Sample time and conversion time of the XC236x's A/D Converters are programmable. The above timing can be calculated using **Table 16**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 16 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	**A/D Converter Basic Clock f_{ADCI}**	**INPCRx.7-0 (STC)**	**Sample Time t_S**
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	$f_{SYS} / 2$	01_H	$t_{ADCI} \times 3$
000010_B	$f_{SYS} / 3$	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	$f_{SYS} / 63$	FE_H	$t_{ADCI} \times 256$
111111_B	$f_{SYS} / 64$	FF_H	$t_{ADCI} \times 257$

Converter Timing Example:

Assumptions: f_{SYS} = 66 MHz (i.e. t_{SYS} = 15.2 ns), DIVA = 03_H, STC = 00_H

Basic clock f_{ADCI} = f_{SYS} / 4 = 16.5 MHz, i.e. t_{ADCI} = 60.6 ns

Sample time t_S = $t_{ADCI} \times 2$ = 121 ns

Conversion 10-bit:

$t_{C10} = 17 \times t_{ADCI} = 17 \times 60.6\text{ ns} = 1.03\ \mu\text{s}$

Conversion 8-bit:

$t_{C8} = 15 \times t_{ADCI} = 15 \times 60.6\text{ ns} = 0.91\ \mu\text{s}$

Converter Timing Example:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H

Basic clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns

Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

$t_{C10} = 20 \times t_{ADCI} = 20 \times 75\text{ ns} = 1.5\ \mu\text{s}$

Conversion 8-bit:

$t_{C8} = 18 \times t_{ADCI} = 18 \times 75\text{ ns} = 1.35\ \mu\text{s}$

4.4 AC Parameters

These parameters describe the dynamic behavior of the XC236x.

4.4.1 Definition of Internal Timing

The internal operation of the XC236x is controlled by the internal system clock f_{SYS}.

Because the system clock signal f_{SYS} can be generated from several internal and external sources via different mechanisms, the duration of system clock periods (TCSs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{SYS}. This influence must be regarded when calculating the timings for the XC236x.

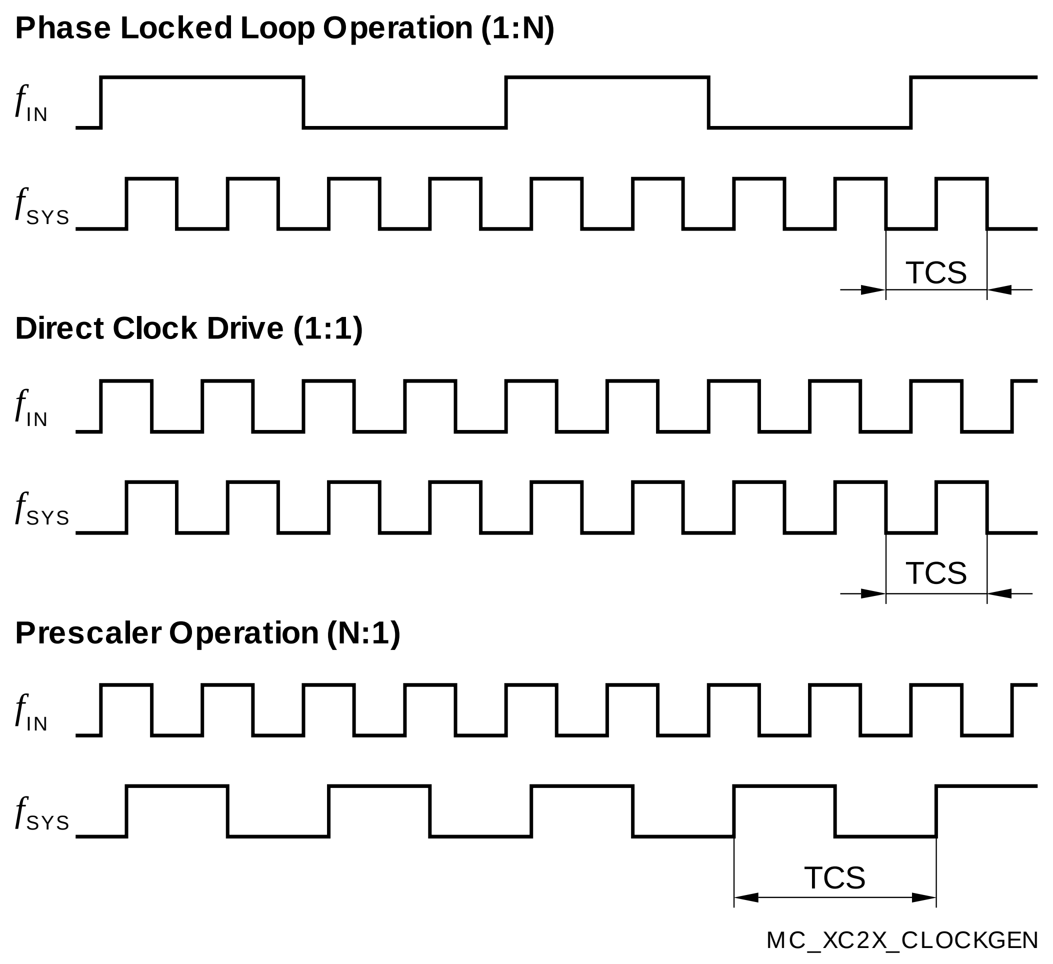


Figure 15 Generation Mechanisms for the System Clock

*Note: The example for PLL operation shown in **Figure 15** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The specification of the external timing (AC Characteristics) depends on the period of the system clock (TCS).

Direct Drive

When direct drive operation is configured (SYSCON0.CLKSEL = 11_B), the system clock is derived directly from the input clock signal DIRIN:

$f_{SYS} = f_{IN}$.

The frequency of f_{SYS} directly follows the frequency of f_{IN}. In this case, the high and low time of f_{SYS} is defined by the duty cycle of the input clock f_{IN}.

A similar configuration can be achieved by selecting the XTAL1[1] input.

Prescaler Operation

When prescaler operation is configured (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 1_B), the system clock is derived either from the crystal oscillator (input clock signal XTAL1) or from the internal clock source through the output-prescaler:

$f_{SYS} = f_{OSC}$ / (K1DIV + 1).

If the divider factor is selected as 1, the frequency of f_{SYS} directly follows the frequency of f_{OSC}. In this case, the high and low time of f_{SYS} is defined by the duty cycle of the input clock f_{OSC} (external or internal).

The lowest system clock frequency can be achieved in this mode by selecting the maximum value for divider factor K1:

$f_{SYS} = f_{OSC}$ / 1024.

Phase Locked Loop (PLL)

When PLL operation is configured (SYSCON0.CLKSEL = 10_B, PLLCON0.VCOBY = 0_B), the on-chip phase locked loop provides the system clock. The PLL multiplies the selected input frequency by the factor **F** ($f_{SYS} = f_{IN} \times$ **F**), which results from the input divider (P), the multiplication factor (N), and the output divider (K2): (**F** = N+1 / (P+1 × K2+1)).

The input clock can be derived either from an external source via XTAL1 or from the on-chip clock source.

The PLL circuit synchronizes the system clock to the input clock. This synchronization is done smoothly, i.e. the system clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{SYS} is constantly adjusted so it is locked to f_{IN}. The slight variation causes a jitter of f_{SYS} which also affects the duration of individual TCSs.

---

1) Voltages on XTAL1 must comply to the core supply voltage V_{DDI1}.

The timing listed in the AC Characteristics refers to TCSs. Therefore, the timing must be calculated using the minimum TCS possible under the respective circumstances.
The actual minimum value for TCS depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator), the accumulated jitter is limited, which means that the relative deviation for periods of more than one TCS is lower than for one single TCS.

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is, therefore, negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K2+1) to generate the system clock signal f_{SYS}. Therefore, the number of VCO cycles can be represented as (K2+1) × **T**, where **T** is the number of consecutive f_{SYS} cycles (TCS).

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 17 VCO Bands for PLL Operation[1]

PLLCON0.VCOSEL	VCO Frequency Range	Base Frequency Range
00	40 … 120 MHz	10 … 40 MHz
01	90 … 160 MHz	20 … 80 MHz
1X	Reserved	

1) Not subject to production test - verified by design/characterization.

Wakeup Clock

When wakeup operation is configured (SYSCON0.CLKSEL = 00_B), the system clock is derived from the low-frequency wakeup clock source:

$f_{SYS} = f_{WU}$.

In this mode, a basic functionality can be maintained without requiring an external clock source and while minimizing the power consumption.

Selecting and Changing the Operating Frequency

When selecting a clock source and the clock generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states.

Many applications change the frequency of the system clock (f_{SYS}) during the operation, to optimize performance and power consumption of the system. Changing the operating frequency also changes the consumed switching current, which influences the power supply. Therefore, while the core voltage is generated by the on-chip EVRs, the operating frequency may only be changed by factors of 5 maximum, or in steps of 20 MHz maximum, whatever condition is tighter.

To avoid the indicated problems, recommended sequences are provided which ensure the intended operation of the clock system interacting with the power system.

4.4.2 On-chip Flash Operation

Accesses to the XC236x's Flash modules are controlled by the IMB.

Built-in prefetching mechanisms optimize the performance for sequential accesses.

Table 18 Flash Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit
			Min.	Typ.	Max.	
Programming time per 128-byte page	t_{PR}	CC	–	3[1]	tbd	ms
Erase time per sector/page	t_{ER}	CC	–	4[1]	tbd	ms

[1] Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles, which only becomes relevant for extremely low system frequencies.

4.4.3 External Clock Drive

These parameters define the external clock supply for the XC236x. The clock signal can be supplied either to pin P2.9 or to pin XTAL1.

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1]	ns
High time[2]	t_1	SR	6	–	ns
Low time[2]	t_2	SR	6	–	ns
Rise time[2]	t_3	SR	–	8	ns
Fall time[2]	t_4	SR	–	8	ns

[1] The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

[2] The clock input signal must reach the defined levels V_{ILC} and V_{IHC} (for XTAL1) or V_{IL} and V_{IH} for P2.9.

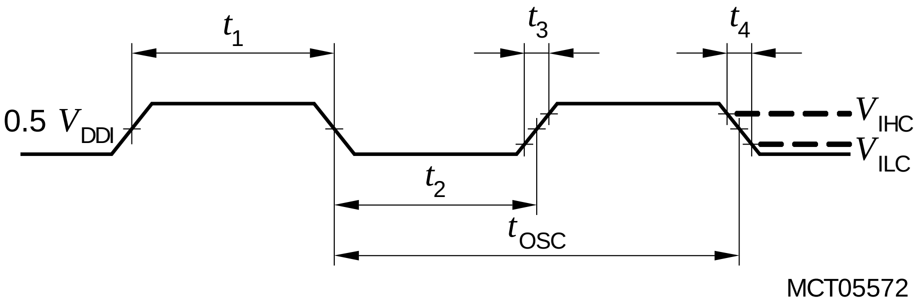
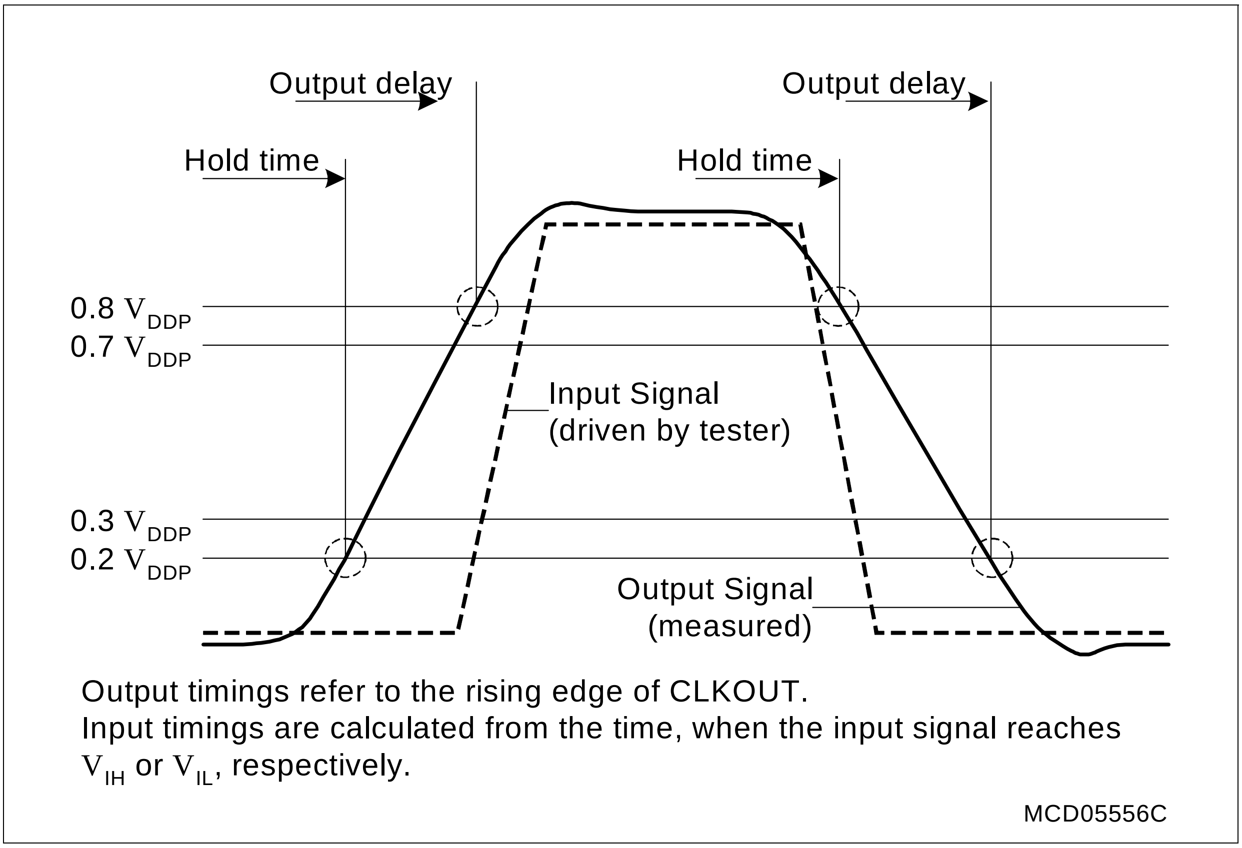


Figure 16 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified input frequency range. Operation at input frequencies below 4 MHz is possible but is verified by design only (not subject to production test).

4.4.4 Testing Waveforms

These references are used for characterization and production testing (except for pin XTAL1).



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

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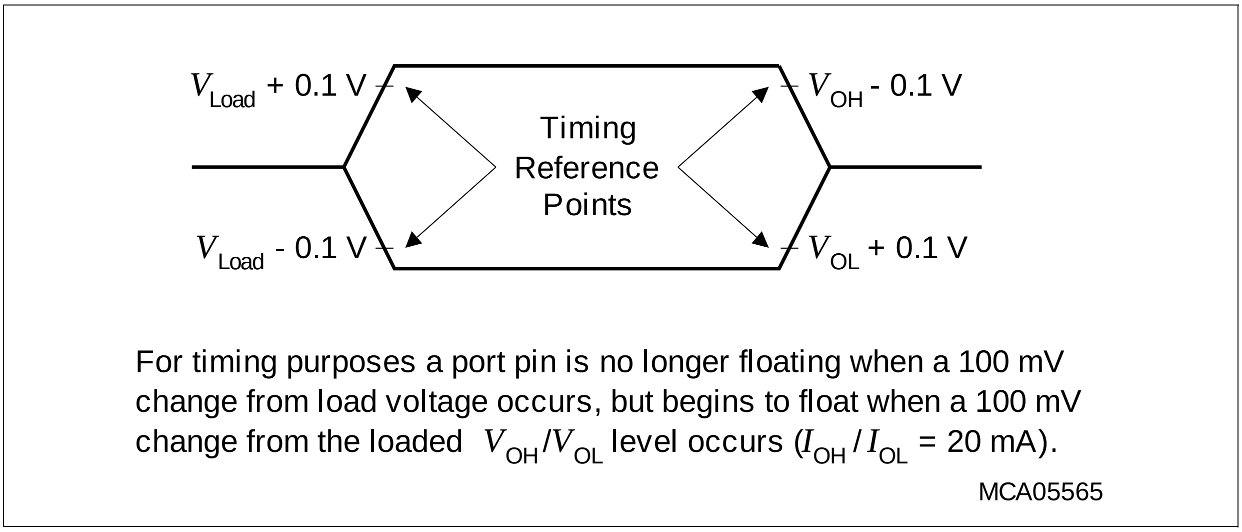
Figure 17 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH} / I_{OL} = 20 mA).

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Figure 18 Float Waveforms

4.4.5 External Bus Timing

The following parameters define the behavior of the XC236x's bus interface.

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/25/15[1]		ns
CLKOUT high time	tc_6	CC	3	–	ns
CLKOUT low time	tc_7	CC	3	–	ns
CLKOUT rise time	tc_8	CC	–	3	ns
CLKOUT fall time	tc_9	CC	–	3	ns

[1] The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/40/66 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

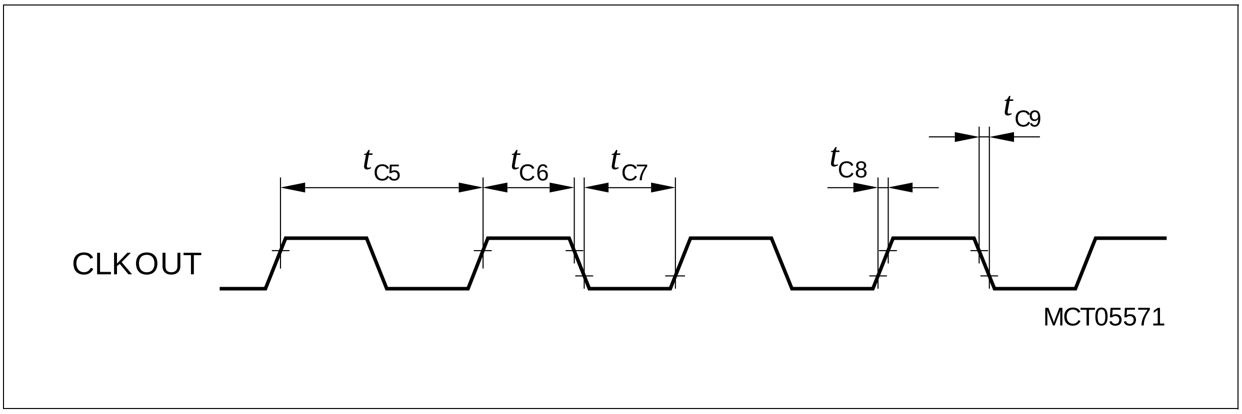

Figure 19 CLKOUT Signal Timing

Note: The term CLKOUT refers to the reference clock output signal which is generated by selecting f_{SYS} as source signal for the clock output signal EXTCLK on pin P2.8 and by enabling the high-speed clock driver on this pin.

Variable Memory Cycles

External bus cycles of the XC236x are executed in five subsequent cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module via the READY handshake input.

This table provides a summary of the phases and the respective choices for their duration.

Table 21 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed	tpAB	1 … 2 (5)	TCS
Command delay phase	tpC	0 … 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 … 1	TCS
Access phase	tpE	1 … 32	TCS
Address/Write Data hold phase	tpF	0 … 3	TCS

Note: The bandwidth of a parameter (minimum and maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Timing values are listed in **Table 22** and **Table 23**. The shaded parameters have been verified by characterization. They are not subject to production test.

Table 22 External Bus Cycle Timing for 4.5 V ≤ V_{DDP} ≤ 5.5 V (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: $\overline{\text{RD}}$, $\overline{\text{WR}}$($\overline{\text{L}}$/$\overline{\text{H}}$)	tc_{10} CC	–		13	ns	
Output valid delay for: $\overline{\text{BHE}}$, ALE	tc_{11} CC	–		13	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	tc_{12} CC	–		14	ns	
Output valid delay for: A15 … A0 (on P2/P10)	tc_{13} CC	–		14	ns	
Output valid delay for: $\overline{\text{CS}}$	tc_{14} CC	–		13	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15} CC	–		14	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16} CC	–		14	ns	
Output hold time for: $\overline{\text{RD}}$, $\overline{\text{WR}}$($\overline{\text{L}}$/$\overline{\text{H}}$)	tc_{20} CC	0		8	ns	
Output hold time for: $\overline{\text{BHE}}$, ALE	tc_{21} CC	0		8	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	tc_{23} CC	0		8	ns	
Output hold time for: $\overline{\text{CS}}$	tc_{24} CC	0		8	ns	
Output hold time for: D15 … D0 (write data)	tc_{25} CC	0		8	ns	
Input setup time for: READY, D15 … D0 (read data)	tc_{30} SR	18		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1]	tc_{31} SR	-4		–	ns	

---

[1] Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of $\overline{\text{RD}}$. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of $\overline{\text{RD}}$.

Table 23 External Bus Cycle Timing for 3.0 V ≤ V_{DDP} ≤ 4.5 V (Operating Conditions apply)

Parameter	Symbol	Limits			Unit	Note
		Min.	Typ.	Max.		
Output valid delay for: $\overline{\text{RD}}$, $\overline{\text{WR}}$($\overline{\text{L}}$/$\overline{\text{H}}$)	tc_{10} CC	–		20	ns	
Output valid delay for: $\overline{\text{BHE}}$, ALE	tc_{11} CC	–		20	ns	
Output valid delay for: A23 … A16, A15 … A0 (on P0/P1)	tc_{12} CC	–		22	ns	
Output valid delay for: A15 … A0 (on P2/P10)	tc_{13} CC	–		22	ns	
Output valid delay for: $\overline{\text{CS}}$	tc_{14} CC	–		20	ns	
Output valid delay for: D15 … D0 (write data, MUX-mode)	tc_{15} CC	–		21	ns	
Output valid delay for: D15 … D0 (write data, DEMUX-mode)	tc_{16} CC	–		21	ns	
Output hold time for: $\overline{\text{RD}}$, $\overline{\text{WR}}$($\overline{\text{L}}$/$\overline{\text{H}}$)	tc_{20} CC	0		10	ns	
Output hold time for: $\overline{\text{BHE}}$, ALE	tc_{21} CC	0		10	ns	
Output hold time for: A23 … A16, A15 … A0 (on P2/P10)	tc_{23} CC	0		10	ns	
Output hold time for: $\overline{\text{CS}}$	tc_{24} CC	0		10	ns	
Output hold time for: D15 … D0 (write data)	tc_{25} CC	0		10	ns	
Input setup time for: READY, D15 … D0 (read data)	tc_{30} SR	29		–	ns	
Input hold time for: READY, D15 … D0 (read data)[1]	tc_{31} SR	-6		–	ns	

[1] Read data are latched with the same (internal) clock edge that triggers the address change and the rising edge of $\overline{\text{RD}}$. Therefore address changes before the end of $\overline{\text{RD}}$ have no impact on (demultiplexed) read cycles. Read data can be removed after the rising edge of $\overline{\text{RD}}$.

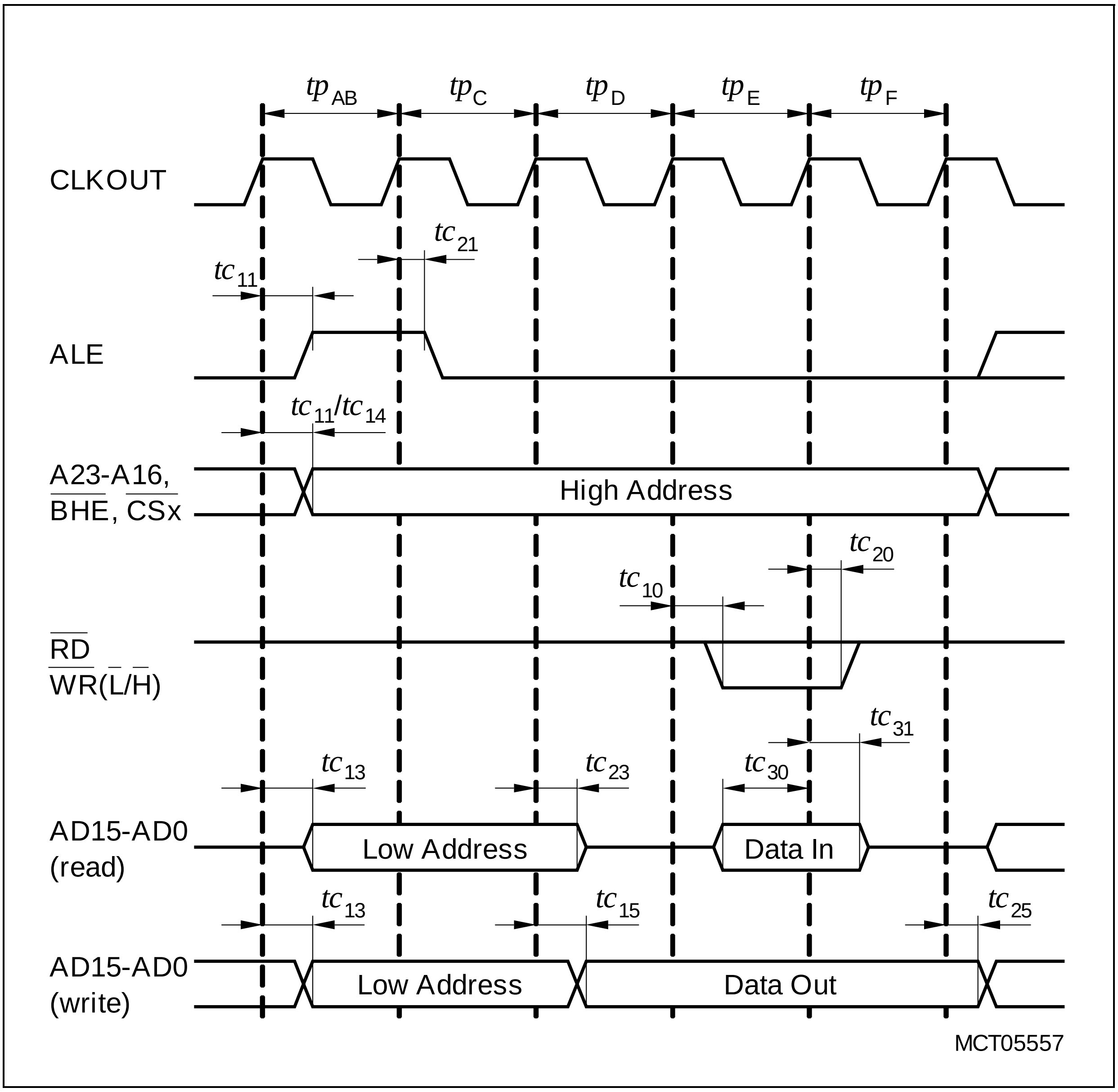

Figure 20 Multiplexed Bus Cycle

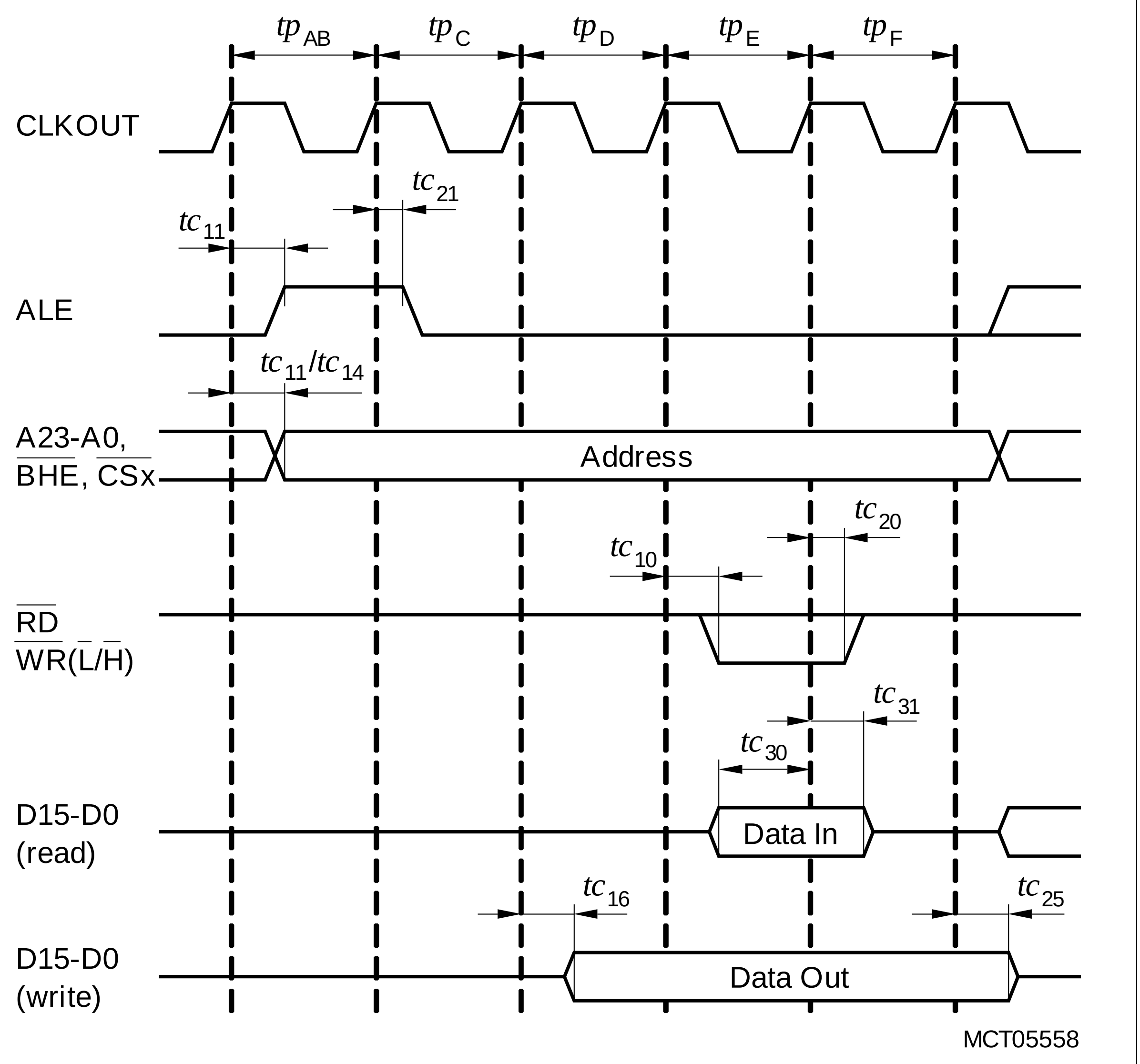

Figure 21 Demultiplexed Bus Cycle

Bus Cycle Control via READY Input

The duration of an external bus cycle can be controlled by the external circuitry via the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous READY puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage. The minimum duration of an asynchronous READY signal to be safely synchronized must be one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).

If the next following bus cycle is READY-controlled, an active READY signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the programmed phases of the next following cycle.

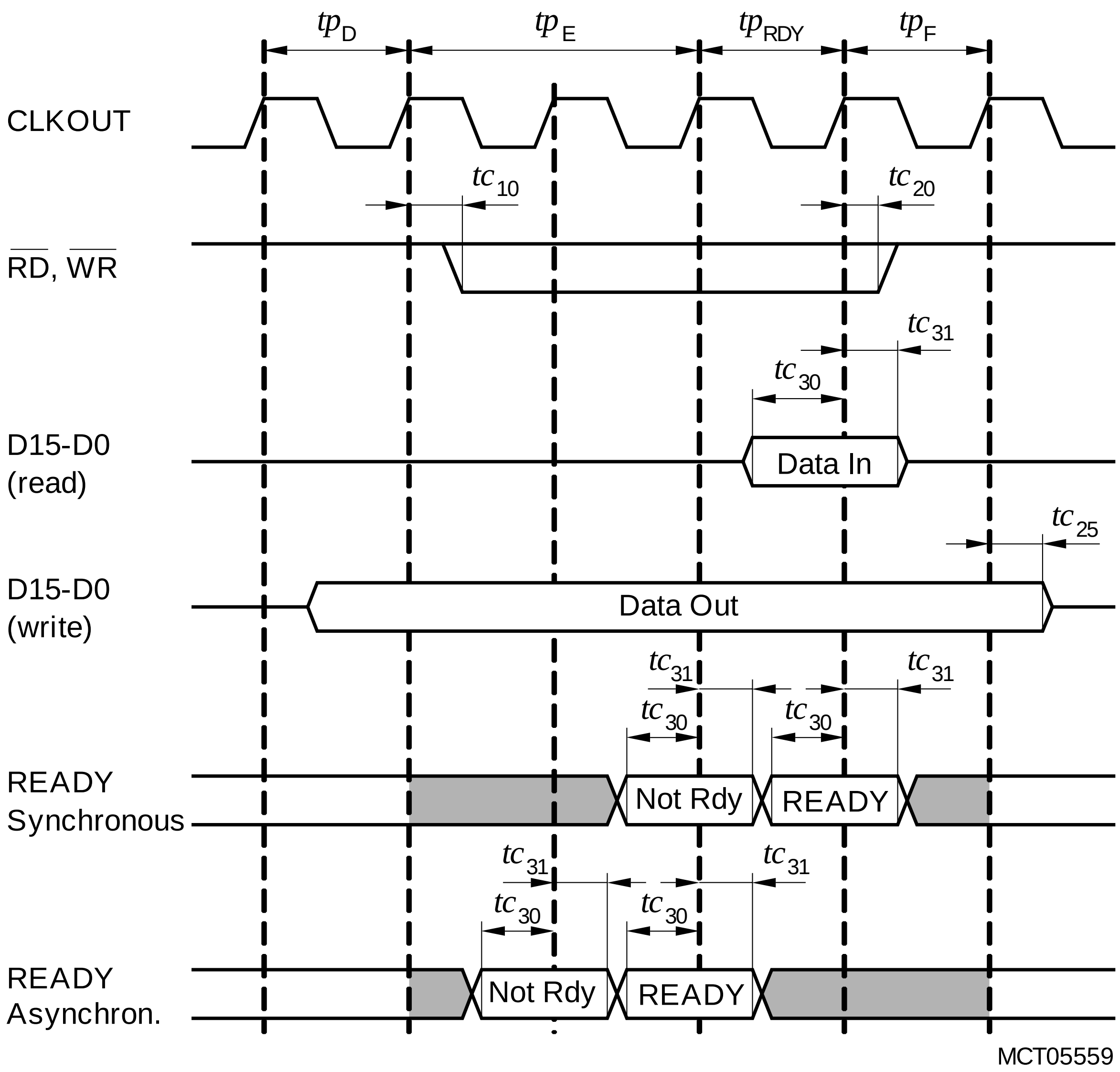

Figure 22 READY Timing

Note: *If the READY input is sampled inactive at the indicated sampling point ("Not Rdy") a READY-controlled waitstate is inserted (tpRDY),*
sampling the READY input active at the indicated sampling point ("Ready") terminates the currently running bus cycle.
Note the different sampling points for synchronous and asynchronous READY.
This example uses one mandatory waitstate (see tpE) before the READY input is evaluated.

5 Package and Reliability

In addition to the electrical parameters, the following information ensures proper integration of the XC236x into the target system.

5.1 Packaging

These parameters describe the housing rather than the silicon.

Table 24 Package Parameters (PG-LQFP-100)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Exposed Pad Dimension	Ex × Ey	–	6.2 × 6.2	mm	–
Power Dissipation	P_{DISS}	–	1.0	W	–
Thermal resistance Junction-Ambient	$R_{\Theta\text{JA}}$	–	49	K/W	No thermal via[1]
			37	K/W	4-layer, no pad[2]
			22	K/W	4-layer, pad[3]

1) Device mounted on a 2-layer or 4-layer board without thermal vias.

2) Device mounted on a 4-layer board with thermal vias, exposed pad not soldered.

3) Device mounted on a 4-layer board with thermal vias, exposed pad soldered to the board.

Package Outlines

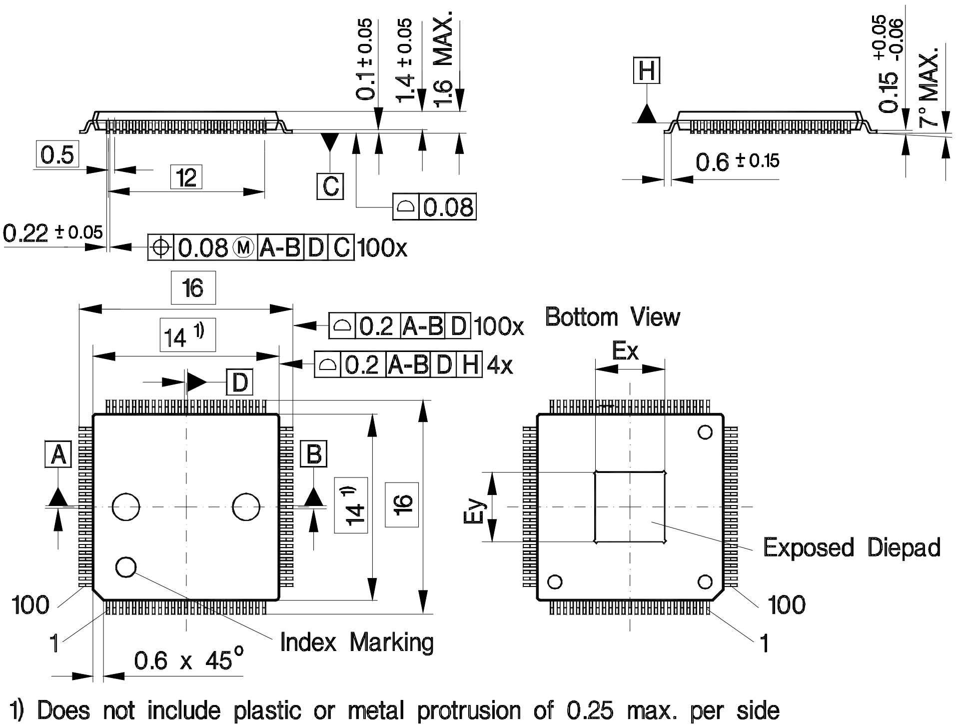

Figure 23 **PG-LQFP-100** (Plastic Green Thin Quad Flat Package)

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Dimensions in mm.

5.2 Thermal Considerations

When operating the XC236x in a system, the total heat generated on the chip must be dissipated to the ambient environment to prevent overheating and resulting thermal damages.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” is a measure for these parameters. The power dissipation must be limited so the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (see **Table 14**).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and the switching frequencies.

If the total power dissipation determined for a given system configuration exceeds the defined limit countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

5.3 Flash Memory Parameters

The data retention time of the XC236x's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 25 Flash Parameters (XC236x, 768 Kbytes)

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Data retention time	t_{RET}	20	–	years	10^3 erase/program cycles
Flash Erase Endurance	N_{ER}	15×10^3	–	cycles	Data retention time 5 years

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