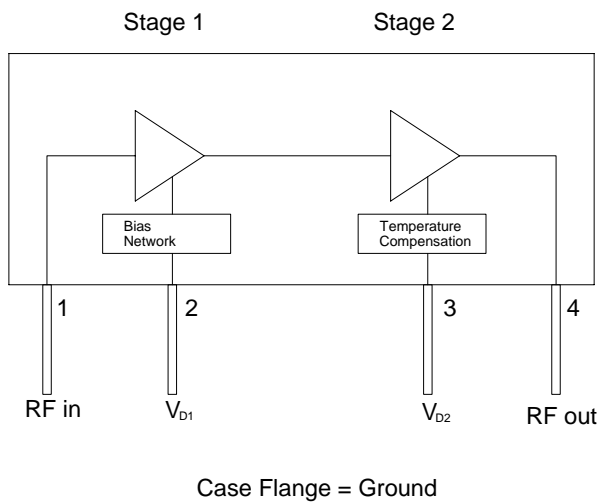




Product Description

Sirenza Microdevices' **XD010-04S-D4F** 12W power module is a robust broadband 2-stage Class A/AB amplifier, suitable for use as a power amplifier driver or output stage. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. It is a drop-in, no-tune, solution for high power applications requiring high efficiency, excellent linearity, and unit-to-unit repeatability. Internal bias current compensation ensures stable performance over a wide temperature range. It is internally matched to 50 ohms.

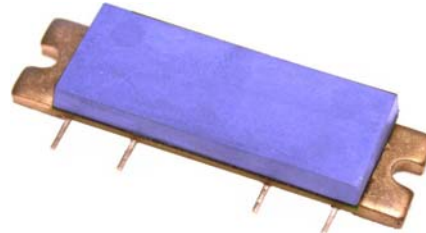
Functional Block Diagram



XD010-04S-D4F XD010-04S-D4FY



350-600 MHz Class AB 12W Power Amplifier Module



Product Features

- Available in RoHS compliant packaging
- 50 Ω RF impedance
- 12W Output P_{1dB}
- Single Supply Operation : Nominally 28V
- High Gain: 32 dB at 450 MHz
- High Efficiency: 30% at 450 MHz
- Robust 8000V ESD (HBM), Class 3B
- XeMOS II LDMOS FETS
- Temperature Compensation

Applications

- DTV
- Public Service
- Wireless Infrastructure
- Military Communications

Key Specifications

| Symbol | Parameter | Unit | Min. | Typ. | Max. |
|-----------------|--|---------------|------|------|------|
| Frequency | Frequency of Operation | MHz | 350 | - | 600 |
| P_{1dB} | Output Power at 1dB Compression, 450MHz | W | - | 12 | - |
| Gain | Gain at 10W Output Power, 450MHz | dB | 30 | 32 | - |
| Gain Flatness | Peak to Peak Gain Variation, 350 - 600MHz | dB | - | 1.0 | 2.0 |
| IRL | Input Return Loss 1W Output Power, 350 - 600MHz | dB | 10 | 15 | - |
| Efficiency | Drain Efficiency at 10W CW, 350-600MHz | % | 26 | 30 | - |
| Linearity | 3 rd Order IMD at 10W PEP (Two Tone), 450MHz & 451MHz | dBc | - | -32 | -28 |
| Delay | Signal Delay from Pin 1 to Pin 4 | nS | - | 2.5 | - |
| Phase Linearity | Deviation from Linear Phase (Peak to Peak) | Deg | - | 0.5 | - |
| Frequency | Frequency of Operation | MHz | 350 | - | 600 |
| $R_{TH, j1}$ | Thermal Resistance Stage 1 (Junction-to-Case) | $^{\circ}C/W$ | | 11 | |
| $R_{TH, j2}$ | Thermal Resistance Stage 2 (Junction-to-Case) | $^{\circ}C/W$ | | 4 | |

Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DQ1} = 230$ mA, $I_{DQ2} = 150$ mA, $T_{Flange} = 25^{\circ}C$

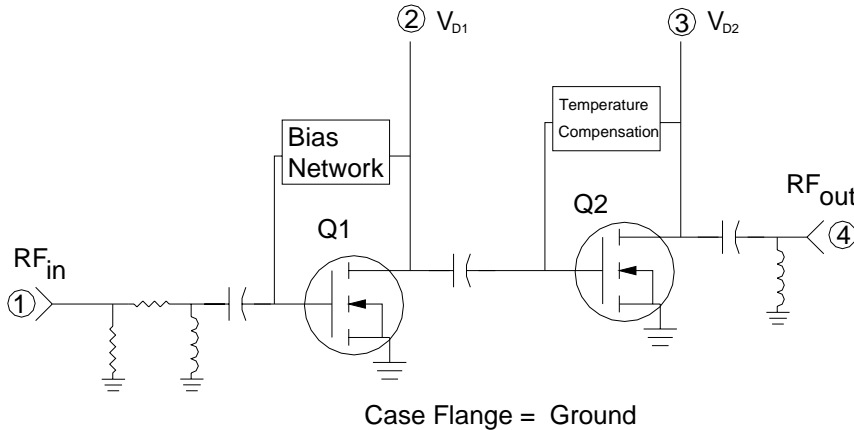
Quality Specifications

| Parameter | | Unit | Typical |
|------------|--|-------|-----------------------|
| ESD Rating | Human Body Model, JEDEC Document - JESD22-A114-B | V | 8000 |
| MTTF | 85°C Leadframe, 200°C Channel | Hours | 1.2 X 10 ⁶ |

Pin Description

| Pin # | Function | Description |
|--------|-----------------|--|
| 1 | RF Input | Module RF input. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices. |
| 2 | V _{D1} | This is the drain voltage for the first stage. Nominally +28Vdc |
| 3 | V _{D2} | This is the drain voltage for the 2 nd stage of the amplifier module. The 2 nd stage gate bias is temperature compensated to maintain constant quiescent drain current over the operating temperature range. See Note 1. |
| 4 | RF Output | Module RF output. This pin is internally connected to DC ground. Do not apply DC voltages to the RF leads. Care must be taken to protect against video transients that may damage the active devices. |
| Flange | Gnd | Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions in application note AN-060 on Sirenza's web site. |

Simplified Device Schematic



Absolute Maximum Ratings

| Parameters | Value | Unit |
|--|-------------|------|
| 1 st Stage Bias Voltage (V _{D1}) | 35 | V |
| 2 nd Stage Bias Voltage (V _{D2}) | 35 | V |
| RF Input Power | +20 | dBm |
| Load Impedance for Continuous Operation Without Damage | 5:1 | VSWR |
| Output Device Channel Temperature | +200 | °C |
| Operating Temperature Range | -20 to +90 | °C |
| Storage Temperature Range | -40 to +100 | °C |

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Note 1:

The internally generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be accomplished with AGC external to the module.

Note 2:

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

Note 3:

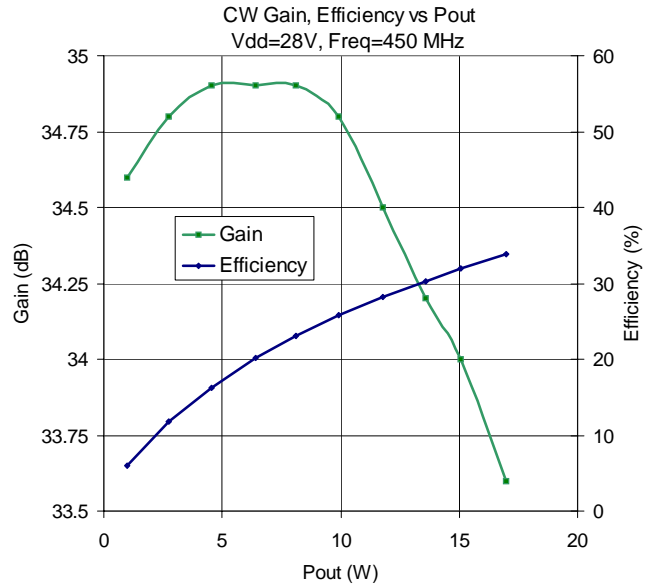
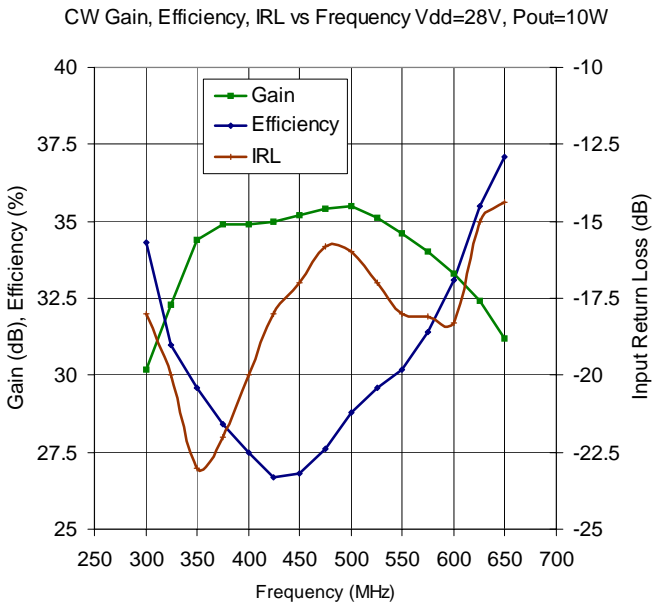
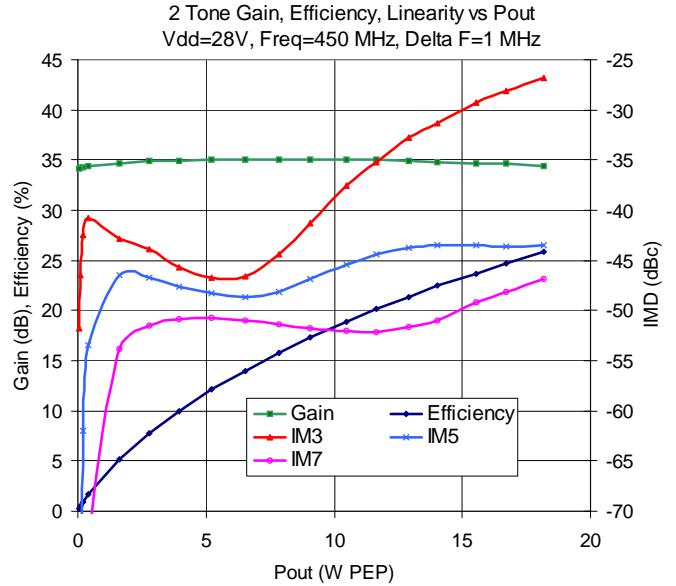
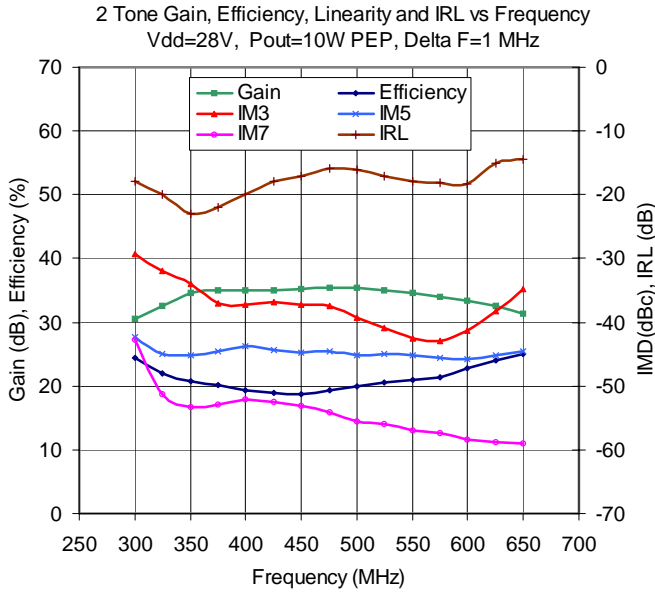
This module was designed to have its leads hand soldered to an adjacent PCB. The maximum soldering iron tip temperature should not exceed 700° F, and the soldering iron tip should not be in direct contact with the lead for longer than 10 seconds. Refer to app note AN060 (www.sirenza.com) for further installation instructions.



Caution: ESD Sensitive

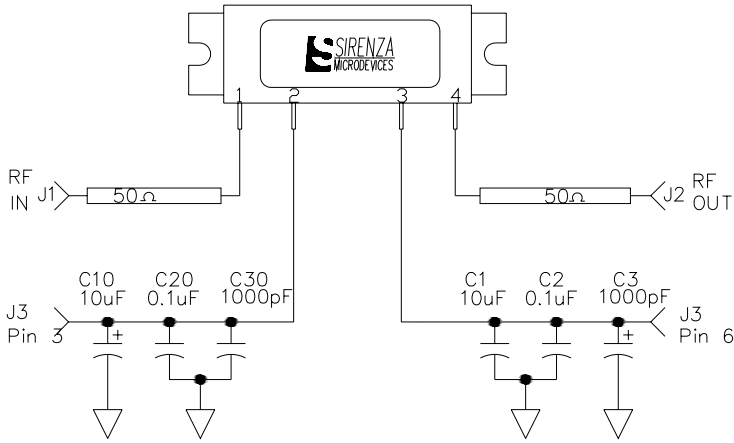
Appropriate precaution in handling, packaging and testing devices must be observed.

Typical Performance Curves



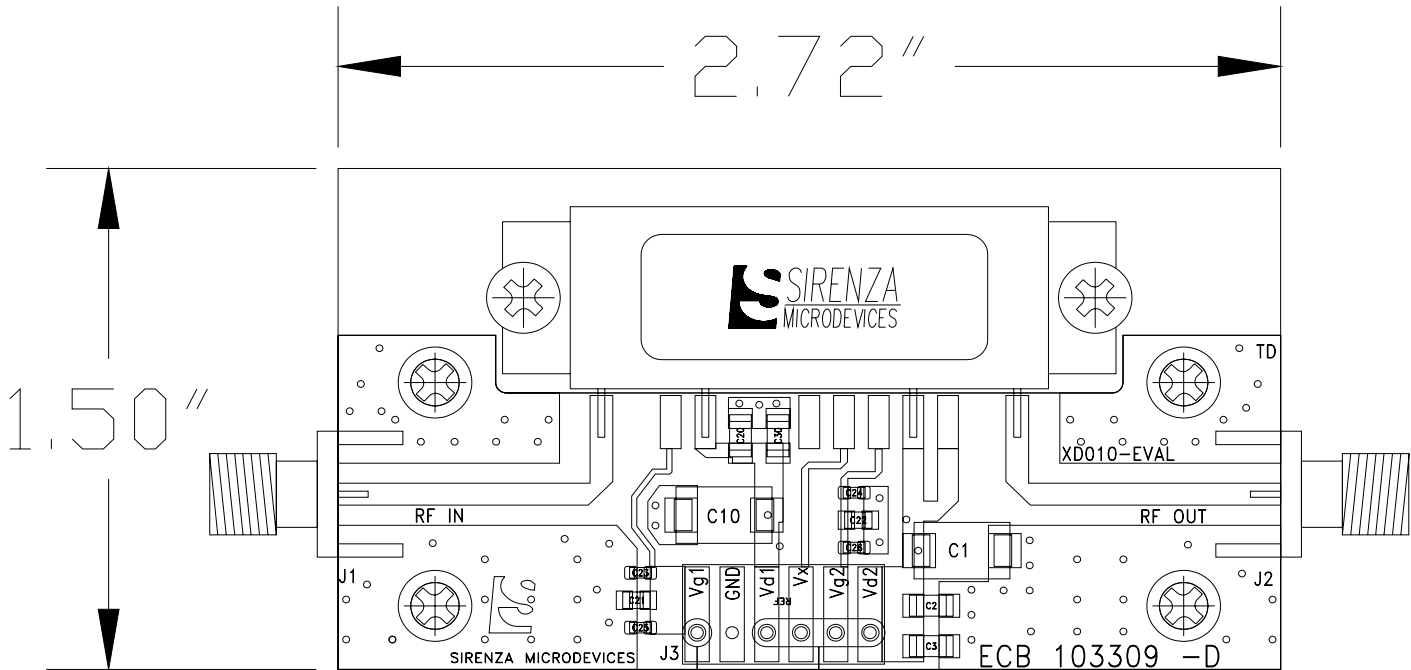
Test Board Schematic with module connections shown

Test Board Bill of Materials



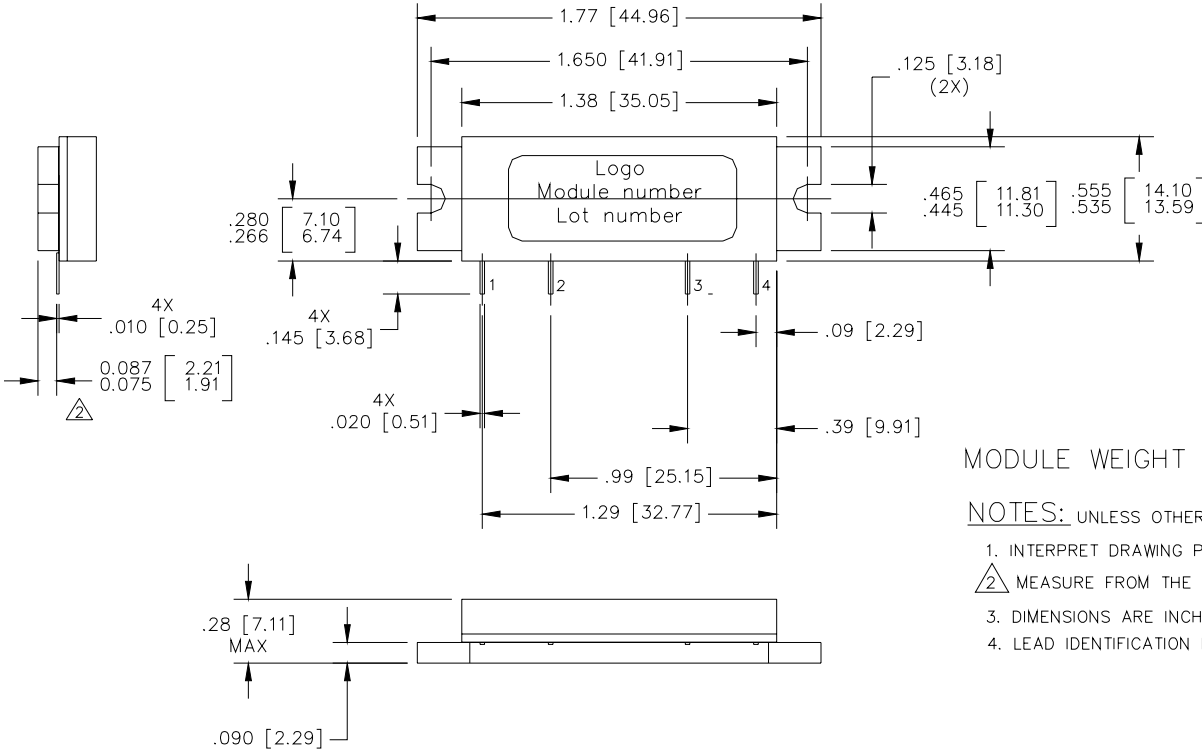
| Component | Description | Manufacturer |
|--------------------|---|--------------|
| PCB | Rogers 4350, $\epsilon_r=3.5$ Thickness=30mils | Rogers |
| J1, J2 | SMA, RF, Panel Mount Tab W / Flange | Johnson |
| J3 | MTA Post Header, 6 Pin, Rect- angle, Polarized, Surface Mount | AMP |
| C1, C10 | Cap, 10μF, 35V, 10%, Tant, Elect, D | Kemet |
| C2, C20 | Cap, 0.1μF, 100V, 10%, 1206 | Johanson |
| C3, C30 | Cap, 1000pF, 100V, 10%, 1206 | Johanson |
| C25, C26 | Cap, 68pF, 250V, 5%, 0603 | ATC |
| C21, C22 | Cap, 0.1μF, 100V, 10%, 0805 | Panasonic |
| C23, C24 | Cap, 1000pF, 100V, 10%, 0603 | AVX |
| Mounting Screws | 4-40 X 0.250" | Various |

Test Board Layout



To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com. Data sheet for evaluation circuit (XD010-EVAL) available from Sirenza website.

Package Outline Drawing

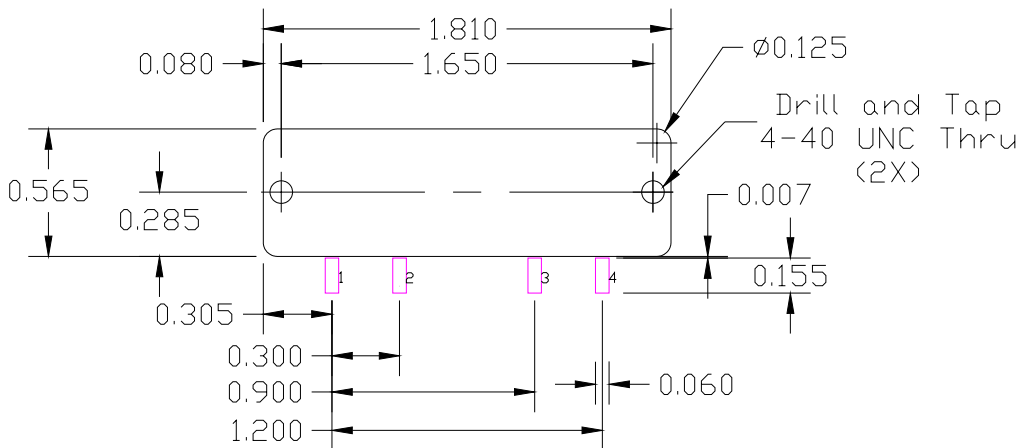


MODULE WEIGHT = 12gm Nominal

NOTES: UNLESS OTHERWISE SPECIFIED

1. INTERPRET DRAWING PER ANSI Y14.5.
2. MEASURE FROM THE BOTTOM OF THE LEADS.
3. DIMENSIONS ARE INCHES [MM].
4. LEAD IDENTIFICATION IS FOR REFERENCE ONLY.

Recommended PCB Cutout and Landing Pads for the D4F Package



Note 3: Dimensions are in inches

Refer to Application note AN-060 "Installation Instructions for XD Module Series" for additional mounting info. App note available at www.sirenza.com