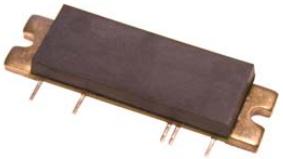
Preliminary

XD010-22S-D2F

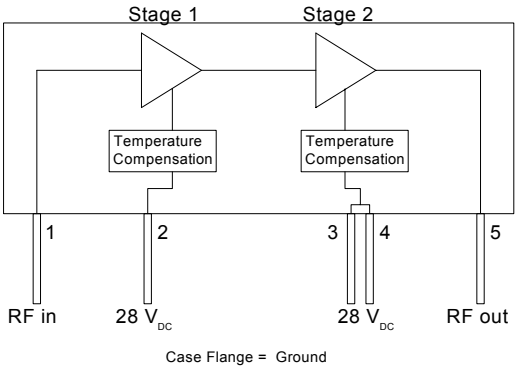
1805-1880 MHz Class A/AB 10W Power Amplifier Module



Product Description

The **XD010-22S-D2F** 10W power module is a 2-stage Class A/AB amplifier module for use in the driver stages of GSM/EDGE RF power amplifiers. The power transistors are fabricated using Sirenza's latest, high performance LDMOS process. The unit operates from a single voltage and has internal temperature compensation of the bias voltage to ensure consistant performance over temperature.

Functional Block Diagram



Product Features

- **50 Ω RF impedance**
- **12W Output P_{1dB}**
- **Single Voltage Operation**
- **High Gain: 30 dB Typical**
- **High Efficiency**
- **Advanced, XeMOS II LDMOS FETS**
- **Temperature Compensation**

Applications

- **Base Station PA driver**
- **Repeater**
- **GSM / EDGE**

Key Specifications

Parameter	Description: Test Conditions $Z_{in} = Z_{out} = 50\Omega$, $V_{DD} = 28.0V$, $I_{DD1} = 230mA$, $I_{DD2} = 115mA$, $T_{Flange} = 25°C$	Unit	Min.	Typ.	Max.
Frequency	Frequency of Operation	MHz	1805		1880
P_{1dB}	Output Power at 1dB Compression (single tone)	W		12	
Gain	Gain at 5W Output Power (CW)	dB		30	
Gain Flatness	Peak to Peak Gain Variation	dB		0.5	
IRL	Input Return Loss 5W Output (CW)	dB		14	
Efficiency	Drain Efficiency at 10W CW	%		25	
Linearity	RMS EVM at 5W EDGE output	%		1.5	
	Peak EVM at 5W EDGE output	%		5	
	3^{rd} Order IMD at 10W PEP (Two Tone; 1MHz ΔF)	dBc		-32	
Delay	Electrical Delay	nS		2.5	
Phase Linearity	Deviation from Linear Phase (Peak to Peak)	Deg		0.5	
$R_{TH, j-l}$	Thermal Resistance Stage 1 (Junction to Case)	°C/W		11	
$R_{TH, j-2}$	Thermal Resistance Stage 2 (Junction to Case)	°C/W		4	

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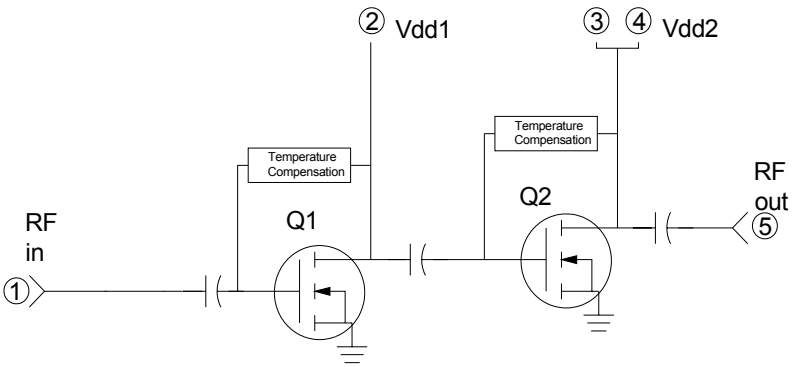
Pin Out Description

Pin #	Function	Description
1	RF Input	Module RF input. Care must be taken to protect against video transients that may damage the active devices.
2	V_{DD1}	This is the bias feed for the 1st stage of the amplifier module. The gate bias is temperature compensated to maintain constant current over the operating temperature range. See Note 1.
3,4	V_{DD2}	This is the bias feed for the 2nd stage of the amplifier module. The gate bias is temperature compensated to maintain constant current over the operating temperature range. See Note 1.
5	RF Output	Module RF output. Care must be taken to protect against video transients that may damage the active devices.
Flange	Gnd	Exposed area on the bottom side of the package needs to be mechanically attached to the ground plane of the board for optimum thermal and RF performance. See mounting instructions for recommendation.

Simplified Device Schematic



Case Flange = Ground

Absolute Maximum Ratings

Parameters	Value	Unit
1st Stage Bias Voltage (V_{DD1})	35	V
2nd Stage Bias Voltage (V_{DD2})	35	V
RF Input Power	+20	dBm
Load Impedance for Continuous Operation Without Damage	5:1	VSWR
Output Device Channel Temperature	200	°C
Lead Temperature During Solder Reflow	+210	°C
Operating Temperature Range	-20 to +90	°C
Storage Temperature Range	-40 to +100	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation see typical setup values specified in the table on page one.

Note 1:

The internal generated gate voltage is thermally compensated to maintain constant quiescent current over the temperature range listed in the data sheet. No compensation is provided for gain changes with temperature. This can only be provided with AGC external to the module.

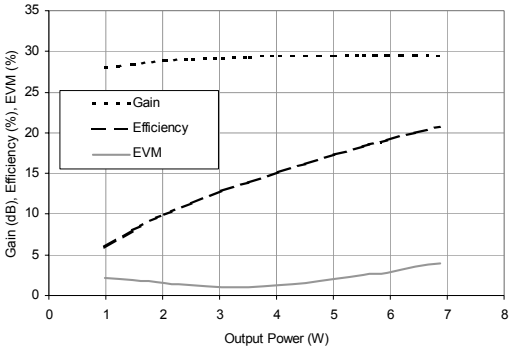
Note 2:

Internal RF decoupling is included on all bias leads. No additional bypass elements are required, however some applications may require energy storage on the drain leads to accommodate time-varying waveforms.

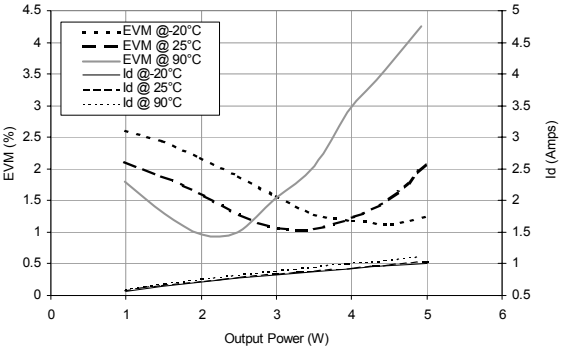
Caution: ESD Sensitive

Appropriate precaution in handling, packaging and testing devices must be observed.

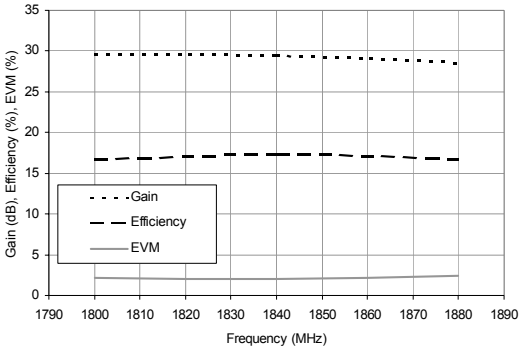
Gain, Efficiency, EVM vs. Output Power
Freq=1840 MHz, Vdd=28 V, T_{Flange}= 25°C



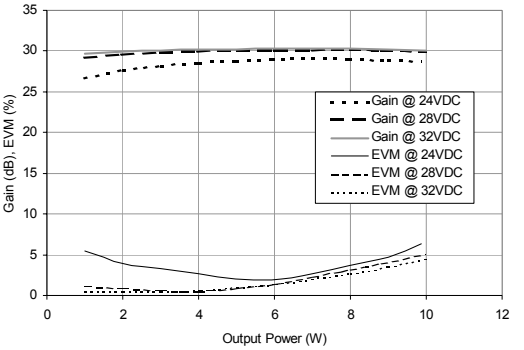
EVM, Id vs. Output Power and Temperature
Freq=1840 MHz, Vdd=28 V, T_{Flange}=-20°C, 25°C, 90°C



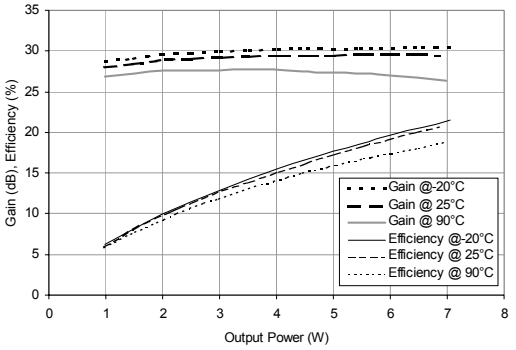
Gain, Efficiency, EVM vs. Frequency
Freq=1840 MHz, Vdd=28 V, T_{Flange}= 25°C



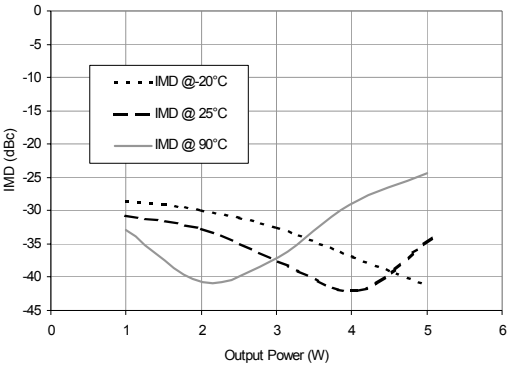
Gain, EVM vs. Output Power and Voltage
Freq=1840 MHz, Vdd=24 V, 28 V, 32 V, T_{Flange}= 25°C



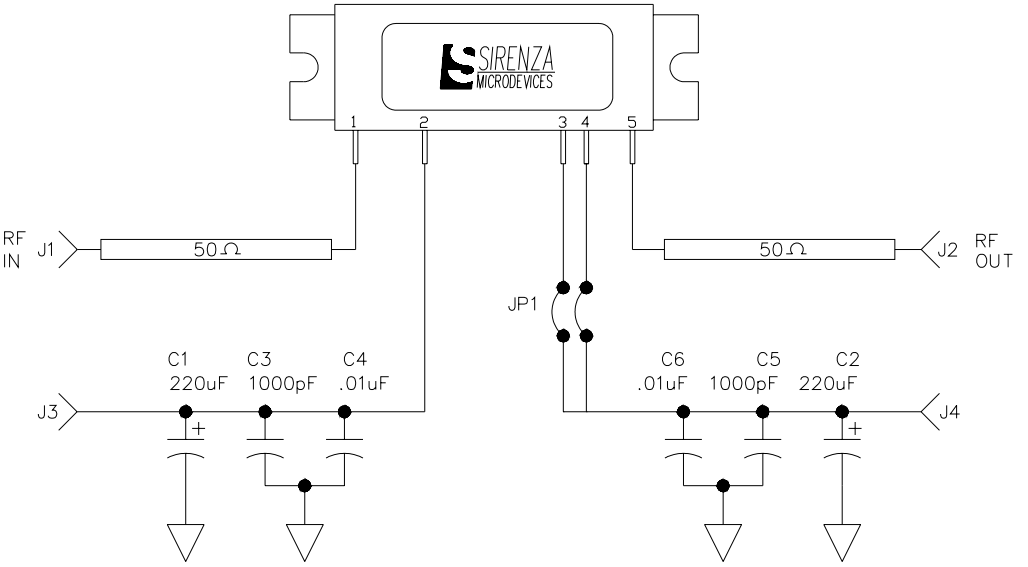
Gain, Efficiency vs. Output Power and Temperature
Freq=1840 MHz, Vdd=28 V, T_{Flange}=-20°C, 25°C, 90°C



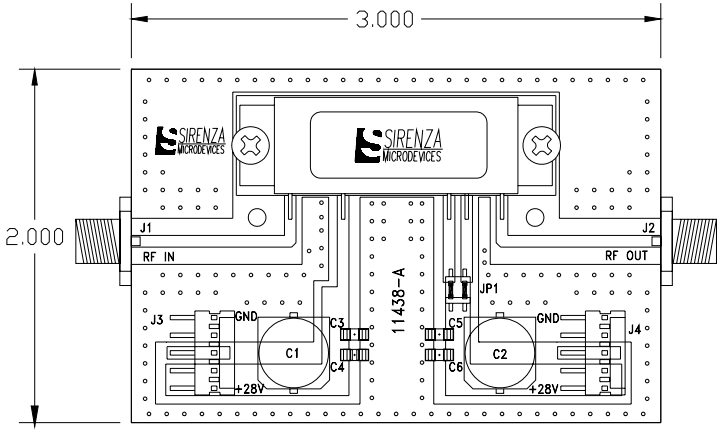
Two Tone IMD vs. Output Power and Temperature
Freq=1840 MHz, Vdd=28 V, T_{Flange}=-20°C, 25°C, 90°C



Test Board Schematic with module attachments shown



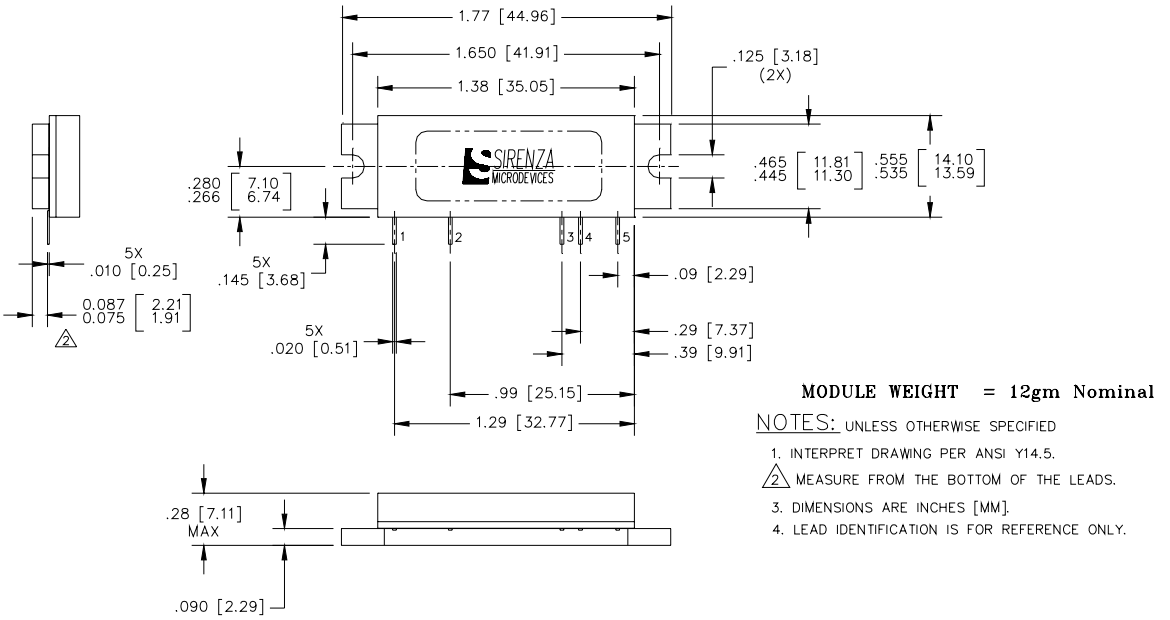
Test Board Layout and Bill of Materials



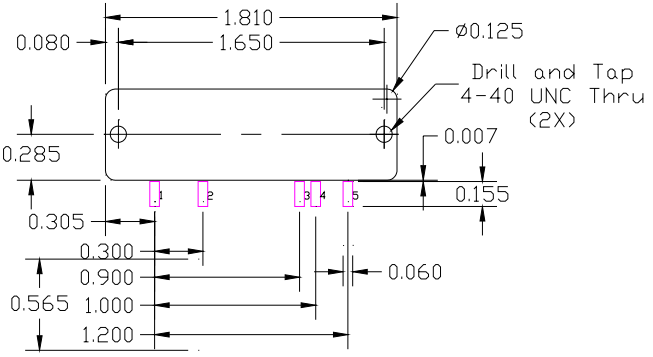
Component	Description	Manufacturer
PCB	Rogers 4350, ε_r=3.5 Thickness=30mils	Rogers
J1, J2	SMA, RF, Panel Mount Tab W / Flange	AMP
J3, J4	MTA Post Header, 5 Pin, Rectangle, Polarized, Surface Mount	AMP
C1, C2	Cap, 220μF 50V, -40 to 85^{o}C, Electrolytic, G	Panasonic
C4, C6	Cap, 0.01μF, 100V, 10%, 1206	Johanson
C3, C5	Cap, 1000pF, 100V, 10%, 1206	Johanson
JP1 Header	SMT Header, Low Profile, 2mm	Specialty Electronics
JP1 Shunt	Shunt, Mate to Header, 2mm	Specialty Electronics
Mounting Screws	4-40 X 0.250”	Various

To download Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture click here

Package Outline Drawing



Recommended PCB Cutout and Landing Pads for the D2F Package



Note 3: Dimensions are in inches