

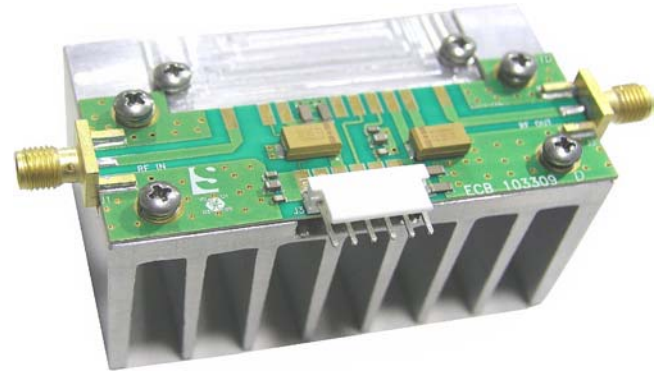


Product Description

The XD010-EVAL connectorized fixture supports test and measurement of the XD series of LDMOS modules available from Sirenza. The fixture includes convenient SMA female RF connectors along with a DC header to facilitate amplifier characterization, or rapid system prototyping. The test circuit is mounted on an aluminum heatsink that requires forced air cooling to ensure proper device operating temperatures.

XD010-EVAL

Test Fixture for Sirenza XD Module Series



Product Features

- 50 Ohm SMA (F) Interface
- Integrated Aluminum Heatsink
- Supports D2, D4, and D5 packages

Applications

- Product Test and Evaluation
- Rapid System Prototyping
- Product Qualification

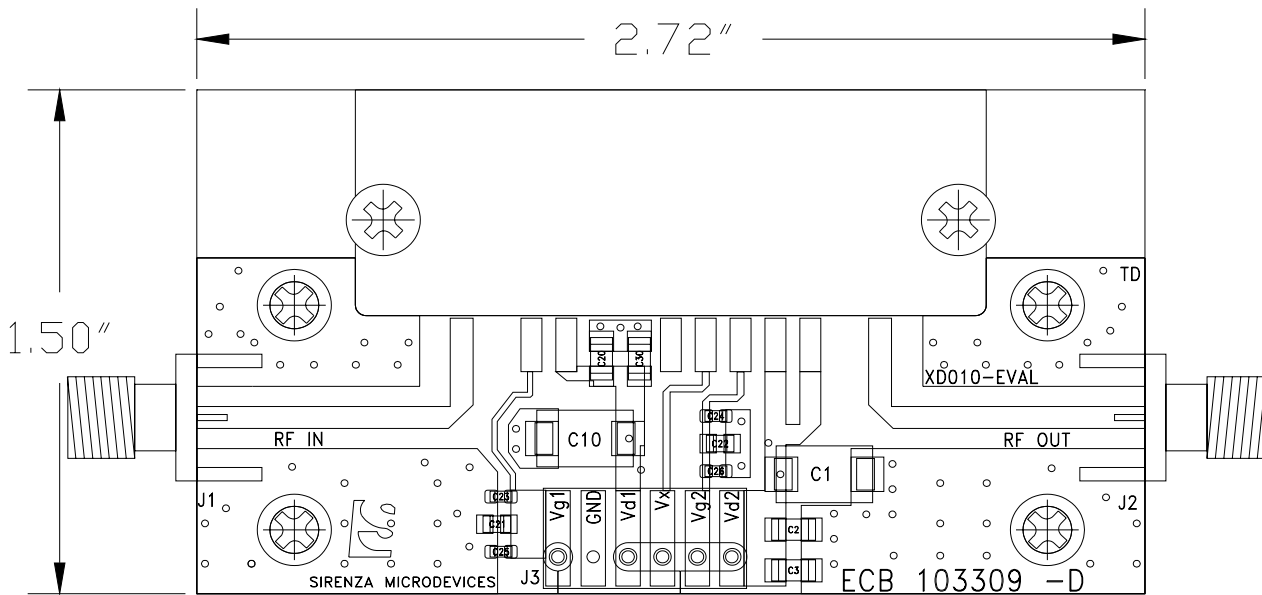
Basic Bill of Materials

Manufacturer	Mfg Part #	Item Description	Qty	Ref Des
Kemet	T494D106M035AS	CAP, 10 UF, 35V, 20%, TANT, ELECT, D	2	C1,C10
Johanson Technology	101R18W104KV4E	CAP, 0.1 UF,100V,10%,1206,LEAD FREE	2	C2,C20
Panasonic	ECJ2YB1H104K	CAP, 0.1 UF, 50V, 10%, 0805	2	C21,C22
AVX	06031C102JAT2A	CAP, 1000 PF, 100V, 10%, 0603	2	C23,C24
ATC	600S680JT250XT	CAP, 68PF,250V,5%,0603,LF LEAD FREE	2	C25,C26
Johanson Technology	101R18W102KV4E	CAP, 1000 PF,100V,10%,1206,LEAD FREE	2	C3,C30
Johnson Comp	142-0751-821	CONNECTOR,SMA END,0.037 JOHNSON COMP	2	J1,J2
Amp	640455-6	CONNECTOR, MTA,SMD,R/A,6 PIN	1	J3
Various		WASHER, #4 LOCK, SPLIT, S S	6	
Various		WASHER, #4 NARROW, .125 ID, .250 OD, .019 T, SS	6	
Various		SCREW, #4-40 PHILLIPS PAN HEAD, 5/16, SS	6	
Rogers 4350, er=3.48, 30 mils thick, 1 oz Cu both sides		PCB, XD010-EVAL	1	
Wakefield	2063-HS Extrusion	Heatsink - Extruded Aluminum, machined	1	

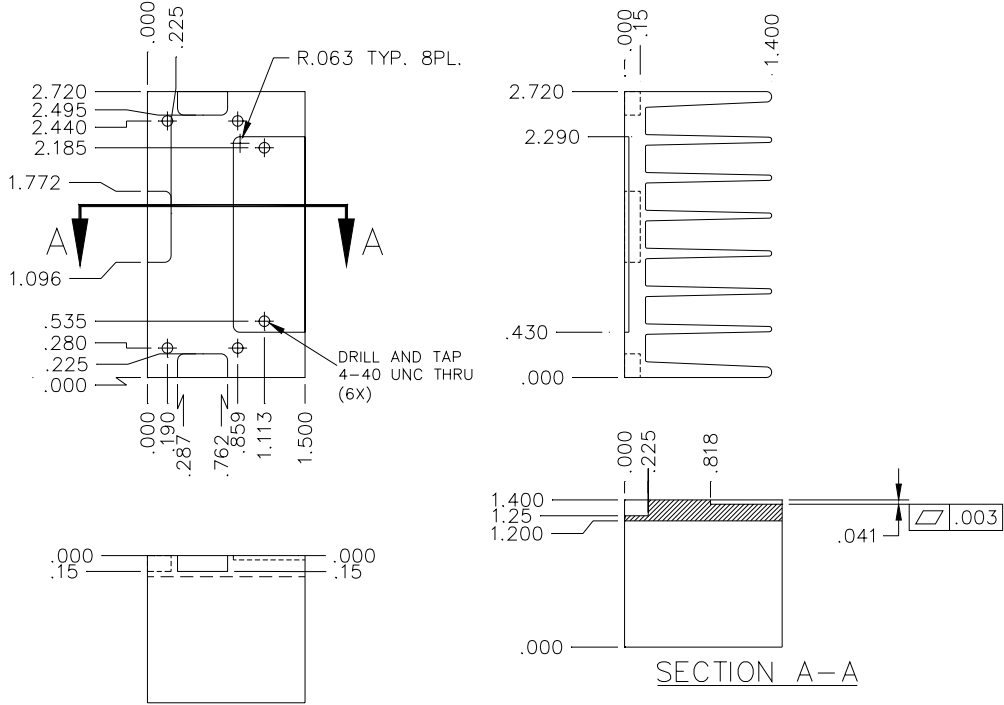
J3 - Pin Description

Pin #	Function	Description
1	V _{G1}	Gate control for stage 1. Sets the quiescent bias current on Pin 3 of the XD Module. Typical values 4.0 – 4.4Vdc. This pin is not used with D2 and D4 modules.
2	Gnd	DC ground for D package module. Also connected to RF ground.
3	V _{D1}	Drain voltage for the first stage. Nominally +28Vdc.
4	V _x	Not used.
5	V _{G2}	Gate control for stage 2. Sets the quiescent bias current on Pin 5. Typical values 4.0 – 4.4Vdc. This pin is not used with D2 and D4 modules.
6	V _{D2}	Drain voltage for the second stage. Nominally +28Vdc

Test Board Layout



Heatsink Diagram



Material = Aluminum,
Wakefield extrusion
HS-2063

To receive Gerber files, DXF drawings, a detailed BOM, and assembly recommendations for the test board with fixture, contact applications support at support@sirenza.com.