3-Channel 12-Bit Linear CCD & CIS Sensor Signal Processors

May 2000-1

FEATURES

- 12–Bit, 13.5 MSPS, A/D Converter
- Triple-Channel,4.5 MSPS CCD Color Scan Mode
- Single-Channel, 9 MSPS Mode
- Triple Correlated Double Sampler
- Triple Programmable Gain Amplifier
- Serial Programming Interface
- CDS for CCD or S/H Mode for CIS Imagers
- Inverting or Non-Inverting Mode
- Internal Voltage Reference
- 5V Operation and 3V I/O Compatibility
- Low Power CMOS: 500mW @ 5V
- 32-Pin TQFP Surface Mount Package

APPLICATIONS

- CCD or CIS Color Scanners
- Multifunction Products
- Image Scanners
- Film Scanners

GENERAL DESCRIPTION

The XRD9815 is a fully integrated, high-performance analog signal processor/digitizer specifically designed for use in high speed, 3-channel linear CCD and CIS imaging applications.

Each channel of the XRD9815 includes a Correlated Double Sampler (CDS), Programmable Gain Amplifier (PGA) and channel offset adjustment. After gain and offset adjustment, the analog inputs are sequentially sampled and digitized by an accurate A/D converter. The analog front-end can be configured for inverting/non-inverting input, CDS or sample-hold (S/H) mode, or AC/DC coupling, making the XRD9815 ideal for use in CCD, CIS and other data acquisition applications. The CDS mode of operation supports both line and pixel-clamp modes and can be used to achieve significant reduction in system 1/f noise and CCD reset clock feed-through.

PGA gain and channel offsets can be updated on a line by line basis. Each channel can have a separate offset and gain setting.

The differential inputs reject common mode noise that can accumulate in a scanner system due to lamp switching and cabling.

In S/H mode the internal DC-restore voltage clamp can be enabled or disabled to support AC-coupled or DC inputs. Sampling mode, PGA gain, channel offset and input signal polarity are all programmable through a serial interface. PGA gain (1-9.2) and channel offset (-210mV to 250mVmin) are programmable in 256 linear steps. The A/D Full-Scale Range (FSR) is programmable to 2V or 3V.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD9815ACQ	32-Lead TQFP	0°C to +70°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017 ◆ www.exar.com

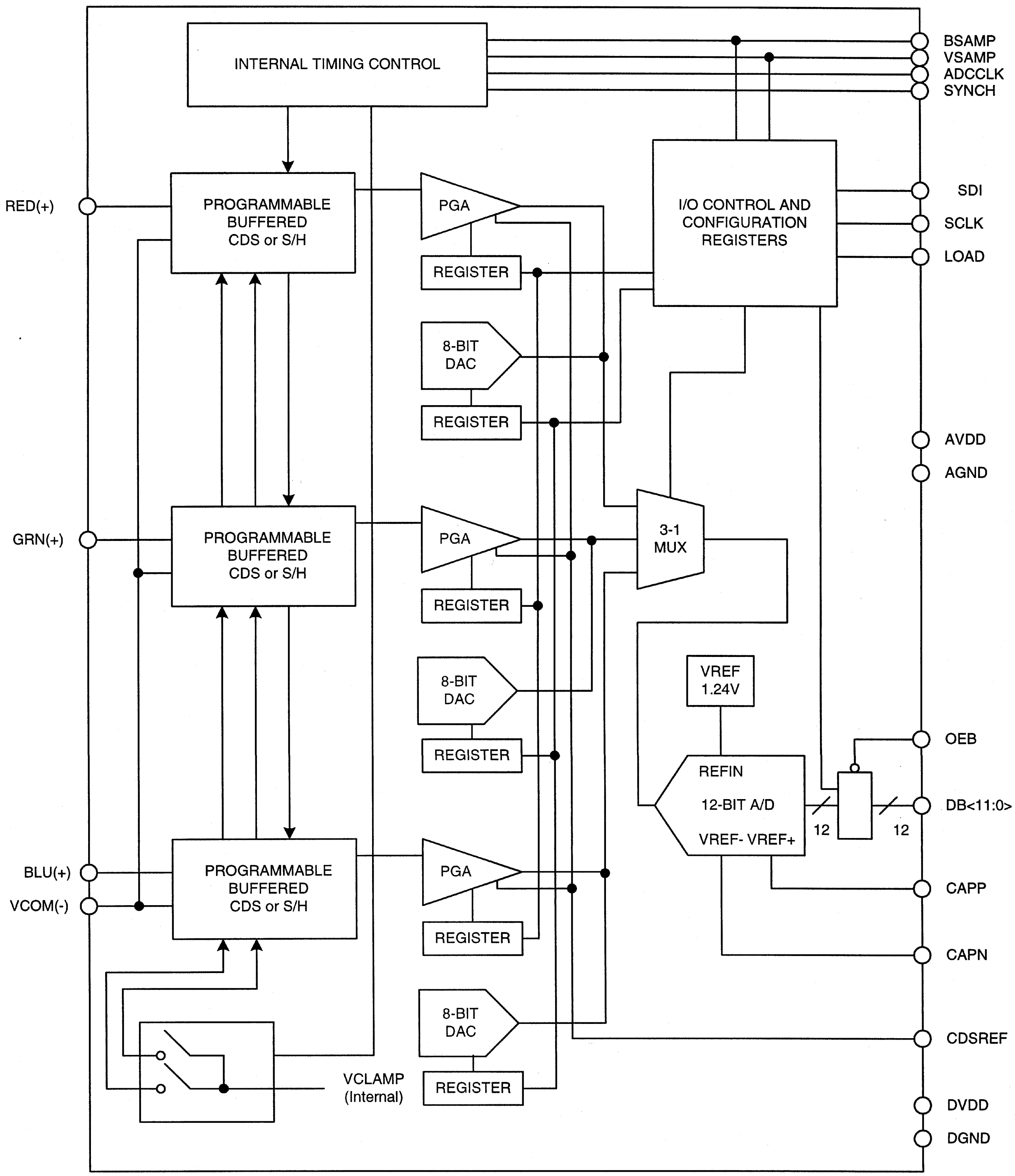
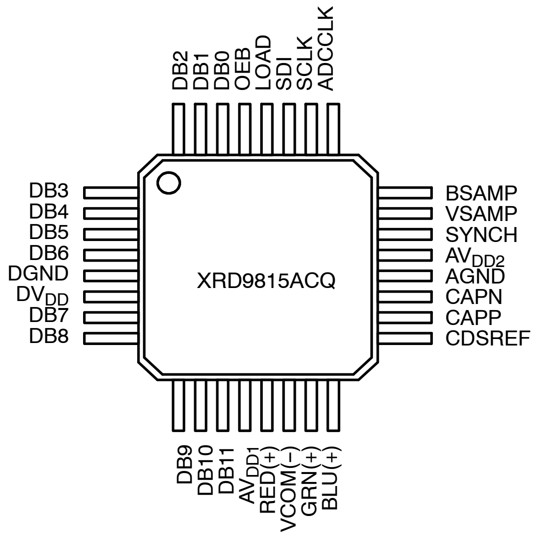


Figure 1. XRD9815 Functional Block Diagram (32 Pin Count)



32 Lead TQFP (7 x 7 x 1.4 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	DB3	Data Output Bit 3
2	DB4	Data Output Bit 4
3	DB5	Data Output Bit 5
4	DB6	Data Output Bit 6
5	DGND	Ground (Output Drivers and Internal Decode Logic)
6	DV_{DD}	Digital Power Supply (Output Drivers and Internal Decode Logic)
7	DB7	Data Output Bit 7
8	DB8	Data Output Bit 8
9	DB9	Data Output Bit 9
10	DB10	Data Output Bit 10
11	DB11	Data Output Bit 11 (MSB)
12	AV_{DD1}	Analog Power Supply
13	RED(+)	Red Positive Analog Input
14	VCOM(–)	Common Negative Input for positive analog inputs (pins 13,15 and 16)
15	GRN(+)	Green Positive Analog Input
16	BLU(+)	Blue Positive Analog Input
17	CDSREF	Decoupling Cap for CDS Reference
18	CAPP	Decoupling Cap for Positive Reference
19	CAPN	Decoupling Cap for Negative Reference
20	AGND	Analog Ground (Substrate)
21	AV_{DD2}	Analog Power Supply

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
22	SYNCH	RGB Start of Line
23	VSAMP	Video Level Sampling Clock
24	BSAMP	Black Level Sampling Clock
25	ADCCLK	A/D Converter Clock
26	SCLK	Serial Shift Clock
27	SDI	Serial Data Input
28	LOAD	Register Write Enable
29	OEB	Data Output Enable
30	DB0	Data Output Bit 0 (LSB)
31	DB1	Data Output Bit 1
32	DB2	Data Output Bit 2

ELECTRICAL CHARACTERISTICS

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
A/D CONVERTER						
R	Resolution	12			BITS	
Fc	Conversion Rate	12	13.5		MSPS	
DNL	Differential Non−Linearity	-1.0	+/-0.5	+1.0	LSB	
INL	Integral Non−Linearity		+/-2.0		LSB	Deviation From Best Fit Line
M	Monotonicity		Yes			Guaranteed
ZSE	Input Referred Offset		-80		mV	
ZSD	Offset Drift		15		V/ºC	
FSE	Input Referred Gain Error		+/- 2		% FS	
FSD	Gain Error Drift		.003		%FS°C	
	Full Scale Differential Input					
FSI	2V Full−Scale Range	1.80		2.04	V	PB5=0, Config Reg #1
FSI	3V Full−Scale Range	2.55		2.90	V	PB5=1, Config Reg #1
CDS – S/H SPECIFICATIONS						
	Input Voltage Range					
INVSR	Input Buffer Disabled (Note 1)	AGND		AVDD	V	AC Coupled, PB1=0, Config Reg #1
INVSRB	Input Buffer Enabled	0.5		AVDD-1	V	DC Coupled, PB1=1, Config Reg #1
	Input Bias Current					
IB	Input Buffer Disabled (Note 2)		25		μA	PB1=0, Config Reg #1, Gain=1
IBB	Input Buffer Enabled			25	nA	T_A=70º C, PB1=1, Config Reg #1
Ron	Input Switch On – Clamp Resistance		85	200	Ω	Clamp Enabled
Roff	Input Switch Off – Clamp Resistance	100	1000		MΩ	Clamp Disabled
	Internal Voltage Clamp					
Vclamp	CCD Input (Inverting)		4.2		V	PB2=0, Config Reg #1
Vclamp	S/H Input (Non−Inverting)		0.7		V	PB2=1, Config Reg #1
Offset Specifications						
OFRES	Offset Adjustment Resolution		2.34		mV	8-Bit 256 Steps, Monotonic
POFR	Positive Offset Adjustment Range	250		340	mV	Gain DAC=00h (min)
NOFR	Negative Offset Adjustment Range	-320		-210	mV	Gain DAC=00h (min)

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
PGA SPECIFICATIONS						
GRAN	Min Gain	-.95	-1.02	-1.10	V/V	12 MSPS, 3-Channel Operation (Tstl ≥ 60ns)
		-.95	-1.02	-1.10	V/V	13.5 MSPS, 3-Channel Operation (Tstl ≥ 50ns)
	Gain 3-Channel (Note 3) Gain Code PB [7:0] = 150d	-5.0	-6.0	-7.0	V/V	13.5 MSPS, 3-Channel Operation (Tstl ≥ 50ns)
	Max Gain 3-Channel	-8.0	-8.7	-9.5	V/V	12 MSPS, 3-Channel Operation (Tstl ≥ 60ns)
	Max Gain 1-Channel	-8.5	-9.0	-9.5		9 MSPS, 1-Channel Operation (Tstl ≥ 70ns)
GRES	Gain Resolution		-0.031 -0.031 -0.031		V/V V/V V/V	8-Bit 256 Steps, 12 MSPS, 3-Channel Operation 8-Bit 256 Steps, 13.5 MSPS, 3-Channel Operation 8-Bit 256 Steps, 9 MSPS, 1-Channel Operation

Notes:

1 *ADC digitizing range = (A/D Full Scale Range/PGA Gain)*

2 *Due to switch capacitor input*

3 *Do not recommend operation over gain code 150d at 13.5 MSPS*

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
SYSTEM SPECIFICATIONS (Includes CDS, PGA and A/D)						
	Differential Non-Linearity					
DNL_{SMIN}	PGA Gain= 00h (min)		+/-0.5		LSB	
DNL_{SMAX}	PGA Gain= ffh (max)		+/-0.5		LSB	
	Integral Non−Linearity (3-Channel CDS Mode)					
INL_{SMIN}	PGA Gain= 00h (min)		+/-3.0		LSB	
	Input Referred Noise					
IRN_{SMIN}	PGA Gain = 00h (min)		1		mV rms	3V, A/D FSR, Conf. Reg. #1, PB5=1
IRN_{SMAX}	PGA Gain = ffh (max)		250		μV rms	3V, A/D FSR, Conf. Reg. #1, PB5=1
	Output Referred Offset					
ORO_{SMIN}	PGA Gain= 00h (min)		+/-50		mV	
ORO_{SMAX}	PGA Gain = ffh (max)		+/-150		mV	
	Input Referred Offset Adjustment Range (Note 1 & 2)					
IRO_{SMIN}	PGA Gain = 00h (min)	-135		110	mV	
IRO_{SMID}	PGA Gain = 80h	-12.5		9.3	mV	
IRO_{SMAX}	PGA Gain = ffh (max)	0		0	mV	Guaranteed to Remove Internal Offsets Only

Notes:

1 *The "Input Referred Offset Adjustment Range is guaranteed for both CDS and S/H modes.*

2 *Please see Graph 1-4 on page 16 for typical "Input Referred Offset Adjustment Range."*

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
TIMING SPECIFICATIONS						
tcr3	3-Channel Conversion Period	250 222			ns ns	 ADCCLK = 13.5MHz
tcr1	1-Channel Conversion Period	111			ns	
tpwb	BSAMP Pulse Width	20			ns	
tbvf	BSAMP falling edge to VSAMP falling edge.	45 70			ns ns	1-Channel CDS Mode 3-Channel CDS Mode
tvbf	VSAMP falling edge to BSAMP falling edge.	65 75			ns ns	1-Channel CDS Mode 3-Channel CDS Mode
tvfcr	VSAMP falling edge delay from rising ADCCLK. (All modes except 1 Channel S/H).	20			ns	
tpwv	VSAMP Pulse Width	20			ns	
tbfcr	BSAMP falling edge delay from rising ADCCLK	10			ns	
taclk	ADCCLK Pulse Width	55.5 41.5 37			ns ns ns	1-Channel S/H Mode 3-Channel CDS Mode ADCCLK = 13.5MHz
tcp1	ADCCLK Period (1 Ch. Mode)	111			ns	
tcp3	ADCCLK Period (3 Ch. Mode)	83 74			ns ns	 ADCCLK = 13.5MHz
tstl	PGA Settling Time for accurate ADC Sampling	55			ns	
ts	SYNCH Rising, Falling Setup	15			ns	
th	SYNCH Rising, Falling Hold	15			ns	
tap	Aperture Delay		5		ns	
VSAMP TIMING OPTION #1						
tvrcf	VSAMP rising edge delay from falling ADCCLK (Note 1)	15			ns	tvrcr is not required, Config REG #1, PB0=0
VSAMP TIMING OPTION #2, Config Reg #1, PB0=1						
tvrcr	VSAMP rising edge delay from rising ADCCLK (Note 1)	15			ns	tvrcf is not required Config REG #1, PB0=1

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
WRITE SPECIFICATIONS						
tds	Data Setup Time	15			ns	
tdh	Data Hold Time	15			ns	
tlcs	Load Setup Time	15			ns	
tldh	Load Hold Time	15			ns	
tplw	Load Pulse Width	25			ns	

Note:

[1] *VSAMP Timing Option #2 allows additional timing flexibility by allowing the rising edge of VSAMP to occur approximately one-half ADCCLK period earlier than Option #1. Option #2 is only available in 3-channel operation (PB4=0, PB3=0, Configuration Register #1).*

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD}=DV_{DD}=5.0V$, ADCCLK=12MHz, $T_A=25°C$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DATA READBACK SPECIFICATIONS						
taa (1)	Address access Time		15		ns	
taoe (1)	Output Enable access Time		15		ns	
ADC DIGITAL OUTPUT SPECIFICATIONS						
tod	Output Delay		20		ns	
tlz	3–State to Data Valid		8		ns	
thz	Output Enable High to 3-State		8		ns	
lat	RGB Inputs		6		ADCCLK	Cycles
DIGITAL INPUTS						
V_{IH}	Input High Logic Level	80			% DV_{DD}	DV_{DD}=3–5V
V_{IL}	Input Low Logic Level			20	% DV_{DD}	DV_{DD}=3–5V
I_{IH}	High Level Input Current		5		μA	
I_{IL}	Low Level Input Current		5		μA	
C_{IN}	Input Capacitance		10		pF	
DIGITAL OUTPUTS (DV_{DD}=5V)						
V_{OH}	Output High Voltage	4.2			V	I_L=2ma
V_{OL}	Output Low Voltage			0.4	V	I_L=–2ma
C_{OUT}	Output Capacitance		10		pF	
DIGITAL OUTPUTS (DV_{DD}=3.3V)						
V_{OH}	Output High Voltage	2.8			V	I_L=2ma
V_{OL}	Output Low Voltage			0.3	V	I_L=–2ma
C_{OUT}	Output Capacitance		10		pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: AV_{DD}=DV_{DD}=5.0V, ADCCLK=12MHz, T_A=25°C unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
POWER SUPPLY						
AV_{DD}	Analog Power Supply	4.5	5.0	5.5	V	$AV_{DD} \geq DV_{DD}$
DV_{DD}	Digital Power Supply	3.0	5.0	5.5	V	
IDDA	Analog Supply Current		90	112	mA	
IDDD	Digital Supply Current		10		mA	Digital Output CLoad=30pF, all pins.
IDDSUM	Total Supply Current		100	120	mA	
PDoff	Sleep Mode Current		15		mA	

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND .... +7.0V
V_{IN} .... V_{DD} +0.5 to GND -0.5V
All Inputs .... V_{DD} +0.5 to GND -0.5V
All Outputs .... V_{DD} +0.5 to GND -0.5V
Storage Temperature .... -65°C to 150°C
Lead Temperature (Soldering 10 seconds) .... 300°C
Maximum Junction Temperature .... 150°C
Package Power Dissipation Ratings (T_A= +70°C)
TQFP .... θ_{JA} = 54°C/W
ESD 2000V

Notes:

1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.*

Function	A2	A1	A0	PB7-PB0
Configuration Reg #1	0	0	0	See Configuration Register #1
Configuration Reg #2	0	0	1	See Configuration Register #2
Red Gain	0	1	0	8-Bit Gain
Green Gain	0	1	1	8-Bit Gain
Blue Gain	1	0	0	8-Bit Gain
Red Offset	1	0	1	8-Bit Offset
Green Offset	1	1	0	8-Bit Offset
Blue Offset	1	1	1	8-Bit Offset

Table 1. XRD9815 Register Overview

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Clamp Mode	Clamp Mode	A/D Full Scale Range	Color Select	Color Select	Signal Polarity	Buffer Enable	Vsamp Timing

Table 2. Configuration Register #1 Bit Assignment

PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Not Used	Not Used	Not Used	Not Used	Test Mode	Not Used	Sleep Mode	Read back

Table 3. Configuration Register #2 Bit Assignment

A2 A1 A0	PB7 PB6	PB5	PB4 PB3	PB2	PB1	PB0
Address	**Clamp Mode**	**A/D FSR**	**Color Select**	**Input Signal Polarity**	**Input Buffer Enable**	**VSAMP Timing**
0 0 0	0 0 - Pixel 0 1 - CDS Line 1 0 - No Clamp 1 1 - S/H Line	0 - 2V 1 - 3V	0 0 - RGB 0 1 - G & RB 1 0 - Green 1 1 - Bayer	0 - Inverted (CCD) 1 - Non-inverted (CIS)	0 - No Buffer (DC or AC Coupling w/Pixel Clamp). 1 - Enable Buffer (AC coupling and Line/No clamp)	0 - Timing #1 1 - Timing #2

Table 4. Configuration Register #1 Definition (Power Up State is 0h)

A2 A1 A0	PB7 PB6 PB5	PB4	PB3	PB2	PB1	PB0
Address	**Used For Register Reset**	**Not Used**	**Test Mode Enable**	**Not Used**	**Sleep Mode**	**Read-back Mode**
0 0 1	If PB3=1, 1 1 1 - Register Reset		0 - Default 1 - Reserved		0 - All circuits active. 1 - Low Power-Mode.	0 - (A/D digital output) 1 - PB7- PB0 (A2:A0 select register data).

Table 5. Configuration Register #2 Definition (Power Up State is 0h)

A2 A1 A0	Function	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0 1 0	Red Gain	MSB							LSB
0 1 1	Green Gain	MSB							LSB
1 0 0	Blue Gain	MSB							LSB
1 0 1	Red Offset	MSB							LSB
1 1 0	Green Offset	MSB							LSB
1 1 1	Blue Offset	MSB							LSB

Table 6. Gain And Offset Registers

Note: *Data PB7-PB0 corresponds to the 8 most significant bits of the data output bus.*

GENERAL

The XRD9815 contains all of the circuitry required to create a complete 3-channel signal processor /digitizer for use in CCD/CIS imaging system. Each channel includes a correlated double sampler, programmable gain amplifier and channel offset adjustment. The input stage can also be configured for use with inverting/non-inverting, AC or DC coupled signals. In order to maximize flexibility the specific operating mode is programmable through two configuration registers. In addition the gain and offset of each channel can be independently programmed through separate gain and offset registers. Configuration register data is loaded serially through a 3-pin serial interface. Specific details for register writes are detailed below. After signal conditioning the three PGA outputs are digitized by a 12-bit A/D converter.

Writing Registers Data

The XRD9815 utilizes eight 8-Bit registers to store configuration, gain and offset information. Register data is written though the 3-pin serial interface consisting of SDI (serial data input), SCLK (serial shift clock) and LOAD (positive edge write enable). A write consists of pulling LOAD low, shifting in 3 bits of address (MSB first) and 8 bits of data (MSB first). Data is written on the rising edge of LOAD. The timing diagram for writing to registers is shown in the timing diagrams.

Configuration Register #1

The bit assignment and definition for this register is detailed in the Configuration Register #1 Definition Table. The primary purpose of this register is to configure the analog input blocks for CCD or S/H operation.

Clamp Mode

The clamp mode setting determines the conditions when the internal clamp is enabled. (see Table 1). The pixel and CCD line-clamp modes are used to DC-restore AC coupled CCD input signals to the PGA common-mode input voltage while using correlated double sampling. S/H Line Mode should be used to DC-restore AC coupled inputs which do not utilize correlated double sampling and have only one control input (VSAMP). No-Clamp mode should be used for DC coupled S/H inputs.

Pixel Mode (CCD with CDS)

The input clamp is active each pixel period with a pulse-width determined by the black- level sampling input (BSAMP). The position of BSAMP can be optimized to eliminate the effects of the CCD reset pulse. Since the input capacitor is recharged to the clamp voltage on each pixel, common-mode droop errors are eliminated.

CCD Line Mode (CCD with CDS)

The input clamp is enabled only at the beginning of the line by gating BSAMP with $\overline{SYNCH}$. Gating with $\overline{SYNCH}$ maintains the ability to position the clamp pulse (BSAMP) away from the CCD reset for varying $\overline{SYNCH}$ position and width. Since the input capacitor is clamped only at the beginning of each line a larger input capacitor is required to satisfy the common-mode input requirements of the analog front-end. (See Coupling Capacitor Requirements). The input buffer should be enabled in this mode (PB1=1, Register #1).

S/H Line Mode (S/H with AC Coupling)

The S/H Line mode clamp is used to DC-restore AC coupled inputs which do not utilize the CDS. VSAMP is used to sample and hold the input signal and $\overline{SYNCH}$ performs the clamp function. This differs from the CDS line and pixel modes which use BSAMP to clamp to the reference level and VSAMP to hold the video input. The input buffer should be enabled in this mode (PB1=1, Register #1).

No -Clamp Mode (S/H with DC Input)

Used for DC coupled inputs. AC coupled inputs must be externally clamped to the proper common-mode input voltage of the XRD9815.

Pixel clamp is the default clamp mode.

Clamp Mode	PB7	PB6	Clamp Enable
Pixel	0	0	BSAMP
CDS Line	0	1	BSAMP • $\overline{\text{SYNCH}}$
No Clamp	1	0	Disabled
S/H Line	1	1	$\overline{\text{SYNCH}}$

Table 7. Clamp Enable Definition

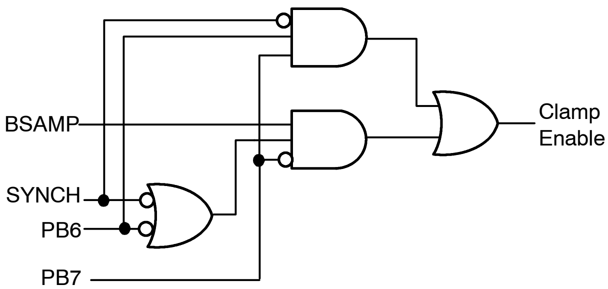


Figure 2. Clamp Enable Logic

A/D Full-Scale Range

This bit sets the Full-Scale Range (FSR) of the A/D converter to 2V or 3V. Use 3V FSR for lowest noise performance.

Color Select

The color input corresponds to the signal input to be digitized by the A/D converter. If set to RGB (default) the A/D input is sequentially cycled through the red, green and blue channels. The red channel input is synchronized by sampling the SYNCH signal on the rising edge of ADCCLK. If set to the GREEN channel the A/D multiplexer will not sequence and the A/D converter input will be continually connected to the GREEN channel.

Signal Polarity

This bit configures the analog inputs for positive or negative transitioning inputs. This is required to provide the correct signal polarity to the A/D input and to set the correct input clamp level. The default configuration is set to inverting mode (CCD input).

Input Buffer Enable

This bit enables the input buffer to the PGA amplifier and is required only for AC coupled inputs operating in CDS Line or S/H Line Clamp modes. Since this input buffer reduces the input voltage range, it's use is not recommended under DC or pixel-mode operation. The default setting is no buffer.

VSAMP Timing

This allows the user to select one of two VSAMP timing controls. Timing Option #2 allows the rising edge of VSAMP to occur approximately one-half ADCCLK earlier than Option #1. This does not affect internal timing and is provided only to allow additional flexibility in the external timing control. Timing Option #2 is available only in the 3-channel mode of operation. (See timing diagram).

Configuration Register #2

The bit assignment and definition for this register is detailed in the Configuration Register #2 Definition Table. A diagnostic read-back mode allows gain, offset and configuration data to be output as the high-byte on the digital output bus. Additional bits are used to enable a low-power sleep state and manufacturing test mode.

Test Mode

This is a reserved bit for testing and must be set to 0 in all writes to Configuration Register 2.

Sleep Mode

Setting this bit to 1 forces the circuit into a low power standby mode. Configuration, offset and gain registers remain unchanged in sleep mode. Pull OEB High to set DB <11:0> to high impedence during sleep mode.

Read Back Mode

This is a special diagnostic mode which can aid in the debugging of new system designs. Setting this bit to 1 allows all configuration, gain and offset register contents to be output on the data output bus (explained below).

Reading Register Data

In read-back mode the A/D output is bypassed and internal register data is output to the 8 most significant bits of the data output bus. Readback mode is enabled by setting PB0 in Configuration Register #2 equal to 1. The LOAD pin must remain high in the readback mode. In order to read a specific register shift in 3 bits of address data (MSB first), followed 8 dummy data bits. Register data will be valid after the 11th data bit is shifted in. In order to exit readback mode perform a write to configuration register 2, PB0=0 and write this register by pulling LOAD high.

Important: *The entire byte of register #2 is written when LOAD is pulled high and will be equal to the data loaded immediately preceeding the positive edge of LOAD.*

PGA Gain Settings

The gain for each color input is individually programmable from 1 to 10 in 256 linear steps.

$$PGA\ Gain = \left(\frac{Code}{256}\right) \cdot 8.0 + 1.0$$

where Code represents the decimal contents of the binary 8-bit gain setting register.

Channel Offset Adjustment

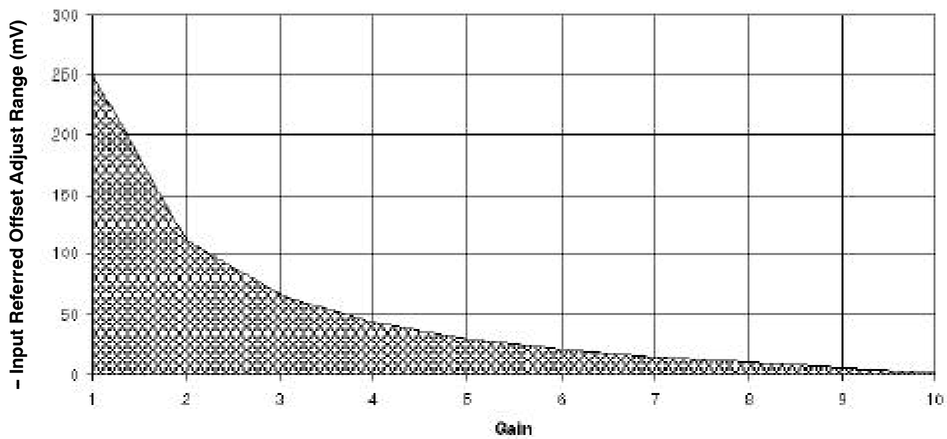
The offset correction for each channel is programmable from -300mV to +300mV via an 8-Bit sign-magnitude Dac.

$$Channel\ Offset = PB7 \cdot \left[\frac{(Code)}{128}\right] \cdot 300mV$$

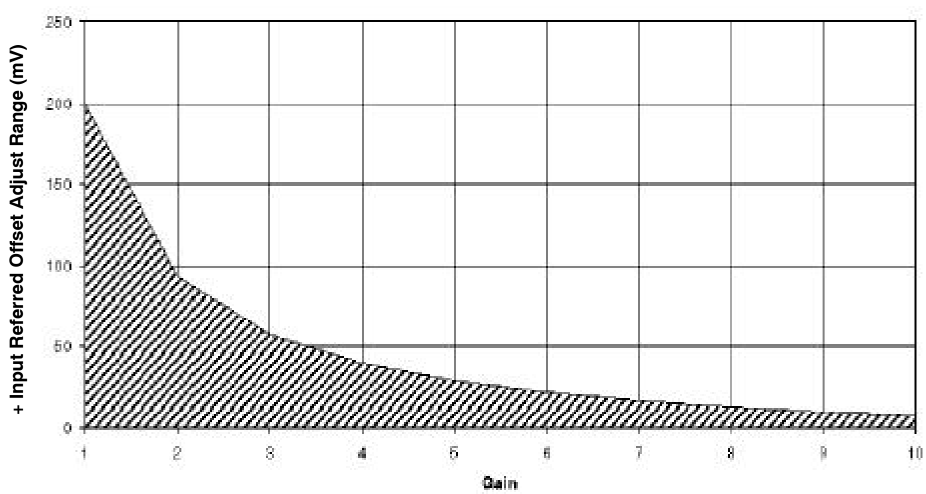
PB7=1 equals -1

PB7=0 equals +1

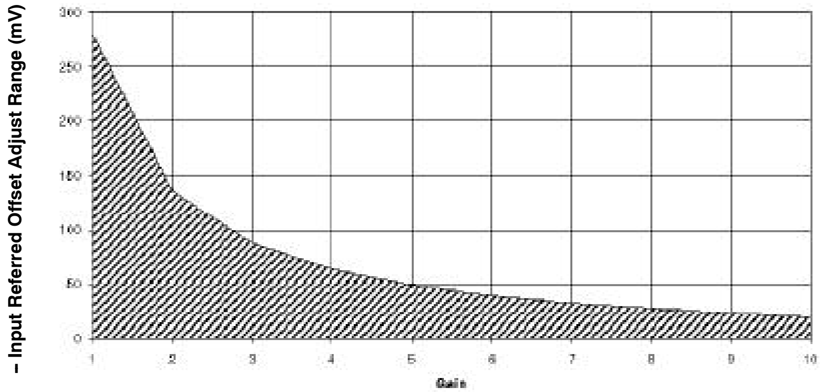
Code = (PB6:PB0) decimal content of the binary 8-bit offset register.



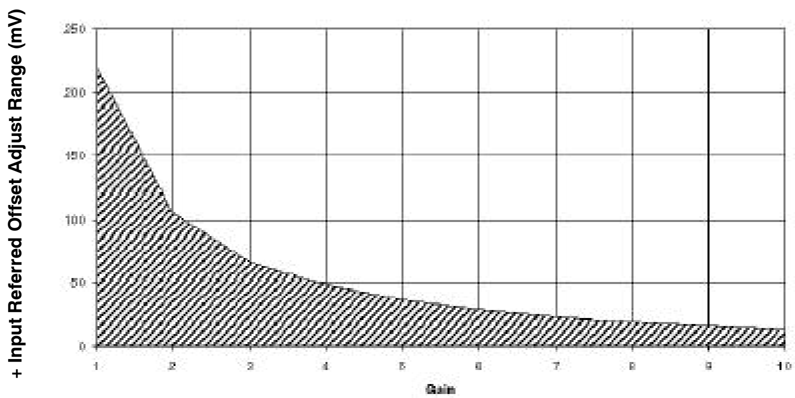
Graph 1. Typical 3–Channel 12MHz CDS Mode –Input Referred Offset Adjust Range



Graph 2. Typical 3–Channel 12MHz CDS Mode +Input Referred Offset Adjust Range



Graph 3. Typical 3–Channel 12MHz S/H Mode
–Input Referred Offset Adjust Range Vosext



Graph 4. Typical 3–Channel 12MHz S/H
+Input Referred Offfset Adjust Range Vosext

Theory of Operation (Correlated Double Sampling)

Correlated double sampling is a technique used to level shift and acquire CCD output signals whose information is equal to the difference between consecutive reference (black) and signal (video) samples. The CDS process consists of three steps.

1) Sampling and holding the reference black level.

2) Sampling the video level.

3) Subtracting the two samples to extract the video information.

Once the video information has been extracted it can be processed further through amplification and/or offset adjustment. Since system noise is also stored and subtracted during the CDS process, signals with bandwidths less than half the sampling frequency will be substantially attenuated.

In order to reject higher frequency power supply noise which is not attenuated near the sampling frequency the XRD9815 utilizes a fully differential input structure.

Since the CDS process uses AC coupled inputs the coupling capacitor must be charged to the common-mode range of the analog front-end. This can be accomplished by clamping the coupling capacitor to the internal clamp voltage when the CCD is at a reference level. This clamp may occur during each pixel (Pixel Clamp), or at the beginning of each line (CDS Line Clamp). If CDS Line Clamp mode is used the input buffer (configuration register #1, PB1) must be enabled to eliminate the effects of input bias current. If Pixel mode is selected the input buffer is not required or recommended.

3-Channel CDS Mode

This mode allows simultaneous CDS of the red, green and blue inputs. Black-level sampling occurs on each pixel and is equal to the width of the BSAMP sampling input. The black level is held on the falling edge of BSAMP and the PGA will immediately begin to track the signal input until the falling edge of VSAMP.

Two VSAMP timing modes are supported to allow additional flexibility in the VSAMP pulse width (see timing diagrams). At the end of the video sampling phase the difference between the reference and video levels is inverted, amplified and offset depending on the contents of the PGA gain and offset registers. The RGB channels are then sequentially converted by a high speed A/D converter. A/D converter data appears on the data output bus after six ADCCLK cycles. Channel synchronization occurs when the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The Red channel is always digitized first following synchronization and will be selected as long as the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The power up default mode is for CDS sampling a CCD input (Pixel Clamp, Inverting input, no input buffer).

1-Channel CDS Mode

The 1-channel CDS mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode described previously. To select a single channel input the color bits of Configuration Register #1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. In single color mode the SYNCH signal has no effect on synchronization but still affects clamping. (See Table 1). If the configuration is toggled from single color to 3-channel mode RGB scanning will not occur until the circuit is resynchronized with the SYNCH pulse.

3-Channel CIS/Sample and Hold Mode

The XRD9815 also supports operation for Contact Image Sensor (CIS) and S/H applications.

Channel synchronization occurs when the rising edge of ADCCLK samples a logic 0 on the SYNCH input. The Red channel is always digitized first following synchronization and will be selected as long as the rising edge of ADCCLK samples a logic 0 on the SYNCH input. For DC-coupled inputs the reference clamp and input buffer should be disabled and input polarity should be set to 1 (non-inverting). In this mode of operation the BSAMP input is connected to DGND and input sampling occurs on the falling edge of VSAMP.

When using AC coupled inputs the coupling capacitor must be clamped to the required common-mode input voltage when the signal source output is at a reference level. This can be accomplished by enabling the S/H Line clamp mode in configuration register 1 and clamping the input capacitor to the internal clamp voltage at the beginning of each line via the SYNCH input. The required width of the SYNCH signal is dependent on the value of the coupling capacitor, XRD9815 clamp resistance, source output resistance and desired accuracy. This is explained further in Coupling Capacitor Requirements. If AC coupling is used the input buffer (configuration register 1) must be enabled to eliminate input-bias current errors inherent to the sampling process. The input buffer is not required or recommended in DC coupled applications.

1-Channel CIS/ Sample and Hold Mode

The 1-Channel CIS S/H mode allows high-speed acquisition and processing of a single channel. The timing, clamp and buffer configurations are similar to the 3-channel mode with the exception that VSAMP timing option #2 is not supported. To select a single channel input the color bits of configuration register 1 must be set to the appropriate value. The A/D input will begin to track the selected color input on the next positive edge of ADCCLK. In single color mode the SYNCH signal has no effect on synchronization but still affects clamping. (See clamp mode). If the configuration is toggled from single color to 3-channel mode, RGB scanning will not occur until the circuit is resynchronized with the SYNCH pulse.

Power Supplies and Digital I/O

The XRD9815 utilizes separate analog and digital power supplies. All digital I/O pins are 3V/5V compatible and allow easy interfacing to external digital ASICs. For single supply systems the analog and digital supply pins can be separately connected and bypassed to reduce noise coupling from digital to analog circuits.

Coupling Capacitor Requirements

The size of the external coupling capacitors depends on a number of items including the clamp mode, pixel rate, channel gain, black-level variation and system accuracy requirements. The major limitation for each clamp mode is shown below.

	CDS Mode	S/H Mode
Pixel Clamp (Buffer Disabled)	Black level pixel-pixel variation Initial charging	Not Applicable
Line Clamp (Buffer Enabled)	Initial charging Capacitor droop (common-mode range)	Initial Charging Capacitor droop (acuracy error)

Table 8. Coupling Capacitor Limitation

The calculation of capacitance described below is for the capacitors connecting to Red/Grn/Blu input pins. Please refer to Figures 21 & 22 for XRD9815 connection diagrams.

Maximum Capacitance (CDS Pixel Mode)

Limitation #1

Since the black-level is clamped during each pixel period the input bias current contributes an insignificant amount of droop during one pixel period. However, pixel-pixel variations in the black level may appear as errors . For a worst case gain of -10, 2V A/D FSR and 12-bit accuracy one lsb of error corresponds to 50μV input-referred. Assuming 1mV of pixel-pixel variation in the black level the maximum coupling capacitor can be determined as a function of the clamping period and internal clamp resistance.

$$C_{max} = \frac{tpwb}{(Rc + Rs) \cdot \ln\left(\frac{1mV}{50\,\mu V}\right)}$$

where tpwb=clamp pulse width (BSAMP)

Rc=Clamp resistance

Rs=Signal source-resistance

For typical values of tpwb=40ns, Rc=85Ω, Rs=50Ω, $C_{MAX} \leq$ 99pF.

Limitation #2

The maximum input capacitance may also be limited by the time allowed to charge the input capacitor to the difference between the black level and clamp levels. The capacitor value can be related to the number of clamp pulses allowed before the capacitor voltage settles to within the desired accuracy.

$$C_{max} = \frac{tpwb \cdot N}{(Rc + Rs) \cdot \ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where tpwb= clamp pulse width (BSAMP)

N= number of pixels allowed to settle

Rc=clamp resistance

Rs=Signal source-resistance

Vr= black level

Vc=XRD9815 clamp voltage

Vε=error voltage

Assuming that Vr=5V, Vc=4V, Vε=50μV, Rc=85Ω, Rs=50Ω, tpwb=40ns and N=10 the maximum allowable input capacitor is ≤ 299pF. In this case the input capacitance is limited by pixel-pixel changes in the black level (first calculation).

Minimum Capacitance (CDS Pixel Mode)

The minimum coupling capacitance is limited by parasitic effects including pin and board capacitance. A minimum value of 68pF is recommended.

Maximum Capacitance (CDS Line Mode)

Since the coupling capacitor is charged only at the beginning of each line and not clamped at each pixel, the pixel-pixel variation in the black level has no effect on the capacitor size. The maximum size will be limited by the number of clamp pulses, clamp pulse-width and number of lines allowed to charge to a given accuracy.

$$C\ max = \frac{N \cdot L \cdot tpwb}{(Rc + Rs) \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)}$$

where tpwb= clamp pulse width (BSAMP)

N= number of clamp pulses at beginning of each line.

L = number of lines to clamp to desired accuracy.

Rc=clamp resistance

Rs=Signal source-resistance

Vr= black level

Vc=XRD 9815 clamp voltage

Vε=error voltage

Assuming that Vr=5V, Vc=4V, Vε=50uV, Rc=85Ω, Rs=50Ω, tpwb=40ns N=10, L=2 the maximum allowable input capacitor is equal to 598pF. If it is desired to settle within one line (L=1) for a given capacitor value, the number of clamp pulses or the clamp pulse-width must be increased using the above equation.

Minimum Capacitance (CDS Line Mode)

In general the minimum value coupling capacitance is limited by the amount of droop which can occur before the input voltage range of

the input amplifier is exceeded. The input capacitor droop is related to the input bias current by:

$$Vdroop = \frac{Ibias \cdot n \cdot T}{C}$$

where I_{bias}=input bias current

n=number of pixels per line

T=pixel period

If the minimum input voltage is allowed to equal the 0V input voltage of the XRD9815, the maximum allowable droop will be equal to the clamp level minus the difference between the black and video levels. For example if Vc=4V, and the CCD video output is -2V relative to the black level the maximum allowable droop is equal to 2V.

Using the previous equation and assuming T=500ns, n=3000

$$C\ min = \frac{10nA \cdot 3000 \cdot 500\ ns}{2V} = 7.5pF$$

$$Vdroop = \frac{Ibias \cdot T}{2 \cdot C\ min}$$

Note: *These are the absolute minimum capacitor requirements. As stated for pixel-mode a minimum value of 68pF is recommended.*

Minimum Capacitance (S/H Line Mode)

Unlike Line or Pixel CDS modes voltage droop across a line appears as an absolute error and is the dominant factor in determining the minimum coupling capacitor size.

$$C\ min = \frac{Ibias \cdot n \cdot T}{V\varepsilon}$$

where I_{bias}=input bias current

n=number of pixels per line

T=pixel period

Assuming n=3000, T=500nS, I=10nA and Vε=50uV the minimum required capacitor is 300nF.

Maximum Capacitance (S/H Line Mode)

The maximum capacitance is determined by the amount of time allowed to charge the coupling capacitor. In order to minimize the charging time the maximum capacitor can be set to the minimum value as previously calculated. In this case the

time required to charge the capacitor is:

$$t = (Rs + Rc) \cdot C\,min \cdot ln\left(\frac{Vr - Vc}{V\varepsilon}\right)$$

where t= clamp pulse -width ($\overline{SYNCH}$)

Rc=clamp resistance

Rs=Signal source-resistance

Vr= Input reference level

Vc=XRD9815 clamp voltage

Vε=error voltage

Cmin = coupling capacitor

Assuming that Vr=0.5V Vc=0V, Vε=50uV, Rc=85Ω, Rs=500Ω and C=300nF, the minimum clamp period is equal to 1.6ms.

3 Channel CDS Mode - Pixel Clamp

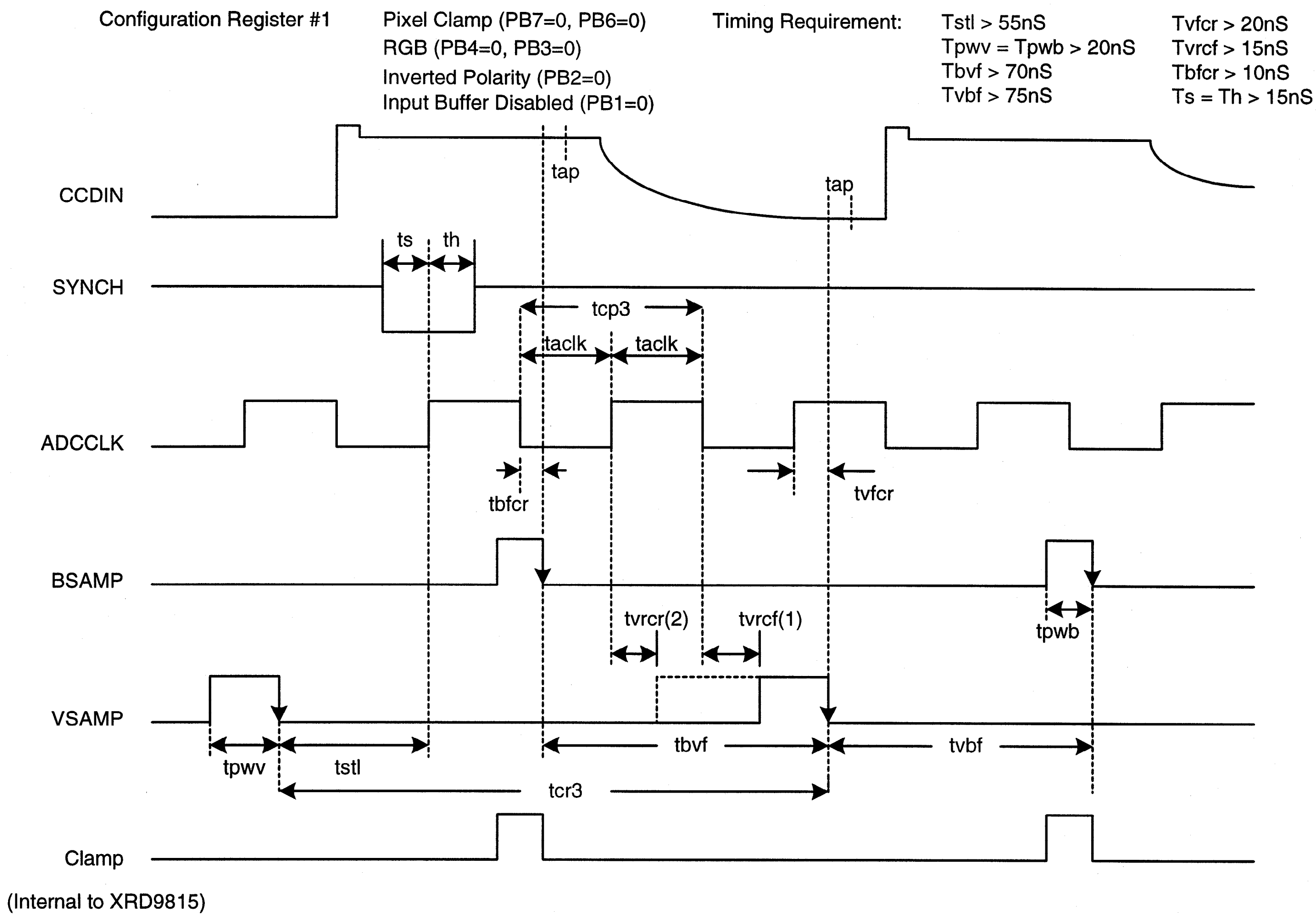
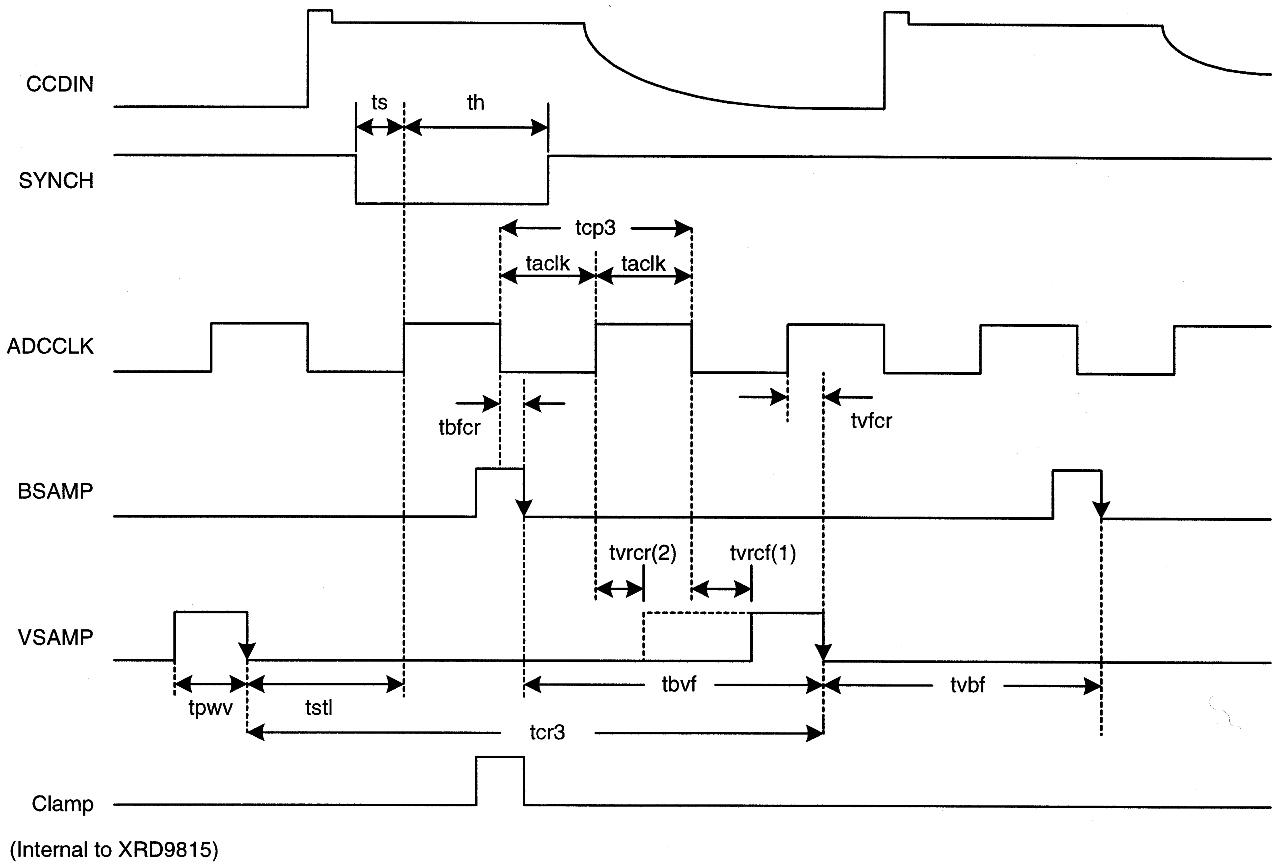


Figure 3. 3 Channel CDS Mode – Pixel Clamp

CDS Mode Event Table	
Event	**Action**
↑BSAMP	Connect CDS Inputs and Track Black Level
↓BSAMP	Hold Black Level and Track Video Level
VSAMP * ADCCLK	Reset PGA (Vsamp and ADCCLK both must be high for AMW of 20ns)
↓VSAMP	Hold Video Level

3 Channel CDS Mode - Line Clamp

Configuration Register #1	Timing Requirement:		
CDS Line (PB7=0, PB6=1)		Tstl > 55nS	Tvfcr > 20nS
RGB (PB4=0, PB3=0)		Tpwv = Tpwb > 20nS	Tvrcf > 15nS
Inverted Polarity (PB2=0)		Tbvf > 70nS	Tbfcr > 10nS
Input Buffer Enabled (PB1=1)		Tvbf > 75nS	Ts = Th > 15nS



Notes: *(1) VSAMP Timing Option #1 uses tvrcf (tvrcr is not required)*
(2) VSAMP Timing Option #2 uses tvrcr (tvrcf is not required)

Figure 4. 3 Channel CDS Mode – Line Clamp

1 Channel CDS Mode - Pixel Clamp

Configuration Register #1
Pixel Clamp (PB7=0, PB6=0)
Green Channel (PB4=1, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Disabled (PB1=0)

Timing Requirement:
Tstl > 55nS
Tpwv = Tpwb > 20nS
Tbvf > 45nS
Tvbf > 65nS
Tvfcr > 20nS
Tbfcr > 10nS

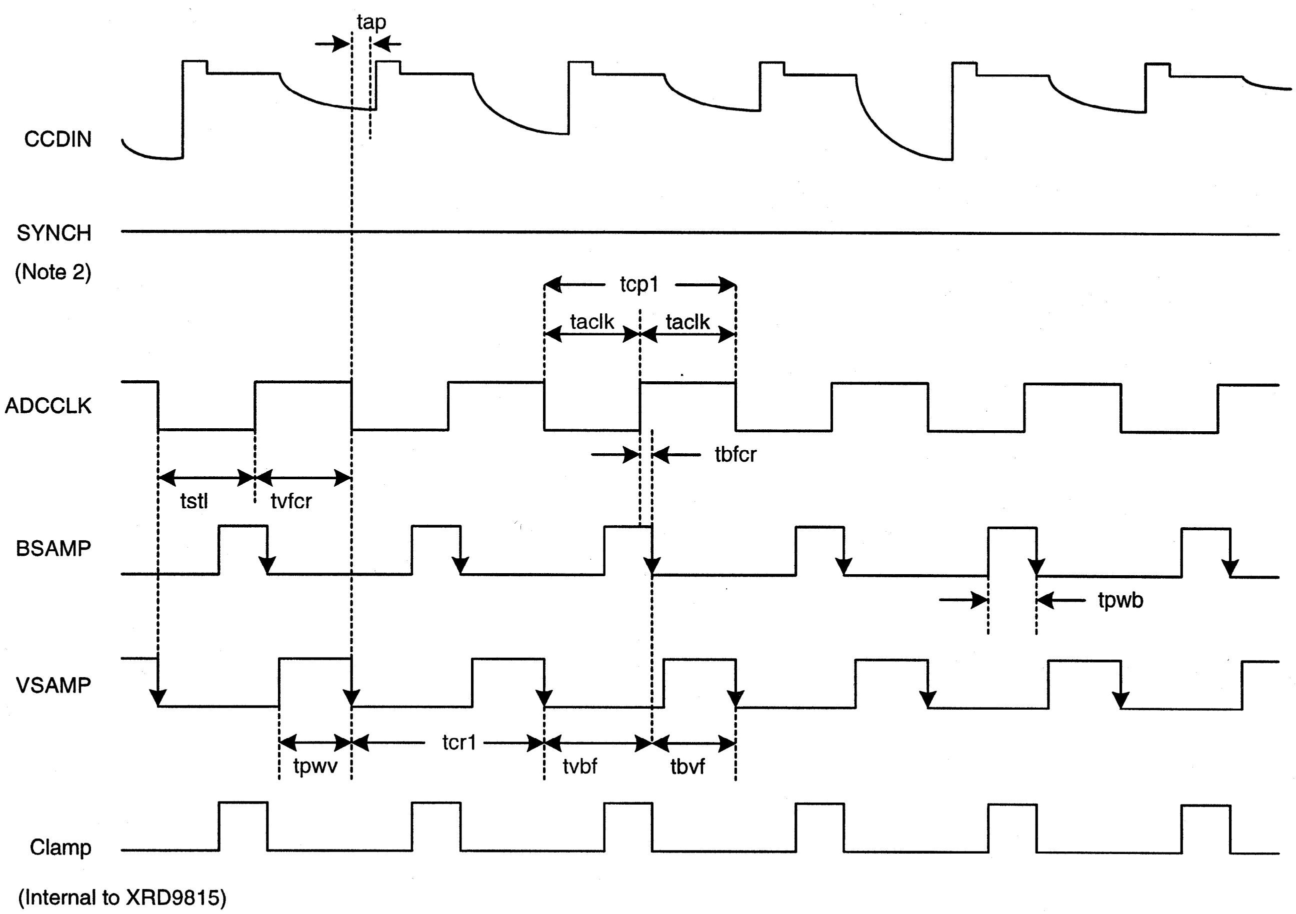
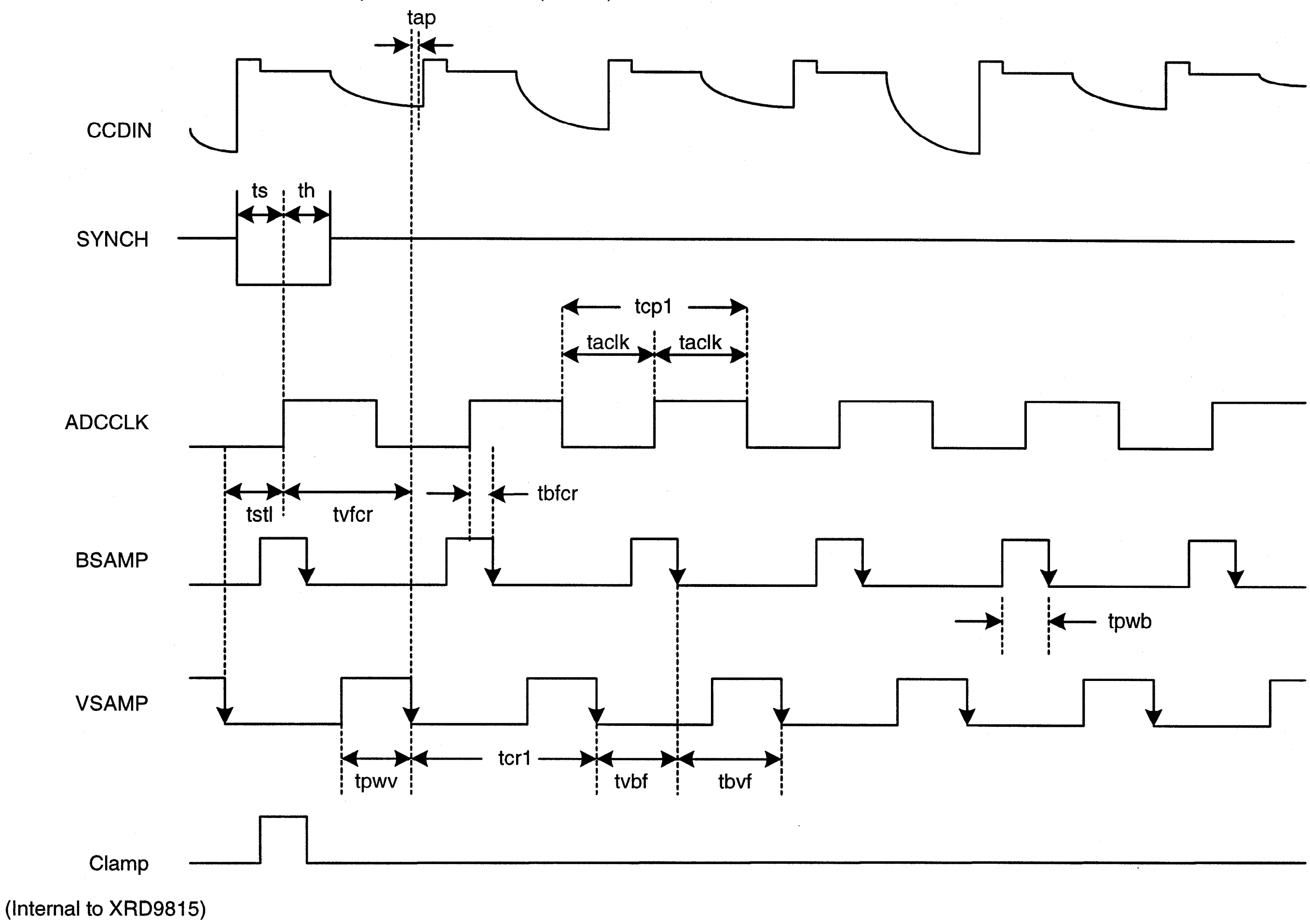


Figure 5. 1 Channel CDS Mode – Pixel Clamp

1 Channel CDS Mode - Line Clamp

Configuration Register #1 CDS Line Clamp (PB7=0, PB6=1)
Green Channel (PB4=1, PB3=0)
Inverted Polarity (PB2=0)
Input Buffer Enabled (PB1=1)

Timing Requirement: Tstl > 55nS, Tpwv = Tpwb > 20nS, Tbvf > 45nS, Tvbf > 65nS, Tvfcr > 20nS, Tbfcr > 10nS



Notes: *(1) Only VSAMP timing option #1 is supported in 1-Channel mode*
(2) Force SYNCH to logic 1 in 1-Channel Pixel-Clamp Mode

Figure 6. 1 Channel CDS Mode – Line Clamp

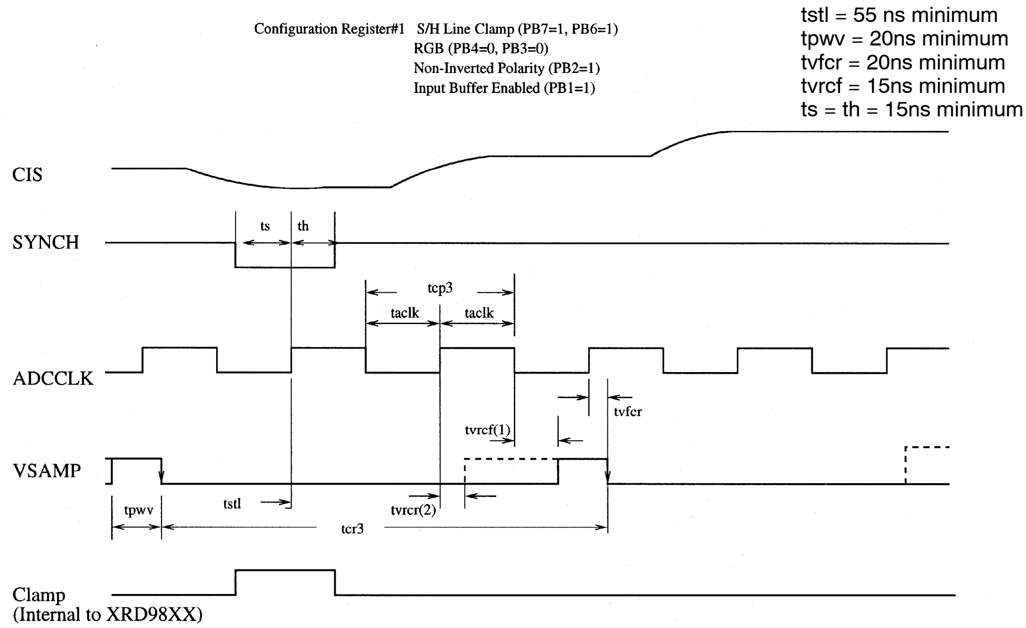
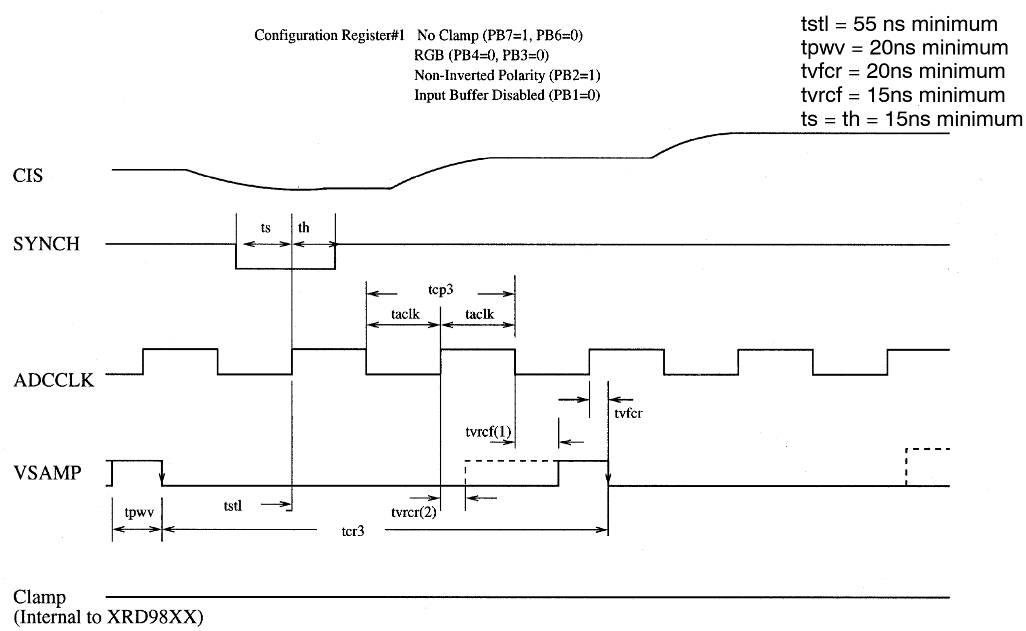


Figure 7. 3 Channel S/H Mode – Line Clamp (AC Coupled)



Notes: (1) VSAMP Timing option #1 uses tvrcf. (tvrcr is not required).
(2) VSAMP Timing option#2 uses tvrcr. (tvrcf is not required).

Figure 8. 3 Channel S/H Mode – No Clamp (DC Coupled)

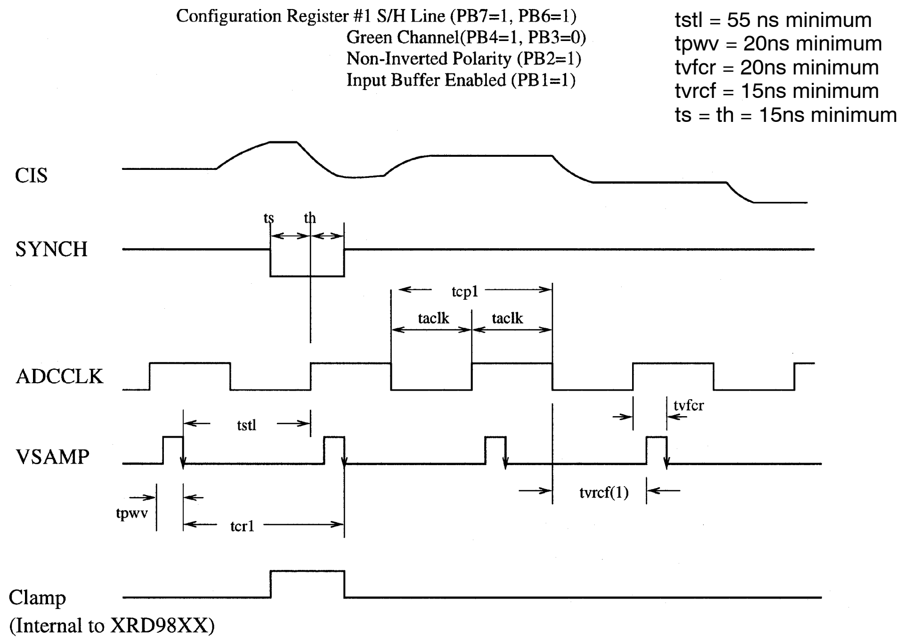
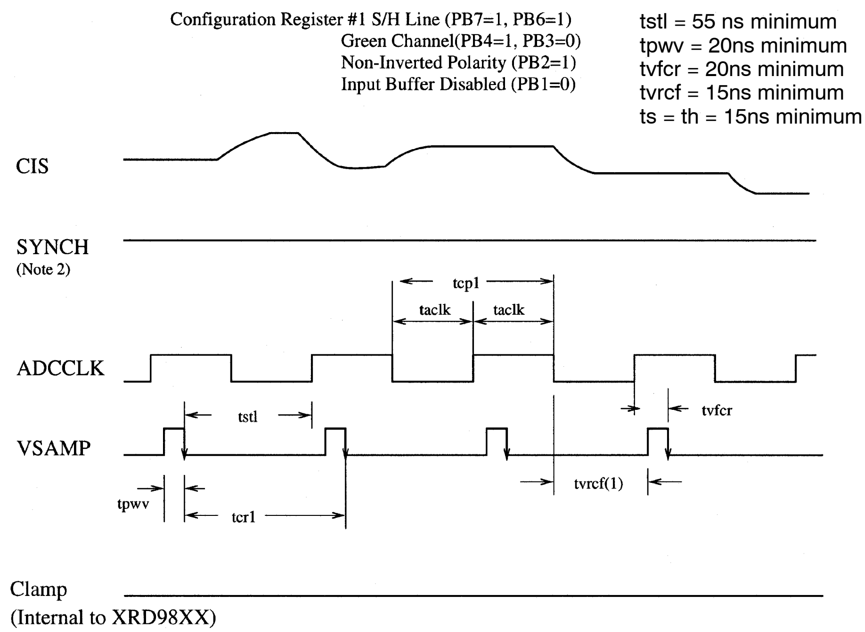


Figure 9. 1 Channel S/H Mode – Line Clamp (AC Coupled)



Notes:(1) Only VSAMP timing option #1 is supported in 1-Channel mode.
(2) Force SYNCH to logic 1 in 1-Channel No-Clamp Mode

Figure 10. 1 Channel S/H Mode – No Clamp (DC Coupled)

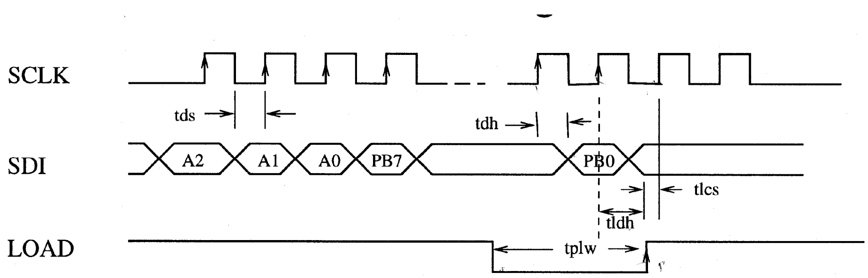
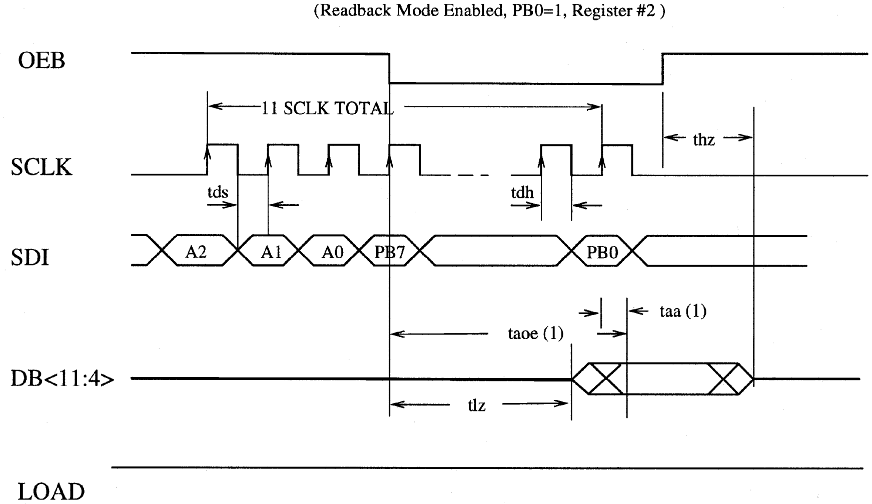


Figure 11. Write Timing



Note 1: Start of valid data depends on which timing becomes effective last taoe or taa.

Figure 12. Read-Back Mode Timing

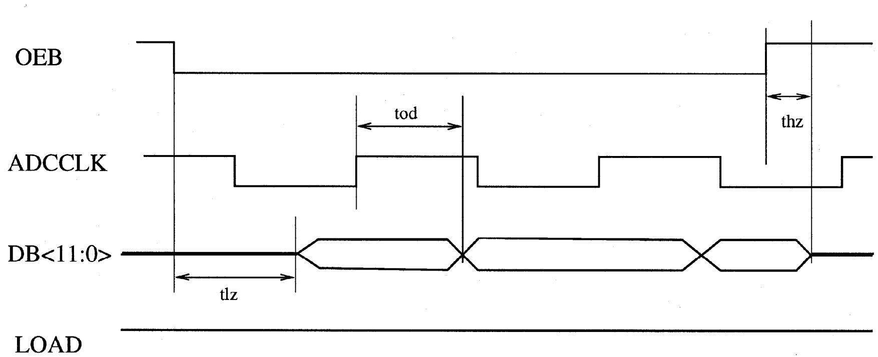


Figure 13. ADC Digital Output Timing

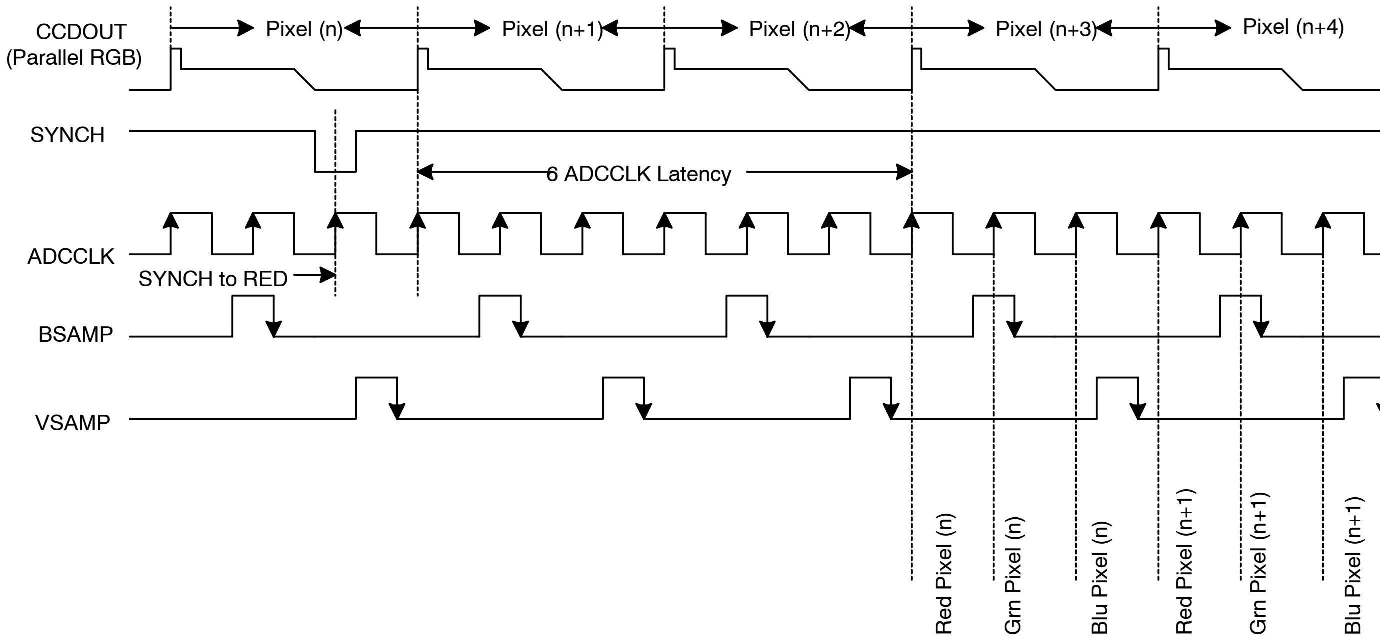


Figure 14. 3-Channel CDS Pixel Clamp Synchronization and ADC Timing

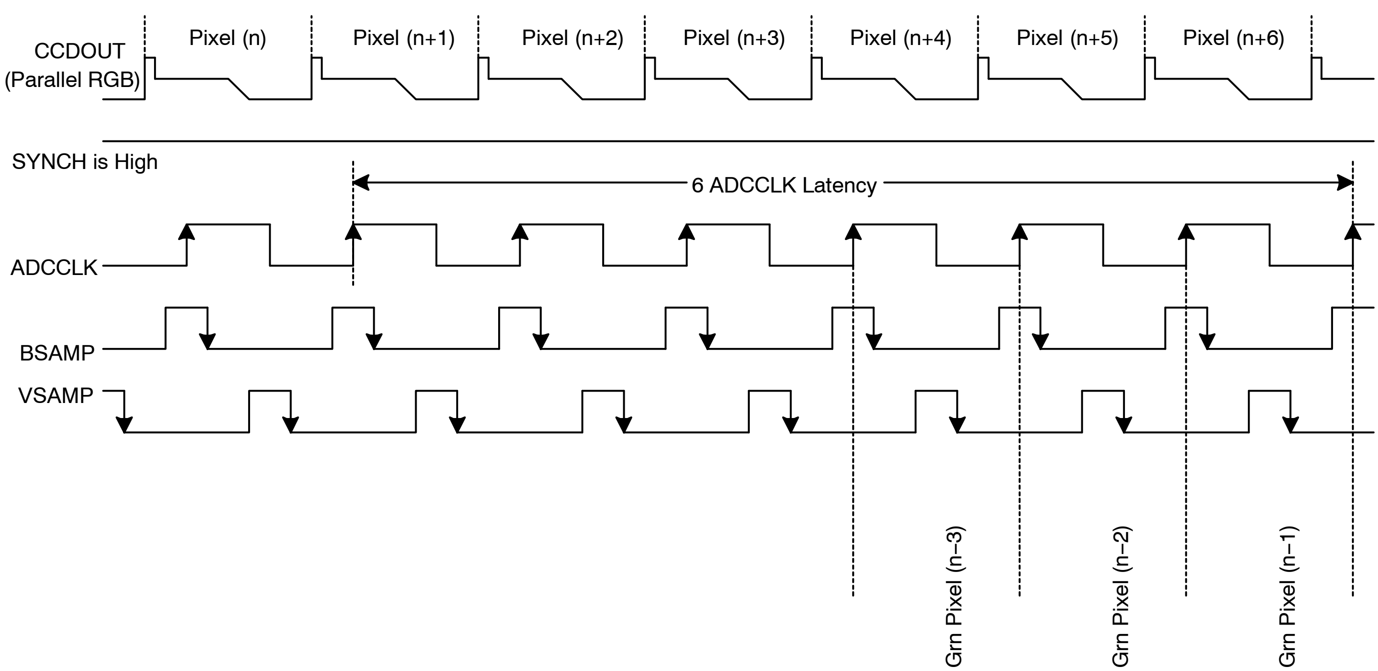


Figure 15. 1-Channel CDS Pixel Clamp Synchronization and ADC Timing

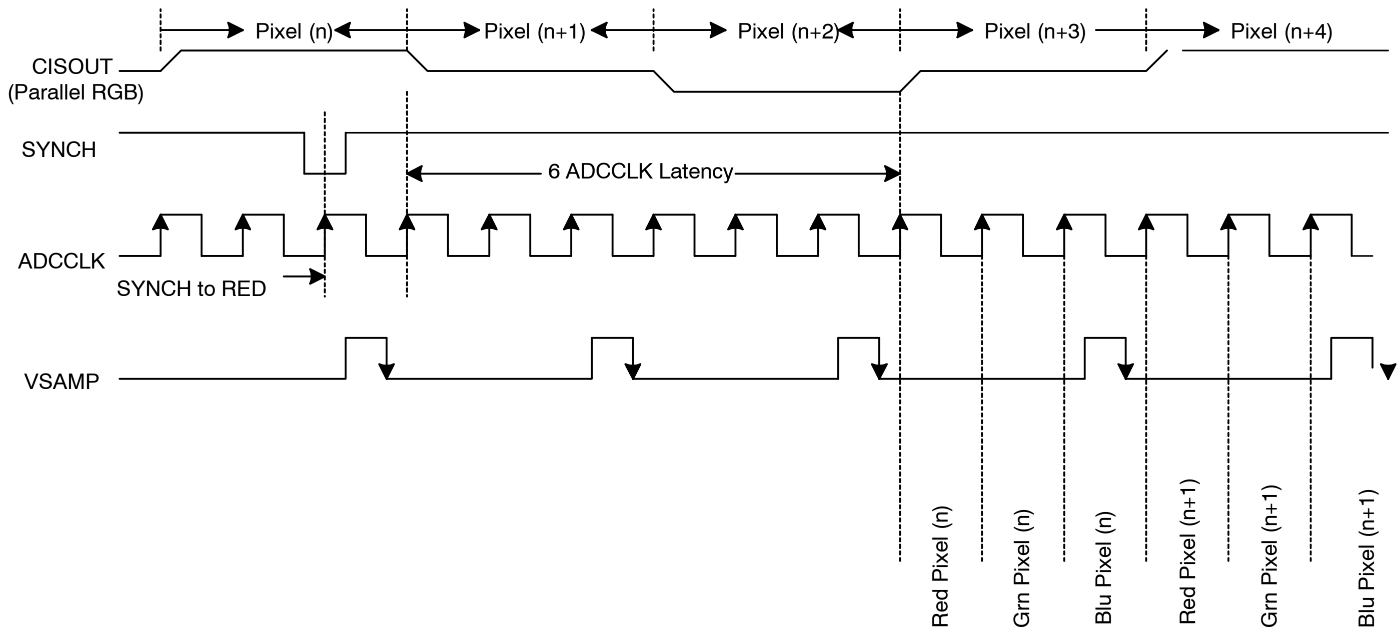


Figure 16. 3-Channel S/H Synchronization and ADC Timing

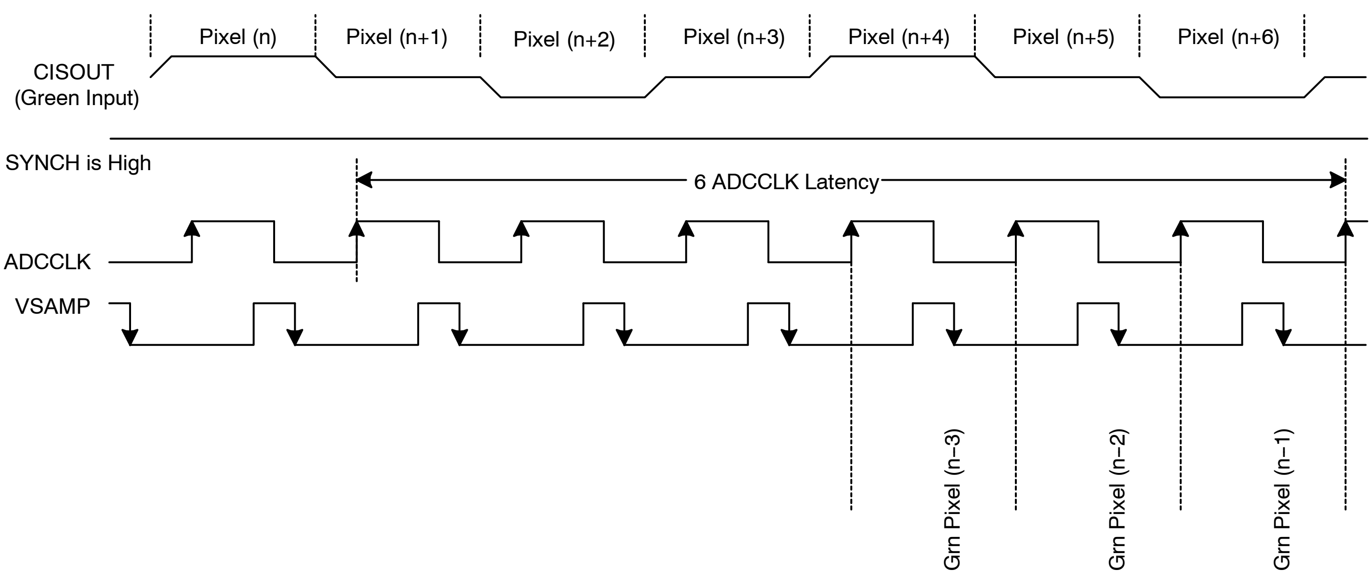


Figure 17. 1-Channel S/H Synchronization and ADC Timing

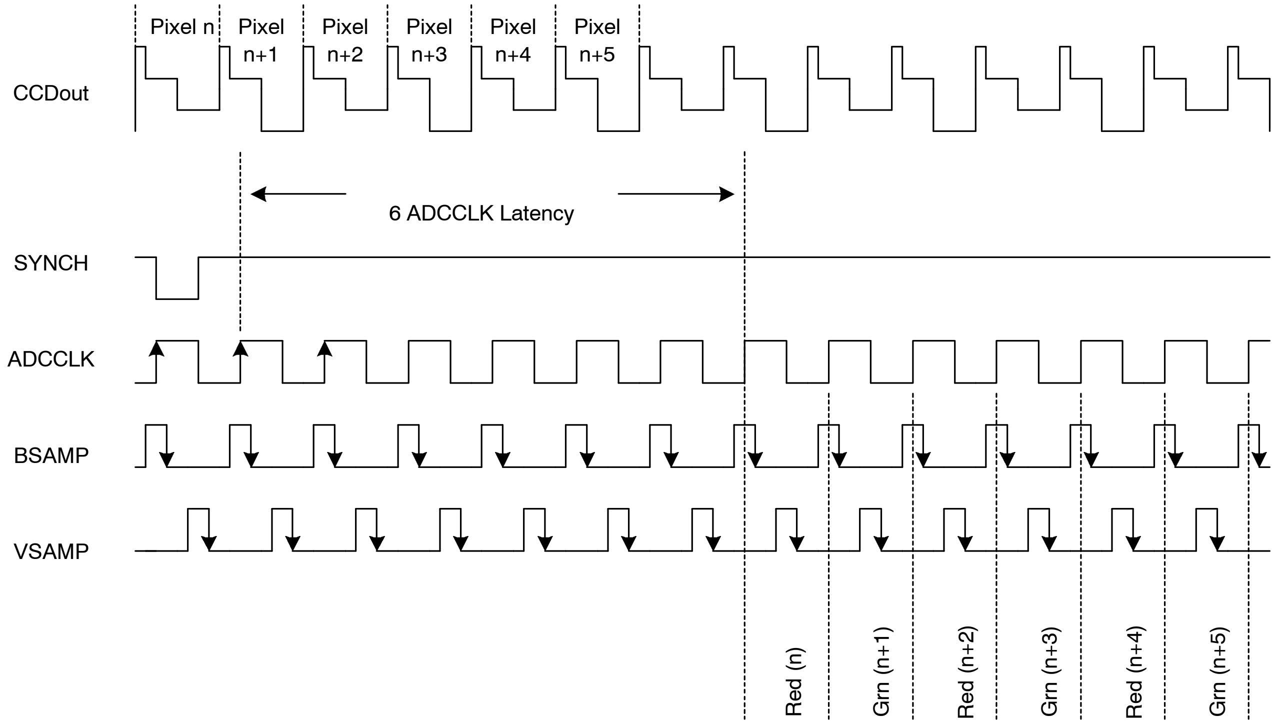


Figure 18. (A) Single Channel Bayer Mode Synchronization and ADC Timing

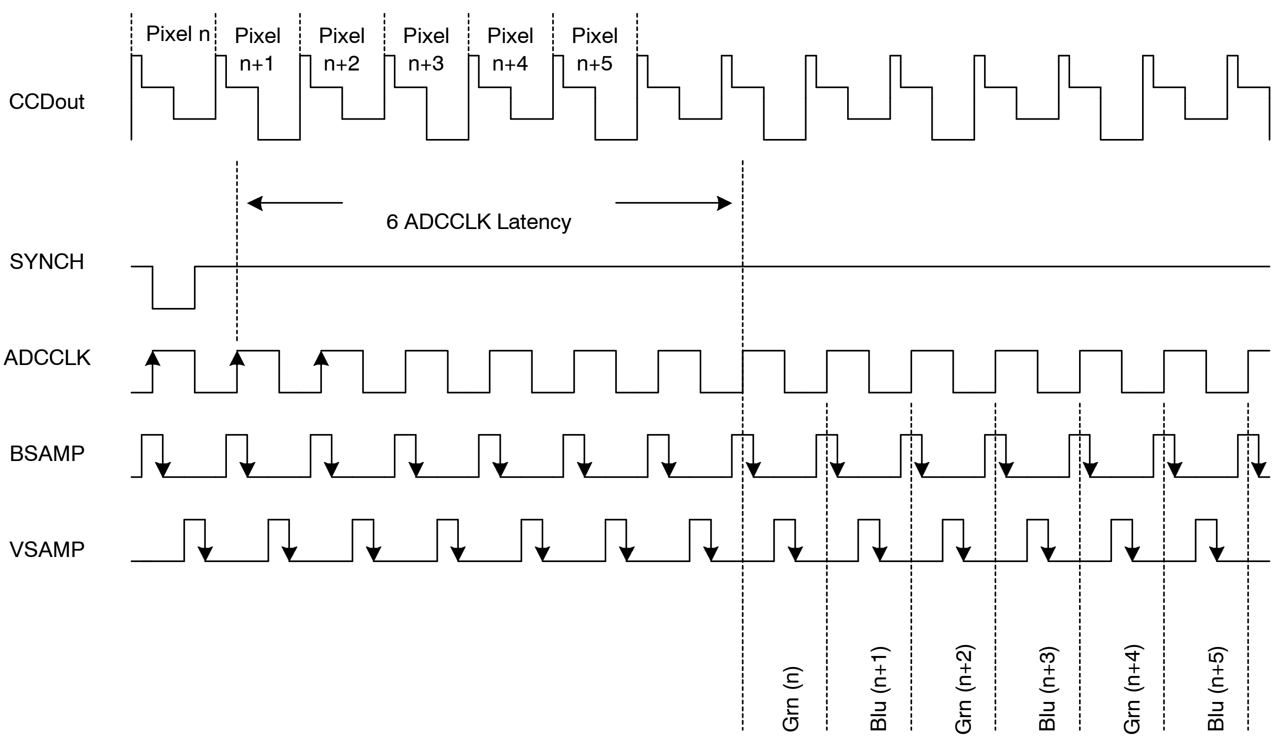


Figure 18. (B) Single Channel Bayer Mode Synchronization and ADC Timing

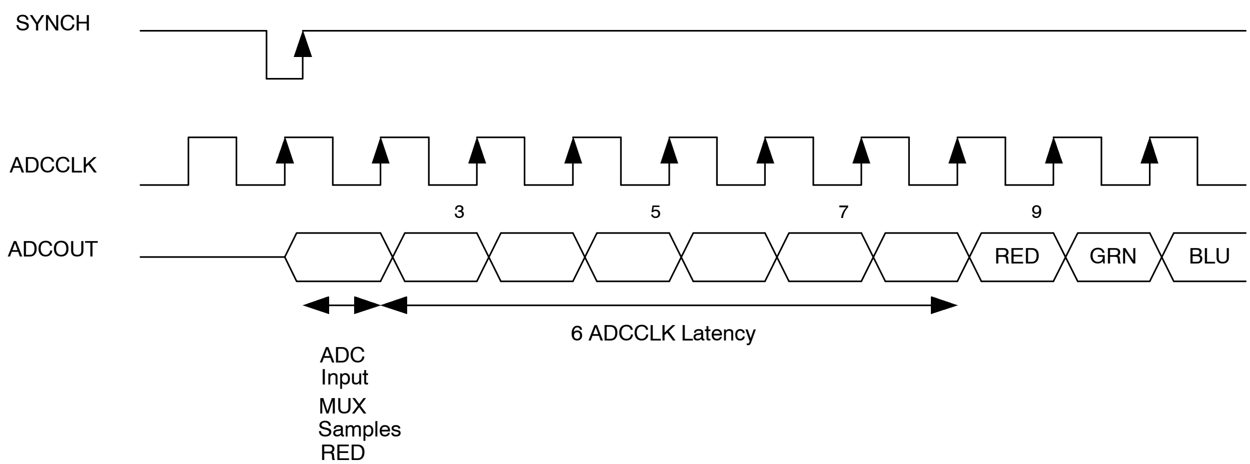
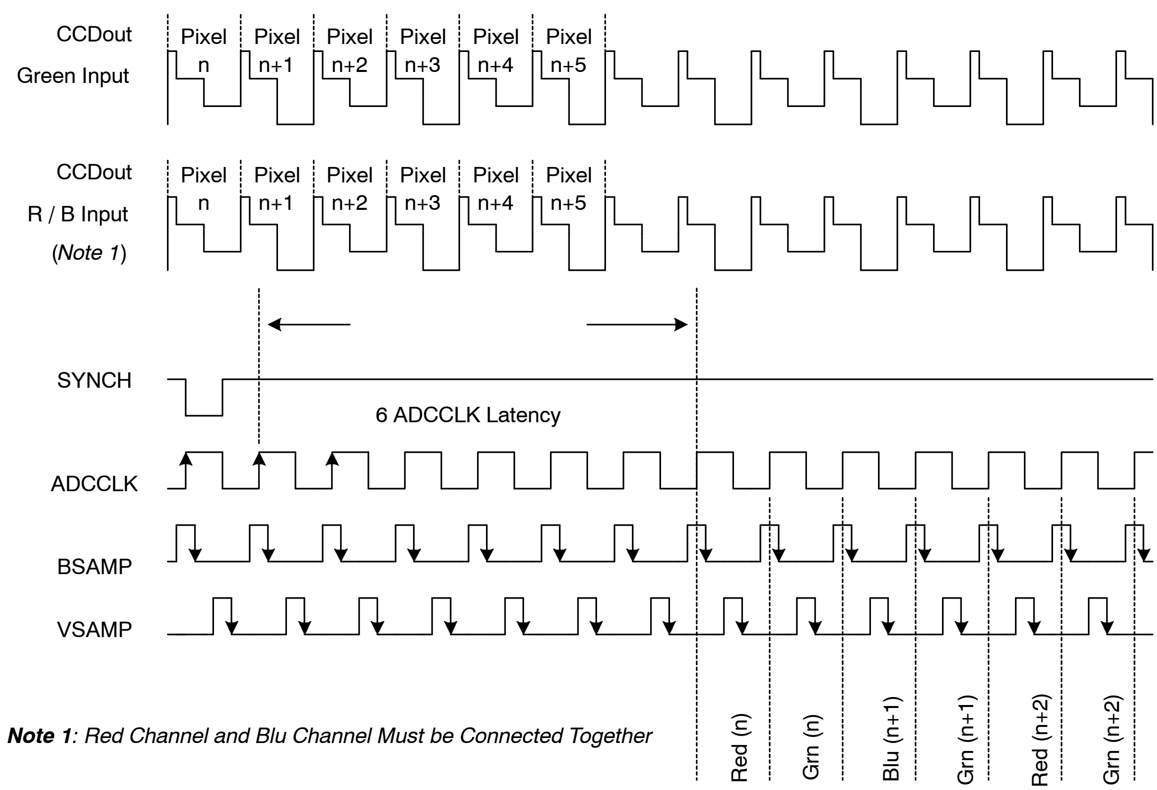


Figure 19. XRD9815 Timing For SYNCH/ADCCLK/ADCOUT



***Note 1**: Red Channel and Blu Channel Must be Connected Together*

Figure 20. 2-Channel G / RB Mode Synchronization and ADC Timing

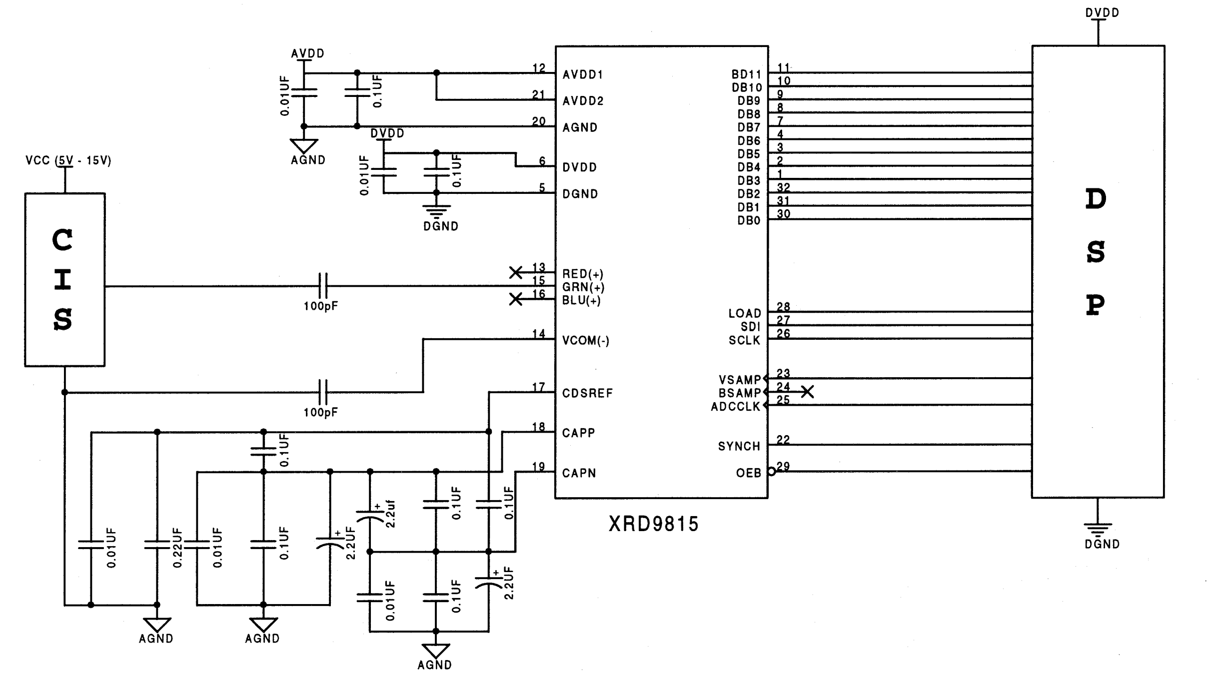


Figure 21. Application Circuit for an AC Coupled, 1-Channel Output CIS

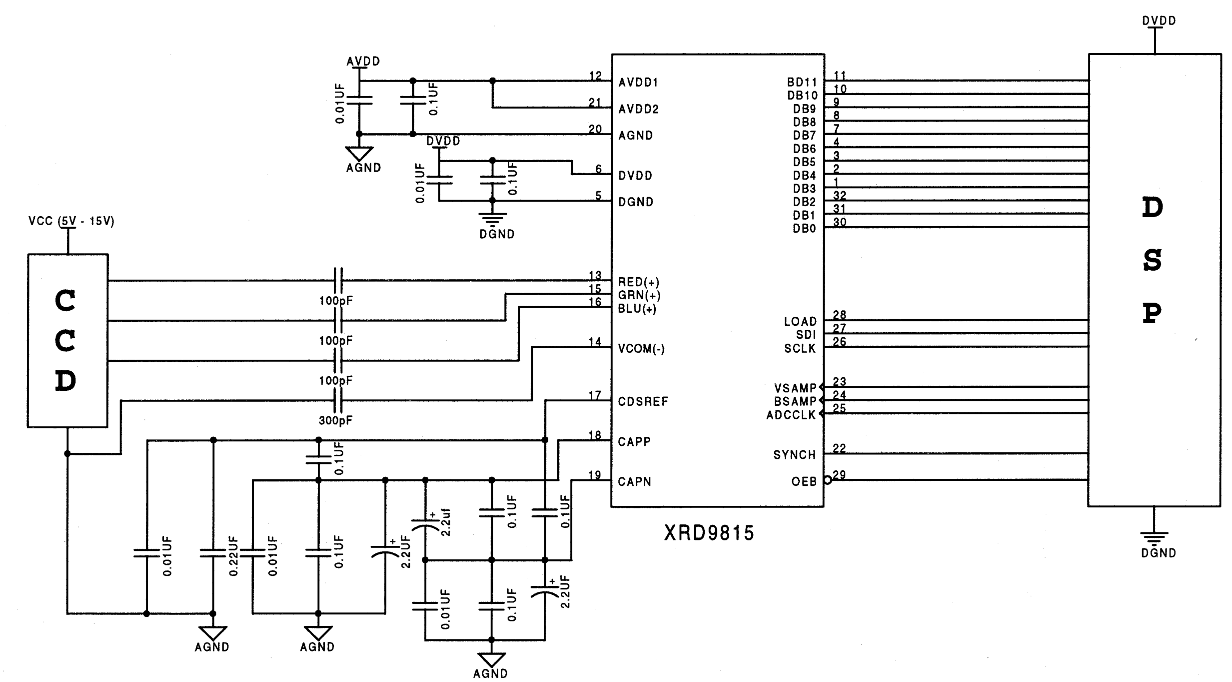
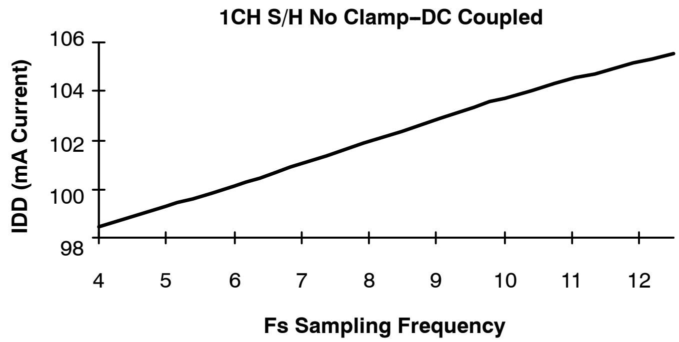
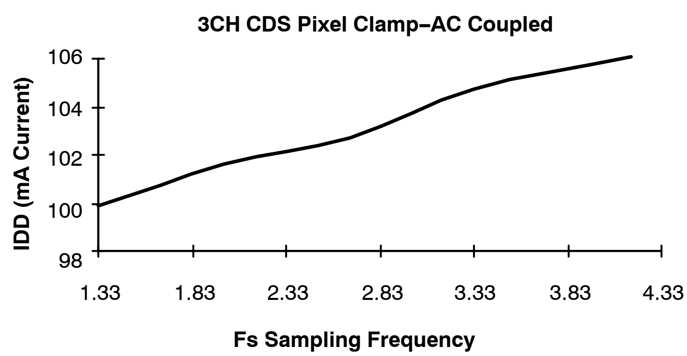


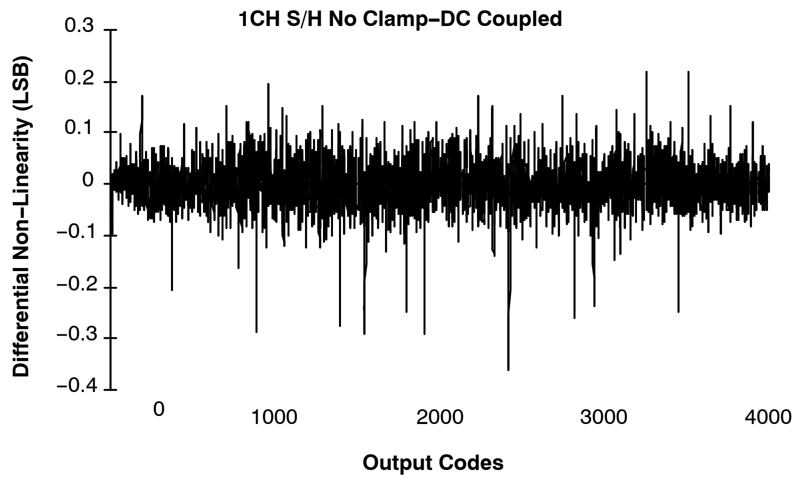
Figure 22. Application Circuit for an AC Coupled 3-Channel Output CCD with Pixel Clamp



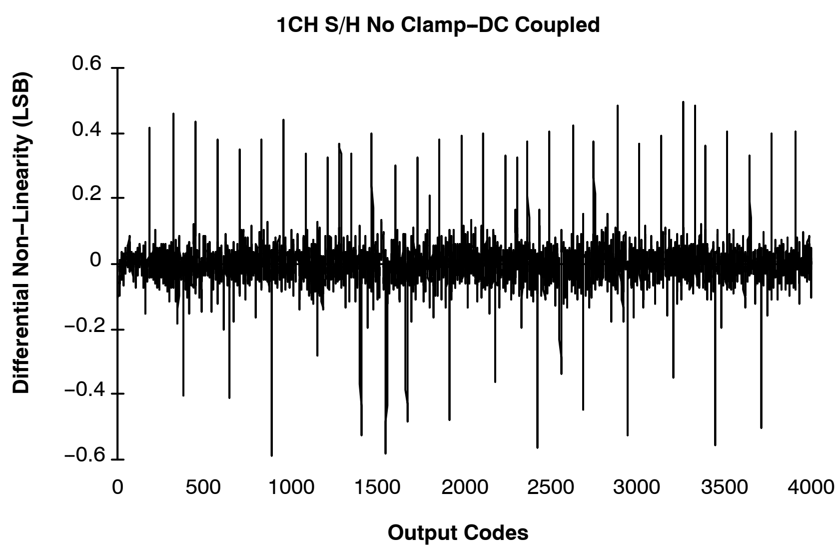
Graph 5. I_{DD} vs Sampling Frequency
1CH S/H No Clamp––DC Coupled



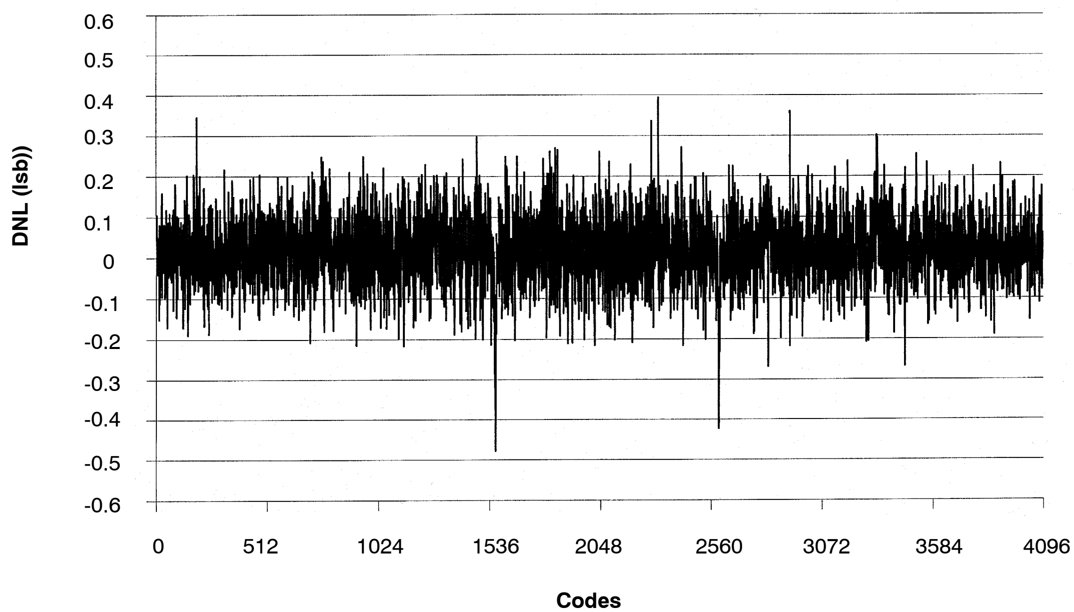
Graph 6. I_{DD} vs Sampling Frequency



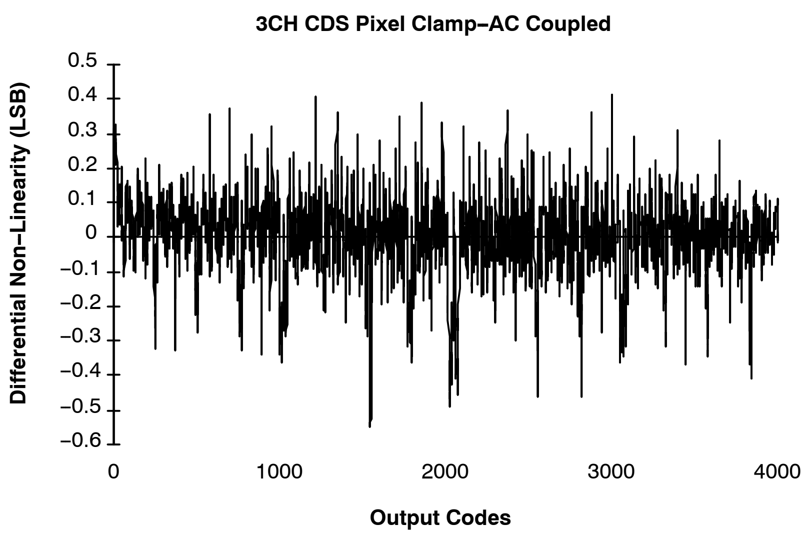
Graph 7. DNL vs Output Codes
Fs = 4 MSPS, fin = 1.0kHz



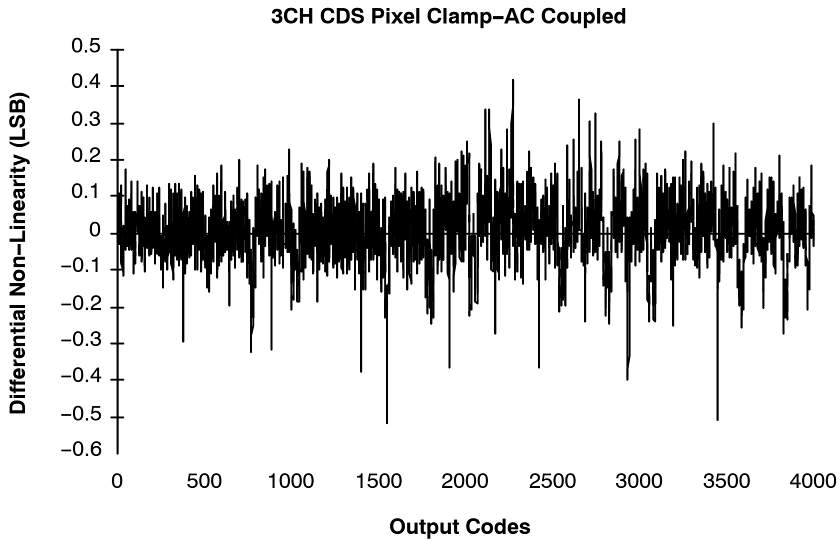
Graph 8. DNL vs Output Codes
Fs = 6 MSPS, fin = 1.0kHz



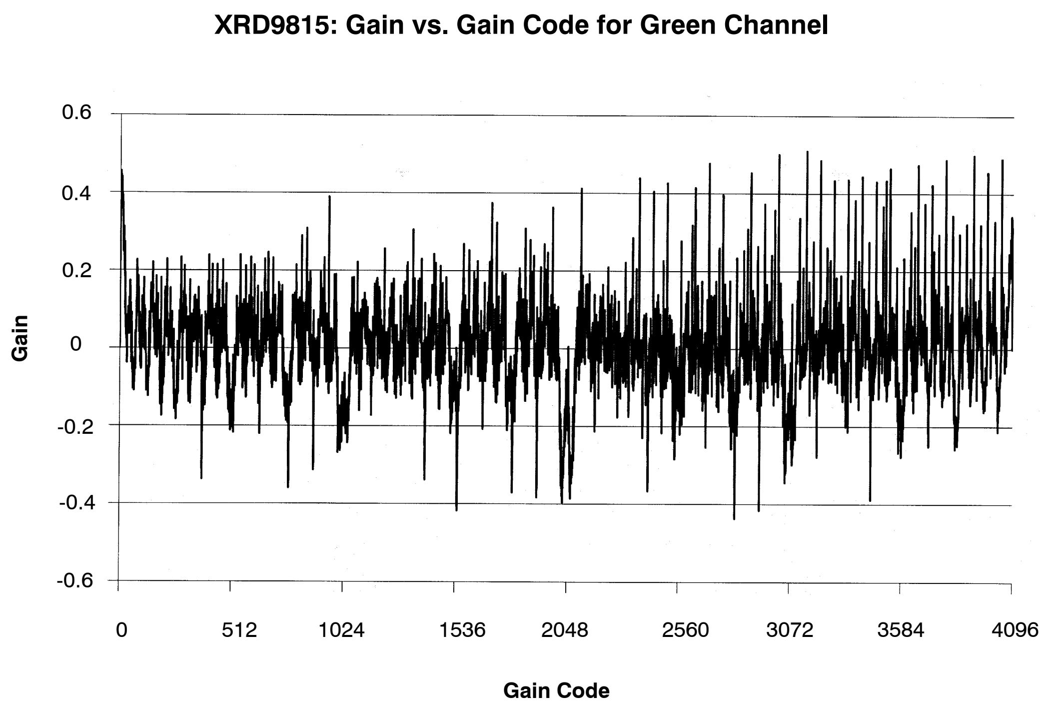
Graph 9. DNL Fs = 9 MSPS, fin = 1.0kHz



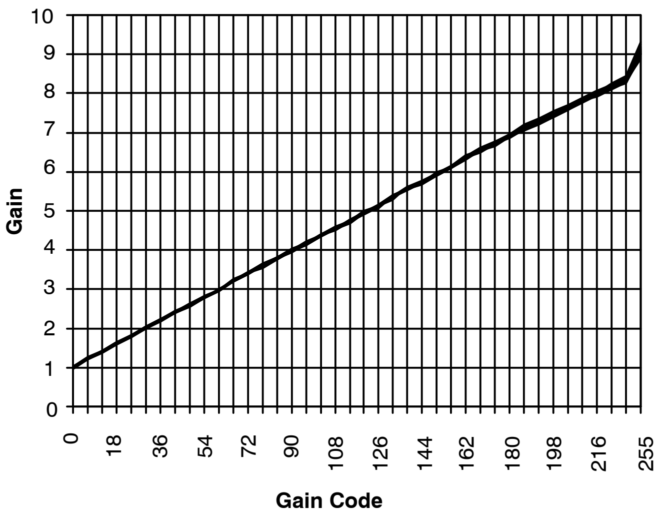
Graph 10. DNL vs Output Codes
Fs = 9 MSPS, fin = 1.0kHz



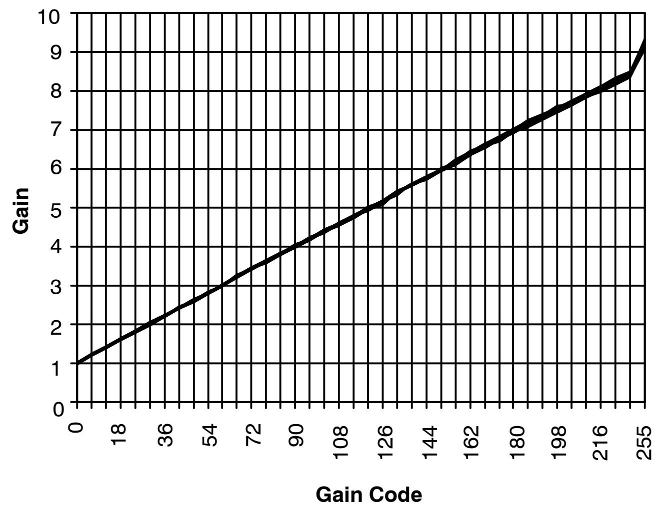
Graph 11. DNL vs Output Codes
Fs = 12 MSPS, fin = 1.0kHz



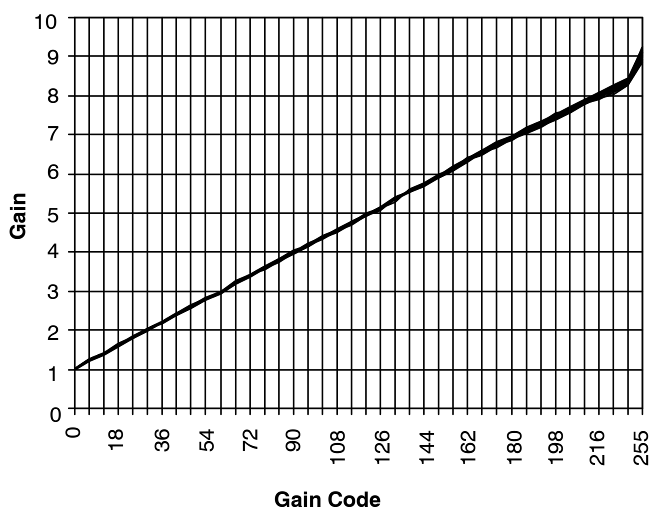
Graph 12. Gain vs Gain Code for Green Channel



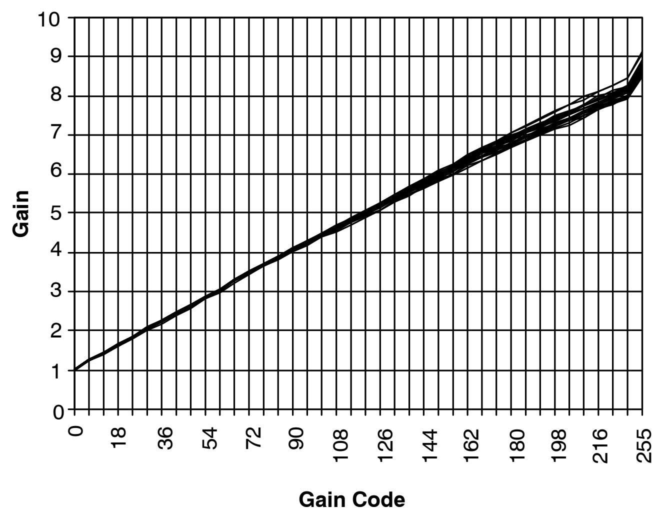
Graph 13. XRD9815 3–Channel S/H Mode 9MHz Gain vs Gain Code (Red)



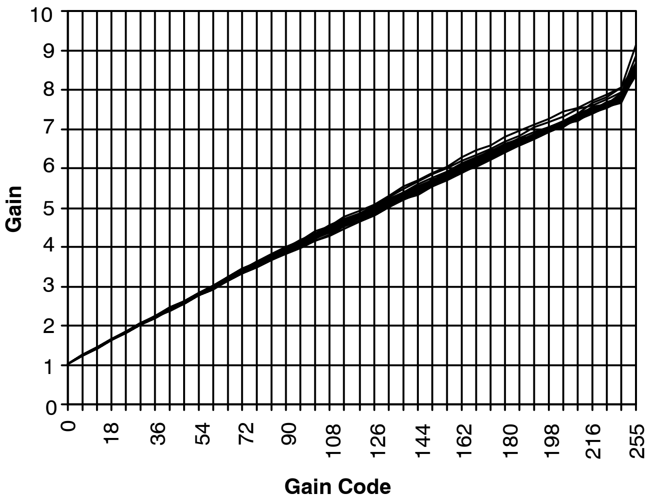
Graph 14. XRD9815 3–Channel S/H Mode 9MHz Gain vs Gain Code (Green)



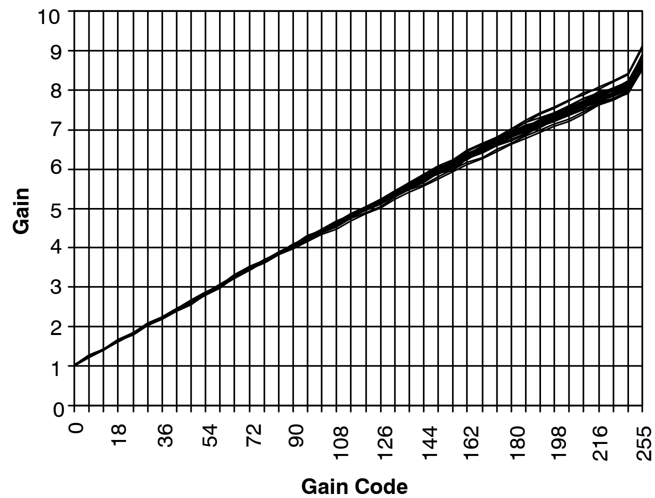
Graph 15. XRD9815 3–Channel S/H Mode 9MHz Gain vs Gain Code (Blue)



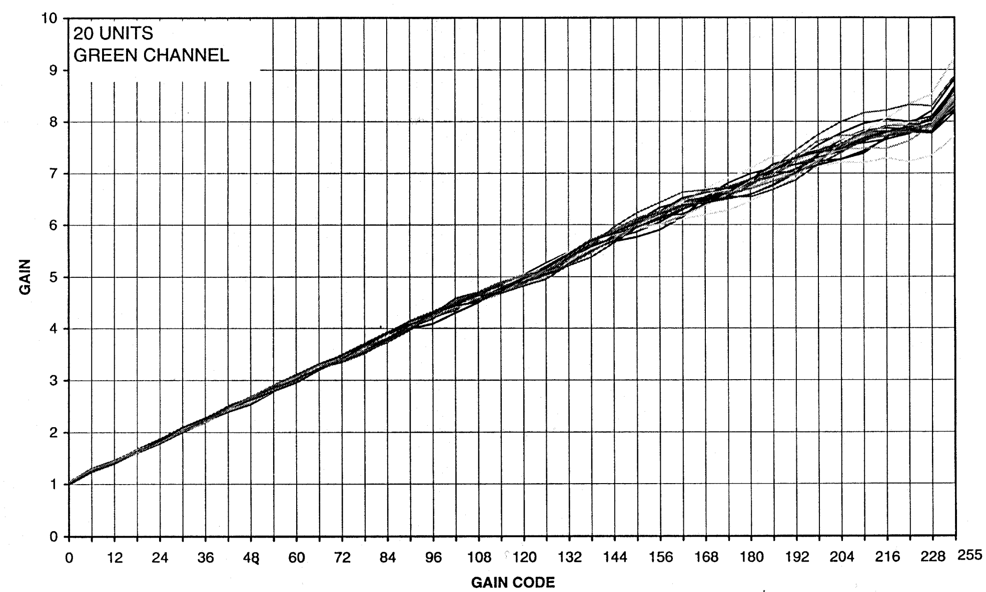
Graph 16. XRD9815 3–Channel S/H Mode 12MHz Gain vs Gain Code (Red)



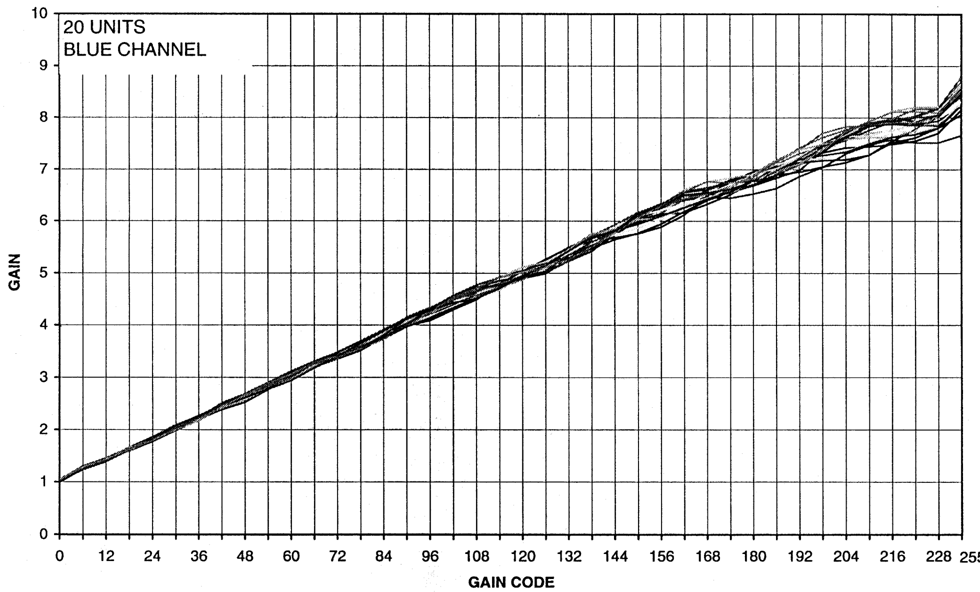
Graph 17. XRD9815 3–Channel S/H Mode 12MHz Gain vs Gain Code (Green)



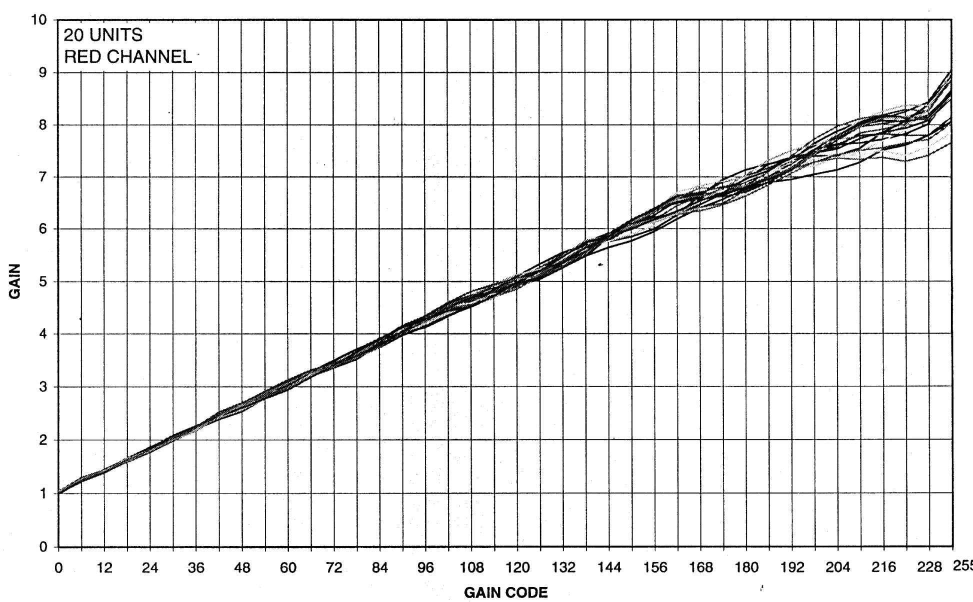
Graph 18. XRD9815 3–Channel S/H Mode 12MHz Gain vs Gain Code (Blue)



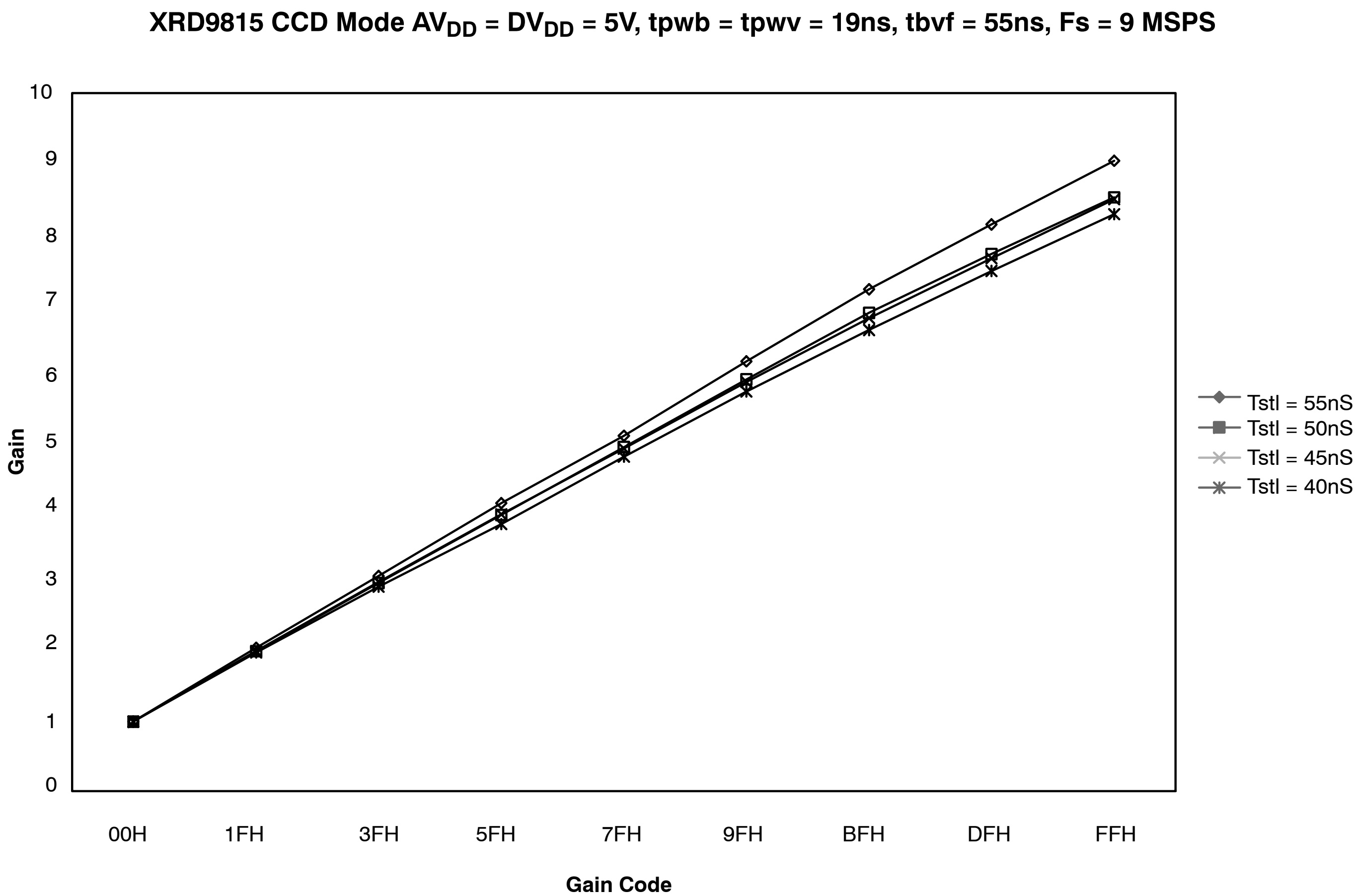
Graph 19. XRD9815 3–Channel S/H Mode 13.5MHz Gain vs Gain Code



Graph 20. XRD9815 3–Channel S/H Mode 13.5MHz Gain vs Gain Code

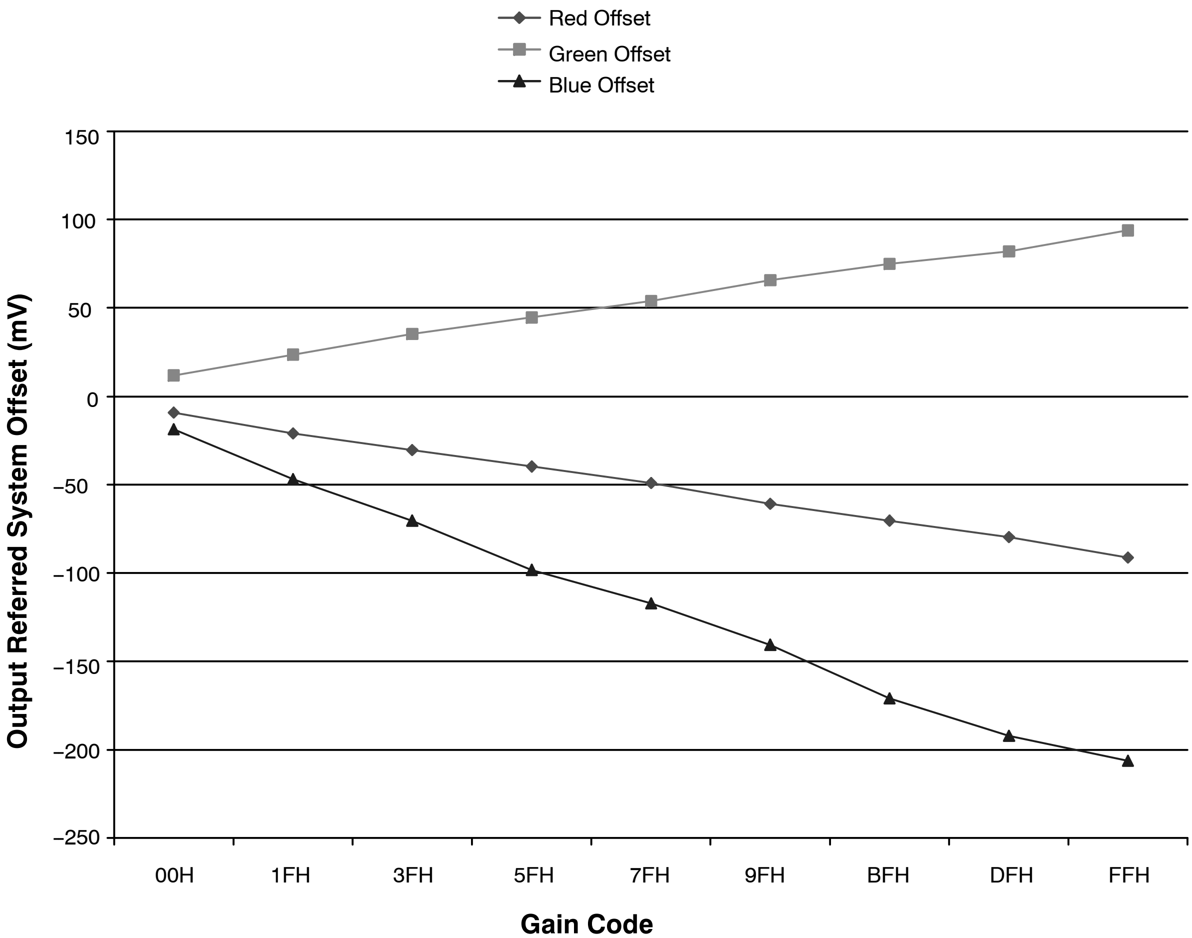


Graph 21. XRD9815 3–Channel S/H Mode 13.5MHz Gain vs Gain Code



Graph 22. Gain vs. Gain Code for Different Settling Time (tstl) for All Channels

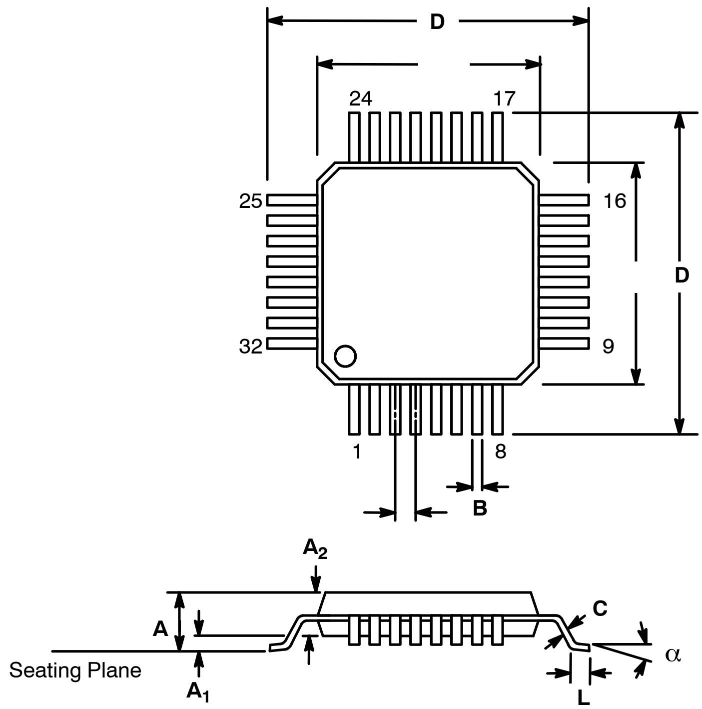
XRD9815 3CH CCD, $AV_{DD} = DV_{DD}$ = 5V, Fs = 12MSPS, PIXEL RATE = 4MSPS, 3Vpp, VCOM CAP = 0.03uF, All Inputs to AGND with 0.01uF CAP



Graph 23. System Offset vs. Gain

32 LEAD THIN QUAD FLAT PacK (7 x 7 x 1.4 mm TQFP)

Rev. 2.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D_1	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

NOTICE