

GENERAL DESCRIPTION

The XR-T5794 demo board is a 4.75 x 9.75 double-sided circuit card that provides the support circuitry necessary for a comprehensive evaluation of the XR-T5794 CMOS Quad E1 Line Interface IC. three board-mounted DIP switches allow complete testing of all loop back, monitor, and transmitter power-down features. The demo board is normally supplied configured for 120Ω balanced E1 operation. However, the information contained in this manual enables the user to modify the hardware for E1 unbalanced 75Ω cable service, or T1 balanced 100Ω use.

BOARD OPERATION

Figures 1, 2 and Table 2 are the board component layout, circuit diagram, and parts list respectively. The Demo Board uses the same pin function and signal names as the XR-T5794 data sheet. This user's manual is designed to be used in conjunction with the XR-T5794 data sheet. The following description is for a demo board set up for balanced 120 Ω E1 use. It also applies to the other modes of operation if the appropriate impedance, cable type, and signal source changes are made.

Power Requirements

Power connections are made to banana jacks located in the upper left hand corner of the board. Power supply requirements are:

$$\begin{aligned} V_{DD} &= +5.0 \text{ V} && 5\% \text{ at } 850 \text{ mA maximum} \\ V_{SS} &= -5.0 \text{ V} && 5\% \text{ at } 850 \text{ mA minimum} \end{aligned}$$

Line-Side Signals

Receiver signal inputs are labeled RXIN1 through RXIN4 for the four channels. The connectors supplied for

balanced 120Ω operation are one quarter inch, 3-circuit audio type jacks. Equipment connections should be made with shielded twisted pair patch cords. The signal applied to any inputs must be a CCITT G.703 compliant pulse that may be attenuated by a twisted-pair cable. The XR-T5794 exceeds G.703 maximum cable loss of requirement of 6.0 dB at 1.024 MHz.

Similarly, transmitter outputs are labeled TXOUT1 through TXOUT4 for the four channels. The monitor channel output is labeled MONOUT. Connector types and connection methods are identical to those specified above for the receive side. The transmitter output, when terminated by a 120Ω resistor, is a pulse meeting the G.703 template requirements. During demo board evaluation, all transmitters, including the monitor channel, that are not powered down should be connected to either a properly terminated cable, a piece of test equipment containing a termination, or a 120Ω load resistor.

Equipment-Side Signal Connections

For convenience, access to the logic-level equipment-side signals is provided by two groups of turret terminals and also by two ribbon cable connectors. The terminals are convenient for simple tests while the ribbon cable connectors reduce the amount of wiring necessary to connect the entire equipment side of the demo board to customer equipment.

Header P1 and a group of terminals that provide channel 1 and 2 I/O are located below the XR-T5794. For channels 3 and 4, P2 and a second group of pins are located above the XR-T5794. P1 and P2 are dual-row 26 pin headers with only the odd-numbered pins used to carry signals. Even-numbered pins are grounded to minimize ribbon cable crosstalk. Pin 13 is also grounded to provide isolation between the transmit and receive directions.

For P1 and P2 respectively, Table 1 and 2 presented below give the header pin, signal symbol, the corresponding XR-T5794 pin, and a brief description of the signal present.

P1 Pin	Symbol	T5794 Pin	Signal Description
1	LOS1	39	Channel 1 - Receive Loss of Signal Output
3	LOS2	40	Channel 2 - Receive Loss of Signal Output
5	RXNEG1	45	Channel 1 - Receive Negative Rail Output
7	RXPOS1	46	Channel 1 - Receive Positive Rail Output
9	RXNEG2	47	Channel 2 - Receive Negative Rail Output
11	RXPOS2	48	Channel 2 - Receive Positive Rail Output
15	TXNEG1	53	Channel 1 - Transmit Negative Rail Input
17	TXPOS1	54	Channel 1 - Transmit Positive Rail Input
19	TXCLK1	55	Channel 1 - Transmit Clock Input
21	TXNEG2	56	Channel 2 - Transmit Negative Rail Input
23	TXPOS2	57	Channel 2 - Transmit Positive Rail Input
25	TXCLK2	58	Channel 2 - Trnasmit Clock Input

Table 1. Header P1 - Channel 1 and 2 Equipment Side I/O Connections

P2 Pin	Symbol	T5794 Pin	Signal Description
1	TXCLK4	12	Channel 4 - Transmit Clock Input
3	TXPOS4	13	Channel 4 - Transmit Positive Rail Input
5	TXNEG4	14	Channel 4 - Transmit Negative Rail Input
7	TXCLK3	15	Channel 3 - Transmit Clock Input
9	TXPOS3	16	Channel 3 - Transmit Positive Rail Input
11	TXNEG3	17	Channel 3 - Transmit Negative Rail Input
15	RXPOS3	22	Channel 3 - Receive Positive rail Output
17	RXNEG3	23	Channel 3 - Recevie Negative Rail Output
19	RXPOS\$	24	Channel 4 - Receive Positive Rail Output
21	RXNEG4	25	Channel 4 - Receive Negative Rail Output
23	LOS4	30	Channel 4 - Receive Loss of Signal Output
25	LOS3	31	Channel 3 - Receive Loss of Signal Output

Table 2. Header P2 - Channel 3 and 4 Equipment Side I/O Connections

Equipment-Side Signal Characteristics

All equipment-side connections at P1 and P2 are TTL logic-level compatible for the inputs and outputs. Specific signal types present at these pins are as follows.

LOS1 Through LOS4

These pins are the loss signal outputs (LOS) for the receive channels. A LOS output will go to a logic 1 state when the input applied to the corresponding receiver is less than the LOS threshold voltage.

RXPOS1 Through RXPOS4

The signal present at these pins is the positive half of the dual-rail receive data. A positive bipolar input pulse at a receiver input will produce a positive-going pulse at the corresponding RXPOS output. Data pulse width at an RXPOS output is approximately equal to the width of the pulse applied to the receiver input at its 50% amplitude point.

RXNEG1 Through RXNEG4

The signal present at these pins is the negative half of the dual-rail receive data. A negative bipolar input pulse at a receiver input will produce a positive-going pulse at the corresponding RXNEG output. Data pulse width is the same as described above for the RXPOS output.

TXCLK1 Through TXCLK4

These pins are the transmit clock inputs of four transmit channels. For a specific channel, TXCLK is a 2.048 MHz 50% duty cycle square wave that is synchronized with the data to be transmitted over that channel.

TXPOS1 Through TXPOS4

These pins are the positive rail inputs for the dual-rail transmit data for the four transmit channels. A positive-going pulse at a TXPOS input will produce a positive bipolar output pulse at the corresponding

transmitter output. The signal applied to a TXPOS input must be wider than the positive half cycle of the corresponding TXCLK, and must also meet the set-up and hold time specified in the XR-T5794 datasheet. When these conditions are met, the pulse width at the transmitter output TXOUT is determined by the positive going half-cycle of TXCLK.

TXNEG1 Through TXNEG4

These pins are the negative rail input for the dual-rail transmit data for the four transmit channels. A positive-going pulse at a TXNEG input will produce a negative bipolar output pulse at the corresponding transmitter output. The pulse width conditions described above for the TXPOS input also apply to TXNEG.

Operation Without TXCLK

Operation without TXCLK is possible if this pin is connected to either DGND or DVDD. Transmit output pulse width in this mode of operation is determined by the widths of the pulses applied to the TXPOS and TXNEG inputs. Therefore, the data applied to these inputs must be one-half width return-to-zero (RZ) pulses in order to produce a normal width bipolar transmit output pulse.

DIP Switch Settings

On the demo board, the logic levels presented at all control-type XR-T5794 input pins may be set with DIP switches. The following circuit is used to switch logic levels. Each IC input that is to be programmed has a 10 K Ω pull-up resistor connected to VDD. A SPAT DIP switch section is also connected between this input and ground. Therefore, when the switch lever is in the ON position as marked on the switch body, the IC input is at a Logic 0 level. For convenience, a small 1 and 0 that indicate IC pin logic level to switch position correspondence is printed on the board at the top end of each DIP switch.

Tables 3, 4 and 5, which are given below, list the switch position, XR-T5794 pin controlled, signal symbol, and function of the three demo board DIP switches.

Switch Position	IC Pin	Symbol	Switch Setting	Function
1	33	MSEL0	Off	MSEL0 = Logic 1
			On	MSEL0 = Logic 0
2	34	MSEL1	Off	MSEL1 = Logic 1
			On	MSEL1 = Logic 0
3	37	MSEL2	On	MSEL2 = Logic 1
			Off	MSEL2 = Logic 0
4 (Not Used)				

Table 3. Dip Switch S1 Functions

Switch Position	IC Pin	Symbol	Switch Setting	Function
1	61	TXEN2	Off	Transmitter 2 Output Enabled
			On	Transmitter 2 Output High Impedance
2	62	TXEN1	Off	Transmitter 1 Output Enabled
			On	Transmitter 1 Output High Impedance
3	60	ZSEL	Off	120 W Mode Selected
			On	75 W Mode Selected
4	52	LPEN2	Off	Channel 2 Loop Mode Enabled
			On	Channel 2 Normal Operation
5	51	LPEN1	Off	Channel 1 Loop Mode Enabled
			On	Channel 1 Normal Operation
6	50	E1/T1B	Off	E1 Mode Selected
			On	T1 Mode Selected
7	42	LPMOD2	Off	Channel 2 Remote Loop Back Mode Selected
			On	Channel 2 Local Loop back Mode Selected
8	41	LPMOD1	Off	Channel 1 remote Loopback Mode Selected
			On	Channel 1 Local Loop Back Mode Selected

Table 4. Dip Switch S2 Functions

Switch Position	IC Pin	Symbol	Switch Setting	Function
1	28	LPMOD3	Off	Channel 3 Remote Loop Back Mode Selected
			On	Channel 3 Local Loop Back Mode Selected
2	27	LPMOD4	Off	Channel 4 Remote Loop Back Mode Selected
			On	Channel 4 Remote Loop Back Mode Selected
3 (Not Used)				
4	19	LPEN3	Off	Channel 3 Loop Mode Enabled
			On	Channel 3 Normal Operation
5	18	LPEN4	Off	Channel 4 Loop Mode Enabled
			On	Channel 4 Normal Operation
6	10	MONEN	Off	Monitor Output Enabled
			On	Monitor Output High Impedance
7	9	TXEN3	Off	Transmitter 3 Output Enabled
			On	Transmitter 3 Output High Impedance
8	8	TXEN4	Off	Transmitter 4 Output Enabled
			On	Transmitter 4 Output High Impedance

Table 5. Dip Switch S3 Functions

HARDWARE CONFIGURATION CHANGES

This section describes hardware changes necessary for different modes of operation. It assumes that the demo board is initially configured for 120Ω balanced E1 service.

75Ω Unbalanced E1 Operation

Replace the 3-circuit audio type jacks used on the line-side inputs and outputs with BNC connectors (9 total). Wire the center pin of each BNC connector to the adjacent circuit board pad labeled 75 .

With the demo board oriented so that the power connections are in the upper left hand corner, reposition

the nine clip-on jumpers so that they now connect the top two pins on the 3-pin headers labeled E1 through E9.

Balanced or unbalanced cable operation is chosen by a clip-on jumper for each channel and by the installation the appropriate types of input and output connectors. T1/E1 rate selection is done by one DIP switch section. 100/120Ω impedance selection for balanced operation involves a resistor change.

100Ω Balanced T1 Operation

Replace 120Ω resistor R2, R4, R6 and R8, with 100Ω parts.

Replace 68Ω resistors R10, R12, R14, R16 and R18, with 62Ω parts.

Qty.	Reference	Description	Supplier
4	T1,2,3,4	Input Transformer, 1:1 Ratio	Pulse Eng. PE-65834
5	T5,6,7,8,9	Output Transformer, 1:1.266 Ratio	Pulse Eng. PE-65839
4	R1,3,5,7	75Ω, 1/4W, 1% Metal Film Resistor	
4	R2,4,6,8	121Ω, 1/4W, 1% Metal Film Resistor	
10	R9, 10, 11,12,13, 14, 15, 16, 17, 18	68.1Ω, 1/4W, 1% Metal Film Resistor	
1	R19	10 K, 2%, 5 Resistor, Thick-film Network	
2	R20, 21	10 K, 2%, 9 Resistor, Thick-film Network	
2	C1, 2	22μF, 16 V, Electrolytic, Axial LEad, 5mm Dia., 2mm Spacing	
15	C3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17	0.1 mF, 63 V, Z5U Dielectric, Axial lead, 0.1 Spacing, Panasonic	
1	S1	4-Position DIP Switch	CTS
2	S2, 3	8-Position DIP Switch	CTS
1		68 Pin PLCC Socket	Amp
2	P1, P2	26 Pin Dual-Row Header, Gold Pins	
2	P1, P2	26 Pin Ribbon Connector For Above	
9	E1, 2, 3, 4, 5, 6, 7, 8, 9	3 Pin Single-Row Header, Gold	
9	(Select option on E1 through E9)	Shorting Jumper For Above Header	
9	Line-Side signal connections	3-Conductor 1/4 Audio Jack, for 3/8 Hole (Connector for Balanced Line)	
3		Banana Jacks, red, Blue, Black	
26		(GND, VSS, VDD) Pins for Digital I/O Pads	
4		Spacers to Elevate Board	
4		4-40 x 5/16 Screws for Spacers	

Table 6. XR-T5794 Demo Board Parts List

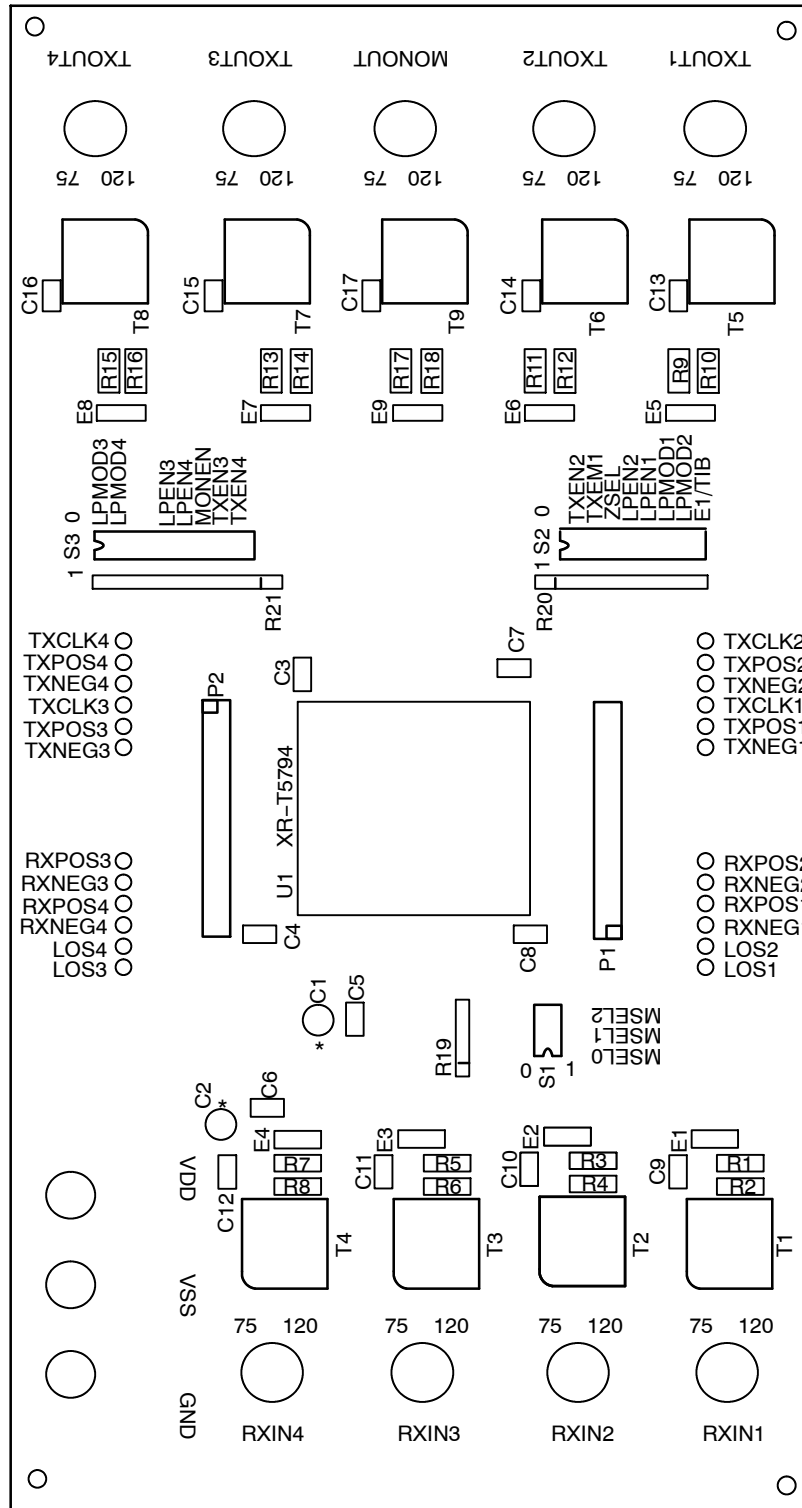


Figure 1. XR-T5794 Demo Board Component Layout

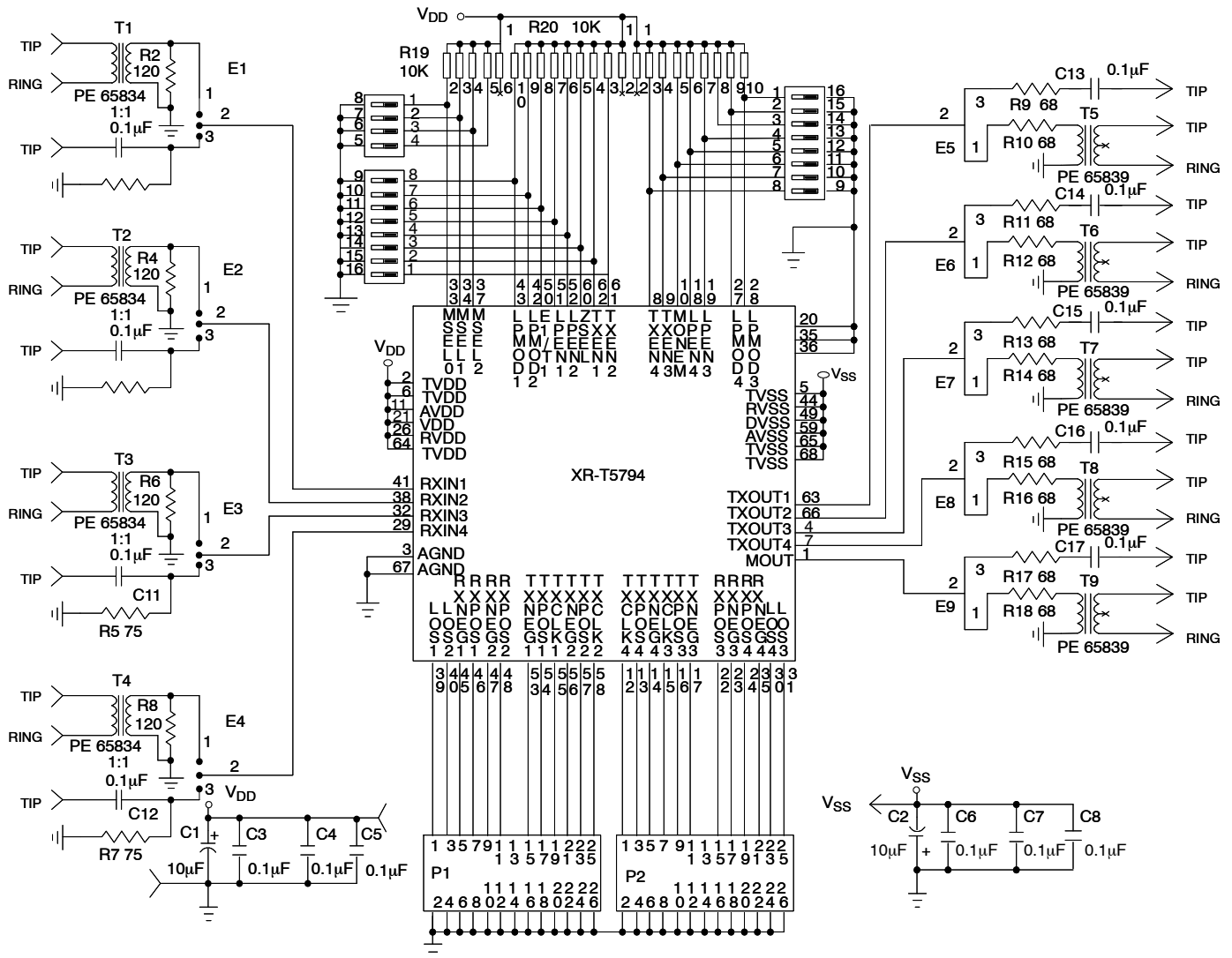


Figure 2. XR-T5794 Demo Board Circuit Diagram

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