XRT8001

XRT8001 WAN Clock

August 1999-3

FEATURES

- Programmable Output Frequencies
- Generates Output Clock Frequencies Ranging From 56kHz Up to 16.384MHz
- Low Power Operation (3.3V and 5V)
- Lock Detect Indication Pin
- Cascadable
- No External Components Needed
- Pin Compatible with the XRT8000 Device
- Operates Over the Industrial Temperature Range
- Available in an 18-Pin PDIP or SOIC Package

APPLICATIONS

- DSU's, CSU's and Access Equipment
- ISDN Terminals
- Concentrators and Multiplexers

GENERAL DESCRIPTION

The XRT8001 WAN Clock IC is a dual-phase-locked loop chip that generates two very low jitter output clock signals that can be used for synchronization applications in wide area networking systems.

The XRT8001 WAN Clock device can be configured to operate in one of six modes:

1. The Forward/Master Mode
2. The Reverse/Master Mode
3. The "Fractional T1/E1" Reverse/Master Mode
4. The "E1 to T1 - Forward/Master" Mode
5. The "High Speed - Reverse" Mode
6. The "Slave" Mode

These modes are briefly discussed on pages 8 - 14.

ORDERING INFORMATION

Part Number	Package	Operating Temperature Range
XRT8001IP	18-Lead 300 Mil PDIP	-40°C to +85°C
XRT8001ID	18-Lead 300 Mil JEDEC SOIC	-40°C to +85°C

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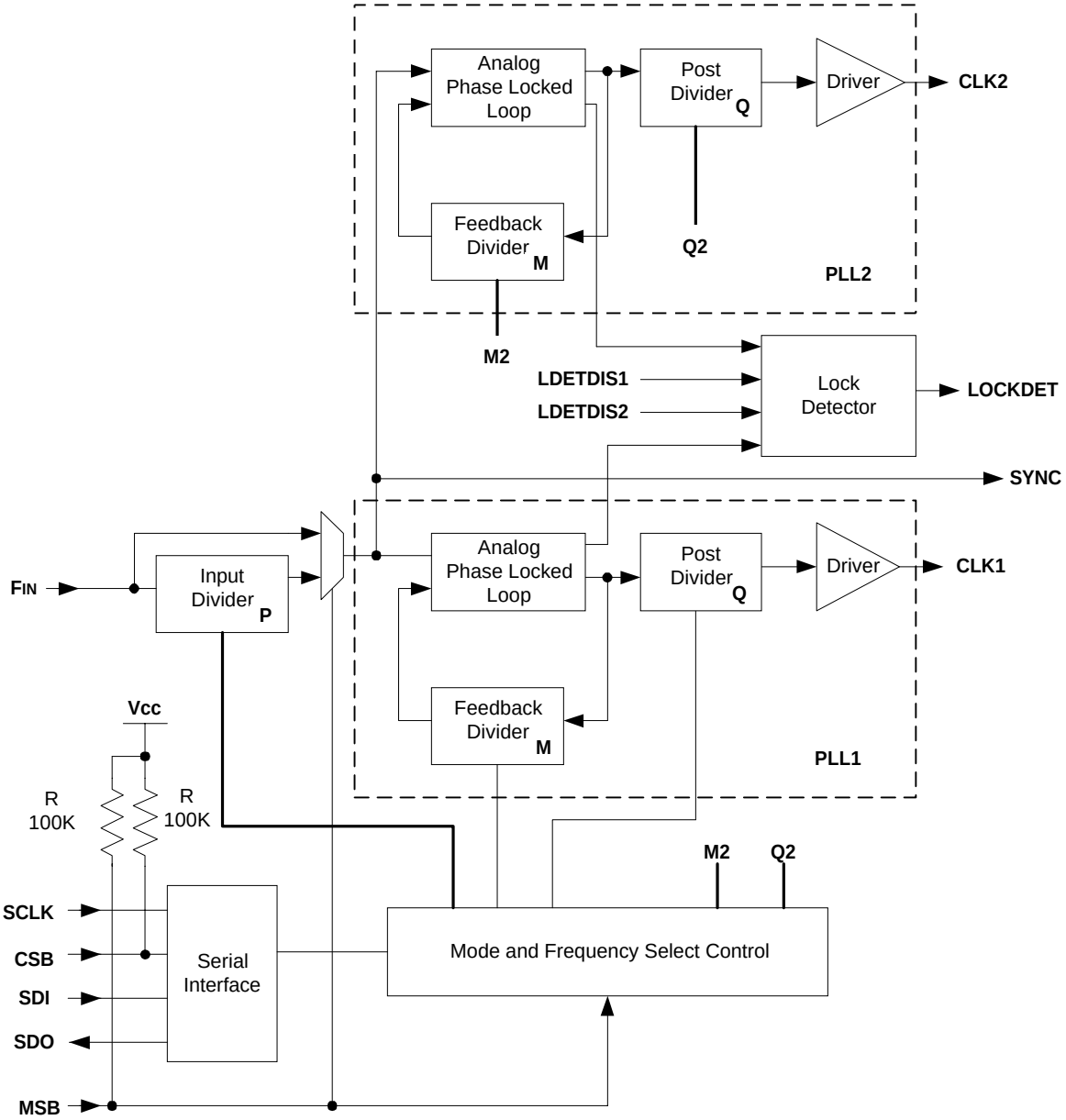
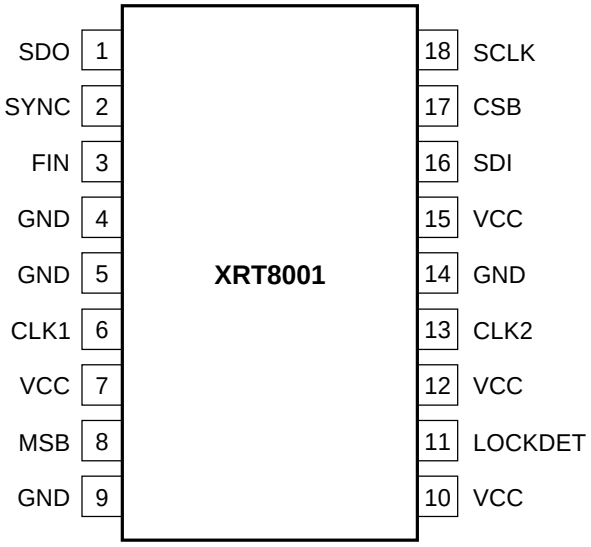


Figure 1. XRT8001 Block Diagram

PIN OUT OF THE XRT8001 DEVICE



PIN DESCRIPTION

Pin #	Name	Type	Description
1	SDO	I	**Serial Data Output from the Microprocessor Serial Interface** This pin will serially output the contents of the specified Command Register, during "Read" Operations. The data, on this pin, will be updated on the falling edge of the SCLK input signal. This pin will be tri-stated upon completion of data transfer.
2	SYNC	O	**Sync Output -** The XRT8001 will typically output an 8kHz clock signal via this output pin. However, when the XRT8001 Device is operating in the "High Speed - Reverse" Mode, then this device will simply output a 64kHz clock signal.
3	FIN	I	**Reference Clock Input -** The Reference Timing signal (from which the CLK1 and CLK2 output signals are derived) is to be input via this pin.
4	GND	-	**Digital Ground**
5	GND	-	**Digital Ground**
6	CLK1	O	**Clock Output 1 -** The XRT8001 device will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
7	VCC	-	**Digital Power Supply**

PIN DESCRIPTION (CONT'D)

Pin #	Name	Type	Description
8	MSB	I	**Master/Slave Mode Select Input -** Setting this input pin "HIGH" configures the XRT8001 device to operate in the "MASTER" Mode. Conversely, setting this input pin "LOW" configures the XRT8001 device to operate in the "SLAVE" Mode.
9	GND	-	**Analog Ground**
10	VCC	-	**Analog Power Supply**
11	LOCKDET	O	**Lock Detect Output -** This output indicates whether or not the "selected" internal PLL(s) are "in-lock" or are "out-of-lock". By default, this output pin is "high" when both PLLs are in-lock" and will go toggle "low" if either one of the PLLs is "out-of-lock". However, the XRT8001 device also permits the user to configure this output pin to reflect the state of any one of the PLLs within the chip. (See Table 3.)
12	VCC	-	**Digital Power Supply**
13	CLK2	O	**Clock Output 2 -** The XRT8001 device will drive the desired "synthesized" signal via this output pin. This output signal will have a 50±5% duty cycle. ***Note:*** *This output pin is tri-stated unless the "CLK1EN" bit-field (within Command Register CR4) has been set to "1".*
14	GND	-	**Digital Ground**
15	VCC	-	**Digital Power Supply**
16	SDI	I	**Microprocessor Serial Interface – Serial Data Input** Whenever, the user wishes to read or write data into the Command Registers, over the Microprocessor Serial Interface, the user is expected to apply the "Read/Write" bit, the Address Values (of the Command Registers) and Data Value to be written (during "Write" Operations) to this pin. This input will be sampled on the rising edge of the SCLK pin (pin 18).
17	CSB	I	**Microprocessor Serial Interface – Chip Select Input:** The Local Microprocessor must assert this pin (e.g., set it to "0") in order to enable communication with the XRT8001 via the Microprocessor Serial Interface. ***Note:*** *This pin is internally pulled "high".*
18	SCLK	I	**Microprocessor Serial Interface-Clock Signal** This signal will be used to sample the data, on the SDI pin, on the rising edge of this signal. Additionally, during "Read" operations, the Microprocessor Serial Interface will update the SDO output on the falling edge of this signal.

DC ELECTRICAL CHARACTERISTICS (Except Microprocessor Serial Interface)

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
V_{IL}	Input Low Level			0.8	V	
V_{IH}	Input High Level	2.0			V	
V_{OL}	Output Low Level (CLK1, CLK2)			0.4	V	I_{OL} = -6.0mA
V_{OH}	Output High Level (CLK1, CLK2)	2.4			V	I_{OL} = 6.0mA
V_{OL}	Output Low Level (LOCKDET, SYNC)			0.4	V	I_{OL} = -3.0mA
V_{OH}	Output High Level (LOCKDET, SYNC)	2.4			V	I_{OL} = 3.0mA
I_{IL}	Input Low Current (CSB, MSB)			-150	µA	
I_{IH}	Input High Current (CSB, MSB)			10	µA	$V_{IN} = V_{CC}$
I_{IL}	Input Low Current (except CSB, MSB)	-10			µA	
I_{IH}	Input High Current (except CSB, MSB)			10	µA	$V_{IN} = V_{CC}$
I_{CC}	Operating Current		TBD			No Load, CLk1, CLK2 = 8 x 2.048MHz
R_{IN}	Internal Pull-up Resistance (CSB, MSB)	50	100	150	kΩ	

AC ELECTRICAL CHARACTERISTICS (See Figure 2A.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t1	Input Frequency	TBD		TBD	MHz	
t2	Minimum Input Signal “High” to “Low” Duration	12			ns	
t3	Output Frequency	56		16.384	kHz	
t6[1]	Duty Cycle	47.5	50	52.5	%	VCC/2 switch point, 30pF Load
t7[4]	Jitter Added 8kHz – 40kHz	TBD	TBD	TBD	UI	Output =1.544MHz (0.025 UI)[3]
t7[4]	Jitter Added 10Hz – 40kHz	TBD	TBD	TBD	UI	Output = 1.544MHz (0.025 UI)[3]
t7[4]	Broadband Jitter		TBD	TBD	UI	Output = 1.544MHz (0.05 UI)[3]
t7[4]	Jitter Added 20Hz – 100kHz		TBD	TBD	UI	Output = 2.048MHz (1.5 UI)[3]
t7[4]	Jitter Added 18kHz – 100kHz		TBD	TBD	UI	Output = 2.048MHz (0.2 UI)[3]
t8	Capture Time			TBD	UI	
t9	Clock Output Rise Time			10ns	ns	30pF load measured at 20/80%
t10	Clock Output Fall Time			10ns	ns	30pF load measured at 20/80%
t11[2]	SYNC Output Signal Duty Cycle	40		60	%	VCC/2 switch point
t12	SYNC Ouput Signal + ½ Cycle					
t13	SYNC Output Signal – ½ Cycle					
t14	Delay Time between the rising edge of of SYNC and the Rising edge of CLK1 and CLK2	t-20		t+20	ns	See Table 8 for values of “t”

Notes:

1 $t6 = \frac{t4}{(t4 + t5)}$

2 $t11 = \frac{t12}{(t12 + t13)}$

3 *Specifications from AT&T Publication 62411 and ITU-T Recommendations G-823 (for 1.544MHz and (2.048MHz, respectively).*

4 *t7 is guaranteed by characterization, not tested.*

AC ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Units
Microprocessor Serial Interface Timing (see Figure 2B.)					
t21	CSB Low to Rising Edge of SCLK Setup Time	50			ns
t22	CSB High to Rising Edge of SCLK Hold Time	20			ns
t23	SDI to Rising Edge of SCLK Setup Time	50			ns
t24	SDI to Rising Edge of SCLK Hold Time	50			ns
t25	SCLK “Low” Time	240			ns
t26	SCLK “High” Time	240			ns
t27	SCLK Period	500			ns
t28	CSB Low to Rising Edge of SCLK Hold Time	50			ns
t29	CSB “Inactive” Time	250			ns
t30	Falling Edge of SCLK to SDO Valid Time			200	ns
t31	Falling Edge of SCLK to SDO Invalid Time			100	ns
t32	Falling Edge of SCLK, or rising edge of CSB to High Z		100		ns
t33	Rise/Fall time of SDO Output			40	ns

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
Voltage at any Pin ..... GND -0.3V to Vcc+0.3V

Operating Temperature..... - 40°C to +85°C
Storage Temperature ..... - 40°C to +85°C
Package Dissipation 500mW

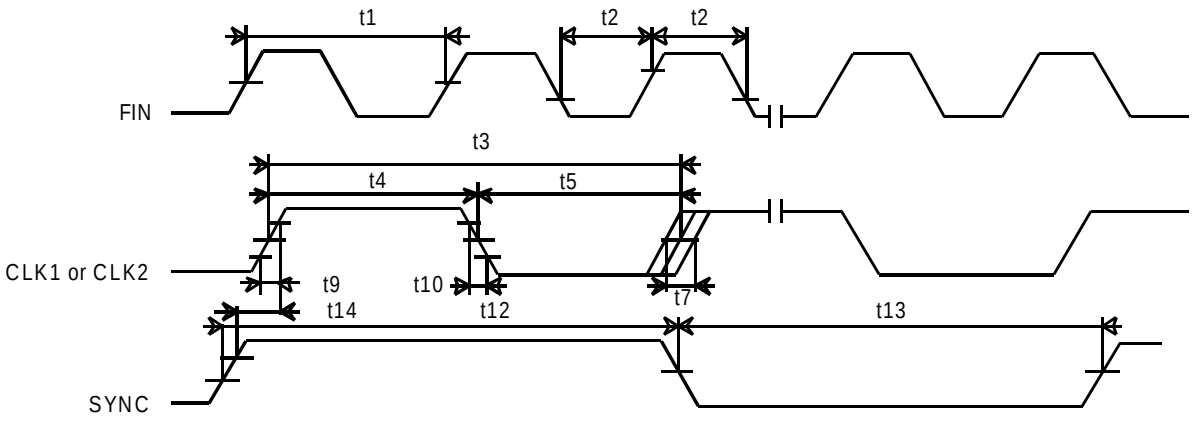


Figure 2A. Timing Diagram for Clocks

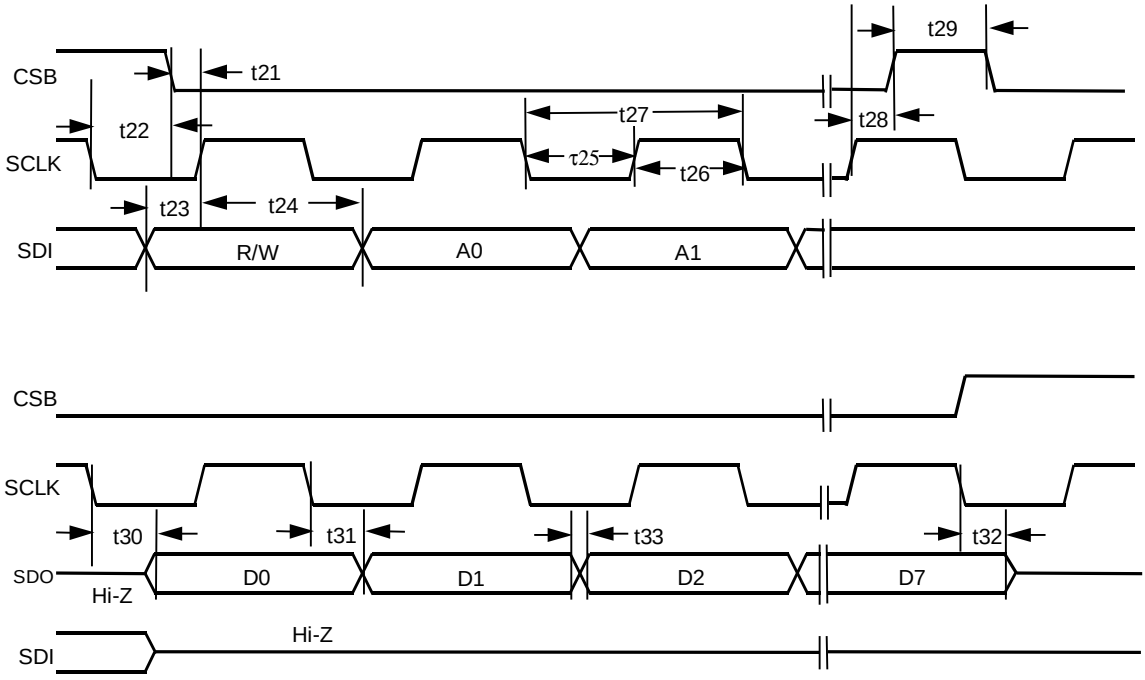


Figure 2B. Timing Diagram for the Microprocessor Serial Interface

The Forward/Master Mode

In the Forward/Master Mode, the XRT8001 Device will accept either an "N x 1.544MHz" or an "N x 2.048MHz" clock signal via the FIN input pin (where: $1 \leq N \leq 16$). From this "reference signal" the XRT8001 device will generate either a "K x 56kHz" or a "K x 64kHz" clock signal (where: $1 \leq K \leq 32$).

Figure 3, presents a simple illustration of the XRT8001 WAN Clock device operating in the "Forward Master/ Mode."

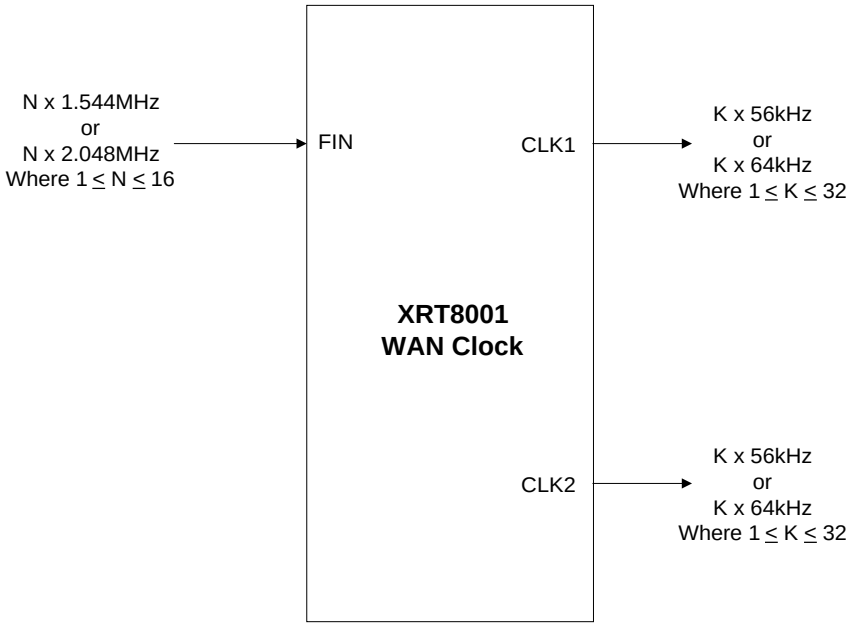


Figure 3. Illustration of the XRT8001 WAN Clock Device Operating in the Forward/Master Mode

The Reverse/Master Mode

In the Reverse/Master Mode, the XRT8001 Device will accept either a 56kHz or a 64kHz clock signal via the FIN input pin, and will generate either a 1.544MHz or a 2.048MHz clock signal via the Clock Output signals.

Figure 4, presents a simple illustration of the XRT8001 WAN Clock device operating in the “Reverse/Master Mode.”

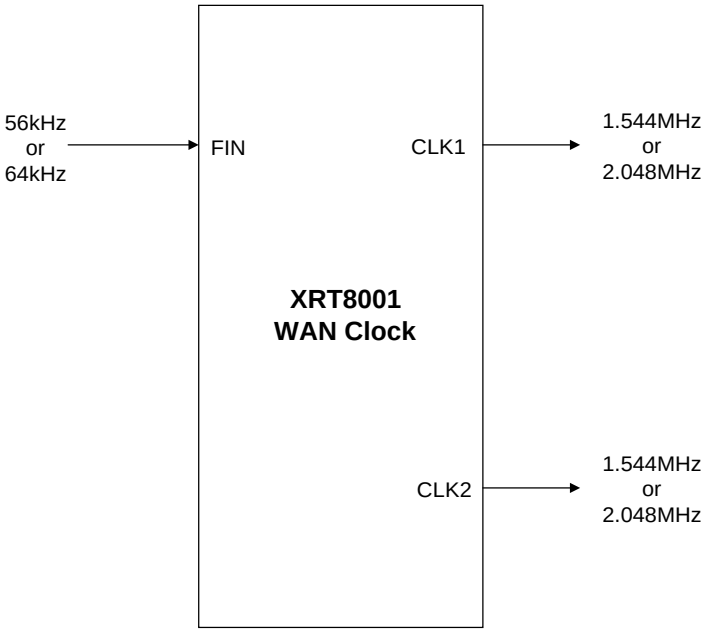


Figure 4. Illustration of the XRT8001 WAN Clock Device Operating in the Reverse/Master Mode

The Fractional T1/E1 Reverse/Master Mode

In the Fractional T1/E1 Reverse/Master Mode, the XRT8001 Device will accept either a “P x 56kHz” or a “P x 64kHz” clock signal via the FIN input pin (where: $1 \leq P \leq 32$). From this “reference signal” the XRT8001 device will generate either a 1.544MHz or a 2.048MHz clock signal.

Figure 5, presents a simple illustration of the XRT8001 WAN Clock device operating in the “Fractional T1/E1 Reverse/Master" Mode.

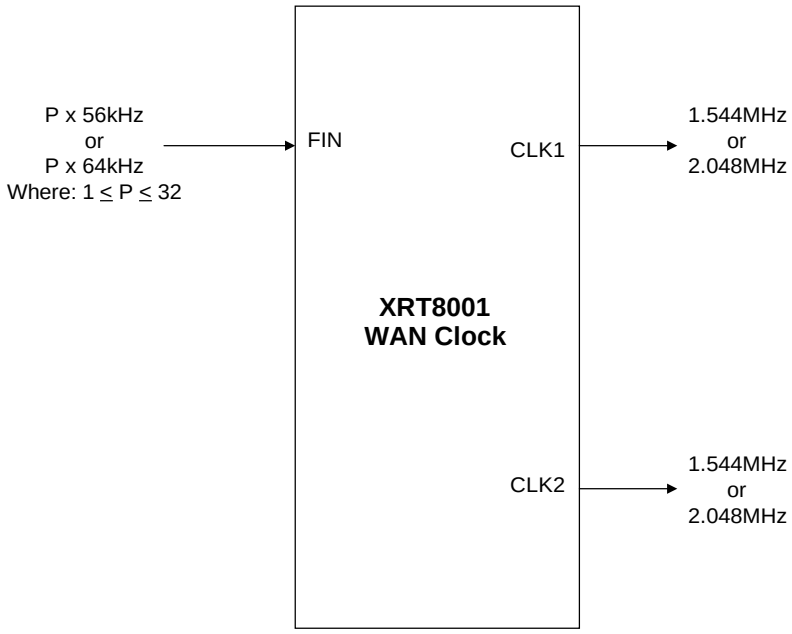


Figure 5. Illustration of the XRT8001 WAN Clock Device Operating in the “Fractional T1/E1 Reverse/Master” Mode

The “E1 to T1 Forward/Master” Mode

In the “E1 to T1 Forward/Master” Mode, the XRT8001 Device will accept a “Q x 2.048MHz” clock signal via the “Reference Clock Input" (FIN), and will output a “1.544MHz” clock signal via the CLK1 and/or CLK2 output pins.

Figure 6, presents a simple illustration of the XRT8001 WAN Clock device operating in the “E1 to T1 Forward/Master” Mode.

Note: *The value of “Q” can range between 1 and 16.*

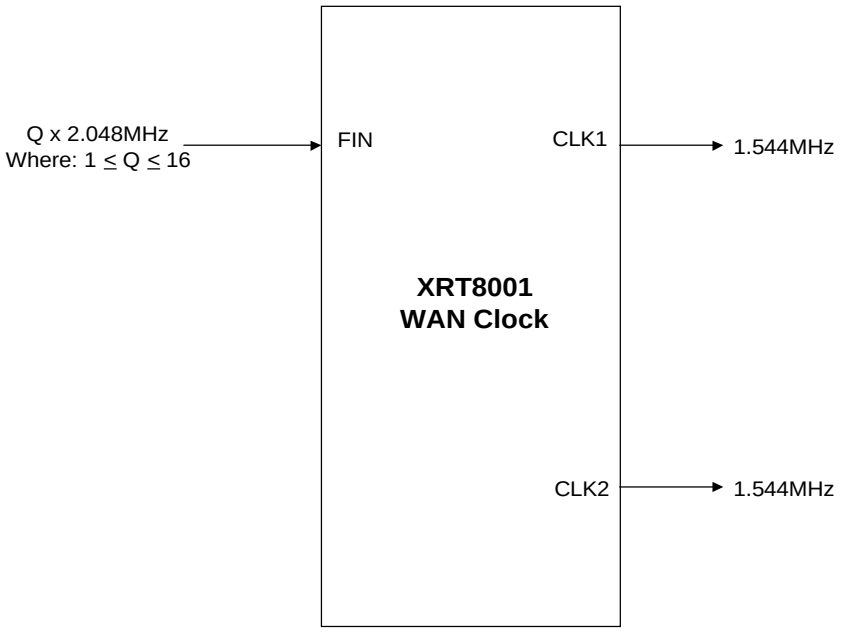


Figure 6. Illustration of the XRT8001 WAN Clock Device Operating in the “E1 to T1 Forward/Master” Mode

The “High Speed – Reverse” Mode

In the “High Speed - Reverse” Mode, the XRT8001 Device will accept a 64kHz clock signal via the “Reference Clock Input" (FIN), and will output a “M x 2.048MHz” clock signal (where M can be equal to 1, 2, 4 or 8) via the CLK1 and/or CLK2 output pins.

Note: The XRT8001 Device will accept and sythesze these clock frequencies independent of whether it has been configured to operate in the "Master" or "Slave" Modes.

Figure 7, presents a simple illustration of the XRT8001 WAN Clock device operating in the “High Speed - Reverse” Mode.

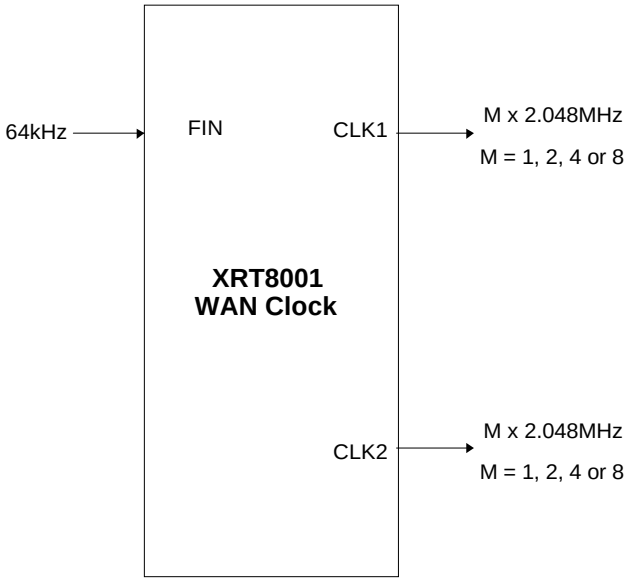


Figure 7. Illustration of the XRT8001 WAN Clock Device Operating in the “High Speed – Reverse” Mode

The "Forward/Slave" Mode

In the "Forward/Slave" Mode, the XRT8001 device will accept an 8kHz clock signal via the Reference Clock Input (FIN), and will output a "L x 64kHz or L x 56kHz" clock signal (where L can range from 1 to 32) via the CLK1 and CLK2 output pins.

Figure 8 presents a simple illustration of the XRT8001 WAN Clock device operating in the "Forward/Slave" Mode.

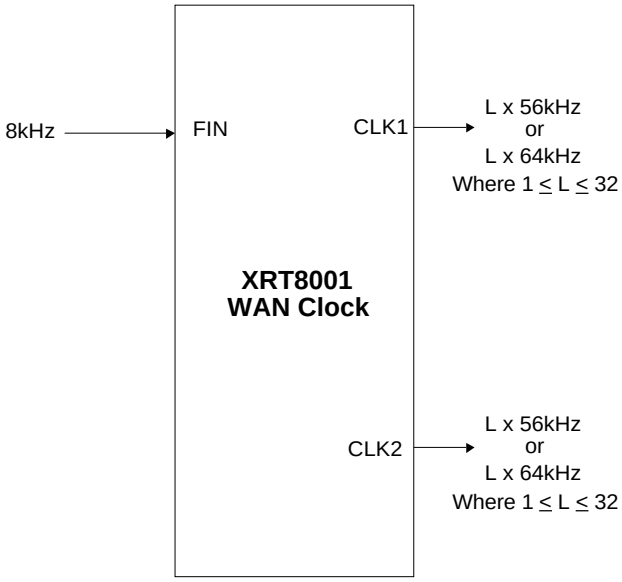


Figure 8. Illustration of the XRT8001 WAN Clock Device Operating in the "Forward/Slave" Mode

SYSTEM DESCRIPTION

1.0 Description of the Command Registers

1.1 Address Map of the "On-Chip" Command Registers

			Register Bit-Format				
Address	**Command Register**	**Type**	**D4**	**D3**	**D2**	**D1**	**D0**
0x00	CR0	R/W	IOC4	IOC3	IOC2	IOC1	PL1EN
0x01	CR1	R/W	M4	M3	M2	M1	PL2EN
0x02	CR2	R/W	SEL14	SEL13	SEL12	SEL11	SEL10
0x03	CR3	R/W	SEL24	SEL23	SEL22	SEL21	SEL20
0x04	CR4	R/W	SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
0x05	CR5	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x06	CR6	R/W	Reserved	Reserved	Reserved	Reserved	Reserved
0x07	CR7	R/W	Reserved	Reserved	Reserved	Reserved	Reserved

1.2 Command Register Description

1.2.1 Command Register CR0 (Address = 0x00)

D4 – D1 (Configuration Mode Select Bits)

These four-bit fields permit the user to select which mode the XRT8001 Device will operate in. Specifically, these four bit-fields make the following configuration selections:

1. Whether the XRT8001 Device will be operating in the “Forward/Master”, “Reverse/Master”, “Fractional T1/E1 Reverse/Master”, "E1 to T1 - Forward/Master" and “High Speed - Reverse” Modes.
2. What kind of input signals are to be applied to the Reference Clock Input (FIN).
3. What kind of signals will be output via the CLK1 and CLK2 output pins.

Table 2A relates the value of these four bit-fields to the four Master Modes and Table 2B relates to the three Slave Modes of the XRT8001 Device.

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Master	N x 1.544MHz	K x 56kHz	K x 56kHz
0001	Forward/Master	N x 1.544MHz	K x 56kHz	K x 64kHz
0010	Forward/Master	N x 1.544MHz	K x 64kHz	K x 64kHz
0011	Reverse/Master	56kHz	1.544MHz	2.048MHz
0100	Forward/Master	N x 2.048MHz	K x 56kHz	K x 56kHz
0101	Forward/Master	N x 2.048MHz	K x 56kHz	K x 64kHz
0110	Forward/Master	N x 2.048MHz	K x 64kHz	K x 64kHz
0111	Reverse/Master	64kHz	1.544MHz	2.048MHz
1000	E1 to T1 – Forward/Master	Q x 2.048MHz	1.544MHz	1.544MHz
1001	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	2.048MHz
1010	Fract. T1/E1 Reverse/Master	P x 56kHz	1.544MHz	1.544MHz
1011	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	1.544MHz
1100	Fract. T1/E1 Reverse/Master	P x 64kHz	2.048MHz	2.048MHz
1101	High Speed - Reverse	64 kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 2A. Relationship between the value of "D4 – D1 (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock Device - Master Modes

D[4:1]	Mode	Input Frequency (at the FIN input)	CLK1 Output Signal	CLK2 Output Signal
0000	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0001	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0010	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0011	Reverse/Slave	8kHz	1.544MHz	2.048MHz
0100	Forward/Slave	8kHz	K x 56kHz	K x 56kHz
0101	Forward/Slave	8kHz	K x 56kHz	K x 64kHz
0110	Forward/Slave	8kHz	K x 64kHz	K x 64kHz
0111	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1000	Reverse/Slave	8kHz	1.544MHz	1.544MHz
1001	Reverse/Slave	8kHz	1.544MHz	2.048MHz
1010	Reverse/Slave	8kHz	1.544MHz	1.554MHz
1011	Reverse/Slave	8kHz	2.048MHz	1.544MHz
1100	Reverse/Slave	8kHz	2.048MHz	2.048MHz
1101	High Speed – Reverse	64kHz	M x 2.048MHz	M x 2.048MHz
1110	Reserved	Reserved	Reserved	Reserved
1111	Reserved	Reserved	Reserved	Reserved

Table 2B. Relationship between the value of "D4 – D1" (within Command Register CR0) and the Operating Modes of the XRT8001 WAN Clock Device – Slave Modes

D0 – PL1EN (PLL # 1 Enable Select)

This bit-field permits the user to enable or disable PLL # 1, within the XRT8001 WAN Clock Device. Setting this bit-field to "1" enables PLL # 1 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 1 for Frequency Synthesis.

1.2.2 Command Register CR1 (Address = 0x01)

D4 – D1: (M4 – M1)

These bit-fields are used to support configuration implementation for both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes. In both the "Forward/Master" and "E1 to T1 - Forward/Master" Modes, the XRT8001 WAN Clock device will be receiving either a "N x 1.544MHz" or a "N x 2.048MHz" clock signal. The M4 through M1 bit-fields, within this register, permit the user to specify the value of "N". As a consequence, the XRT8001 device can be configured to accept a maximum frequency of "16 x 1.544MHz" or "16 x 2.048MHz".

D0 – PL2EN (PLL # 2 Enable Select)

This bit-field permits the user to enable or disable PLL # 2, within the XRT8001 WAN Clock Device. Setting this bit-field to "1" enables PLL # 2 for Frequency Synthesis. Conversely, setting this bit-field to "0" disables PLL # 2 for Frequency Synthesis.

1.2.3 Command Register CR2 (Address = 0x02)

D4 – D0 (SEL1[4:0])

These bit-fields are used to support configuration implementation for both the "Forward/Master", "Fractional T1/E1 Reverse/Master" and "High Speed – Reverse" Modes.

In the Forward/Master Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK1 output pin. These five (5) bit-fields within Command Register CR2 are used to define the value of "K" for the CLK1 Output. As a consequence, the XRT8001 device can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK1 output pin.

In the "Fractional T1/E1 Reverse/Master" Mode

In the "Fractional T1/E1 Reverse/Master" Mode, the XRT8001 WAN Clock will be receiving either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin. The XRT8001 WAN Clock device will, in response, generate either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 output pins. These five (5) bit-fields are used to define the value of "P". As a consequence, the XRT8001 device can be configured to accept a maximum frequency of "32 x 56kHz" or "32 x 64kHz".

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock device will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR2 are used to define the value "M" for the CLK1 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

1.2.4 Command Register CR3 (Address = 0x03)

D4 – D0 (SEL2[4:0])

These bit-fields are used to support configuration implementation for the "Forward/Master" and the "High Speed – Reverse" Modes of operation.

In the "Forward/Master" Mode

In the "Forward/Master" Mode, the XRT8001 WAN Clock will output either a "K x 56kHz" or a "K x 64kHz" clock signal via the CLK2 output pin. These five (5) bit-fields within Command Register CR3 are used to define the value of "K" for the CLK2 Output. As a consequence, the XRT8001 device can be configured to generate a maximum frequency of "32 x 56kHz" or "32 x 64kHz" via the CLK2 output pin.

In the "High Speed – Reverse" Mode

In the "High Speed – Reverse" Mode, the XRT8001 WAN Clock will be receiving a 64kHz clock signal via the "FIN" input pin. The XRT8001 WAN Clock device will, in response, generate an "M x 2.048MHz" clock via the CLK1 and CLK2 output pins. These five (5) bit-fields within Command Register CR3 are used to define the value "M" for the CLK2 output.

Note: *The only acceptable values for "M" are 1, 2, 4, or 8.*

1.2.5 Command Register CR4 (Address = 0x04)

D4 – SYNCEN (SYNC Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the SYNC output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D3 – CLK1EN (CLK1 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK1 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D2 – CLK2EN (CLK2 Output Driver Enable Select)

This "read/write" bit-field permits the user to enable or disable the Driver associated with the CLK2 output pin. Setting this bit-field to "1" enables this Driver. Setting this bit-field to "0" disables this Driver.

D1, D0 – LDETDIS[2:1] – Lock Detector Output Control

The combination of these two bit-fields permit the user to specify the signal that will be output via the LOCKDET output pin. The user's options are shown in Table 3.

LDETDIS[2:1]	Signal output via the LOCKDET Signal
00	**The LOCK Condition of PLL1 AND PLL2** With this selection, the LOCKDET output pin will be "high" if either one of the following conditions are true. a. If both PLL1 and PLL2 are in the "LOCK" condition, (**applies if both PLL1 and PLL2 are enabled**) or b. If the only enabled PLL is in the "LOCK" condition (**applies only if one of the PLLs are enabled**).
01	**The LOCK Condition of PLL2 Only** With this selection, only the "LOCK" state of PLL2 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL2 is in "LOCK". LOCKDET = "low" if PLL2 is out of "LOCK".
10	**The LOCK Condition of PLL1 Only** With this selection, only the "LOCK" state of PLL1 will be reflected in the LOCKDET output pin. LOCKDET = "high" if PLL1 is in "LOCK". LOCKDET = "low" if PLL1 is out of "LOCK".
11	LOCKDET will be unconditionally pulled to "LOW"

Table 3. Relationship Between the Values of the LDETDIS[2:1] Bit-Fields and the Meaning of the LOCKDET Output Signal

2.0 Instructions for Configuring the XRT8001 WAN Clock Device

As mentioned earlier, the XRT8001 WAN Clock Device can be configured to operate in the following modes:

- The "Forward/Master" Mode
- The "Reverse/Master" Mode
- The "Fractional T1/E1 Reverse/Master" Mode
- The "E1 to T1 – Forward/Master" Mode
- The "High Speed – Reverse" Mode
- The "Forward/Slave" Mode

A detailed description of the operation and the configuration steps for each of these configurations follows.

2.1 The "Forward/Master" Mode.

When the XRT8001 WAN Clock Device has been configured to operate in the "Forward/Master" Mode, then it will accept an "N x 1.544MHz" or an "N x 2.048MHz" clock signal via the "Reference Clock" input at FIN (pin 3); where "N" can range anywhere between 1 and 16. In response to this clock signal, the XRT8001 WAN Clock Device will output either a "K x 56kHz" or a "K x 64kHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock device, operating in the "Forward/Master" Mode is shown in figure 9.

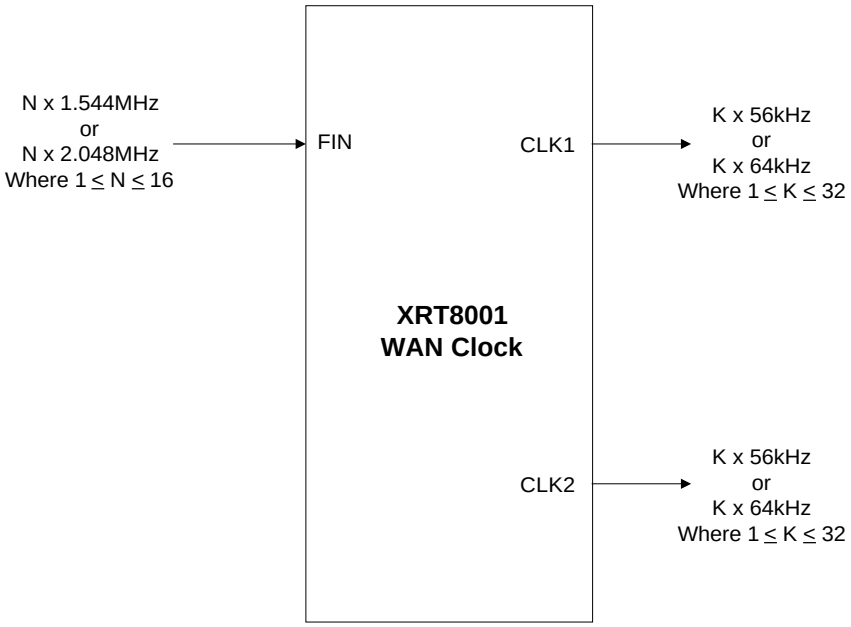


Figure 9. Illustration of the XRT8001 WAN Clock Device Operating in the "Forward/Master" Mode

Configuring the XRT8001 WAN Clock Device into the "Forward/Master" Mode

The user can configure the XRT8001 WAN Clock Device to operate in the "Forward/Master" Mode, by executing the following steps:

Step 1 – Configure the XRT8001 device to operate in the "MASTER" Mode, by pulling the MSB pin (pin 8) to VDD.

Step 2 – Review Table 4, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4-D1 in CR0
N x 1.544MHz	K x 56kHz	K x 56kHz	0000
N x 1.544MHz	K x 56kHz	K x 64kHz	0001
N x 1.544MHz	K x 64kHz	K x 64kHz	0010
N x 2.048MHz	K x 56kHz	K x 56kHz	0100
N x 2.048MHz	K x 56kHz	K x 64kHz	0101
N x 2.048MHz	K x 64kHz	K x 64kHz	0110

Table 4. Listing of "Input Frequency and "Output Frequency" Cases for "Forward/Master" Mode Operation

Step 3 – Upon reviewing Table 4, write the listed value (under the "Value to Write to D4 – D1 in CR0" Register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below.

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 device to operate in the "Forward/Master" Mode.

Step 4 – Next, you need to specify the value for "N" (e.g., as in the "N x 1.544MHz" or "N x 2.048MHz" clock signal which is to be applied to the "FIN" input pin.)

In order to specify the value for "N", one needs to write the value of "N - 1" (in binary format) into the "D4 through D1" bits within Command Register CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Value of "N - 1" (in Binary Format)				X

For example, if the user wishes to configure the XRT8001 device to accept a 1.544MHz clock signal, via the "FIN" input pin (e.g., N = 1), then the user should write in the value "0", into Command Register CR1.

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 5 – Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK1 output signal).

In order to specify the value for "K", one needs to write the value of "K - 1" (in binary format) into Command Register CR2, as illustrated below.

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 device to output a clock signal of either "56kHz" or "64kHz" (e.g., where "K" = 1) via the CLK1 output pin, then he/she should write the value "0", into Command Register CR2.

Step 6 – Specify the value of "K" (e.g., as in the "K x 56kHz" or "K x 64kHz" clock signal which is to be output via the CLK2 output signal).

In order to specify the value for "K", one needs to write the value of "K - 1" (binary format) into Command Register CR3, as illustrated below.

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
Value of "K - 1" (in Binary Format).				

For example, if one wishes to configure the XRT8001 device to output a clock signal of either "1.792MHz" or "2.048MHz" (e.g., where "K" = 32) via the CLK2 output pin, then he/she should write the value "31" (or "1 1 1 1 1" in binary format) into Command Register CR3.

Step 7 – Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

2.2 The "Reverse/Master" Mode

When the XRT8001 WAN Clock Device has been configured to operate in the "Reverse/Master" Mode, then it will accept either a "56kHz" or a "64kHz" clock signal via the "Reference Clock" input at FIN (pin 3). In response to this clock signal, the XRT8001 WAN Clock Devicewill output either a "1.544MHz" or a "2.048MHz" clock signal, via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock device, operating in the "Reverse/Master" Mode is presented in Figure 10.

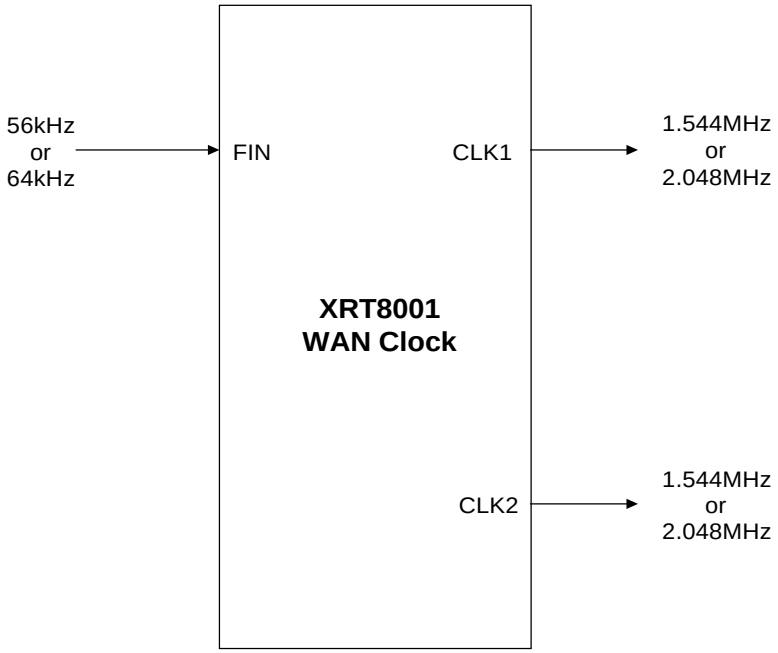


Figure 10. Illustration of the XRT8001 WAN Clock Device operating in the "Reverse/Master" Mode

Configuring the XRT8001 WAN Clock Device into the "Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock Device to operate in the "Reverse/Master" Mode, by executing the following steps:

Step 1 – Configure the XRT8001 Device to operate in the "MASTER" Mode by pulling the "MSB" pin (pin 8) to VDD.

Step 2 – Review Table 5, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
56kHz	1.544MHz	2.048MHz	0011
64kHz	1.544MHz	2.048MHz	0111

Table 5. Listing of "Input Frequency" and "Output Frequency" Cases for "Reverse/Master" Mode Operation

Step 3 – Upon reviewing Table 5, write the listed value (under the "Value to Write to D4 – D1 in CR0" register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below:

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 device to operate in the "Reverse/Master" Mode.

Step 4 – Write a "1" into the "PL2EN" bit-field within Command Register CR1 (if you wish to output a clock signal via the "CLK2" output pin), as illustrated below:

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Don't Care				1

Notes:

1. *The value of the "D4 through D1" bit-fields within Command Register, CR1 are "Don't Care".*
2. *The contents of Command Registers CR2 and CR3 are "Don't Care".*

Step 5 – Enable any of the following output signals as appropriate: SYNC", CLK1, CLK2 and LOCKDET.

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

Note: *For information on the "LDETDIS1" and "LDETDIS2" bit-fields, please see Table 3.*

2.3 The "Fractional T1/E1 Reverse/Master" Mode

When the XRT8001 WAN Clock Device has been configured to operate in the "Fractional T1/E1 Reverse/Master" Mode, then it will accept either a "P x 56kHz" or a "P x 64kHz" clock signal via the "FIN" input pin (pin 3). In response, the XRT8001 device will output either a 1.544MHz or a 2.048MHz clock signal via the CLK1 and/or CLK2 outputs.

A simple illustration of the XRT8001 WAN Clock device, operating in the "Fractional T1/E1 Reverse/Master" Mode is presented in Figure 11.

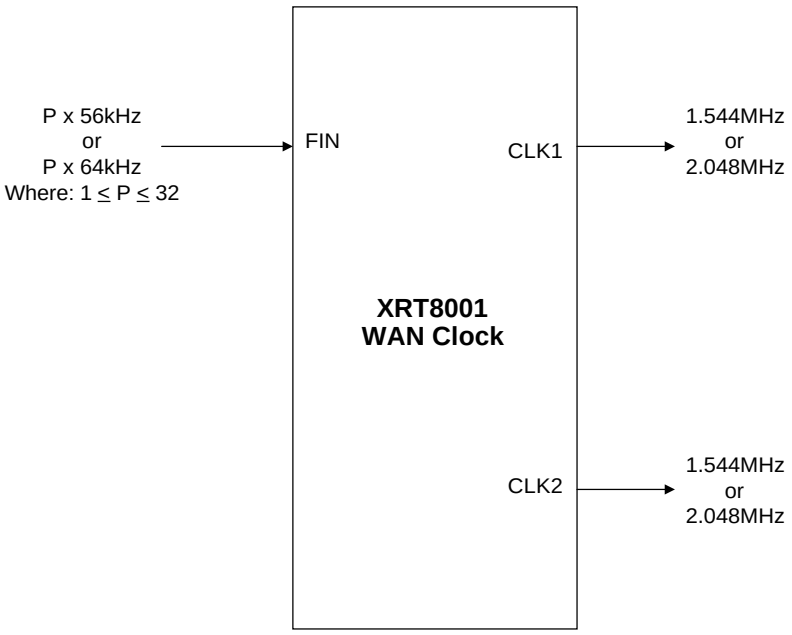


Figure 11. Illustration of the XRT8001 WAN Clock Device Operating in the "Fractional T1/E1 Reverse/Master" Mode

Configuring the XRT8001 WAN Clock Device into the "Fractional T1/E1 Reverse/Master" Mode

The user can configure the XRT8001 WAN Clock device to operate in the "Fractional T1/E1 Reverse/ Master" Mode by executing the following steps.

Step 1 – Configure the XRT8001 Device to operate in the "MASTER" Mode, by pulling the "MSB" input pin (pin 8) to VDD.

Step 2 – Review Table 6, and determine which combination of "Input Frequency" and "Output Frequencies" (via PLL1 and PLL2) correlate with the desired configuration.

Input Frequency	PLL1 Output Frequency	PLL2 Output Frequency	Value to Write to D4 – D1 in CR0
P x 56kHz	1.544MHz	2.048MHz	1001
P x 56kHz	1.544MHz	1.544MHz	1010
P x 64kHz	2.048MHz	1.544MHz	1011
P x 64kHz	2.048MHz	2.048MHz	1100

Table 6. Listing of "Input Frequency" and "Output Frequency" Cases for "Fractional T1/E1 Reverse/Master" Mode Operation

Step 3 – Upon reviewing Table 6, write the listed value (under the "Value to Write to D4 – D1 in CR0" register) into the D4 through D1 bit-fields within Command Register CR0, as illustrated below:

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
Value to Write to D4 – D1 in CR0				X

Notes:

1. *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*
2. *The contents of bit-fields D4 through D1 (within Command Register CR1) are "Don't Care"*
3. *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

This step configures the XRT8001 device to operate in the "Fractional T1/E1 Reverse/Master" Mode.

Step 4 – Specify the value of "P" (e.g., as in the "P x 56kHz" or "P x 64kHz" clock signal which is to be input via the FIN Reference Clock input).

In order to specify the value for "P", one needs to write in the value of "P - 1" (binary format) into Command Register CR2, as illustrated below:

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value of "P - 1" (in Binary Format).				

In other words, if one intends to input either a "56kHz" or "64kHz" clock signal via the "FIN" input pin (e.g., where P = 1), then he/she should write a "0" into Command Register CR2.

Step 5 – Write the binary expression "11111" into Command Register CR3.

This step is necessary in order to insure proper operation of the XRT8001 Device. This step is also illustrated below:

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
1	1	1	1	1

Step 6 – Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

2.4 The "E1 to T1 –Forward/Master" Mode

When the XRT8001 WAN Clock Device has been configured to operate in the "E1 to T1 – Forward/Master" Mode, then it will accept a "Q x 2.048MHz" clock signal via the "Reference Clock" input at FIN (pin 3), where "Q" can range anywhere between 1 - 16. In response to this clock signal, the XRT8001 WAN Clock device will output a 1.544MHz clock signal via the Clock Output pins (CLK1 and/or CLK2).

A simple illustration of the XRT8001 WAN Clock device, operating in the "E1 to T1 - Forward/Master" Mode is presented in Figure 12.

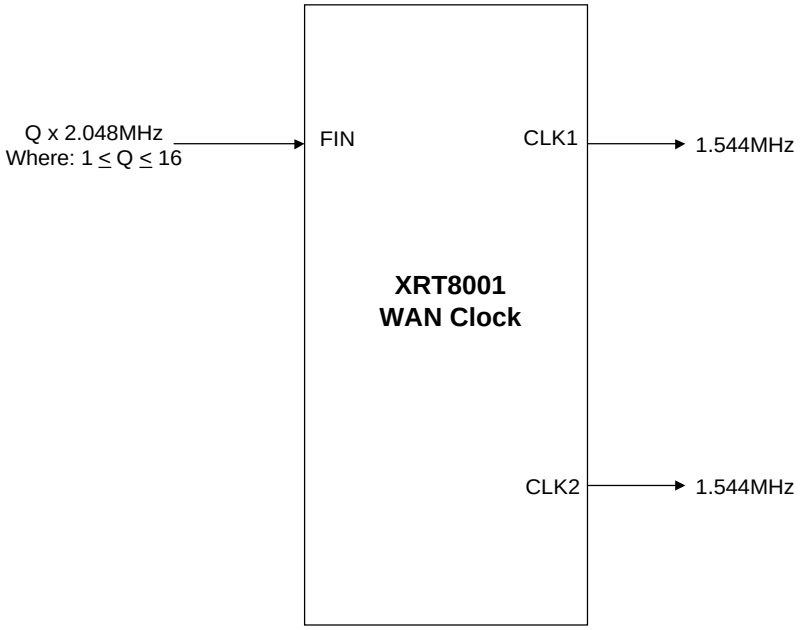


Figure 12. Illustration of the XRT8001 WAN Clock Device Operating in the "E1 to T1 – Forward/Master" Mode

Configuring the XRT8001 WAN Clock Device into the "E1 to T1 – Forward/Master" Mode

The user can configure the XRT8001 WAN Clock Device to operate in the "E1 to T1 – Forward/Master" Mode by executing the following steps:

Step 1 – Configure the XRT8001 Device to operate in the "MASTER" Mode, by pulling the "MSB" input pin (pin 8) to VDD.

Step 2 – Write the binary value "1000" into Command Register CR0, as illustrated below:

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	0	0	0	X

This step configures the XRT8001 WAN Clock device to operate in the "E1 to T1 – Forward/ Master" Mode.

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register, CR0.*

*Step 3 – Next, you need to specify the value for "Q" *(e.g., as in the "Q x 2.048MHz" clock signal which will be applied to the "FIN" input pin).*

The user accomplishes this writing the binary expression for "Q - 1" into Command Register, CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
Value of "Q - 1" (in Binary Format)				X

For example, if the user wishes to input a clock signal of 2.048MHz, to the "FIN" input pin (e.g., where Q = 1), then he/she should write a "0" into Command Register CR1.

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 4 – Write the binary expression "11111" into Command Register CR2, as illustrated below.

This step is necessary in order to insure proper operation of the XRT8001 Device. This step is also illustrated below:

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
1	1	1	1	1

Step 5 – Write the binary expression "11111" into Command Register CR3, as illustrated below.

This step is necessary in order to insure proper operation of the XRT8001 Device. This step is also illustrated below.

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
1	1	1	1	1

Step 6 – Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below.

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

2.5 The "High Speed – Reverse" Mode

When the XRT8001 WAN Clock Device has been configured to operate in the "High Speed – Reverse" Modes, its operation is independent of whether it has been configured in the "Master" or "Slave" Mode.

When the XRT8001 WAN Clock Device has been configured to operate in the "High Speed – Reverse" Modes, then it will accept a "64kHz" clock signal via the "Reference Clock" input at FIN (pin 3). In response, to this clock signal, the XRT8001 WAN Clock Device will output an "M x 2.048MHz" clock signal via the Clock Output pins (CLK1 and/or CLK2); where M can only have the values 1, 2,4 or 8.

A simple illustration of the XRT8001 WAN Clock Device, operating in the "High Speed – Reverse" Mode is presented in Figure 13.

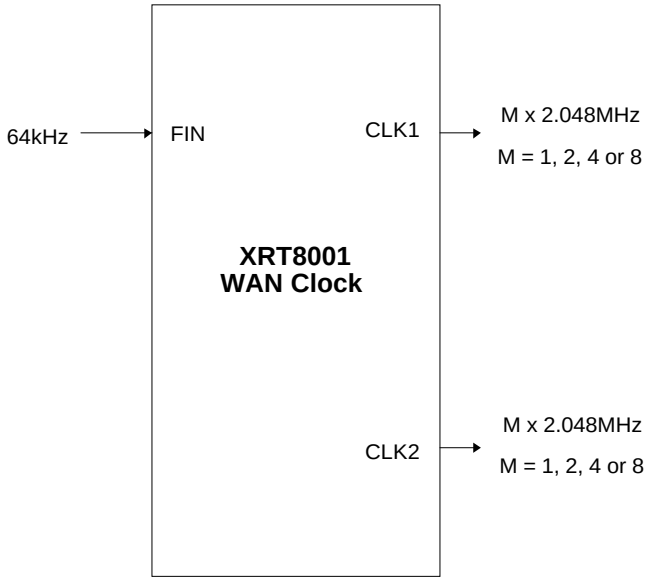


Figure 13. Illustration of the XRT8001 WAN Clock Device Operating in the "High Speed – Reverse" Mode

Configuring the XRT8001 WAN Clock Device into the "High Speed – Reverse" Mode.

The user can configure the XRT8001 WAN Clock Device to operate in the "High Speed – Reverse" Mode, by executing the following steps.

Step 1 – Configure the XRT8001 Device to operate in the "SLAVE" Mode, by pulling the "MSB" input pin (pin 8) to GND.

Command Register CR0 (Address = 0x00)

D4	D3	D2	D1	D0
IOC4	IOC3	IOC2	IOC1	PL1EN
1	1	0	1	X

Note: *If the user wishes to output a clock signal via the CLK1 output signal, then he/she should also write a "1" into the "PL1EN" bit-field within Command Register CR0.*

This step configures the XRT8001 device to operate in the "High Speed – Reverse" Mode.

Step 2 – Write the binary expression "0000" into bit-fields "D4 through D1" within Command Register, CR1, as illustrated below.

Command Register, CR1 (Address = 0x01)

D4	D3	D2	D1	D0
M4	M3	M2	M1	PL2EN
0	0	0	0	1

Note: *If the user wishes to output a clock signal via the CLK2 output signal, then he/she should also write a "1" into the "PL2EN" bit-field within Command Register CR1.*

Step 3 – Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to be output via the "CLK1" output pin.

This is accomplished by reviewing Table 7, and determining the 5 bit binary value which corresponds with the desired value of "M". Afterwards, the user should write this value into Command Register CR2.

Value of "M"	Value to be Written into Command Register CR2
1	0000X
2	0001X
4	001XX
8	X1XX or 1XXX

Table 7. Relationship Between the Value of "M" and the Value to Be Written into Command Register CR2 (in Order to Configure the "CLK1" Output Frequency)

Note: *The expression "X" indicates a "Don't Care" value for that particular bit-field.*

Command Register, CR2 (Address = 0x02)

D4	D3	D2	D1	D0
SEL14	SEL13	SEL12	SEL11	SEL10
Value from Table 7				

Step 4 – Specify the value for "M" (e.g., as in the "M x 2.048MHz" clock signal) which is to be the output on the "CLK2" output pin.

This is accomplished by reviewing Table 8, and determining the 5-bit binary value which corresponds with the desired value of "M". Afterwards, the user should write this value into Command Register, CR3.

Value of "M"	Value to be Written into Command Register CR3
1	0000X
2	0001X
4	001XX
8	X1XXX or 1XXXX

Table 8. Relationship Between the Value of "M" and the Value to Be Written into Command Register CR3 (in Order to Configure the "CLK2" Output Frequency)

Note: *The expression "X" indicates a "Don't Care" value for that particular bit-field.*

Command Register, CR3 (Address = 0x03)

D4	D3	D2	D1	D0
SEL24	SEL23	SEL22	SEL21	SEL20
Value from Table 8				

Step 5 – Enable any of the following output signals as appropriate: "SYNC", "CLK1", "CLK2" and "LOCKDET".

This is accomplished by writing a "1" into the corresponding bit-fields, within Command Register CR4, as illustrated below:

Command Register CR4, (Address = 0x04)

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	LDETDIS2	LDETDIS1
1	1	1	0	0

2.6 The "Forward/Slave" Mode

When the XRT8001 WAN Clock Device has been configured to operate in the "Forward/Slave" Mode, then it will accept an 8kHz clock signal via the "Reference Clock" input at FIN (pin 3). In response to this clock signal, the XRT8001 WAN Clock device will output either a "L x 56kHz" or "L x 64kHz" clock signal via the "Clock Output pins" (CLK1 and CLK2); where L can range in value from 1 to 32.

A simple illustration of the XRT8001 WAN Clock device operating in the "Forward/Slave" Mode" is presented in Figure 14.

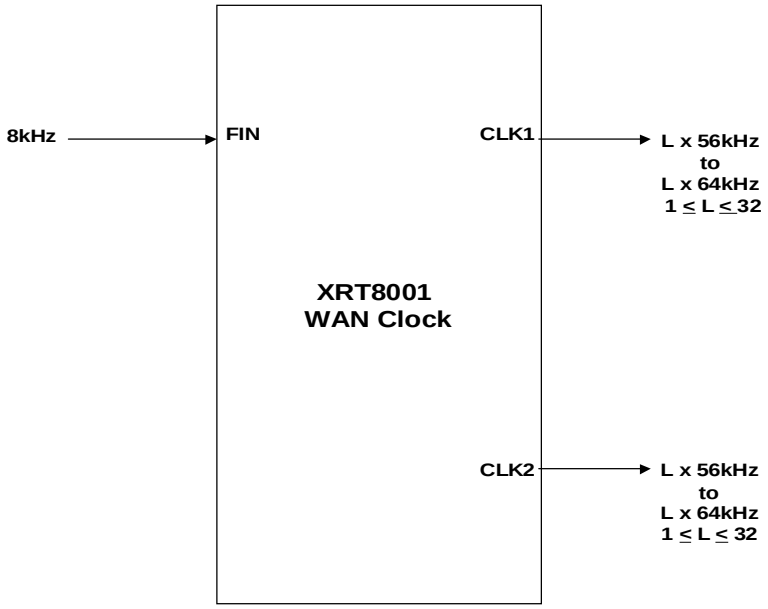


Figure 14. Illustration of the XRT8001 WAN Clock Device operating in the "Forward/Slave" Mode

Configuring the XRT8001 WAN Clock Device into the "Forward/Slave" Mode.

The user can configure the XRT8001 WAN Clock device to operate in the "Forward/Slave Mode" by executing the following steps:

STEP 1 – Configure the XRT8001 device to operate in the "SLAVE" Mode by pulling the MSB input pin (pin 8) to GND.

STEP 2 – Refer to Table 2B and write the value that corresponds to the desired "Forward/Slave" Mode into Bits D[4:1] within Command Register CR0.

STEP 3 – Define the values for L, for the CLK1 output by writing the appropriate value into the CR2 register. This is achieved by writing the value "L – 1" into this register.

Notes:

1. *For example, if the user writes "00000" into this register, then the XRT8001 device will output a 64kHz signal via the CLK1 output pin.*
2. *If the user intends to output data via CLK1, then he/she must ensure that the PL1EN bit-field within Command Register CR0 is set to "1".*

STEP 4- Define the value for L, for the CLK2 output by writing the appropriate value into the CR3 register. This is achieved by writing the value "L – 1" into this register.

Note: *If the user intends to output data via CLK2, then he/she must ensure that the PL2EN bit-field within Command Register CR1 is set to "1".*

STEP 5 – Set the CLK1EN and CLK2EN bit-fields, within Command Register CR4 to 1 in order to enable the output drivers for CLK1 and CLK2, as illustrated below.

Command Register CR4

D4	D3	D2	D1	D0
SYNCEN	CLK1EN	CLK2EN	X	X
x	1	1	0	0

Table 8, presents information on the delay between the rising edge of SYNC and CLK1 or CLK2 output signals. It is important to Note that this delay behaves as a function of the settings within the CR3 register.

t Values (nS)			
SEL14~SEL10	K	Kx56 MODE	Kx64 MODE
00000	1	372	326
00001	2	372	326
00010	3	372	326
00011	4	372	326
00100	5	446	391
00101	6	372	326
00110	7	319	279
00111	8	279	244
01000	9	496	434
01001	10	446	301
01010	11	406	355
01011	12	372	326
01100	13	343	301
01101	14	319	279
01110	15	298	260
01111	16	279	244
10000	17	525	460
10001	18	496	434
10010	19	470	411
10011	20	446	391
10100	21	425	372
10101	22	406	355
10110	23	388	340
10111	24	372	326
11000	25	357	312
11001	26	343	301
11010	27	331	289
11011	28	319	279
11100	29	308	279
11101	30	298	260
11110	31	288	252
11111	32	279	244

Table 8. Delay Time Between SYNC and CLK1 or CLK2

Note:
This table only applies when the XRT8001 Device is configured to operate in the "Forward/Master" or "Forward/Slave" Modes.

3.0 Operating the Microprocessor Serial Interface

The XRT8001 Serial Interface is a simple four-wire interface that is compatible with many of the microcontrollers available in the market. This interface consists of the following signals:

CSB - Chip Select (Active Low)
SCLK - Serial Clock
SDI - Serial Data Input
SDO - Serial Data Output

Using the Microprocessor Serial Interface

The following instructions, for using the Microprocessor Serial Interface, are best understood by referring to the diagram in Figure 15 on page 32.

In order to use the Microprocessor Serial Interface the user must first provide a clock signal to the SCLK input pin. Afterwards, the user will initiate a "Read" or "Write" operation by asserting the "active-low" Chip Select input pin (CSB). It is important to assert the CSB pin (e.g., toggle it "low") at least 50ns prior to the very first rising edge of the clock signal.

Once the CSB input pin has been asserted, the type of operation and the target register address must now be specified by the user. The user provides this information to the Microprocessor Serial Interface by writing eight serial bits of data into the SDI input. Note: each of these bits will be "clocked" into the SDI input on the rising edge of SCLK. These eight bits are identified and described below.

Bit 1 - "R/W" (Read/Write) Bit

This bit will be clocked into the SDI input on the first rising edge of SCLK (after CSB has been asserted). This bit indicates whether the current operation is a "Read" or "Write" operation. A "1" in this bit specifies a "Read" operation; whereas, a "0" in this bit specifies a "Write" operation.

Bits 2 Through 5: The Four (4) Bit Address Values (Labeled A0, A1, A2 and A3)

The next four rising edges of the SCLK signal will clock in the 4-bit address value for this particular Read (or Write) operation. The address selects the Command Register, within the XRT8001 device, that the user will either be reading data from, or writing data to. The user must supply the address bits to the SDI input pin in ascending order with the LSB (least significant bit) first.

Bits 6 and 7:

The next two bits, A4 and A5, must be set to "0", as shown in Figure 15.

Bit 8 - A6

The value of "A6" is a "don't care".

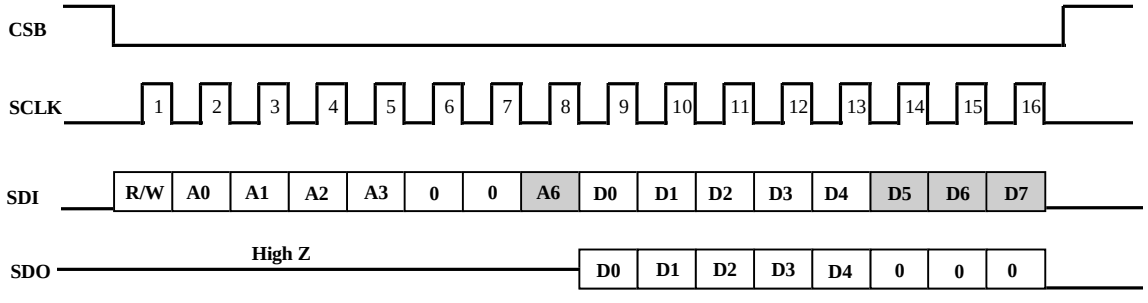
Once these first eight bits have been written into the Microprocessor Serial Interface, the subsequent action depends upon whether the current operation is a "Read" or "Write" operation.

Read Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Read" operation will proceed through an idle period, lasting three SCLK periods. On the falling edge of SCLK Cycle #8 (see Figure 15) the serial data output signal (SDO) becomes active. At this point the user can begin reading the data contents of the addressed Command Register (at Address [A3, A2, A1, A0]) via the SDO output pin. The Microprocessor Serial Interface will output this 5-bit data word (D0 through D4) in ascending order (with the LSB first), on the falling edges of the SCLK pin. As a consequence, the data (on the SDO output pin) will be sufficiently stable for reading (by the Microprocessor), on the very next rising edge of the SCLK pin.

Write Operation

Once the last address bit (A3) has been clocked into the SDI input, the "Write" operation will proceed through an idle period, lasting three SCLK periods. Prior to the rising edge of SCLK Cycle # 9 (see Figure 11) the user must begin to apply the 8-bit data word, that he/she wishes to write to the Microprocessor Serial Interface, onto the SDI input pin. The Microprocessor Serial Interface will latch the value on the SDI input pin, on the rising edge of SCLK. The user must apply this word (D0 through D7) serially, in ascending order with the LSB first.



Notes:

A4 and A5 are always "0".

R/W = "1" for "Read" Operations

R/W = "0" for "Write" Operations

- Denotes a "don't care" value

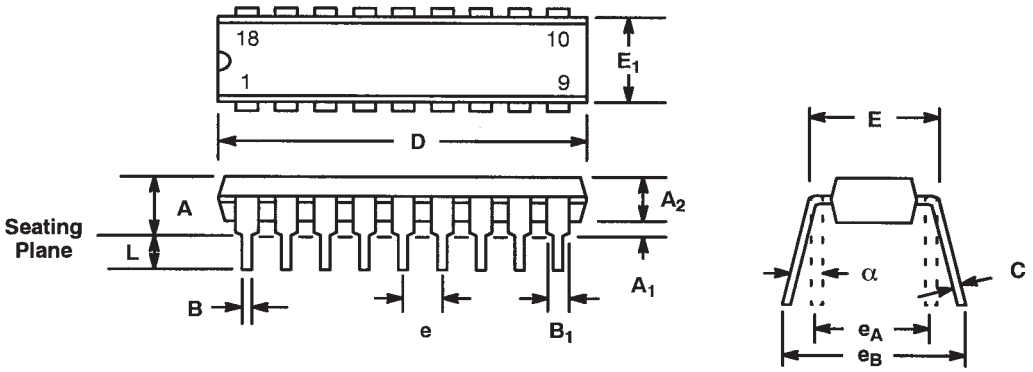
Figure 15. Microprocessor Serial Interface Data Structure

Simplified Interface Option

The user can simplify the design of the circuitry connecting to the Microprocessor Serial Interface by tying both the SDO and SDI pins together, and reading data from and/or writing data to this "combined" signal. This simplification is possible because only one of these signals are active at any given time. The inactive signal will be tri-stated.

18 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

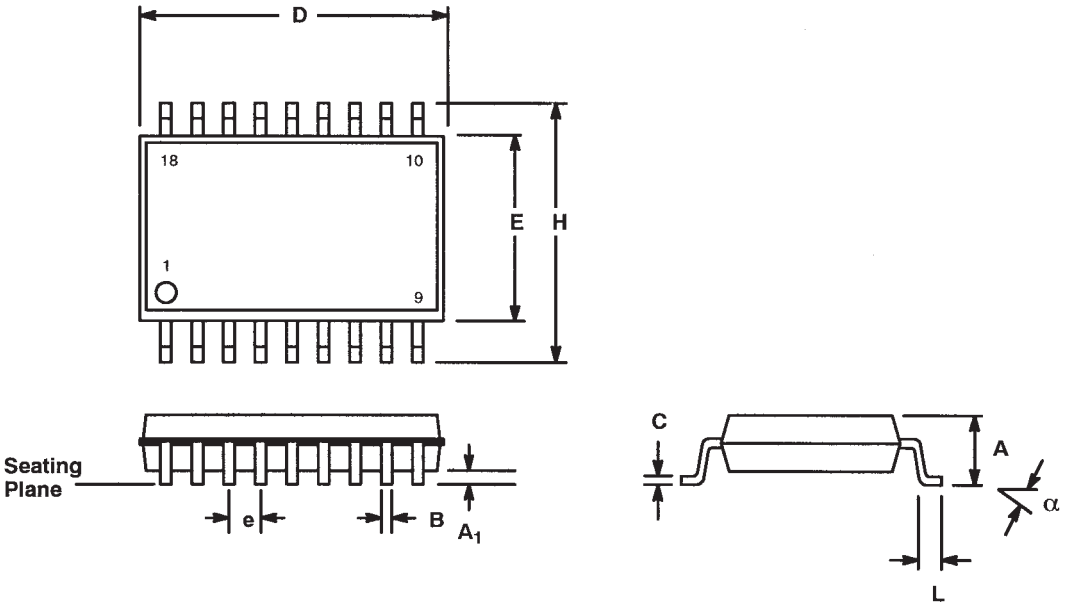


SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.145	0.210	3.68	5.33
A_1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B_1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.845	0.925	21.46	23.50
E	0.300	0.325	7.62	8.26
E_1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

18 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A_1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

Notes

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