YAMAHA

YDA135

D-20

STEREO 5W-20W DIGITAL AUDIO POWER AMPLIFIER CONTROLLER

■Outline

YDA135 is digital audio power amplifier controller IC that is output power of 20W/channel on a 12V power supply operation.
This IC is combined with the general purpose Power MOSFET (hereafter called Power MOSFET) that are connected through BTL can configure an audio power amplifier with output power of 5W or 20W.
This IC accepts analog signal, converts it into digital pulse signal by the digital modulation circuitry and outputs the digital pulse signal for driving Power MOSFET. The Power MOSFET that is driven by this IC outputs large current digital pulses. The digital pulse signal is converted to audio signal through an external low pass filter, and sent to the speakers.
By using a general purpose Power MOSFET, very low cost digital amplifier system is configured. By adapting Yamaha's proprietary modulation system, the device provides low distortion and high signal to noise ratio at the highest level among digital amplifiers in the equiralent class.
This IC has the overcurrent detection function that detects overcurrent state by voltage drop of external resistors that detects the output current.
This IC has the high temperature detection function that detects high temperature by resistor value change of external element that detects temperature.
The operation of this IC is limited by using two control signal, SLEEP or MUTE. SLEEP signal stops all functions of this IC, and restrain to the power consumption at the minimum. MUTE signal brings Power MOSFET into nonconductive state, and mute the output of the device.
This IC is configured by two power supply ; 5V for signal processing circuits, and 12V for Power MOSFET driving circuits.

■Features

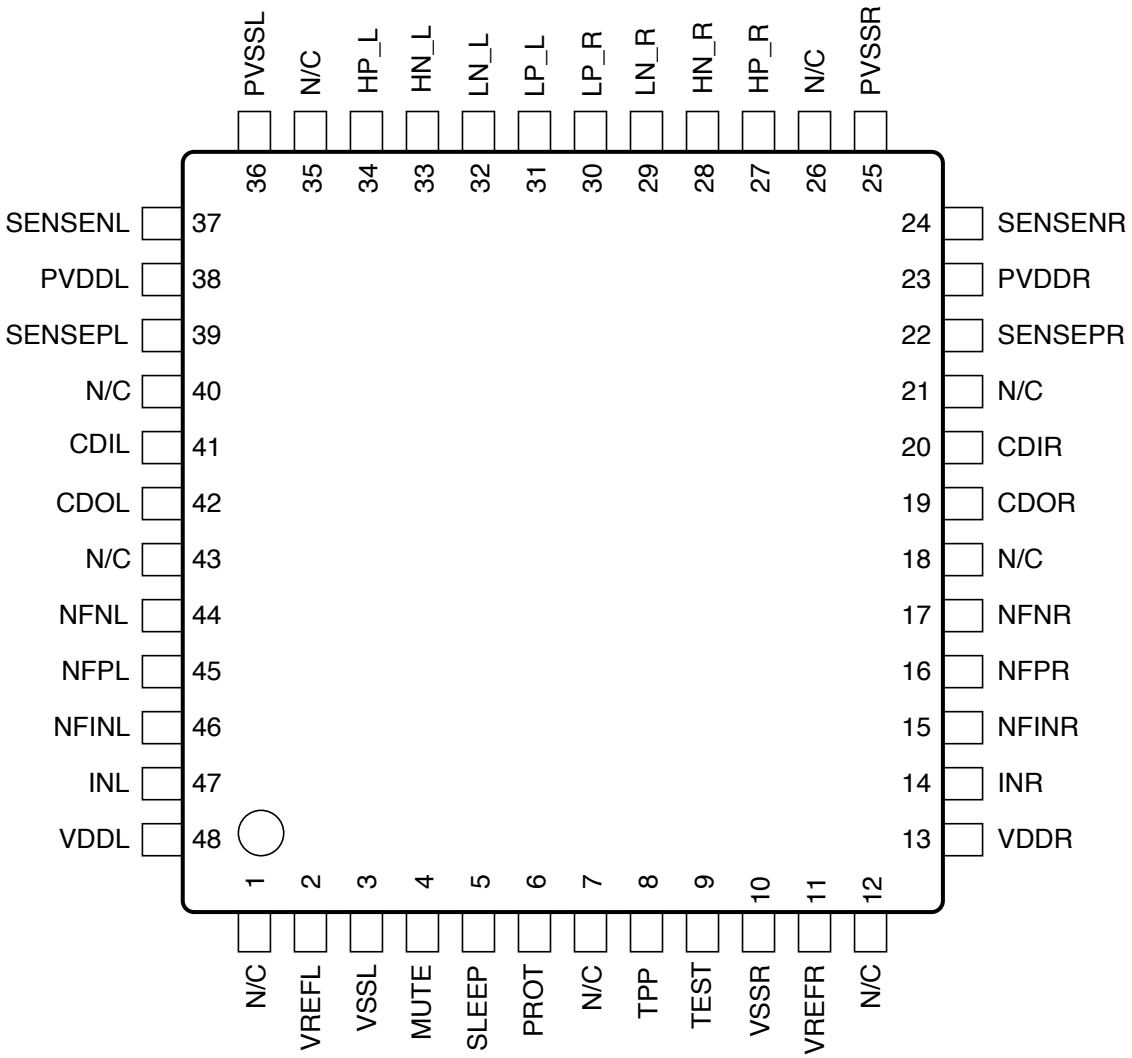
- High output power
  20W @ V_{DDP}=12.0V R_L=4Ω THD+N<10%
- High efficiency operation
  80 % @ V_{DDP}=12.0V R_L=4Ω Po=20W
  85 % @ V_{DDP}=12.0V R_L=8Ω Po=10W
- Low distortion(THD+N)
  0.03 % @ 1kHz R_L=4Ω Po=7W
- High signal to noise ratio
  100 dB @ V_{DDP}=12.0V Input sensitivity1.0V R_L=4Ω
  97 dB @ V_{DDP}=12.0V Input sensitivity150mV R_L=4Ω
- Low consumption current (12V/5V power supply)
  When Power MOSFET (FW332) is connected.
  30mA /7mA @ V_{DDP}=12.0V no signal
  0.1mA/7mA @ V_{DDP}=12.0V at mute
  1μA/1μA @ V_{DDP}=12.0V at sleep
- CS(Channel separation)
  80 dB @ 1kHz
- Any gain setting by external resistors
- Sleep function by SLEEP terminal
- Output mute function by MUTE terminal
- Over current detection function
  (Power supply short-circuiting, Ground short-circuiting, Load short-circuiting)
- High temperature detection function
- Pop noise suppression function at turn-on and turn-off
- 48-pin plastic LQFP (YDA135-VZ)

YAMAHA CORPORATION

YDA135CATALOG
CATALOG No.:LSI-4DA135A2
2003.3

■ Terminal configuration

YDA135-VZ



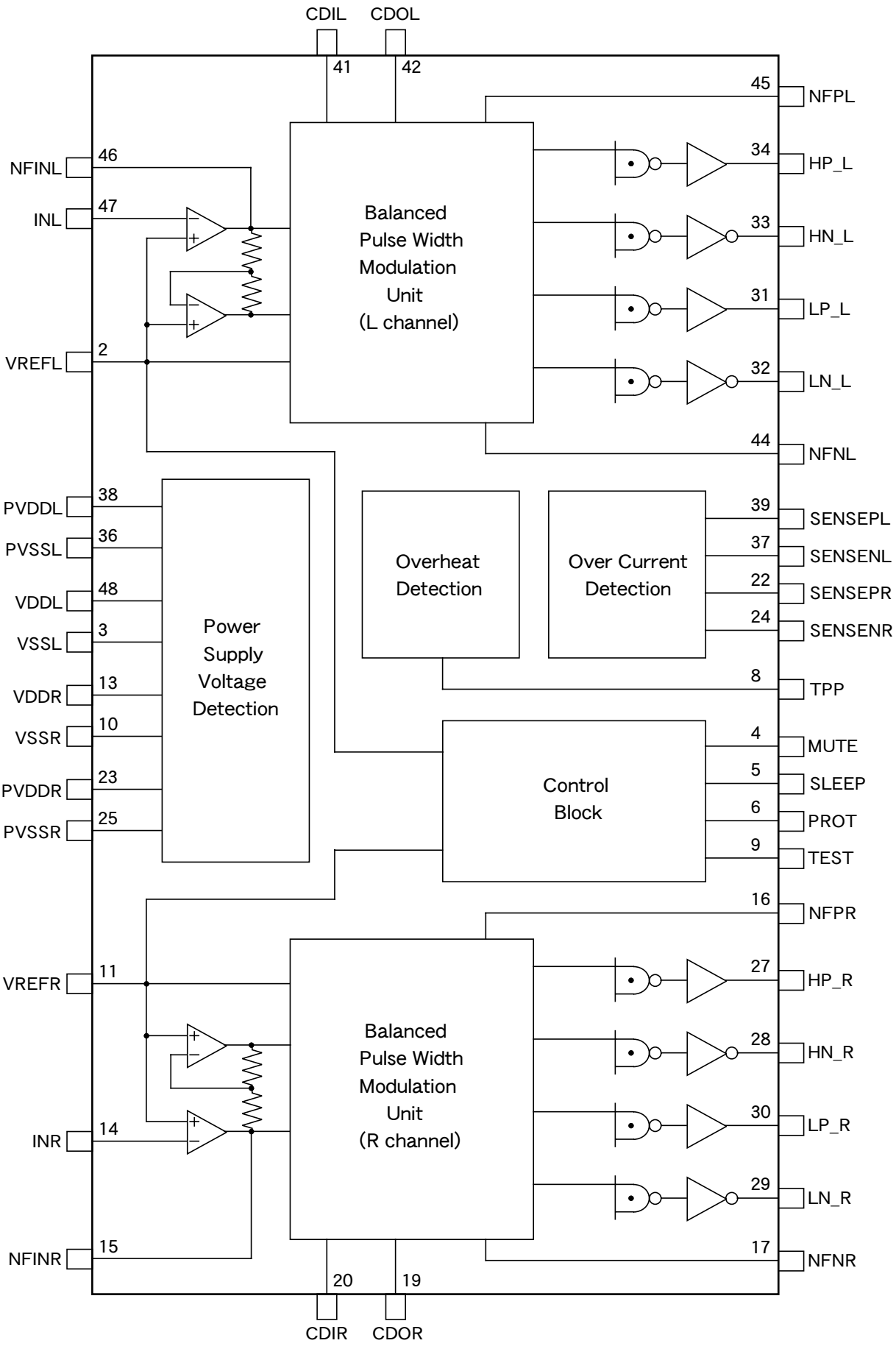
<48 pin LQFP Top View>

■ Terminal function

No.	Name	I/O	Function
1	N/C	—	Non connection
2	VREFL	O	L channel reference voltage output
3	VSSL	—	Ground for 5V power supply of L channel
4	MUTE	I	Mute control
5	SLEEP	I	Sleep control
6	PROT	O	Warning signal output for detection function
7	N/C	—	Non connection
8	TPP	I	High temperature detection
9	TEST	I	IC test. Connect to VSSR
10	VSSR	—	Ground for 5V power supply of R channel
11	VREFR	O	R channel reference voltage output
12	N/C	—	Non connection
13	VDDR	—	5V Power supply of R channel
14	INR	I	R channel analog signal input
15	NFINR	O	R channel input gain setting
16	NFPR	I	R channel positive side feedback input
17	NFNR	I	R channel negative side feedback input
18	N/C	—	Non connection
19	CDOR	O	R channel off time setting (output)
20	CDIR	I	R channel off time setting (input)
21	N/C	—	Non connection
22	SENSEPR	IH	R channel overcurrent detection (PVDD side)
23	PVDDR	—	12V power supply of R channel
24	SENSENR	IH	R channel overcurrent detection (PVSS side)
25	PVSSR	—	Ground for 12V power supply of R channel
26	N/C	—	Non connection
27	HP_R	OH	R channel positive side PMOS driving
28	HN_R	OH	R channel positive side NMOS driving
29	LN_R	OH	R channel negative side NMOS driving
30	LP_R	OH	R channel negative side PMOS driving
31	LP_L	OH	L channel negative side PMOS driving
32	LN_L	OH	L channel negative side NMOS driving
33	HN_L	OH	L channel positive side NMOS driving
34	HP_L	OH	L channel positive side PMOS driving
35	N/C	—	Non connection
36	PVSSL	—	Ground for 12V power supply of L channel
37	SENSENL	IH	L channel overcurrent detection (PVSS side)
38	PVDDL	—	12V power supply of L channel
39	SENSEPL	IH	L channel overcurrent detection (PVDD side)
40	N/C	—	Non connection
41	CDIL	I	L channel off time setting (input)
42	CDOL	O	L channel off time setting (output)
43	N/C	—	Non connection
44	NFNL	I	L channel negative side feedback input
45	NFPL	I	L channel positive side feedback input
46	NFINL	O	L channel input gain setting
47	INL	I	L channel analog signal input
48	VDDL	—	5V power supply of L channel

Note. I/O: 5V input/ 5V output, IH/OH: 12V input/12V output

■ Internal block diagram



■ Description of terminal function

In the following explanations, "L" level and "H" level of SLEEP and MUTE terminals mean "V_{IL}" and "V_{IH}" respectively, and "L" level and "H" level of PROT terminal mean "V_{OL}" and "V_{OH}" respectively.
"L" level and "H" level of output terminals such as HP_L and HN_L terminals also mean "V_{HOL}" and "V_{HOH}" respectively.

• Power supply and ground terminals

VDDL, VSSL, VDDR, VSSR (Pin No.48, 3, 13, 10)
VDDL and VSSL terminals are 5.0V power supply terminal and ground terminal for left channel signal processing circuit respectively. VDDR and VSSR terminals are 5.0V power supply terminal and ground terminal for right channel signal processing circuit respectively.
Left and right channels are equipped independent power supply terminal and ground terminal, respectirely.
All the ground terminals are connected through IC board (low resistor), but the power supply terminals for left and right channels are separated from each other.

PVDDL, PVSSL, PVDDR, PVSSR (Pin No.38, 36, 23, 25)
PVDDL and PVSSL are 12 V power supply and ground terminals for left channel Power MOSFET driving circuit respectively.
PVDDR and PVSSR are 12 V power supply and ground terminals for right channel Power MOSFET driving circuit respectively.
Left and right channels are equipped independent power supply terminal and ground terminal, respectirely.
All the ground terminals are connected through IC board (low resistor), but the power supply terminals for left and right channels are separated from each other.

• Analog terminals

INL, NFINL, INR, NFINR (Pin No.47, 46, 14, 15)
INL and NFINL are analog signal input and gain adjustment terminals for left channel.
INR and NFINR are analog signal input and gain adjustment terminals for right channel.
The terminals are connected respectively to the negative input terminal and output terminal of the first stage inversion operational amplifiers.
The amplifier gain is set by connecting an input resistor and a feedback resistor to both terminals as shown the "Example of application circuit".
The use of this inversion operational amplifier allows making a filter such as low band boost filter.

VREFL, VREFR (Pin No.2, 11)
VREFL is the reference voltage output terminal for the left channel. It outputs 1/2 of 5V power supply terminal (VDDL) voltage.
VREFR is the reference voltage output terminal for the right channel. It outputs 1/2 of 5V power supply terminal (VDDR) voltage.
Connect a capacitor with capacitance necessary to stabilize the voltage. Refer to "Pop noise reduction functions".

NFPL, NFNL, NFPR, NFNR (Pin No.45, 44, 16, 17)
NFPL and NFNL are the digital amplifier feedback input terminals for left channel.
NFPR and NFNR are the digital amplifier feedback input terminals for right channel.
Connect the feedback signal of positive side and negative side of H-bridge configuration Power MOSFET output to each terminal. At this time, as described in the "Example of application circuit", divide the voltage of feedback signal with external resistor to prevent the maximum voltage from exceeding 5V and input to each terminal.

HP_L, HN_L, LP_L, LN_L, HP_R, HN_R, LP_R, LN_R (Pin No.34, 33, 31, 32, 27, 28, 30, 29)
HP_L, HN_L, LP_L and LN_L are Power MOSFET driving terminals for left channel.
HP_L is a driving output terminal for positive side P channel Power MOSFET (PMOS), HN_L is the one for positive side N channel Power MOSFET (NMOS), LP_L is the one for negative side P channel Power MOSFET (PMOS), and LN_L is the one for negative side N channel Power MOSFET (NMOS).
HP_R, HN_R, LP_R and LN_R are Power MOSFET driving terminals for right channel.
HP_R is a driving output terminal for positive side P channel Power MOSFET (PMOS), HN_R is the one for positive side N channel Power MOSFET (NMOS), LP_R is the one for negative side P channel Power MOSFET (PMOS), and LN_R is the one for negative side N channel Power MOSFET (NMOS).

CDIL, CDOL, CDIR, CDOR (Pin No.41, 42, 20, 19)
CDIL and CDOL are for connecting a resistor and a capacitor for setting off time of external Power MOSFET for left channel (refer to "Amplifier functions").
CDIR and CDOR are for connecting a resistor and a capacitor for setting off time of external Power MOSFET for right channel.
It is necessary to determine the resistor and capacitor to obtain a time constant according the characteristics of Power MOSFET that is to be used and distortion rate of amplifier you need. Refer to "Amplifier functions".

SENSEPL, SENSENL, SENSEPR, SENSENR (Pin No.39, 37, 22, 24)
SENSEPL and SENSENL are the overcurrent detection terminals for left channel.
SENSEPR and SENSENR are the overcurrent detection terminals for right channel.
As described in the "Example of application circuit", connect an end of the current detection resistor to power supply side and ground side of Power MOSFET, and connect other end of the resistor to SENSEPL and SENSENL terminals, and SENSEPR and SENSENR terminals respectively.
This IC determines that overcurrent state has occurred when the voltage drop at the current detection resistor becomes specified values (V_{OCPN} and V_{DDP}-V_{OCPP}) or over.
It is necessary to determine the resistance of the current detection resistor optimally according to the characteristics of Power MOSFET.
When the overcurrent detection circuitry of left channel or right channel determines overcurrent state, "H" level is outputted from the warning signal output (PROT) terminal.
When the warning signal is outputted due to overcurrent detection, this IC keeps the warning signal output (PROT="H" level) after the current return to normal state.

TPP (Pin No.8)
TPP is the high temperature detection terminal.
As described in the "Example of application circuit", connect a temperature detection element (such as a posistor) between TPP terminal and 5 V system ground terminal. In addition, connect a resistor with proper value between TPP terminal and 5V system power supply terminal. At this time, arranges the temperature detection near Power MOSFET. As the temperature of Power MOSFET rises, the resistor value of the temperature detection element increases, and the voltage of TPP terminal also increases accordingly. This IC determines that high temperature state has occurred when the voltage of TPP terminal has become specified value (V_{TPP}) or over, and outputs "H" level from the warning signal output (PROT) terminal.
When the warning signal is outputted due to high temperature detection, this IC keeps the warning signal output (PROT="H" level) after the temperature return to normal state.

• Digital terminals

SLEEP (Pin No.5)
SLEEP is the sleep control terminal. It controls both left and right channels simultaneously.
When SLEEP terminal is set at "H" level, all functions of this IC is stopped, and this IC is placed in the sleep state. At this time, all Power MOSFET driving terminals output signals that turn off the Power MOSFETs.
Though all Power MOSFETs are placed in the off state (non conductive state), the speaker terminal is made ground potential by the externally connected resistor.
At this time, restrain the power consumption at the minimum, and warning signal (PROT terminal output) is set at "L" level.When SLEEP terminal is changed from "H" level to "L" level, this IC goes into normal operation after sufficient time (starting time) to make each reference voltage reaches a fixed potential.

MUTE (Pin No.4)
MUTE is the mute control terminal. It controls both left and right channels simultaneously.
When MUTE terminal is set at "H" level, all Power MOSFET driving terminals output signals that turns off the Power MOSFETs. Though all Power MOSFETs are placed in the off state (non conductive state), the speaker terminal is made ground potential by the externally connected resistor, and the amplifier becomes mute state. At this time, the overcurrent protection function stops.
When MUTE terminal is set to "L" level, this IC goes into normal operating state.

PROT (Pin No.6)
PROT is the warning signal output terminal that has both overcurrent and high temperature detection functions.
The terminal outputs "H" level when either function detects an abnormality state.
When the warning signal (PROT terminal="H" level) is outputted by abnormality state detection, this IC keep the warning signal output after return to normal state.
The warning signal is cancelled by changing the state of SLEEP terminal to "H" level or turning off the power supply.

TEST (Pin No.9)
This is the terminal for testing. Connect to VSSR terminal.

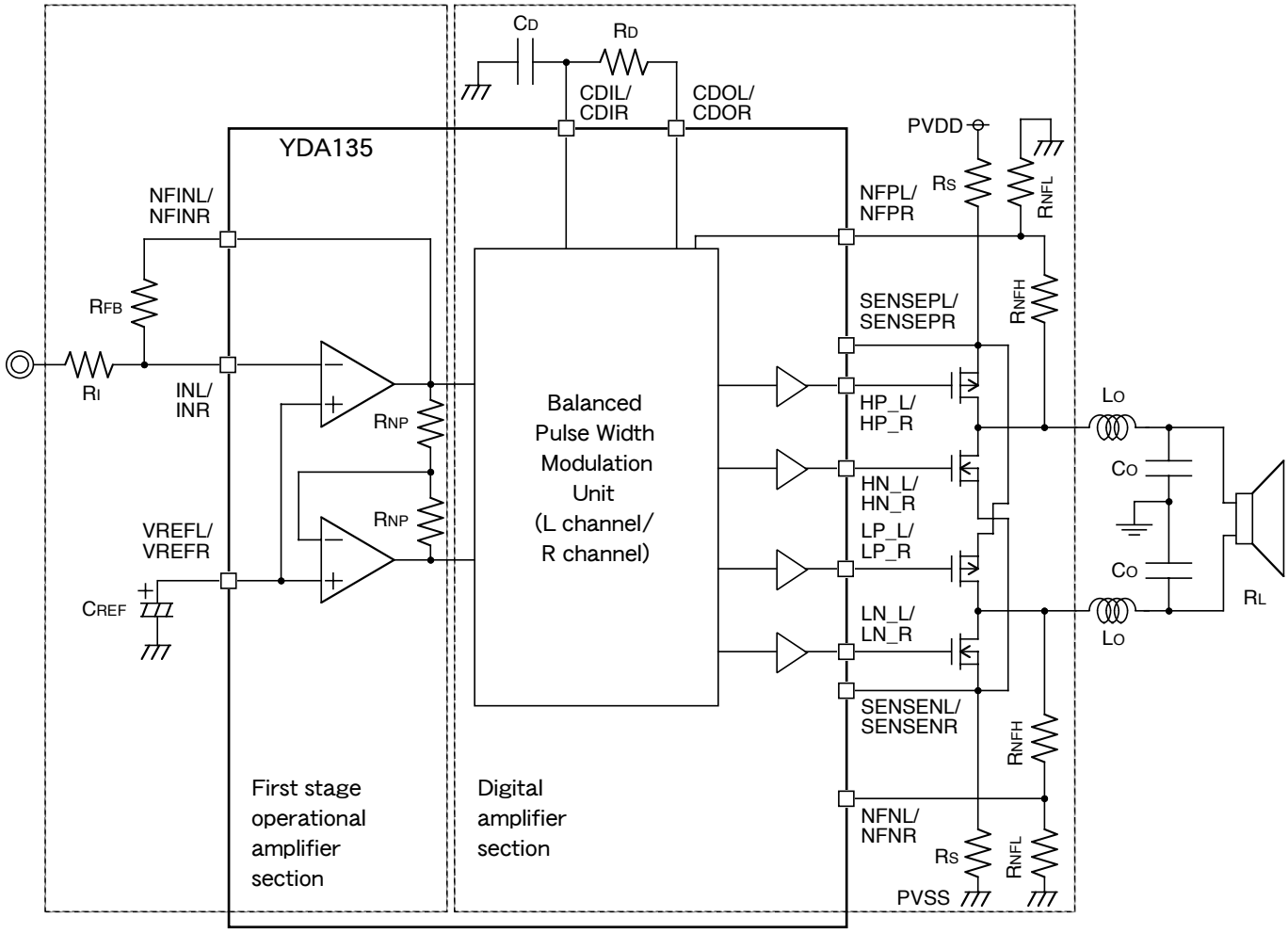
■ Mode setting and error detection

SLEEP	MUTE	TPP	L channel								R channel								PROT	Mode
			SENSPL	SENSNL	HP_L	HN_L	LP_L	LN_L	HMOS_L	LMOS_L	SENSPR	SENSNR	HP_R	HN_R	LP_R	LN_R	HMOS_R	LMOS_R		
H	*	*	*	*	H	L	H	L	L	L	*	*	H	L	H	L	L	L	L	Sleep mode
L	H	P	*	*	H	L	H	L	L	L	*	*	H	L	H	L	L	L	X	Mute mode
L	H	F	*	*	H	L	H	L	L	L	*	*	H	L	H	L	L	L	H	Mute mode / High temperature detection
L	L	P	P	P	X	X	X	X	X	X	P	P	X	X	X	X	X	X	X	2 channel output mode
L	L	F	P	P	X	X	X	X	X	X	P	P	X	X	X	X	X	X	H	2 channel output mode / High temperature detection
L	L	P	F	P	X	X	X	X	X	X	P	P	X	X	X	X	X	X	H	2 channel output mode / L channel overcurrent detection
L	L	P	P	F	X	X	X	X	X	X	P	P	X	X	X	X	X	X	H	2 channel output mode / L channel overcurrent detection
L	L	P	P	P	X	X	X	X	X	X	F	P	X	X	X	X	X	X	H	2 channel output mode / R channel overcurrent detection
L	L	P	P	P	X	X	X	X	X	X	P	F	X	X	X	X	X	X	H	2 channel output mode / R channel overcurrent detection

Note:
1) HMOS_L, LMOS_L, HMOS_R and LMOS_R terminal mean outputs of Power MOSFET that are positive at left channel side, negative at left channel side, positive at right channel side, and negative at right channel side respectively.
"L" means that the terminals are pulled down by the resistor that is used in the "Example of application circuit".
"X" means pulse outputting state.
2) "X" of PROT terminal means that is in state of either "L" or "H" by the previous state.
3) "P" of SENSE* and TPP terminals means normal state (Pass), and "F" means abnormal state (Fail).
4) "X" of output terminals such as HP_L, HN_L terminals means pulse outputting state.
5) "*" means "Don't care".

■ Description of functions

• Amplifier functions



Amplifier functions block diagram

The amplifier section of this IC consists of the first stage operational amplifier and the second digital amplifier.
The gain of the first stage operational amplifier is set with externally connecting an input resistor (R_I) and feedback resistor (R_{FB}). The second stage digital amplifier connects Power MOSFET externally, of which output is fed back to the modulation circuitry of the digital amplifier section through the external feedback resistors (R_{NFH} and R_{NFL}). This feature realizes the low distortion rate.
To prevent occurrence of penetration current caused by simultaneous on state of external Power MOSFET, a period in which both PMOS and NMOS are not on state ("off time") is provided. This time is set by using an external resistor (R_D) and capacitor (C_D).
The output of Power MOSFET is connected to the speakers through the secondary low pass filter consisting of an inductor (Lo) and a capacitor (Co). This feature removes the carrier frequency component contained in the output of Power MOSFET, and sent only audio signals to the speakers.

Gain setting

The gain of first stage operational amplifier is calculated by the following formula. The gain of the digital amplifier section that includes the gain (8dB) of internal digital amplifier section and gain of the external feedback resistor is calculated by the following formula.

	Gain
First stage operational amplifier section	$20*\log(2*R_{FB}/R_I)$ dB (Gain is set by R_I and R_{FB}. Condition : $R_I > 2k\Omega$)
Digital amplifier section	$8+20*\log(1+R_{NFH}/R_{NFL})$ dB

An "Example of application circuit" uses R_I=8.2kΩ, R_{FB}=39kΩ, R_{NFH}=3.3kΩ and R_{NFL}=2.4kΩ, which give total gain (Av) that is calculated by using the following formula. With this setting, the input sensitivity is 150mVrms, where the maximum output can be obtained when the input is 150mVrms.

Av (dB) = 20*log(2*39/8.2) + 8 + 20*log(1+3.3/2.4)
= 35.1 dB

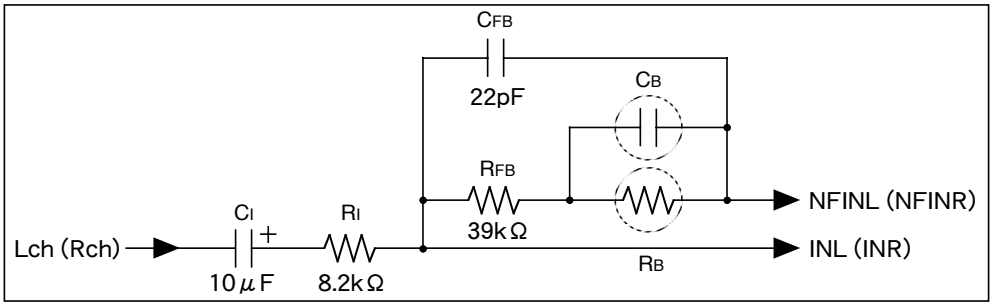
This section explains how to set the gain for maximum level of the input signal. The relationship between the maximum level of input signal, Vin (peak value), R_I and R_{FB} is given by the following formula. (When R_{NFH}=3.3kΩ, R_{NFL}=2.4kΩ.)

Vin(peak value) = R_I / R_{FB}

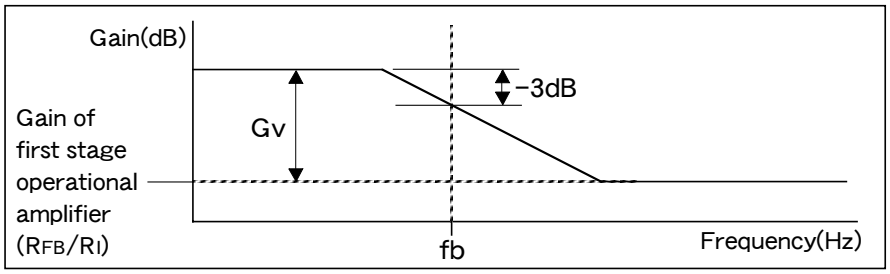
For example, when setting as Vin = 300mVrms, the formula is "300mVrms* $\sqrt{2}$ = R_I / R_{FB}". When R_{FB} = 39kΩ, the value of R_I is approximately 16kΩ. Set the value of R_I as 2kΩ or less.

When setting the gain of the operational amplifier, which is initial stage, it is necessary to observe the restrictions that are described in "Pop noise reduction functions". Due to the limitation on operational amplifier driving capability, it is necessary to make the feedback resistance (R_{FB}) 10kΩ or over.

The use of the initial stage operational amplifier section allows configuration of a "Low band boost filter circuit" described below.
This filter has a frequency response which is similar to the "Characteristics of low band boost filter" described below, and the amount of boost (Gv) for the gain of initial stage inversion operational amplifier, and the cut-off frequency (fb) at a point where the boost gain is reduced by 3dB can be described by the following formula.



Low band boost filter circuit



Characteristics of low band boost filter

Gv(dB) = 20*log((RFB + RB)/RFB)
fb(Hz) = 1/(2π*CB*RB)

When low band boost function is used, the total gain in the low band that is boosted after it is amplified by the digital amplifier section becomes "total gain (Av) + boost amount (Gv)".

For the "Example of application circuit", a capacitor (C_{FB}) for cutting off high frequency range is attached for limiting the band of input signal. The value can be adjusted if necessary. (Cut-off frequency = 1/(2π*CFB*RFB)). DC cutting capacitor (C_I) is attached for limiting the input DC current. This capacitor and input resistor (R_I) constitutes a low cutoff filter. Set the filter for sufficiently low cutoff frequency. (Cut-off frequency = 1/(2π*CI*RI)).

The external feedback resistors (R_{NFH} and R_{NFL}) are set so that they meet the following relational expression depending on the input stage power supply voltage (V_{DD}) and output stage power supply voltage (PV_{DD}). For R_{NFL}, select the largest value resistor meeting this expression.
Use the resistor with an accuracy of 1% for reduction of offset voltage.

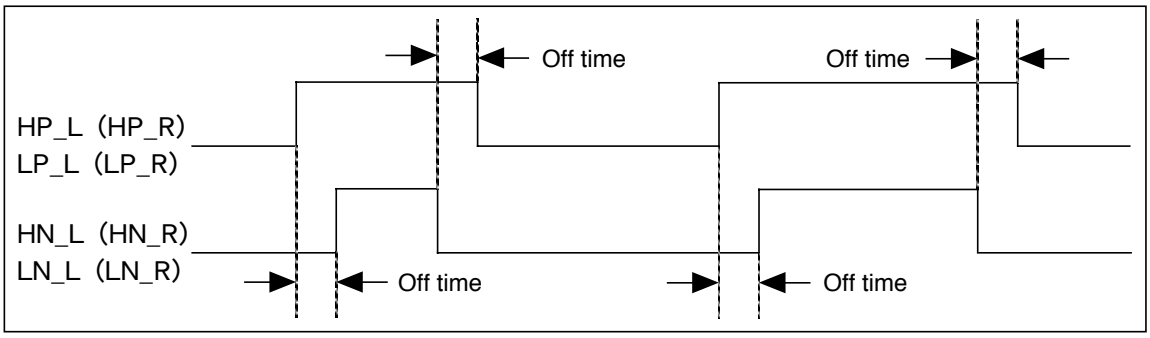
$R_{NFL} \leqq V_{DD}/(V_{DDP} - V_{DD})*R_{NFH}$
$600\Omega \leqq (R_{NFH} + R_{NFL}) \leqq 6k\Omega$

Selection of Power MOSFET

Power MOSFET can be selected on the user side within the range of the absolute maximum rating.
When selecting Power MOSFET, take note of the following matters.

- The drain side voltage may be twice the maximum power supply voltage due to the counter electromotive force developed in the inductive load.
  When V_{DDP}=12V, use Power MOSFET of which withstand voltage V_{DS} is 30V or higher.
- For the gate voltage, the voltage V_{DDP} is applied. Therefore, use Power MOSFET of which withstand voltage V_{GS} is 20V or higher.
- Due to the limitation of allowable power consumption of this IC, use Power MOSFET of which total input charges (V_{DS}=10V, V_{GS}=10V) is 9 nC or less.

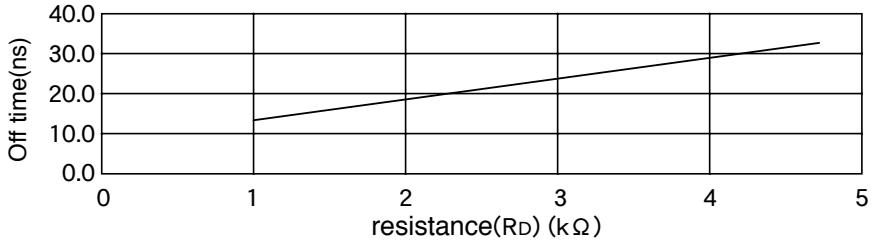
To prevent destruction of Power MOSFET caused by simultaneous turn-on of PMOS and NMOS of Power MOSFET, off time such as the following "Power MOSFET output waveform and off time" can be set for Power MOSFET depending on the resistor (R_D) and capacitor (C_D) that are connected to CDIL, CDIR, CDOL and CDOR terminals.
Connect a proper resistor (R_D) and capacitor (C_D) according the characteristics of Power MOSFET.
As the time constant is made smaller, off time becomes shorter. Adjust the off time so that the penetration current does not flow through the Power MOSFET, as shorter off time can cause penetration current to flow.
As the time constant is made larger, off time becomes longer. Longer off time makes the margin from the moment of simultaneous turn on of the Power MOSFET larger, but at the same time, the distortion characteristic changes for the worse.



Power MOSFET output waveform and off time

An indication of off time is in the range approximately from 10ns to 40ns. As an example, the relationship between the resistance (R_D) and off time is as described by the “Relationship between off time and resistance (R_D)” described below when the capacitance (C_D) = 15pF.

Relationship between off time and resistance (R_D) : (C_D=15pF)



Selection of inductor for output filter

The cutoff frequency (fc) of the LC low pass filter that is connected to the output of the Power MOSFET can be obtained by using the following formula.
To obtain an ideal frequency response, set the Q value of LCR resonance circuit to approximately 0.7.

$$fc(Hz) = 1/(2*\pi*\sqrt{(Lo*Co)})$$

$$Q = 1/R_L*\sqrt{(Lo/Co)} = 0.7$$

Typically, the one with the following value is used depending on the speaker impedance assuming that the cutoff frequecy of 50kHz is used.

R_L(Load impedance)	Lo(Inductance)	Co(Capacitor)
4Ω	10μH	1μF
8Ω	22μH	0.47μF
16Ω	39μH	0.27μF

The distortion factor and voice quality may be affected by the type of coil to be used. Select the best suited one according to the response required.

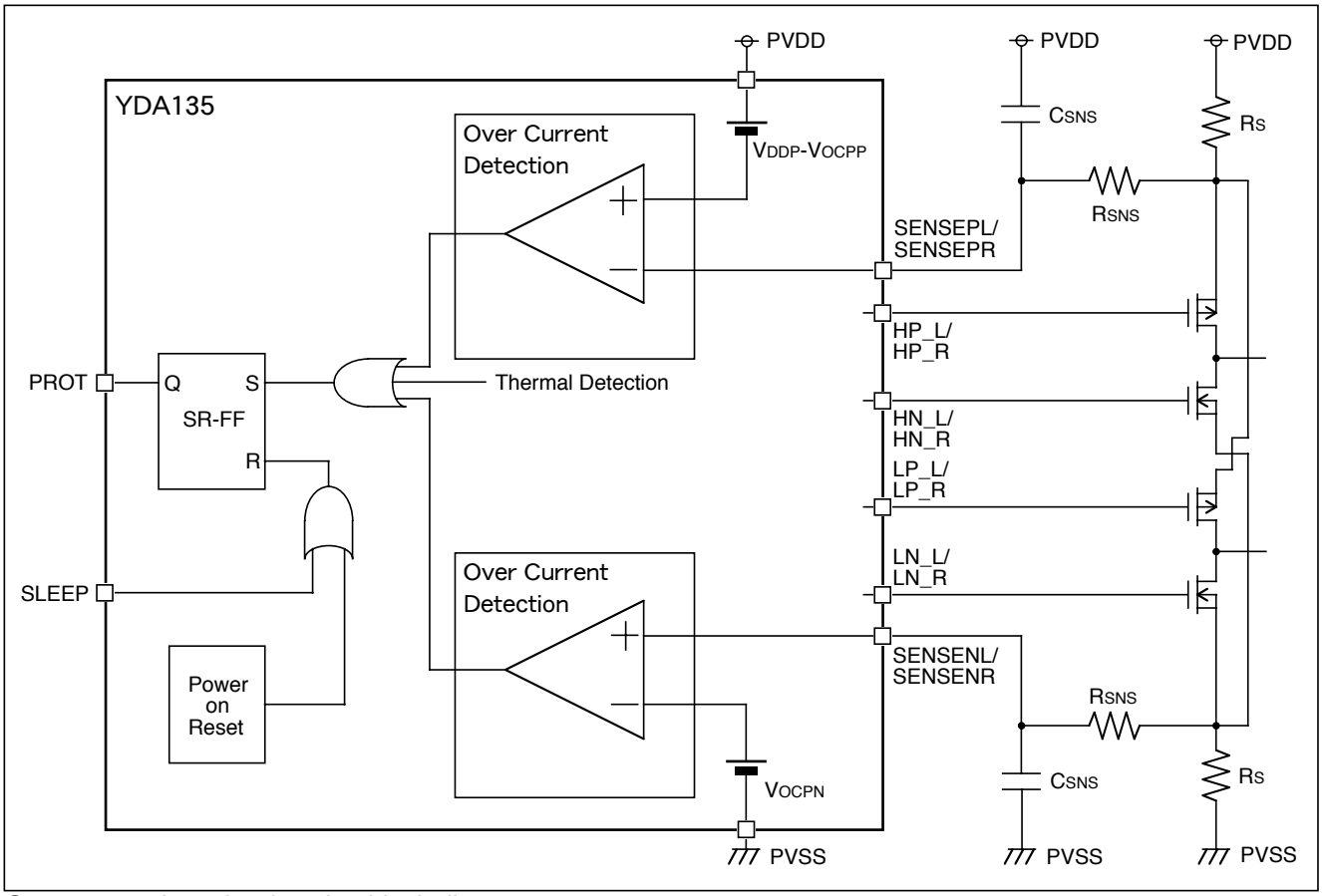
• Overcurrent detection functions

The overcurrent detection is a function that determines that the overcurrent state has occurred and set PROT terminal to "H" level, when the current flowing in the external Power MOSFET has become equal to or higher than the specified value. (This IC does not internally perform processing that turns off Power MOSFET automatically in such case.)
For the "Example of application circuit", the circuit related to the overcurrent detection function is as shown in the following figure, "Overcurrent detection function block diagram".

Connect a current detection resistor (R_S) between PMOS (source side) pin and power supply pin PVDD of Power MOSFET, and between NMOS (source side) pin and PVSS pin. Connect PMOS (source side) pin and SENSEPL pin through the low pass filter consisting of R_{SNS} and C_{SNS}, and NMOS (source side) and SENSENL pins as well. To prevent erroneous detection of glitch noise that can occur at switching of Power MOSFET, be sure to use the low pass filter consisting of R_{SNS} and C_{SNS}. Connect SENSEPR pin and SENSENR pin in the same way.
This IC recognizes an overcurrent state when the potential of SENSEPL pin or SENSEPR pin has decreased below the overcurrent detection threshold voltage (V_{OCPP}) for a certain period (T_{OCP}), bringing PROT pin to "H" level. When the potential of SENSENL pin or SENSENR pin has increased over the overcurrent detection threshold voltage (V_{OCPN}) for a certain period, it recognizes the overcurrent state, bringing PROT pin to "H" level. At this time, set SLEEP pin of MUTE pin to "H" to force the Power MOSFET to OFF.
After this, inputting "H" level once to SLEEP or turning off the power supply and then on again can restore the output of PROT pin to initial "L" state.
When it is not necessary to use the overcurrent detection function, connect SENSEPL pin and SENSEPR to PVDD, and SENSENL pin and SENSENR pin to PVSS (to disable the function).

When in sleep mode (SLEEP pin = "H" level) or in mute mode (MUTE pin = "H" level), this IC sets the Power MOSFET to OFF state, and thus, the overcurrent detection function of both L channel and R channel are stopped. For this circuit, use the overcurrent detection resistor (R_S) with low inductive component. The resistance is to be determined based on the drain current rating (I_{DMAX}: pulse current) and overcurrent threshold voltages (V_{OCPP}, V_{OCPN}) according to the conditions described below.

$R_S \geqq V_{OCPN} / I_{DMAX}$

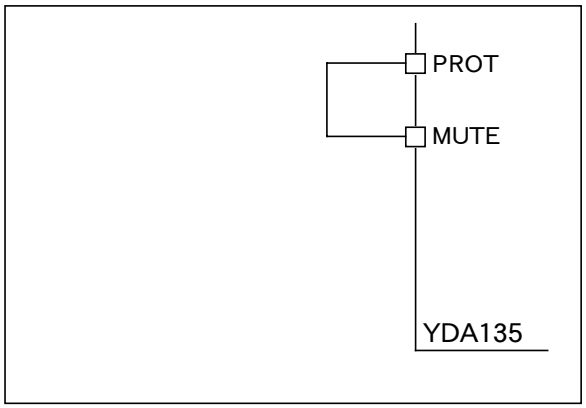


Overcurrent detection function block diagram

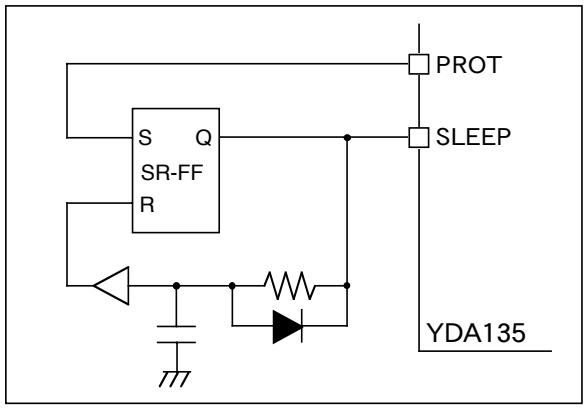
When overcurrent has been detected, Power MOSFET can be protected by the following methods.

(1)Turning off Power MOSFET when overcurrent has been detected.
Connect PROT terminal and MUTE terminal externally as shown in the following "Power MOSFET protection circuit". With this method, the device is brought into mute state when overcurrent has been detected, where Power MOSFET is turned off to limit the current flowing into Power MOSFET. At this time, the protected state can be cancelled by setting SLEEP terminal to "H" level or by bringing V_{DD} or PV_{DD} power supply terminal voltage to the level below the shut off voltage once.

(2)Turning off Power MOSFET when overcurrent has been detected and restarting it.
Connect PROT terminal and SLEEP terminal through external circuit as shown in the following "External automatic restoration circuit". With this method, SLEEP terminal becomes "H" level when overcurrent has been detected, and this IC is brought into sleep state (Power MOSFET is turned off). After this, when a certain period that depends on the RC time constant has elapsed, SLEEP terminal becomes "L" level where this IC restarts automatically.



Power MOSFET protection circuit

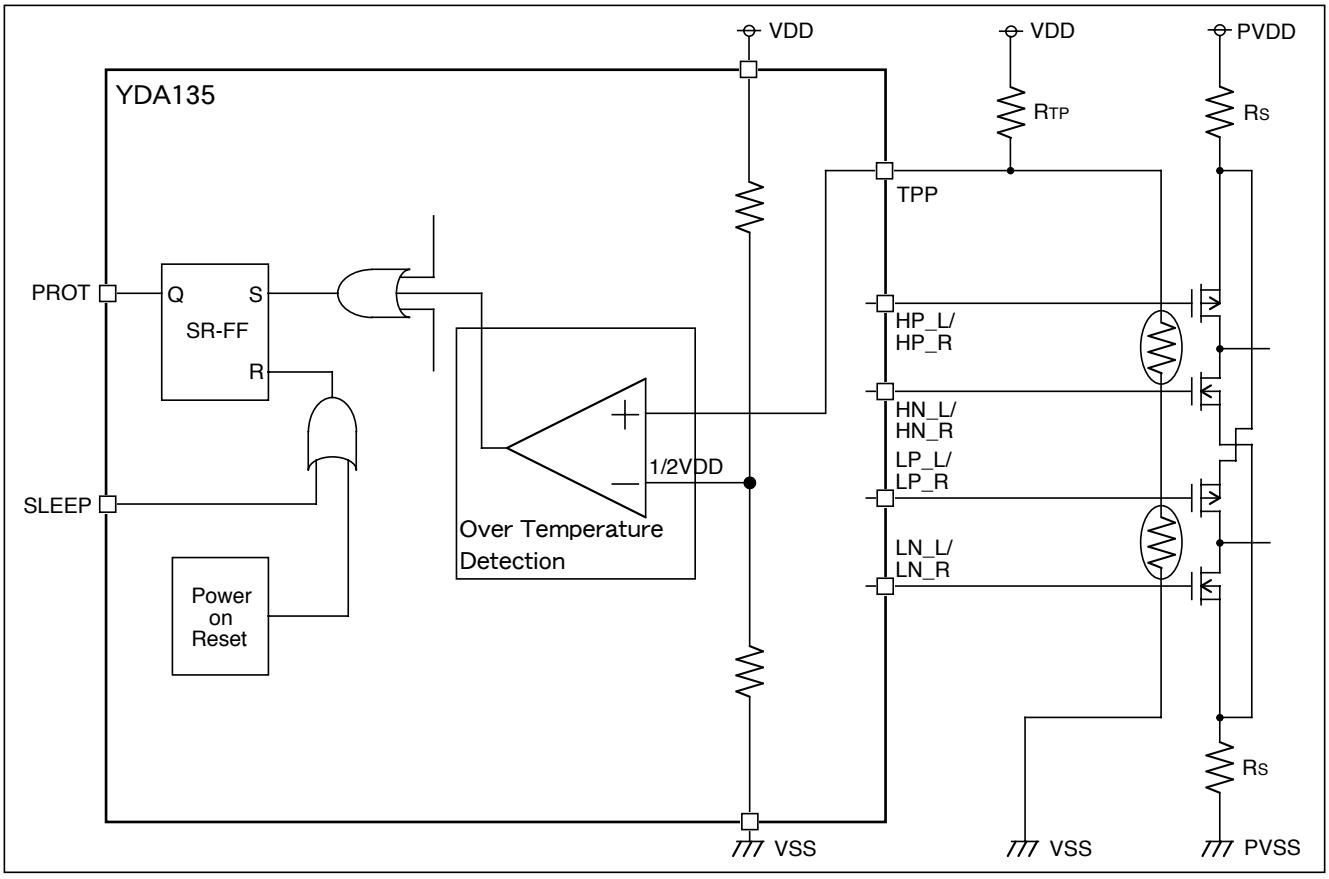


External automatic restoration circuit

• High temperature detection functions

The high temperature detection is a function that determines that the high temperature state has occurred and set PROT terminal to "H" level when the temperature of the temperature detection element (such as posistor*1) that is placed in the location that is thermally equivalent with Power MOSFET has become equal to or higher than the specified value. (This IC does not internally perform processing that turns off Power MOSFET automatically in such case.)
For the "Example of application circuit", the circuit related to the high temperature detection function is as shown in the next page, "High temperature detection function block diagram".

*1: "posistor" is a registered trade mark of Murata Manufacturing Co., Ltd. for their positive thermisters.



High temperature detection function block diagram

Connect the temperature detection element with positive temperature coefficient between VSS and TPP terminal by the number of pieces required.
In addition, connect a resistor(R_{TP}) between TPP terminal and VDD power supply terminal. Resistor value of temperature detection element is changed by rise in temperature. Select a resistor so that the threshold (V_{TPP}) is attained depending on the characteristic of the temperature detection element.
This IC determines that high temperature state has occurred when the potential of TPP terminal has exceeded the high temperature detection threshold voltage (V_{TPP}) for a certain period (T_{TPP}), and then sets PROT terminal to "H" level. At this time, set SLEEP terminal or MUTE terminal to "H" level to turn off Power MOSFET forcibly to limit the temperature rise.
PROT terminal output can be returned to initial "L" level output state by inputting "H" level once to SLEEP terminal or by turning off the power and then on again.
In sleep mode (SLEEP="H"), the high temperature detection function of this IC is disabled.

Since TPP terminal is a single terminal, the temperature detection circuit detects temperature of two channels collectively outside of this IC.
When the high temperature detection function is not used, connet TPP to the ground (to disable the high temperature detection function).

When high temperature state has been detected, Power MOSFET can be protected by the following methods.
(1)Turning off Power MOSFET when high temperature has been detected.
Connect PROT terminal and MUTE terminal externally as shown in the "Power MOSFET protection circuit" of the previous page. With this method, the device is brought into mute state when high temperature has been detected, where Power MOSFET is turned off to limit the current flowing into Power MOSFET to allow reduction of the temperature. At this time, the protected state can be cancelled by setting SLEEP terminal to "H" level once or by bringing VDD or PVDD power supply terminal voltage to the level below the shut off voltage once.

(2)Turning off Power MOSFET when high temperature has been detected and restarting it after a certain period.
Connect PROT terminal and SLEEP terminal through external circuit as shown in the "External automatic restoration circuit" of the previous page.
With this method, SLEEP terminal becomes "H" level when high temperature has been detected, and this IC is brought into sleep state (Power MOSFET is turned off). After this, when a certain period that depends on the RC time constant has elapsed, SLEEP terminal becomes "L" level where this IC restarts automatically.

• Sleep control functions

When SLEEP terminal is set to H" level, this IC changes into sleep mode. When SLEEP terminal is set to "L" level, this IC changes into normal operating state. In sleep mode, all functions are disabled, and power consumption is minimized.
At this time, all Power MOSFET driving terminals output signals that turns off the Power MOSFETs. Though all Power MOSFETs become off state, the speaker terminal is made ground potential by the externally connected resistors (R_{NFL} and R_{NFH}).
When MUTE terminal is changed from "H" level to "L" level, restarting sequence operates internally. This IC changes into normal operating state after the period that is set with a capacitor connected to VREFL terminal and VREFR terminal (starting time) has elapsed.
When SLEEP terminal is set to "H" level, PROT terminal is set to "L" level forcibly.

• Output mute control functions

When MUTE terminal is set to H" level, this IC change into mute mode. When MUTE terminal is set to "L" level, this IC change into normal operating state. In the mute mode, the internal clock stops. At this time, all Power MOSFET driving terminals output signals that turns off the Power MOSFETs. Though all Power MOSFETs become off state, the speaker terminal is made ground potential by the externally connected resistors (R_{NFL} and R_{NFH}).

• Pop noise reduction functions

This IC includes pop noise reduction function that works when turn on and turn off the power supply and enabling or canceling sleep mode.
At power on, this IC starts the starting sequence after 12V system's power supply voltage (V_{DDP}) for Power MOSFET driving circuit and 5 V system's power supply voltage (V_{DD}) for signal processing circuit has exceeded their low voltage malfunction prevention threshold (V_{UV12} and V_{UV5}) respectively. In the starting sequence, the pop noise can be reduced because the mute mode is canceled after the potential of input signal terminals (INL and INR) and potential of reference voltage output terminals (VREFL and VREFR) have stabilized sufficiently (after the elapse of starting period).
Also, when shutting off the power supply, the pop noise can be reduced by reducing 12V power supply voltage and 5V power supply voltage below the low voltage malfunction prevention threshold (V_{UV12} and V_{UV5}) earlier than the shift of the potential of input signal terminals (INL and INR) and potential of reference voltage output terminals (VREFL and VREFR).
The pop noise is also reduced by enabling the mute mode when the 5V system power supply voltage has changed 10% of 1/2 of VREF terminal voltage. Moreover, the pop noise can be reduced by using MUTE terminal control circuit as shown in the "Example of application circuit" when the speed of reduction of the power supply voltage is slow.
When the sleep mode is disabled, the pop noise can be reduced by using the starting sequence.
When the sleep mode is enabled, the pop noise is reduced because the mute mode is enabled simultaneously.
To make the pop noise reduction function operate effectively when turning on the power supply, it is necessary to set the values of capacitor (C_{REF}) that is connected to VREFL terminal and VREFR terminal, the resistor (R_I) and capacitor (C_I) that are connected to INL terminal and INR terminal as described below.

$$C_{REF} > R_I * C_I / 5000$$

• Pop noise reduction functions

Starting time is a period for each reference voltage to reach the specified potential (for charging capacitors (C_{REF}) of VREFL and VREFR terminals) when the power supply is turned on or is turned on again. This period varies in relation to the capacitance (C_{REF}) of VREFL and VREFR terminals. The table of starting time is as follows:

C_{REF} capacitor(μF)	Starting time (sec)
2	0.13
10	0.33
30	0.85
50	1.40

• How to supply power to 5V system

Since the operation of the 5V system power supply of this IC is guaranteed in the wide fluctuation range (10%), the power can be generated from 12V system power supply by using a zener diode. This features allows to operate this IC by using only a 12V power supply.

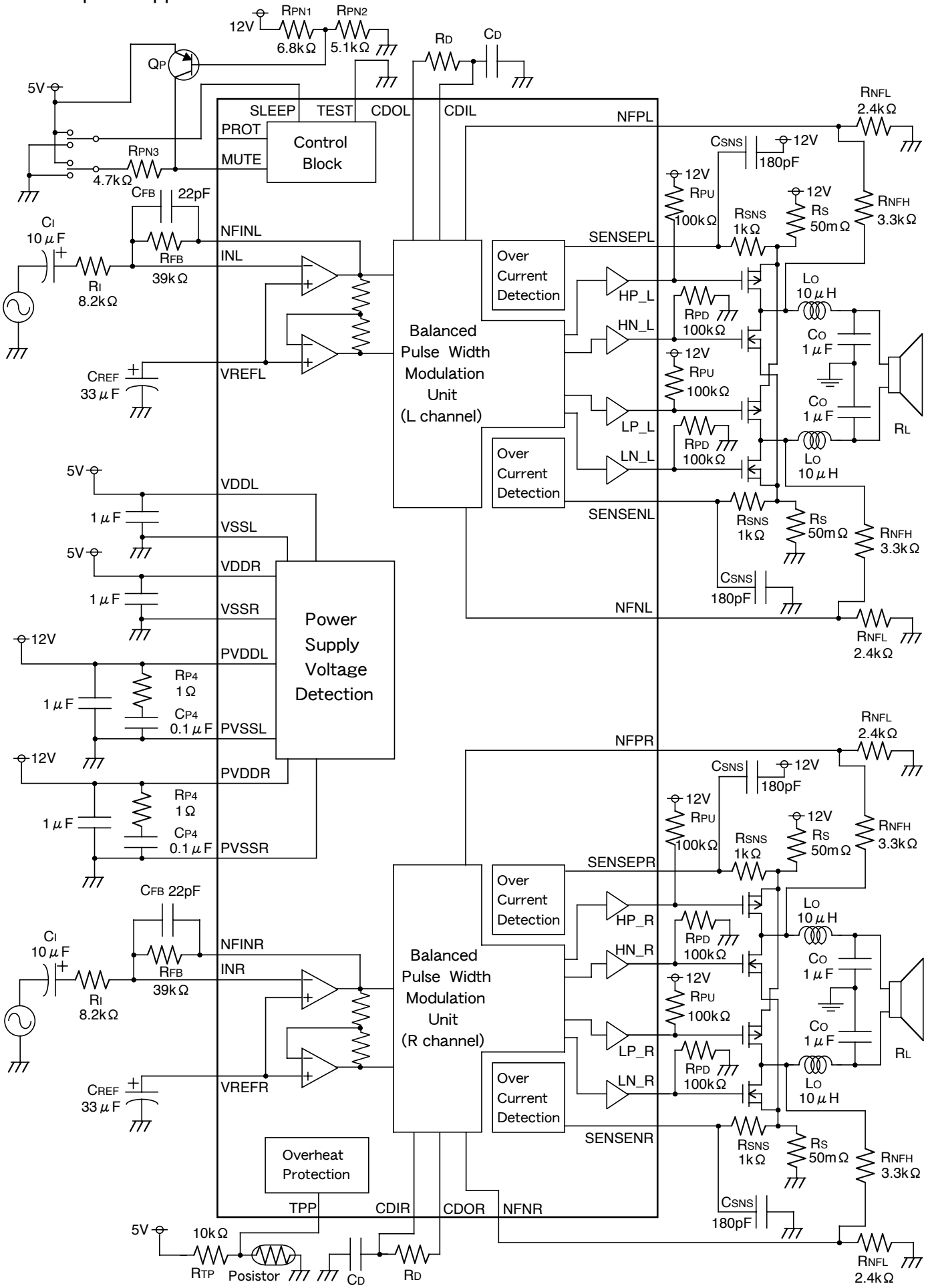
• Monaural operation

This IC can be operated in monaural mode by modifying the "Example of application circuit" as follows.
At this time, left channel is to be used.
It is not necessary to connect the resistors and capacitors, Power MOSFET and filter coils for right channel.

Terminal treatment in monaural operation

Pin No.	Name	Terminal treatment
10	VSSR	Connect to ground
11	VREFR	Non connection
13	VDDR	Connect to 5V power supply
14	INR	Connect to 47Pin INL
15	NFINR	Non connection
16	NFPR	Connect to 5V power supply
17	NFNR	Connect to ground
19	CDOR	Connect to 20Pin CDIR
20	CDIR	Connect to 19Pin CDOR
22	SENSEPR	Connect to 12V power supply
23	PVDDR	Connect to 12V power supply
24	SENSENR	Connect to ground
25	PVSSR	Connect to ground
27	HP_R	Non connection
28	HN_R	Non connection
29	LN_R	Non connection
30	LP_R	Non connection

■ Example of application circuit



■ Electrical characteristics

1. Absolute maximum rating

Item	Symbol	Min.	Max.	Unit
Power supply voltage for 12V system (PVDD) *1,*2, *3	V_{DDP}	-0.3	14.0	V
Power supply voltage for 5V system (VDD) *1, *2, *4	V_{DD}	-0.3	7.0	V
Input and output voltage for 12V system *5	V_{INP}	-0.5	V_{DDP}+0.5	V
Input and output voltage for 5V system *6	V_{IN}	-0.5	V_{DD}+0.5	V
Storage temperature	T_{STG}	-50	125	℃

Note: The absolute maximum rating is a value that must not be exceeded to guarantee the reliability and life of this IC, and thus, the use of this IC over the rating even for a moment may break down the device immediately or deteriorate its reliability severely.

*1: V_{SS} covers all ground terminals including VSS, VSSL, VSSR, PVSSL and PVSSR. Place all VSS terminals in the same potential.

*2: The voltage is referenced to V_{SS}=0V.

*3: 12V system power supply terminal (PVDD) covers PVDDL and PVDDR terminals.

*4: 5V system power supply terminal (VDD) covers VDDL and VDDR terminals.

*5: 12V system input/output terminal covers SENSENL, SENSEPL, SENSENR, SENSEPR, HP_L, HN_L, LP_L, LN_L, HP_R, HN_R, LP_R and LN_R terminals.

*6: 5V system input/output terminal covers SLEEP, MUTE, PROT, TPP, INL, NFINL, VREFL, NFPL, NFNL, CDIL, CDOL, INR, NFINR, VREFR, NFPR, NFNR, CDIR and CDOR terminals.

2. Recommended operating conditions

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage for 12V system *1	PV_{DD}	9.0	12.0	13.5	V
Power supply voltage for 5V system *2	V_{DD}	4.5	5.0	5.5	V
Operating ambient temperature(ambient temperatureTa)	T_{OP}	0	25	70	℃

Note: When this IC is used outside of the above voltage range may lead to malfunction of the IC, possibly causing generation of noise on the speakers.

*1: The voltage is referenced to V_{SS}=0V.

3.DC characteristics (V_{SS}=0V, V_{DD}=5V±0.5V, V_{DDP}=9V～13.5V, Ta=0℃～70℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HP_L,HN_L,LP_L,LN_L,HP_R,HN_R, LP_R,LN_R output voltage "H" level	V_{HOH}	I_{OH}=-10mA	V_{DDP}-0.4			V
HP_L,HN_L,LP_L,LN_L,HP_R,HN_R, LP_R,LN_R output voltage "L" level	V_{HOL}	I_{OL}=10mA			0.4	V
PROT output voltage "H" level	V_{OH}	I_{OH}=-80μA	V_{DD}-1.0			V
PROT output voltage "L" level	V_{OL}	I_{OL}=1.6mA			0.4	V
SLEEP, MUTE input voltage "H" level	V_{IH}		0.7*V_{DD}			V
SLEEP, MUTE input voltage "L" level	V_{IL}				0.3*V_{DD}	V
Power supply side overcurrent detection threshold voltage *1	V_{OCPP}			V_{DDP}-0.5		V
Ground side overcurrent detection threshold voltage *2	V_{OCPN}			0.5		V
Overcurrent detection delay time	T_{OCP}			0.4		μs
High temperature detection threshold voltage	V_{TPP}			1/2*V_{DD}		V
High temperature detection delay time	T_{TPP}			0.4		μs
12V power supply side threshold voltage prevention of low voltage malfunction	V_{UV12}			5.0		V
5V power supply side threshold voltage prevention of low voltage malfunction	V_{UV5}			3.5		V
Consumption current (sleep mode) VDD	I_{SLEEP}			1		μA
PVDD				1		μA
Consumption current (mute mode) VDD	I_{MUTE}			7		mA
PVDD				0.1		mA
Consumption current (2 channel output mode) VDD	I_{DD}			7		mA
(no signal, no filter) PVDD				30		mA

Note: *1: PVDD side overcurrent detection terminal covers SENSEPL, SENSEPR terminals.

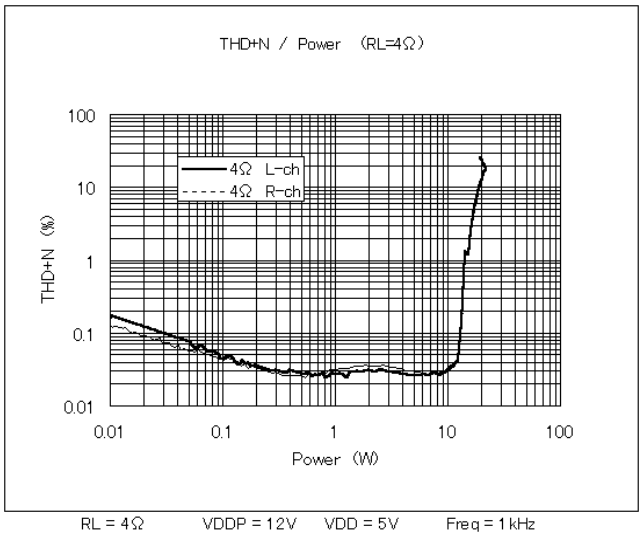
*2: PVSS side overcurrent detection terminal covers SENSENL, SENSENR terminals.

4. Analog characteristics (V_{SS}=0V, V_{DD}=5.0V, V_{DDP}=12.0V, Ta=25℃, load impedance=4Ω, Frequency=1kHz)

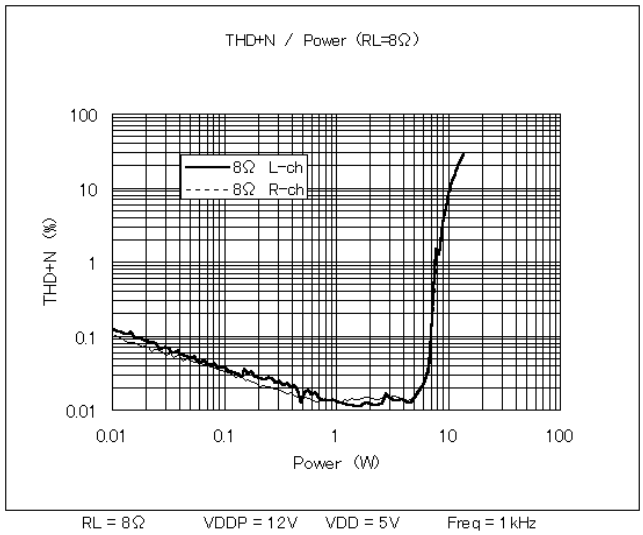
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum output	P_O	THD=0.1%		13		W
		THD=1%		14		W
		THD=10%		20		W
Voltage gain (R_I=8.2kΩ, R_{FB}=39kΩ)	A_V			35.1		dB
Total harmonic distortion (Band Width: 20kHz)	THD+N	Po=7W		0.03		%
Signal/noise ratio(A-Filter, Band Width: 20kHz, Po=20W)	SNR	Input sensitivity 150mV		97		dB
		Input sensitivity 1.0V		100		dB
Channel separation	CS			80		dB
Maximum efficiency	η	Load impedance=8Ω		85		%
		Load impedance=4Ω		80		%
Output offset voltage	V_O			30		mV

Note: All analog characteristics shown above are the values obtained on the Yamaha's evaluation environment. The characteristics may vary according to the Power MOSFET, coils, capacitors and pattern layout that are used in the system.

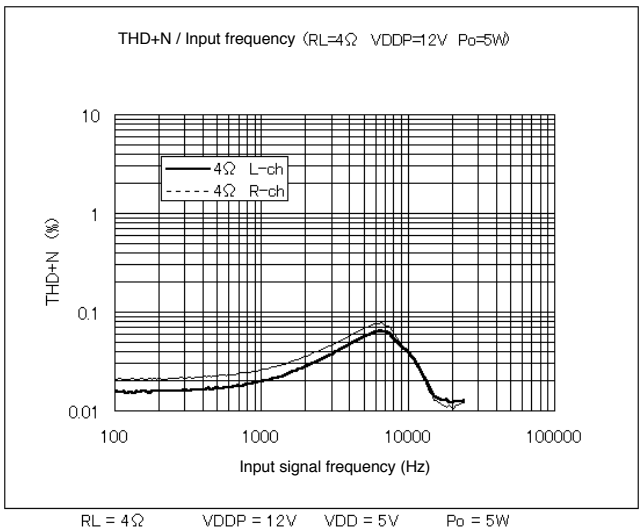
■Characteristics example



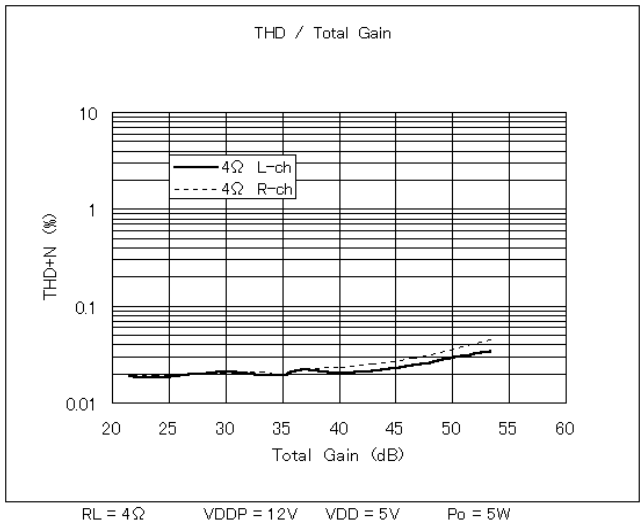
RL = 4Ω VDDP = 12V VDD = 5V Freq = 1kHz
Filter : < 20kHz



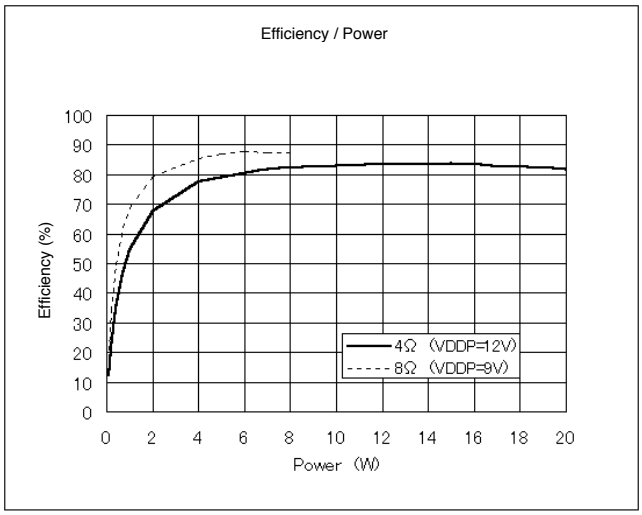
RL = 8Ω VDDP = 12V VDD = 5V Freq = 1kHz
Filter : < 20kHz



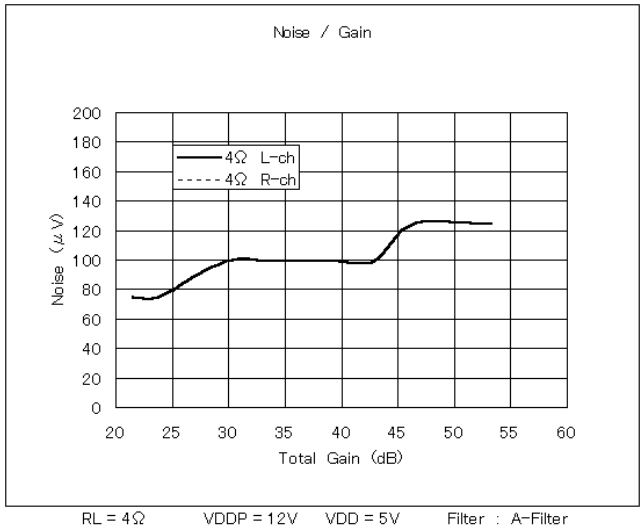
RL = 4Ω VDDP = 12V VDD = 5V Po = 5W
Filter : < 20kHz



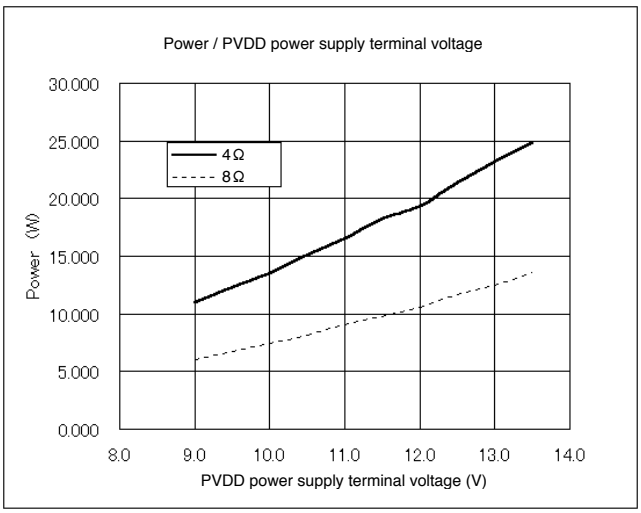
RL = 4Ω VDDP = 12V VDD = 5V Po = 5W
Filter : < 20kHz



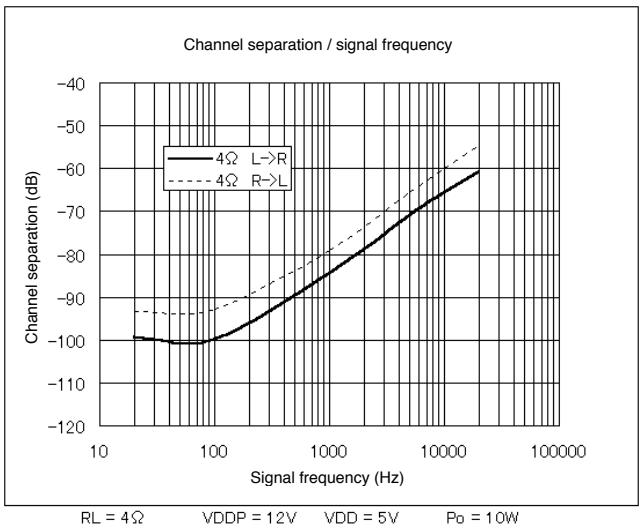
RL = 4Ω/8Ω VDDP = 12V@4Ω 9V@8Ω VDD = 5V



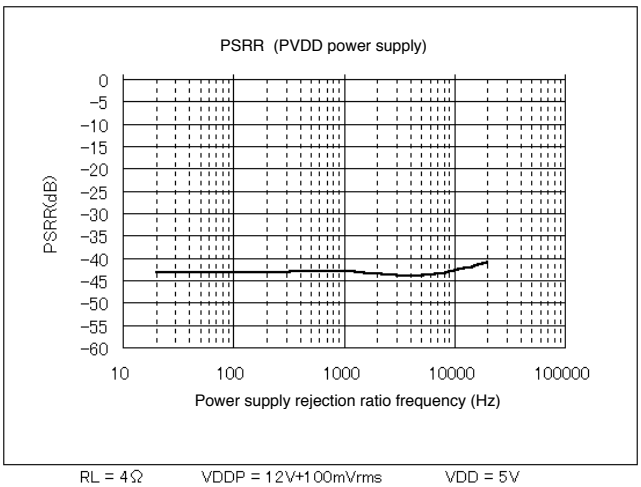
RL = 4Ω VDDP = 12V VDD = 5V Filter : A-Filter



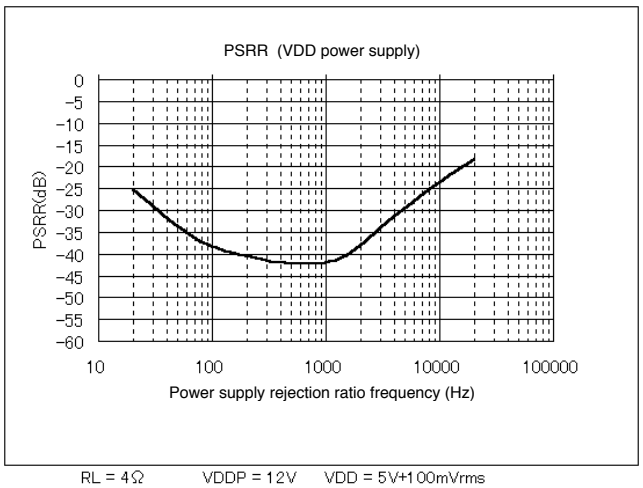
RL = 4Ω/8Ω VDD = 5V THD+N=10% Filter : < 20kHz



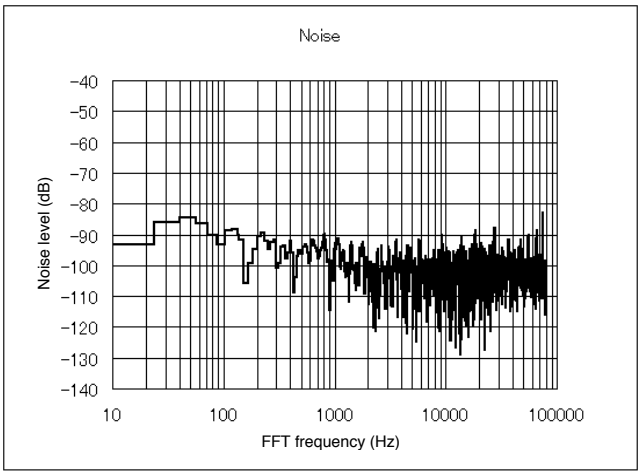
RL = 4Ω VDDP = 12V VDD = 5V Po = 10W
Filter : < 20kHz



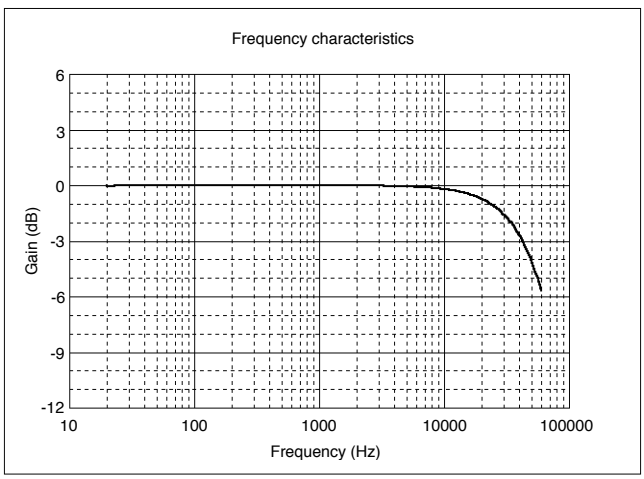
RL = 4Ω VDDP = 12V+100mVrms VDD = 5V
Filter : < 20kHz



RL = 4Ω VDDP = 12V VDD = 5V+100mVrms
Filter : < 20kHz



RL = 4Ω VDDP = 12V VDD = 5V L-ch
Total Gain 35dB (Input sensitivity=150mV)

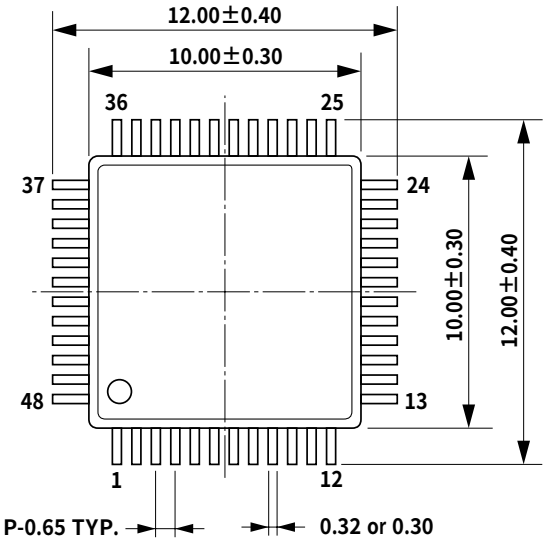


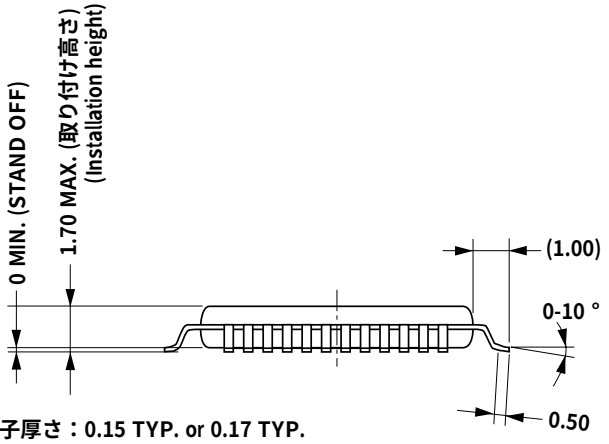
RL=4Ω VDDP=12V VDD=5V Lo=10μH Co=1μF

■ External dimensions of package

YDA135-VZ

C-PK48VP-0





端子厚さ：0.15 TYP. or 0.17 TYP.
(LEAD THICKNESS)

モールドコーナー形状は、本図面と
若干異なるタイプもあります。
カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm(millimeters)

The shape of the molded corner
may slightly different from the
shape in this diagram.
The figure in the parenthesis ( )
should be used as a reference.
Plastic body dimensions do not
include burr of resin.
UNIT: mm

注）表面実装 LSI は保管条件及び、半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせ下さい。

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